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- (71) Applicant (for all designated States except US): **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, M/S: RNB-4-150, Santa Clara, California 95052 (US).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **ROYTMAN, Eduard** [US/US]; 7 Kendall Road, Newton Centre, Massachusetts 02459 (US). **XU, Jian** [CN/US]; 3 Indian Pond Road, Westborough, Massachusetts 01581 (US). **SHAH, Rahul R.** [US/US]; 64 Bergron Road, Marlborough, Massachusetts 01752 (US). **MUNSHI, Kambiz R.** [US/US]; 92 Holden Street, Shrewsbury, Massachusetts 01545 (US). **BEDARD, Ronald L.** [US/US]; 24 East Road, Westmin-

ster, Massachusetts 01473 (US). **NAGARAJAN, Mahalingam** [IN/US]; 4 Christopher Drive, Grafton, Massachusetts 01519 (US).

(74) Agents: **VINCENT, Lester J.** et al.; Blakely, Sokoloff, Taylor & Zafinan LLP, 1279 Oakmead Parkway, Sunnyvale, California 94085-4040 (US).

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(54) Title: AN APPARATUS, SYSTEM, AND METHOD FOR VOLTAGE SWING AND DUTY CYCLE ADJUSTMENT

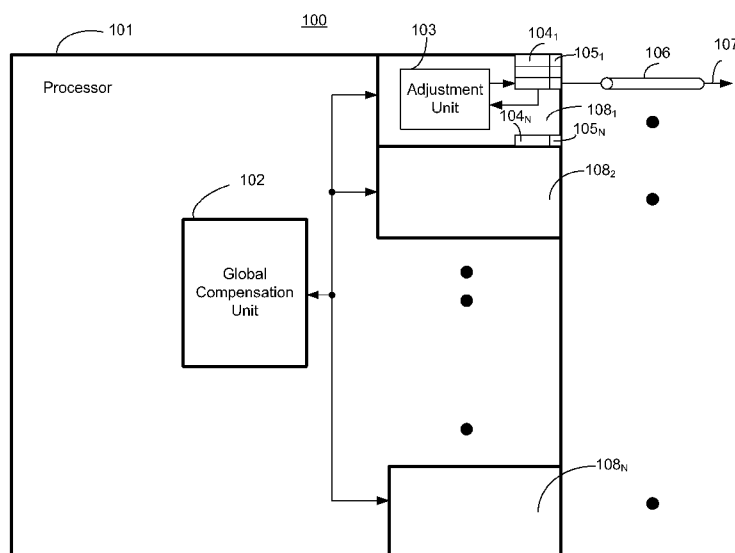


FIG. 1

(57) Abstract: Described herein are an apparatus, system, and method for compensating voltage swing and duty cycle of a signal on an input-output (I/O) pad of a processor by adjusting the voltage swing and duty cycle of the signal. The apparatus comprises a driver to transmit a signal on an I/O pad, the signal on the I/O pad having a voltage swing and a duty cycle; and an adjustment unit, coupled to the driver, to receive the signal from the I/O pad transmitted by the driver and to generate voltage swing and duty cycle control signals for adjusting the voltage swing and duty cycle of the signal on the I/O pad respectively. Described herein is also an analog-to-digital (A2D) converter for measuring and/or calibrating various signal attributes including current, voltage, and time.



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**AN APPARATUS, SYSTEM, AND METHOD FOR VOLTAGE SWING AND DUTY CYCLE
ADJUSTMENT**

FIELD OF THE INVENTION

5 Embodiments of the invention relate generally to the field of processors. More particularly, embodiments of the invention relate to an apparatus, system, and method for voltage swing and duty cycle adjustments of signals on input-output (I/O) pads of a processor. The embodiments of the invention also relate to an apparatus for measuring various signal attributes including current, voltage, and time.

BACKGROUND

10 As input-output (I/O) transceivers operate at higher frequencies, voltage and timing margins become smaller and harder to meet for a given design. Furthermore, high degree of random variation (also referred to as within-die variation) in modern process technology results
15 in excessive variations in voltage swing and duty cycle of signals transmitted by the I/O transceivers on transmission media. Identical I/O transceivers (i.e., transceivers with identical designs and transistor sizes) may exhibit different signaling attributes within internal nodes and at the outputs of their respective I/O pads e.g., the voltage swing and duty cycle of a signal generated by a first I/O transceiver of a processor may be different from the voltage swing and
20 duty cycle of another signal generated by a second I/O transceiver of the processor, even when the second I/O transceiver being physically located next to the first I/O transceiver.

 Such variability in the voltage swing and duty cycle of signals at the I/O pads result in reduced performance of the processor—performance as measured in terms of overall I/O speeds and satisfaction of I/O specifications of the processor.

25 Furthermore, characterizing various attributes of such high speed devices (e.g., the devices of the high speed I/Os) require expensive debugging testers. To reduce the cost and test time such high speed devices, on-die processor self-testing measures are applied. Traditional analog to digital (A2D) converters can be used to measure a single analog attribute of a device e.g., current levels of a current source of an I/O transmitter, to characterize the device. However,
30 such A2D converters are unable to measure multiple internal analog and digital attributes of a device e.g., current levels flowing through a node, duty-cycle of a high-speed node, phase difference between two different high-speed nodes, voltage level of a signal on a node.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the invention, which, however, should not be taken to limit the invention to the specific embodiments, but are
5 for explanation and understanding only.

Fig. 1 is a high level view of a processor with a per input-output (I/O) lane voltage swing and duty cycle adjustment unit, according to one embodiment of the invention.

Fig. 2 is a block diagram of an I/O transmitter of the processor comprising a voltage swing and duty cycle adjustment unit, according to one embodiment of the invention.

10 **Fig. 3** is a block diagram of the components of the adjustment unit for adjusting voltage swing and duty cycle of signals on an I/O pad, according to one embodiment of the invention.

Fig. 4A is a circuit level diagram of a low pass filter of the adjustment unit, according to one embodiment of the invention.

15 **Fig. 4B** is a circuit level diagram of a low pass filter of the adjustment unit, according to another embodiment of the invention.

Fig. 5 illustrates components of an I/O driver for adjusting voltage swing of a signal for transmission by the I/O driver, according to one embodiment of the invention.

Fig. 6 illustrates components of a duty cycle corrector for adjusting duty cycle of a signal for transmission by the I/O driver, according to one embodiment of the invention.

20 **Fig. 7** illustrates a state diagram of a finite state machine (FSM) of the adjustment unit for generating control signals to adjust voltage swing and duty cycle of a signal, according to one embodiment of the invention.

Fig. 8 illustrates a method flowchart for adjusting voltage swing and duty cycle of a signal for transmission by the I/O driver, according to one embodiment of the invention.

25 **Fig. 9A** illustrates a logical view of an analog-to-digital (A2D) converter for measuring various signal attributes including current, voltage, and time, according to one embodiment of the invention.

Fig. 9B illustrates components of the A2D converter for measuring various signal attributes, according to one embodiment of the invention.

30 **Fig. 10** illustrates a circuit level diagram of the A2D converter for measuring various signal attributes, according to one embodiment of the invention.

Fig. 11 illustrates components for providing inputs to the A2D converter for measuring various digital and analog signal attributes, according to one embodiment of the invention.

35 **Fig. 12** illustrates a waveform of a capacitor of the A2D converter for measuring various signal attributes, according to one embodiment of the invention.

Fig. 13 illustrates a system level diagram having the adjustment unit for adjusting voltage swings and duty cycle of signals, and the A2D converter, according to one embodiment of the invention.

Fig. 14 illustrates transistor level components of the A2D converter, according to another embodiment of the invention.

DETAILED DESCRIPTION

Embodiments of the invention relate to an apparatus, system, and method for voltage swing and duty cycle adjustments of signals on input-output (I/O) pads of a processor.

10 Embodiments of the invention also relate to an apparatus, system, and method for measuring various attributes of device(s) by means of an analog-to-digital (A2D) converter.

In one embodiment, the apparatus comprises an I/O transceiver including a driver to transmit a signal on an I/O pad, the signal on the I/O pad having a voltage swing and a duty cycle. The apparatus also comprises an adjustment unit, coupled to the driver, to receive the signal from the I/O pad transmitted by the driver and to generate voltage swing and duty cycle control signals for adjusting the voltage swing and duty cycle of the signal on the I/O pad. As mentioned in the background section, random variations in devices of the I/O transceivers cause variations in voltage swings and duty cycles of signals on the I/O pads even though the drivers, coupled to the I/O pads, that generate the signals on the I/O pads have identical designs. In one embodiment, the adjustment unit is operable to compensate for such random variations by adjusting both the voltage swing and the duty cycle of signals, for an I/O lane, by generating voltage swing and duty cycle control signals based on the signals on an I/O pad of the I/O lane.

By operating on the signals on the I/O pad, all sources of variation and distortion that cause variation in voltage swing and duty cycle are compensated by the adjustment unit.

25 An example of a high speed I/O transceiver is the QuickPath Interconnect® (QPI) developed by Intel Corp. of Santa Clara, California. The QPI of a processor operates at clock rates of 2.4 GHz, 2.93 GHz, or 3.2 GHz and may generate signals at the QPI I/O pads of the processor with data rates of 25.6 GB/s. Any random variability in voltage swings and duty cycles between QPI signals of different I/O lanes of the processor, operating at such high data rate, degrade the overall performance of the processor. In one embodiment, the QPI I/O transceiver comprises the adjustment unit which is operable to receive the signals on the I/O pad of the QPI I/O transceiver and to compensate all sources of variation and distortion that cause variation in voltage swing and duty cycle in the signals at the I/O pad.

The term “I/O lane” herein refers to a group of I/O transceivers with data and clock I/O transceivers. For example, a lane may have 21 I/O transceivers (20 for transmitting and receiving data signals, and 1 for clock signal), and a processor may have 20 lanes.

5 The term “voltage swing” herein refers to a voltage difference between the logical low (Vol) and the logical high (Voh) levels of the signal at the I/O pad. The term “voltage swing adjustment” herein refers to adjusting a voltage level of either the logical low or logical high level of the signal at the I/O pad. The term “adjusting a voltage level” herein refers to raising or lowering the logical low or logical high voltage levels of the signal at the I/O pad.

10 The term “duty cycle” herein refers to the pulse width of a logical high pulse relative to a logical low pulse in a period of a signal. For example, a signal having a 50% duty cycle refers to a signal with an equal logical high and low pulse widths within the period of the signal i.e., the signal is logical high for half the period of time and logical low for the remaining half of the period of time of the signal.

15 In the following description, numerous details are discussed to provide a more thorough explanation of embodiments of the present invention. It will be apparent, however, to one skilled in the art, that embodiments of the present invention may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring embodiments of the present invention.

20 Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate more constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. Such indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented
25 signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme, e. g., differential pair, single-ended, etc.

Fig. 1 is a high level view 100 of a processor 101 with a per I/O lane voltage swing and duty cycle adjustment unit 103, according to one embodiment of the invention. In one
30 embodiment, the processor 101 comprises ‘N’ I/O lanes labeled as 108_{1-N} . In one embodiment, $N=20$. So as not to obscure the embodiments of the invention, the embodiments are discussed with reference to the I/O lane 108_1 .

In one embodiment, the I/O lane 108_1 comprises multiple I/O transceivers 104_{1-N} including I/O pads 104_{1-N} coupled to corresponding I/O pins 105_{1-N} . In one embodiment, $N=21$ i.e., 21 I/O
35 transceivers per I/O lane. In one embodiment, the I/O lane 108_1 comprises an adjustment unit

103 operable to receive a signal, from an I/O pad of an I/O transceiver (e.g., 104₁), for transmission to an I/O pin (e.g., 105₁) and operable to adjust the voltage swing and duty cycle of the signal for transmission. In one embodiment, each I/O pin (105_{1-N}) is coupled to a corresponding transmission medium 106. In one embodiment, the transmission medium 106 is a point-to-point interconnect. The signal 107 from the transmission media 106 is received by a receiver (not shown) of another processor (not shown).

In one embodiment, the processor 101 comprises a global compensation unit 102 to compensate for termination impedance and analog bias signals of a driver of the I/O transceiver (e.g., 104₁). In one embodiment, the adjustment unit 103 begins to adjust the voltage swing and duty cycle of the I/O pad signals for each I/O lane after the global compensation unit 102 completes an initial compensation of the termination impedance and analog bias signals for all I/O pads in all I/O lanes.

Fig. 2 is a block diagram 200 of an I/O transceiver (e.g., 104₁) of the processor 101 coupled to a voltage swing and duty cycle adjustment unit 103, according to one embodiment of the invention. In one embodiment, the I/O transceiver comprises a driver 207 which generates differential output signals 203p and 203n from an input signal 201. So as not to obscure the embodiments of the invention, other components of the transceiver (e.g., 104₁) such as a pre-driver, a serializer, double pump multiplexer, buffers, clock tree, etc., are not shown.

In one embodiment, the driver 207 receives an analog bias signal 202 to set the driving strength of the driver 207. In one embodiment, the analog bias signal 202 is set by the global compensation unit 102. In one embodiment, the voltage swing of the signals 203p and 203n is adjusted by turning on/off devices of a bias circuit (or generator), in the driver 207, that generates a bias voltage level for a current source of the driver 207 that provides current to the final driving stage, of the driver 207. The final driving stage generates the signals 203p and 203n on the I/O pad. The components that adjust the bias voltage level for the current source are later discussed with reference to **Fig. 5**.

Referring back to **Fig. 2**, the adjustment unit 103 receives the differential signals 203p and 203n transmitted by the driver 207 and generates voltage swing control signal 204 and duty cycle control signal 205. In one embodiment, the adjustment unit 103 generates a common mode voltage signal of the two signals 203p and 203n. In one embodiment, the two differential signals 203p and 203n are terminated by termination resistors 'R_t' which are compensated for process, temperature, and voltage variations by the global compensation unit 102.

In one embodiment, the voltage swing control signal 204 is received by the driver 207. In such an embodiment, the voltage swing control signal 204 is received by gates of transistors that control the bias voltage level for a current source that provides current to the final driving stage

of the driver 207. In one embodiment, the voltage swing control signal 204 is a bus comprising multiple control signals, each control signal representing a bit code (1 or 0) to turn on/off a transistor in the driver 207. By turning on/off the various transistors in the bias generation circuit of the driver 207 by means of the bit codes of the control signal 204, the voltage swing of the signals 203p and 203n is adjusted. In one embodiment, the bus 204 is thermometer coded. In other embodiments, the bus 204 is binary coded.

In one embodiment, the adjustment unit 103 continues to update the voltage control signal 204 till the voltage swing of the signals 203p and 203n achieves a threshold level. In one embodiment, the threshold level is programmable. In one embodiment, the adjustment unit 103 generates the duty cycle control signal 205 after generating the voltage swing control signal 204 and after the voltage swing of the signals 203p and 203n achieves the threshold level. One reason for adjusting the voltage swing of the signals 203p and 203n prior to adjusting the duty cycle of the signals 203p and 203n is that an adjustment of the voltage swing of the signals 203p and 203n changes the duty cycle of the signals 203p and 203n.

In one embodiment, the I/O transceiver (e.g., 104₁) comprises a duty cycle corrector 206 to adjust the duty cycle of the signal 201 in view of the duty cycle control signal 205. In one embodiment, the duty cycle control signal 205 is a bus having multiple signals, each signal representing a bit code (1 or 0) to turn on/off a transistor in the duty cycle corrector 206. In one embodiment, the bus 205 is thermometer coded. In other embodiments, the bus 205 is binary coded. Sources of duty cycle distortion of signals 203p and 203n include clock tree buffers, double pumped multiplexers, pre-drivers, driver 207, driver termination resistors 'R_t' etc. In the embodiments discussed herein, the duty cycle of the signals 203p and 203n are adjusted by sampling the duty cycle of the signals 203p and 203n at the I/O pads instead of sampling the duty cycle of the to be transmitted signals e.g., signals from a clock tree buffer or any other circuit/unit prior to the driver 207.

By monitoring the output of the driver 207 i.e., the differential signals 203p and 203n on the I/O pads, by the adjustment unit 103, and determining the duty cycle control signal 205 from the monitored signals 203p and 203n, all sources of duty cycle distortion are accounted for by the duty cycle control signal 205. In one embodiment, the duty cycle corrector 206 corrects the duty cycle of the to be transmitted signal 201 in view of the duty cycle control signal 205 to compensate for duty cycle distortions of signals 203p and 203n at the I/O pads.

Fig. 3 is a block diagram of the components of the adjustment unit 300/103 for adjusting voltage swing and duty cycle of signals on an I/O pad, according to one embodiment of the invention. In one embodiment, the adjustment unit 300/103 comprises a multiplexer 302. In one embodiment, the multiplexer 302 multiplexes signals including differential signals 203p and

203n from the driver 207, a reference voltage signal 303, and a common mode voltage signal 304. In one embodiment, the common mode voltage signal 304 is generated by averaging the signals 203p and 203n by means of resistors 312 of equal resistance R. In one embodiment, the value of the resistor is 5KOhms.

5 In one embodiment, the reference voltage signal 303 is generated by a voltage divider (not shown). In one embodiment, the voltage divider is a resistor ladder. In another embodiment, the reference voltage signal 303 is generated by a band-gap circuit (not shown). In one embodiment, the reference voltage signal 303 is a DC voltage signal of 250mV. In one embodiment, the multiplexer 302 is controlled by a select signal 314. In one embodiment, the select signal 314
10 causes the multiplexer 302 to select the reference voltage signal 303 and the common mode voltage signal 304 for generating the voltage swing control signal 204. In one embodiment, the select signal 314 causes the multiplexer 302 to select 203n and 203p for generating the duty cycle control signal 205.

In one embodiment, the output of the multiplexer 302 is a differential output comprising of
15 signals 305 and 306 that correspond to either both the reference voltage signal 303 and the common mode voltage signal 304 or signals 203n and 203p. In one embodiment, the outputs 305 and 306 of the multiplexer 302 are filtered by a low pass filter (LPF) 313. In one embodiment, the LPF 313 is bypassed by a bypassing logic (not shown) when the select signal 314 selects the reference voltage 303 and the common mode voltage signal 304 for generating
20 the voltage swing control signal 204. In such an embodiment, the outputs of the multiplexer 305 and 306 are directly input to a comparator 309.

Fig. 4A illustrates a circuit level diagram 400 of the LPF 313 of the adjustment unit 103, according to one embodiment of the invention. In this embodiment, the LPF 313 is a differential LPF including a capacitor C connected between the resistors R1 and R2. In one embodiment,
25 the values of the resistors R1 and R2 are 5KOhms each, the capacitor C is 1.6pF, and the 3dB cut-off frequency of the differential LPF is 10MHz. Higher or lower values of the 3dB cut-off frequencies can be designed for the differential LPF to optimize between accuracy and lower residual noise from the differential LPF on the one hand and design area on the other hand.

Fig. 4B illustrates a circuit level diagram 410 of the LPF 313 of the adjustment unit 103, according to another embodiment of the invention. In this embodiment, the LPF 313 comprises
30 independent RC filters for each output signals 305 and 306 of the multiplexer 302. In one embodiment, the values of the resistors R3 and R4 are 5KOhms each, the value of the capacitors C1 and C2 are 3.2pF each, and the 3dB cut off frequency of the LPF 410/313 is 10Mhz. Higher or lower values of the 3dB cut-off frequencies can be designed for the LPF to optimize between

accuracy and lower residual noise from the LPF on the one hand and design area on the other hand.

Referring back to **Fig. 3**, in one embodiment the adjustment unit 103 further comprises a comparator 309 which compares the filtered output 307 and 308 with one another. The filtered output s 307 and 308 correspond to signals 305 and 306 respectively. In one embodiment, the comparator 309 generates an output signal 310 in response to comparing the signals 307 and 308. In one embodiment, the comparator 309 is an offset cancellation comparator which cancels input offset to reduce errors when comparing the input signals 307 and 308 with one another. In one embodiment, the comparator 309 receives a clock signal 311 to sample the output 310 of the comparator 309. In such an embodiment, the sampling means are integrated within the comparator 309. In other embodiments, the sampling means (not shown) are separate from the comparator 309. In one embodiment, the sampling means comprises a flip flop or a latch. In other embodiments, other types of sampling means may be used.

In the embodiments discussed herein, the comparator 309 is a common comparator in the feedback loop (driver 207→adjustment unit 103→driver 207, and driver 207→adjustment unit 103→duty cycle corrector 206→driver 207) for adjusting both voltage swing and duty cycle of the signals 203p and 203n on the I/O pads. Having the common comparator 309 for adjusting both voltage swing and duty cycle of the signals 203p and 203n reduces the active area of silicon because a single common comparator 309 uses less silicon area than two different comparators for adjusting voltage swing and duty cycle of the signals 203p and 203n respectively. The common comparator 309 also reduces residual I/O lane to I/O lane variability in the voltage swings and duty cycles because the same comparator is used for adjusting both the voltage swings and duty cycles of the signals on the I/O pads.

In one embodiment, the adjustment unit 103 further comprises a finite state machine (FSM) 301. In one embodiment, when the output 310 of the comparator 309 switches (from logical low level to logical high level or vice versa), the FSM 301 determines, based on the current mode of operation, whether the voltage swing of the signals 203p and 203n reached the voltage swing threshold or whether the duty cycle of the signals 203p and 203n is adjusted to the target percentage. In one embodiment, the target percentage for the duty cycle is 50%.

In the embodiments discussed herein, the FSM 301 is a common FSM for generating control signals for both voltage swing and duty cycle adjustment. Having a common FSM 301 reduces overall silicon area and power consumption of the processor 101. The FSM 301 also operates at a frequency less than the clock frequency of the I/O transceiver 108₁. In one embodiment, the FSM 301 operates at a clock frequency which is ¼ of the clock frequency of the I/O transceiver 104₁. In such an embodiment, the slow FSM 301, relative to the clock

frequency of the I/O transceiver 104₁, consumes less power supply and has relaxed timing constraints. The term “timing constraints” refers to setup and hold timing requirements. In one embodiment, the FSM 301 output comprises the voltage swing control signal 204, duty cycle control signal 205, and the comparator sampling clock signal 311. In one embodiment, the select signal 314 of the multiplexer 302 is also generated by the FSM 301. The state diagram of the FSM 301 is discussed later with reference to **Fig. 7**.

Fig. 5 illustrates a high level block diagram of the I/O driver 500/207 for adjusting voltage swing of the signals 203p and 203n at the I/O pad, according to one embodiment of the invention. So as not to obscure the embodiments of the invention, a high level block diagram is shown to illustrate that the voltage swing control signal 204 from the adjustment unit 103 is used to adjust the bias level of the signal 503 which in turn adjusts the voltage swing of the signals 203p and 203n.

In one embodiment, the driver 207 comprises a bias generator 501 to provide a bias signal to the driving stage 502. In one embodiment, the bias generator 501 receives a reference bias signal 202 to generate the bias signal 503. In one embodiment, the reference bias signal 202 is the global bias signal generated by the global compensation unit 102.

In one embodiment, the bias generator 501 comprises a current mirror including transistors M1-M5 to generate the bias signal 503 from the reference bias signal 202. In one embodiment, the voltage control signal 204 adjusts the level of the bias signal 503 by turning on/off transistors M5 [1:N]. The term ‘N’ indicated on the transistor 504 implies more than one identical transistor in parallel to one another. As mentioned above, the voltage control signal 204 is a bus having multiple signals, each signal representing a bit code to turn on/off one of the ‘N’ transistors 504 to adjust the DC level of the bias signal 503.

In one embodiment, the driver 500/207 comprises a driving stage 502 which receives the input data 201 and outputs a differential data 203p and 203n for transmission to an I/O pad (not shown). In one embodiment, the driving stage 502 is a differential amplifier with ground termination resistors (shown as ‘Rt’ in **Fig. 2**), wherein the differential amplifier is biased by a current source M6 controlled (i.e., biased) by the bias signal 503, and wherein the transistors M7 and M8 receive the input signal 201 as complementary signals.

In one embodiment, as the number of transistors 504 are turned on by the voltage swing control signal 204, the level of the bias signal 503 moves farther from the supply level of the PMOS device M7 in the current-mode driving stage 502 to cause the signals 203p and 203n to have a higher drive current and as a result higher voltage swing generated on resistors Rt. In one embodiment, as the number of transistors 504 are turned off by the voltage swing control signal 204, the level of the bias signal 503 moves closer to the supply voltage level of the PMOS device

M7 in the current-mode driving stage 502 to cause the signals 203p and 203n to have a lower drive current and as a result lower voltage swing generated on resistors Rt. A person skilled in the art would realize that there are many ways of influencing the bias level of signal 503 by means of the voltage swing control signal 204. All such alternatives are contemplated in these
5 embodiments.

Fig. 6 illustrates components 600 the duty cycle corrector 206 for adjusting duty cycle of a signal 201 for transmission by the I/O driver 207, according to one embodiment of the invention. In one embodiment, the duty cycle corrector 206 comprises a current starved inverter 600. In one embodiment, the duty cycle control signal 205 from the adjustment unit 103 controls the
10 strength of the current starved inverter 600. By controlling the strength of the transistors 601 and 602, of the current starved inverter 600, the duty cycle of the signal 201 is adjusted. In one embodiment, the current starved inverter 600 receives a signal 201a which is inverted and delayed to generate signal 201.

Fig. 7 illustrates a state diagram or flowchart 700 of the FSM 301 of the adjustment unit
15 103 for generating control signals 204 and 205 to adjust voltage swing and duty cycle of signals 203p and 203n, according to one embodiment of the invention. The state diagram 700 is illustrated with reference to **Figs. 1-6**.

In one embodiment, the FSM 301 begins to operate after system reset 701. In one embodiment, system reset 701 is any one of a hard reboot, soft reboot, and wakeup after sleep
20 mode. In one embodiment, at block 702 the FSM 301 begins to generate voltage swing control signal 204 by setting the code (i.e., all bits) of the signal 204 to zero. The length of the code depends on the granularity required for adjusting the voltage swing of signals 203p and 203n. After the multiplexer 302 selects the reference voltage signal 303 and the common mode signal 304, and the comparator 309 compares them (i.e., either the filtered version 307 and 308 or the
25 unfiltered bypassed version of signals 305 and 306), the FSM 301 at block 703 samples the output of the comparator 309 by means of a sampling signal 311, according to one embodiment of the invention. In one embodiment, a counter value is incremented by the FSM 301 after every sampling operation of the comparator output 310. The logic gates including the counter that form the FSM 301 are not disclosed so as not to obscure the embodiments of the invention.

At block 704, the FSM 301 compares the counter value with a predetermined voltage swing threshold value M, according to one embodiment of the invention. In one embodiment, if the counter value is below the value of M, then the FSM 301 at block 705 adjusts the voltage swing control signal 204 to cause the driver 207 to raise the voltage level of the output signals 203p and 203n. In one embodiment, the comparator 309 then compares a new common mode
30 voltage signal 304 with the reference signal 303. In one embodiment, the output of the
35

comparator 309 is then sampled again at block 703. After sampling the output 310 of the comparator 309, the counter value is incremented and compared with the predetermined voltage swing threshold M at block 704, according to one embodiment of the invention.

5 In one embodiment, the process of raising the voltage level of the output signals 203p and 203n, by means of the driver 207 which receives the voltage swing control signal 204, is performed till the counter value exceeds the predetermined voltage swing threshold value M. At that point, the FSM 301 transfers control to block 706 to signal a completion of the voltage swing adjustment operation of the signals 203p and 203n, according to one embodiment of the invention. In one embodiment, the FSM 301 then adjusts the duty cycle of the signals 203p and 10 203n. In one embodiment, the voltage control signal codes 204 are stored in a register.

In one embodiment at block 707, the FSM 301 generates the duty cycle control signal 205 by setting the code (i.e., all bits) of the signal 205 to zero. The length of the code depends on the granularity for adjusting the duty cycle of signals 203p and 203n. After the multiplexer 302 selects the signals 203p and 203n from the I/O pads, and the comparator 309 compares the 15 filtered versions 307 and 308 of the signals 203p and 203n, the FSM 301 at block 708 samples the output 310 of the comparator 309 by means of the sampling signal 311, according to one embodiment of the invention. In one embodiment, a counter value is incremented by the FSM 301 after every sampling of the comparator output 310. In one embodiment at block 709, a determination is made whether the counter value is above a predetermined threshold M. In this 20 embodiment, M corresponds to a value that results in the target duty cycle. In one embodiment, the target duty cycle is 50%.

If the counter value is below the value of M, then the FSM at block 710 adjusts the code of the duty cycle control signal 205 to cause the duty cycle corrector 206 to increase the duty cycle of signal 201 and thus of the output signals 203p and 203n, according to one embodiment of the 25 invention. In one embodiment, the comparator 309 then compares the output signals 203p and 203n with one another. The output of the comparator 309 is then sampled again at block 708. As discussed with reference to **Fig 3**, the comparator 309 may sample the output of the comparator 309 within the comparator block 309, or a separate sampling means (not shown) may sample the output 310 of the comparator 309 before the signal 310 is input to the FSM 301.

30 Referring back to **Fig. 7**, in one embodiment after sampling the output 310 of the comparator 309, the counter value is incremented and compared with the predetermined threshold M at block 709. In one embodiment, the counter of the FSM 301 is the same counter that is used at blocks 703 and 704.

In one embodiment, the process of increasing the duty cycle of the output signals 203p and 35 203n, by means of the duty cycle control signal 205 and the duty cycle corrector 206, is

performed till the counter value exceeds the predetermined threshold value M. At that point, the FSM 301 transfers control to block 711 to signal a completion of duty cycle adjustment of the signals 203p and 203n, according to one embodiment of the invention. In one embodiment, the duty cycle signal codes 205 are stored in a register. In one embodiment, the FSM transfers control to block 712 to indicate that both the voltage swing adjustment and the duty cycle adjustment is complete.

While the embodiments of the state diagram 700 are illustrated by increasing the voltage swing from an initial setting, it is contemplated that the FSM 301 includes all necessary logic to decrease the voltage swing from an initial setting and/or to both increase and decrease the voltage swings of the signals 203p and 203n to bring the voltage swings of the signals 203p and 203n to the target voltage swing level. Similarly, it is contemplated that in one embodiment the FSM 301 includes all necessary logic to decrease the duty cycle from an initial setting and/or to both increase and decrease the duty cycles of the signals 203p and 203n to bring the duty cycles of the signals 203p and 203n to the target duty cycle level.

Fig. 8 illustrates a method flowchart 800 for adjusting voltage swing and duty cycle of a signal for transmission by the I/O driver 207, according to one embodiment of the invention. The flowchart 800 is illustrated with reference to **Figs. 1-7**.

At block 801, the global compensation logic 102 initiates the process, voltage, and temperature compensation of termination impedance and bias voltage/current for all I/O lanes 108_{1-N} of the processor 101. The compensation process results in generating of compensation codes for termination impedance and bias voltage/current. At block 802, after completing the compensation process, the global compensation logic 102 freezes the compensation codes for termination impedance and bias voltage/current for all I/O lanes 108_{1-N} of the processor 101.

At block 803, the processor 101 initiates the adjustment of voltage swing and duty cycle of signals on the I/O pads for each I/O lane 108_{1-N} of the processor 101. Blocks 804-808 of the flowchart 800 summarize the high level operations of the adjustment unit 103. Details of how the voltage swing and duty cycle control signals are generated are discussed above with reference to **Fig. 5**.

Referring back to **Fig. 8**, at block 804 the driver 207 transmits signals 203p and 203n on an I/O pad of an I/O lane (e.g., 108₁), wherein the signals 203p and 203n have a voltage swing and a duty cycle. At block 805, the adjustment unit 103 receives the signals 203p and 203n to generate voltage swing and duty cycle control signals 204 and 205 respectively. At block 806, the adjustment unit 103 first generates the voltage swing control signal 204. The driver 207 receives the voltage swing control signal 204 to adjust the voltage swing of the signals 203p and 203n. At block 807, the adjustment unit 103 generates the duty cycle control signal 205 after

completing the voltage swing adjustment of the signals 203p and 203n. The duty cycle corrector 206 receives the duty cycle control signal 205 to adjust the duty cycle of the signals 203p and 203n.

5 The process of adjusting the voltage swing and the duty cycle is repeated for all remaining I/O lanes 108_{2-N}. At block 808, a determination is made whether voltage swing and duty cycle is corrected for all I/O lanes 108_{1-N}. If any I/O lane still needs voltage swing and duty cycle adjustment, the process from blocks 804 to 808 continues. Upon completion of the adjustment of voltage swing and duty cycle for all I/O lanes 108_{1-N}, the compensation codes are unfrozen at block 809. The term “unfrozen” means that the compensation codes are allowed to change. At 10 block 810, the global compensation unit 102 continues to compensate termination impedance and bias voltage/current for all I/O lanes 108_{1-N} of the processor 101 for process, voltage, and temperature.

Fig. 9A illustrates a logical view 950 of an analog-to-digital (A2D) converter 900 for measuring various signal attributes including current, voltage, and time, according to one 15 embodiment of the invention. In one embodiment, the A2D converter 900 receives signal 951 to be measured by the A2D converter. The term “measure” herein refers to converting an analog to a corresponding digital counter value. In one embodiment, the A2D converter converts the signal 951 to a corresponding counter value 913. In one embodiment, the signal 951 is a current through a node, a voltage on a node, or a time domain signal having a pulse width. In one 20 embodiment, the A2D converter 900 is operable to receive an operational signal 952 which configures the A2D converter 900 to implement one of the three distinct measurement functions—current measurement, voltage measurement, or time measurement.

In the embodiments discussed herein, the A2D converter 900 is operable to perform three distinct measurement functions that allow the A2D converter 900 to measure delay locked loop 25 (DLL) phase separation, measure phase interpolator (PI) phase separation, measure duty cycle of a clock signal, calibrate and measure reference voltages, calibrate and measure reference currents etc.

Fig. 9B illustrates high level components of A2D converter 900 for measuring various signal attributes, according to one embodiment of the invention. In one embodiment, the A2D 30 converter 900 comprises an integrating capacitor 904, a comparator 906, and a counter 910. In one embodiment, the integrating capacitor 904 comprises two terminals. The first terminal of the integrating capacitor 904 is node 905 which is electrically connected as input to the comparator 906. The term “node 905” is herein interchangeably used as “signal 905” to refer to the signal on that node. The second terminal of the integrating capacitor 904 is a ground

terminal. In one embodiment, the integrating capacitor 904 is an on-die capacitor having a capacitance C. In one embodiment, the value of C is 5pF.

In one embodiment, the comparator 906 also receives a reference voltage signal 909. In one embodiment, the reference voltage signal 909 is generated from a voltage divider. In one
5 embodiment, the reference voltage signal 909 is generated by a band-gap circuit. In one embodiment, the reference voltage signal 909 is a programmable signal wherein the levels of the reference voltage signal 909 can be adjusted according to the signal to be measured by the A2D converter 900.

In one embodiment, the comparator 906 is an offset cancellation comparator which is
10 capable of cancelling any input offset in the signals 905 and 909 to reduce residual error in the output 907 of the comparator 906. In one embodiment, the output 907 of the comparator 906 is input to the counter 910 and causes the counter 910 to stop counting when the output 907 trips. The term “trip” herein refers to a signal transitioning from a logical low level to a logical high level or vice versa.

15 In one embodiment, the comparator 906 receives a clock signal 908 for sampling the output of the comparator 906 before it is input to the counter 910. In such an embodiment, the output 907 of the comparator 906 is a sampled output i.e., sampled by the clock signal 908. In one embodiment, the counter 910 and the comparator 906 receive the same clock signal 908.

20 In one embodiment, the A2D converter 900 is operable to inject a variable amount of charge on the node 905 of the integrating capacitor 904 during a clock cycle of a clock signal 903. The A2D converter 900 then counts (up or down), by means of the counter 910, the cycles it takes for the node 905 of the capacitor 904 to reach a target voltage level 909 (also referred to as the reference voltage signal) from a known initial state.

In one embodiment, the counter 910 is a count-up counter that begins to count from zero
25 and up in response to a start count (or reset) signal 912. In one embodiment, the counter 910 is a count-down counter that begins to count down from a predetermined count value to zero in response to the start count (or reset) signal 912. In one embodiment, when the start count signal 912 is asserted (or de-asserted), the node 905 is discharged through the device (also called the second switch) 911 to set initial conditions of the integrating capacitor 904.

30 In one embodiment, once the capacitor node 905 reaches the target voltage level 909, the output 907 of the comparator 906 trips and stops the counter 910 from counting. The size of the counter 910 depends on the type of accuracy with which to measure a signal or the accuracy of converting the analog signal to its digital version.

As mentioned above, in the embodiments discussed herein regarding the A2D converter
35 900, three distinct measurement functions are implemented in a single A2D converter 900.

The first measurement function is the integrating current function that allows the A2D converter 900 to measure current through a node. In one embodiment, the A2D converter 900 comprises a current source 901 to implement the first measurement function. As later discussed with reference to **Fig. 10**, in one embodiment, the current source 901 is coupled to a measuring node by means of a current mirror, wherein the A2D converter is operable to measure the current through the measuring node. In this embodiment, the signal 952 of **Fig. 9A** causes the to be measured current to flow from current source 901 to the capacitor node 905, and also causes a clock signal 903 to periodically switch on and off the first switch 902. In this embodiment, the counter output 913 is inversely proportional to the current from the current source 901.

Referring back to **Fig. 9**, the second measurement function is an integrating time per cycle function that allows the A2D converter 900 to measure duty cycle and phase of a time domain signal 903. In one embodiment, the first switching device 902 is used to implement the second measurement function. In this embodiment, the signal 952 of **Fig. 9A** causes a fixed current to flow from the current source 901 to the node 905, and also causes the signal to be measured to couple to 903. In this embodiment, the counter output 913 is inversely proportional to the pulse width of the signal 903 received by the first switching device 902. In this embodiment, the first switching device 902 remains on, to allow the current source 901 to charge the node 905, during the pulse width of the signal 903.

The third measurement function is the voltage measurement function that allows the A2D converter 900 to measure a voltage on the node 905 of the integrating capacitor 904 relative to an initial voltage level on the node 905. In one embodiment, the A2D converter 900 comprises a switching mechanism to switch off devices 902 and 911 and directly couple a signal, whose voltage is to be measured, to the node 904. In this embodiment, the signal 952 of **Fig. 9A** causes a fixed current to flow from the current source 901 to the capacitor node 905, and also causes the signal 903 to keep the first switch 902 on. In this embodiment, the voltage to be measured is coupled to node 905. In this embodiment, the counter output 913 is directly proportional to the voltage on the node 905.

Fig. 10 illustrates a circuit level diagram 1000 of the A2D converter 900 for measuring various signal attributes, according to one embodiment of the invention. In one embodiment, current source 901 is implemented as a PMOS transistor with its gate tied to a diode connected PMOS transistor 1002 which forms a current mirror. In one embodiment, the current 1001 to be measured is input to the PMOS transistor 1002. In one embodiment, the device sizes (width and length) of the transistors 901 and 1002 are the same and so the current flowing into the first switch 902 from the current source 901 is equal to the input current 1001.

In one embodiment, the switch 902 comprises PMOS pass gates controlled by strobe# and strobe signals which are represented by signal 903. In one embodiment, the strobe# and strobe signals are clock signals having a frequency which is the same as the frequency of the counter clock signal 908. The term ‘#’ herein refers to an inverse function. For example, strobe# signal is an inverse signal of the strobe signal. In one embodiment, when the A2D converter 900 is configured to measure a time difference (e.g., pulse width or duty cycle of a signal), then a signal similar to 1003 is input as the strobe signal. In one embodiment, a dummy load (diode connected NMOS transistor) is coupled to one of the PMOS transistors of the switch 902 to mimic the load of the second switch 911. In one embodiment, the second switch 911 is implemented as an NMOS transistor which is operable to discharge the integrating capacitor 904 in response to a reset signal 912.

Fig. 11 illustrates components 1100 for providing inputs to the A2D converter 900 for measuring various signal attributes, according to one embodiment of the invention. In one embodiment, a multiplexer 1102 provides selective signals 1109 and 1110 via a strobe generator 1101 to the A2D converter 900. The signals 1109 and 1110 are collectively shown as signal 903 in **Fig. 9B**.

Referring back to **Fig. 11**, in one embodiment the multiplexer receives the signals for measurement 1103 and a clock signal. In one embodiment, the multiplexer outputs signals 1105 and 1106 in response to a select signal 1104. In one an embodiment, the strobe generator 1101 compares the phases of the signals 1105 and 1106 and generates the strobe and strobe# signals 1109 and 1110 respectively. In such an embodiment, the A2D converter 900 outputs a count value 913 which represents the phase difference between the signals 1109 and 1110.

In one embodiment, the phase detector of the strobe generator 1101 is bypassed when the A2D converter 900 is being used to measure a phase of the strobe signal 1109, or the pulse width of the strobe signal 1109, wherein the strobe signal 1109 is one of the signals for measurement 1103.

Fig. 12 illustrates a graphical plot 1200 of waveforms of the node 905 of the integrating capacitor 904 of the A2D converter 900 with respect to the reference voltage signal 909, according to one embodiment of the invention. The y-axis represents the voltage on the node 905, which is the voltage on the integrating capacitor 904. The x-axis represents the counter value 913 of the counter 910. Waveform 1201 shows a case when the counter begins to count from zero after being discharged through the device 911 in response to the reset signal 912. When the voltage on the node 905 crosses the reference voltage signal 909, the output 907 of the comparator 906 trips. In response to the output 907 tripping, the node 909 is discharged.

Waveform 1202 illustrates a case when the node 909 take a longer time to charge to reach the

level of the reference voltage signal 909 relative to the time it takes the waveform 1201 to charge.

Fig. 13 illustrates a system level diagram having the adjustment unit for adjusting voltage swings and duty cycle of signals, and the A2D converter, according to one embodiment of the invention. **Fig. 13** also includes a machine-readable storage medium to execute computer readable instructions to perform the methods of various embodiments. Elements of embodiments are also provided as a machine-readable medium (e.g., 1362) for storing the computer-executable instructions (e.g., instructions to implement the flowcharts of **Figs. 7-8**). The machine-readable medium may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, or other type of machine-readable media suitable for storing electronic or computer-executable instructions. For example, embodiments of the invention may be downloaded as a computer program (e.g., BIOS) which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

In one embodiment, the system 1300 includes, but is not limited to, a desktop computer, a laptop computer, a netbook, a tablet, a notebook computer, a personal digital assistant (PDA), a server, a workstation, a cellular telephone, a mobile computing device, a smart phone, an Internet appliance or any other type of computing device. In another embodiment, the system 1300 implements the methods disclosed herein and may be a system on a chip (SOC) system.

In one embodiment, the processor 1310 has one or more processing cores 1312 and 1312N, where 1312N represents the Nth processor core inside the processor 1310 where N is a positive integer. In one embodiment, the system 1300 includes multiple processors including 1310 and 1305, where processor 1305 has logic similar or identical to logic of processor 1310. In one embodiment, the processing core 1312 includes, but is not limited to, pre-fetch logic to fetch instructions, decode logic to decode the instructions, execution logic to execute instructions and the like. In one embodiment, the processor 1310 has a cache memory 1316 to cache instructions and/or data of the system 1300. In another embodiment of the invention, the cache memory 1316 includes level one, level two and level three, cache memory, or any other configuration of the cache memory within the processor 1310.

In one embodiment, processor 1310 includes a memory control hub (MCH) 1314, which is operable to perform functions that enable the processor 1310 to access and communicate with a memory 1330 that includes a volatile memory 1332 and/or a non-volatile memory 1334. In one embodiment, the MCH 1314 is the same as the memory controller 101 of the embodiments discussed herein.

In one embodiment, the processor 1310 is operable to communicate with the memory 1330 and a chipset 1320. In one embodiment, the processor 1310 is also coupled to a wireless antenna 1378 to communicate with any device configured to transmit and/or receive wireless signals. In one embodiment, the wireless antenna interface 1378 operates in accordance with, but is not limited to, the IEEE 802.11 standard and its related family, HomePlug AV (HPAV), Ultra Wide Band (UWB), Bluetooth, WiMAX, or any form of wireless communication protocol.

In one embodiment, the volatile memory 1332 includes, but is not limited to, Synchronous Dynamic Random Access Memory (SDRAM), Dynamic Random Access Memory (DRAM), RAMBUS Dynamic Random Access Memory (RDRAM), and/or any other type of random access memory device. The non-volatile memory 1334 includes, but is not limited to, flash memory, phase change memory (PCM), read-only memory (ROM), electrically erasable programmable read-only memory (EEPROM), or any other type of non-volatile memory device.

The memory 1330 stores information and instructions to be executed by the processor 1310. In one embodiment, memory 1330 may also store temporary variables or other intermediate information while the processor 1310 is executing instructions. In one embodiment, chipset 1320 connects with processor 1310 via Point-to-Point (PtP or P-P) interfaces 1317 and 1322. In one embodiment, chipset 1320 enables processor 1310 to connect to other modules in the system 1300. In one embodiment of the invention, interfaces 1317 and 1322 operate in accordance with a PtP communication protocol such as the Intel® QuickPath Interconnect (QPI) or the like.

In one embodiment, the chipset 1320 is operable to communicate with the processor 1310, 1305, display device 1340, and other devices 1372, 1376, 1374, 1360, 1362, 1364, 1366, 1377, etc. In one embodiment, the chipset 1320 is also coupled to a wireless antenna 1378 to communicate with any device configured to transmit and/or receive wireless signals.

In one embodiment, chipset 1320 connects to a display device 1340 via an interface 1326. In one embodiment, the display 1340 includes, but is not limited to, liquid crystal display (LCD), plasma, cathode ray tube (CRT) display, or any other form of visual display device. In one embodiment of the invention, processor 1310 and chipset 1320 are merged into a single SOC. In addition, the chipset 1320 connects to one or more buses 1350 and 1355 that interconnect various modules 1374, 1360, 1362, 1364, and 1366. In one embodiment, buses 1350 and 1355 may be interconnected together via a bus bridge 1372 if there is a mismatch in bus speed or communication protocol. In one embodiment, chipset 1320 couples with, but is not limited to, a non-volatile memory 1360, a mass storage device(s) 1362, a keyboard/mouse 1364, and a network interface 1366 via interface 1324, smart TV 1376, consumer electronics 1377, etc.

In one embodiment, the mass storage device 1362 includes, but is not limited to, a solid state drive, a hard disk drive, a universal serial bus flash memory drive, or any other form of computer data storage medium. In one embodiment, network interface 1366 is implemented by any type of well known network interface standard including, but not limited to, an Ethernet interface, a universal serial bus (USB) interface, a Peripheral Component Interconnect (PCI) Express interface, a wireless interface and/or any other suitable type of interface. In one embodiment, the wireless interface operates in accordance with, but is not limited to, the IEEE 802.11 standard and its related family, HomePlug AV (HPAV), Ultra Wide Band (UWB), Bluetooth, WiMAX, or any form of wireless communication protocol.

While the modules shown in **Fig. 13** are depicted as separate blocks within the system 1300, the functions performed by some of these blocks may be integrated within a single semiconductor circuit or may be implemented using two or more separate integrated circuits. For example, although the cache memory 1316 is depicted as a separate block within the processor 1310, the cache memory 1316 can be incorporated into the processor core 1312 respectively. In one embodiment, the system 1300 may include more than one processor/processing core in another embodiment of the invention.

Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

While the invention has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description. One such alternative for the A2D converter is shown by **Fig. 14**.

Fig. 14 illustrates transistor level components 1400 of the A2D converter 900, according to another embodiment of the invention. For purposes of not repeating the description of components discussed with previous figures, only the main differences between **Fig. 10** and **Fig. 14** are discussed. In this alternative embodiment, the A2D converter 900 provides two circuit

paths for measuring current levels input at 1101. In one embodiment, when the to-be measured current through 1101 is a negative current, then switch 1401 is closed while switch 1402 is open (i.e., no current flows through transistors M3 and M4). In one embodiment, when the to-be measured current through 1101 is a positive current then switch 1401 is open while switches
5 1402 are closed ((i.e., current flows through transistors M3 and M4).

In one embodiment, when the A2D converter 900 is operable to measure voltage at node 905, switch 1405 is closed and fixed bias voltage is supplied to transistor M2 via an analog multiplexer 1407. In one embodiment, fixed bias is also provided to transistor M5. In such an embodiment, the signals 1110 and 1109 toggle at the same frequency as the frequency of the
10 counter 910. In one embodiment, when the A2D converter 900 is operable to measure time different e.g., pulse width of the strobe signal 1110, then switch 1405 is open and fixed bias voltage is supplied to transistor M2 via the analog multiplexer 1407. In the above embodiments, signal 1406 is used to discharge the node 905 after the comparator 906 trips. In one embodiment, signals 1401, 1402, 1403, 1404, and 1406 are generated by a finite state machine
15 (not shown).

The embodiments of the invention are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

CLAIMS

We claim:

1. An apparatus comprising:
5 a driver to transmit a signal on an input-output (I/O) pad, the signal on the I/O pad having a voltage swing and a duty cycle; and
an adjustment unit, coupled to the driver, to receive the signal from the I/O pad transmitted by the driver and to generate voltage swing and duty cycle control signals for adjusting the voltage swing and duty cycle of the signal on the I/O pad respectively.
10
2. The apparatus of claim 1 further comprises:
a duty cycle corrector, coupled to the driver and the adjustment unit, to receive the duty cycle control signal for adjusting a duty cycle of a signal for transmission by the driver.
- 15 3. The apparatus of claim 1, wherein the signal transmitted by the driver to the I/O pad is a differential signal.
4. The apparatus of claim 3, wherein the adjustment unit comprises:
a multiplexer to receive multiple signals including: a common mode voltage signal of the
20 differential signal from the I/O pad transmitted by the driver, a reference voltage signal, and the differential signal from the I/O pad;
a low-pass-filter to receive an output of the multiplexer and to generate a filtered signal;
a comparator to receive the filtered signal and to generate an output signal; and
a finite state machine to receive the comparator output signal and to generate the voltage
25 swing and duty cycle control signals for adjusting the voltage swing and duty cycle of the signal on the I/O pad respectively.
5. The apparatus of claim 4, wherein the multiplexer is operable to select the
common mode voltage signal and the reference voltage signal for generating the voltage swing
30 control signal.
6. The apparatus of claim 4, wherein the multiplexer is operable to select the
differential signal from the I/O pad for generating the duty cycle control signal.

7. The apparatus of claim 4, wherein the low pass filter is a differential low pass filter, and wherein the filtered signal is a differential filtered signal for input to the comparator.

8. The apparatus of claim 4, wherein the comparator is operable to cancel offset.

5

9. The apparatus of claim 4, wherein the finite state machine operates at a frequency less than the frequency of the signal on the I/O pad.

10. The apparatus of claim 1, wherein the driver receives the voltage swing control signal to adjust a bias level of a transistor in the driver to adjust the voltage swing of the signal transmitted by the driver.

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11. The apparatus of claim 4 further comprises a bypass logic unit to bypass the low pass filter when the adjustment unit is configured to generate the voltage swing control signal.

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12. The apparatus of claim 1, wherein the adjustment unit is operable to generate the voltage swing control signal for adjusting the voltage swing of the signal on the I/O pad prior to generating the duty cycle control signal for adjusting the duty cycle of the signal on the I/O pad.

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13. A method comprising:
initiating voltage swing and duty cycle adjustment operation for every input-output (I/O) lane of a processor having multiple I/O pads by:
transmitting a signal on an I/O pad of the I/O lane, wherein the signal on the I/O pad having a voltage swing and a duty cycle;
receiving the signal from the I/O pad; and
generating voltage swing and duty cycle control signals for adjusting the voltage swing and duty cycle of the signal on the I/O pad.

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14. The method of claim 13 further comprises:
prior to initiating the voltage swing and duty cycle adjustment operation, initiating a compensation operation for all I/O lanes of the processor for process, voltage, and temperature variations in signals at the multiple I/O pads for all I/O lanes, the compensation operation to generate compensation codes;

30

freezing the compensation codes; and

initiating the voltage swing and duty cycle adjustment operation.

35

15. The method of claim 14 further comprises, in response to completing the voltage swing and duty cycle adjustment operation:

unfreezing the compensation codes; and

5 continuing the compensation operation for all I/O lanes in response to unfreezing the compensation codes.

16. A system comprising:

a memory; and

10 a processor coupled to the memory, the processor comprising:

a driver to transmit a signal on an input-output (I/O) pad, the signal on the I/O pad having a voltage swing and a duty cycle; and

an adjustment unit, coupled to the driver, to receive the signal from the I/O pad transmitted by the driver and to generate voltage swing and duty cycle control signals for adjusting the
15 voltage swing and duty cycle of the signal on the I/O pad respectively.

17. The system of claim 16, wherein the processor further comprises:

a duty cycle corrector, coupled to the driver and the adjustment unit, to receive the duty cycle control signal for adjusting a duty cycle of a signal for transmission by the driver.

20

18. The system of claim 16, wherein the signal transmitted by the driver to the I/O pad is a differential signal, and wherein the adjustment unit comprises:

a multiplexer to receive multiple signals including: a common mode voltage signal of the differential signal from the I/O pad transmitted by the driver, a reference voltage signal, and the
25 differential signal from the I/O pad;

a low-pass-filter to receive an output of the multiplexer and to generate a filtered signal;

a comparator to receive the filtered signal and to generate an output signal; and

a finite state machine to receive the comparator output signal and to generate the voltage swing and duty cycle control signals for adjusting the voltage swing and duty cycle of the signal
30 on the I/O pad respectively.

19. The system of claim 18, wherein the multiplexer is operable to select the common mode voltage signal and the reference voltage signal for generating the voltage swing control signal, and wherein the multiplexer is operable to select the differential signal from the I/O pad
35 for generating the duty cycle control signal.

20. The system of claim 18, wherein the finite state machine operates at a frequency less than the frequency of the signal on the I/O pad.

5 21. The system of claim 18, wherein the driver receives the voltage swing control signal to adjust a bias level of a transistor in the driver to adjust the voltage swing of the signal transmitted by the driver.

10 22. The system of claim 18 further comprises a bypass logic unit to bypass the low pass filter when the adjustment unit is configured to generate the voltage swing control signal.

15 23. The system of claim 16, wherein the adjustment unit is operable to generate the voltage swing control signal for adjusting the voltage swing of the signal on the I/O pad prior to generating the duty cycle control signal for adjusting the duty cycle of the signal on the I/O pad.

24. An analog-to-digital (A2D) converter comprising:
a capacitor with first and second terminals;
a comparator to compare a voltage signal on the first terminal with a reference voltage
signal level;
20 a current source to charge or discharge the capacitor; and
a first switch, coupled between the current source and the first terminal, the first switch to control the speed of charging or discharging the capacitor.

25 25. The A2D converter of claim 24 further comprises a phase detector to compare phases of two signals and to generate a signal to control the switching speed of the first switch.

26. The A2D converter of claim 25 further comprises a multiplexer to generate the two signals by selecting the two signals from multiple signals including phase delayed signals and clock signals.

30 27. The A2D converter of claim 24 further comprises a counter to receive an output of the comparator and to count up or down in response to a reset signal, where the counter to output a signal which represents one of:

35 a current input to the current source;
a pulse width of a signal input to the first switch; and

a voltage, on the first terminal of the capacitor, relative to a reference voltage.

28. The A2D converter of claim 27 further comprises a second switch to discharge the capacitor in response to the reset signal.

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29. The A2D converter of claim 24, wherein the second terminal of the capacitor is connected to a ground terminal, and wherein the comparator is operable to cancel offset.

30. The A2D converter of claim 24, wherein the current source is coupled to a current mirror for providing a current to charge the capacitor, and wherein current source is operable to provide a fixed current for charging the capacitor when the first switch receives a time domain signal having a pulse width.

10

15

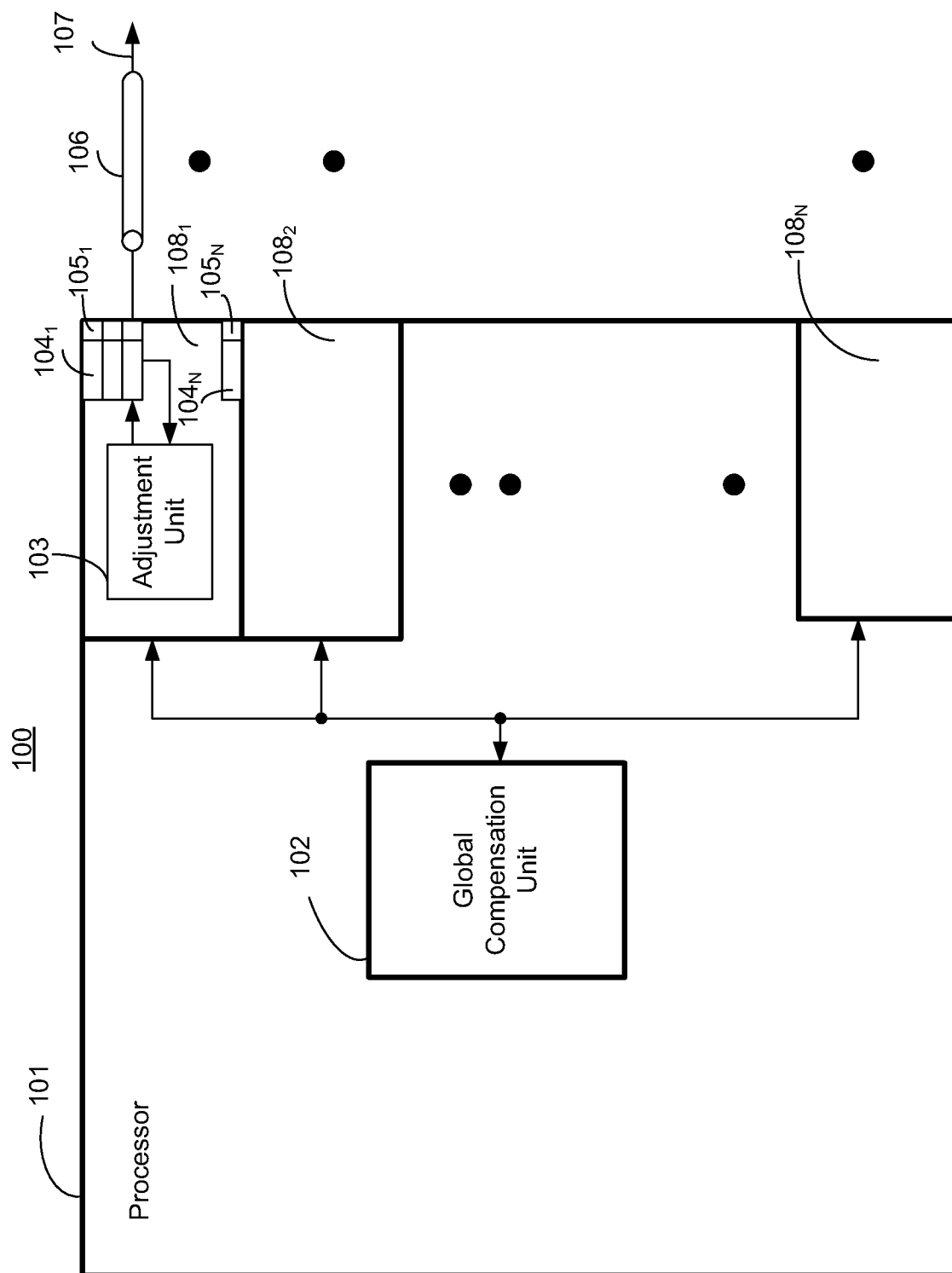


FIG. 1

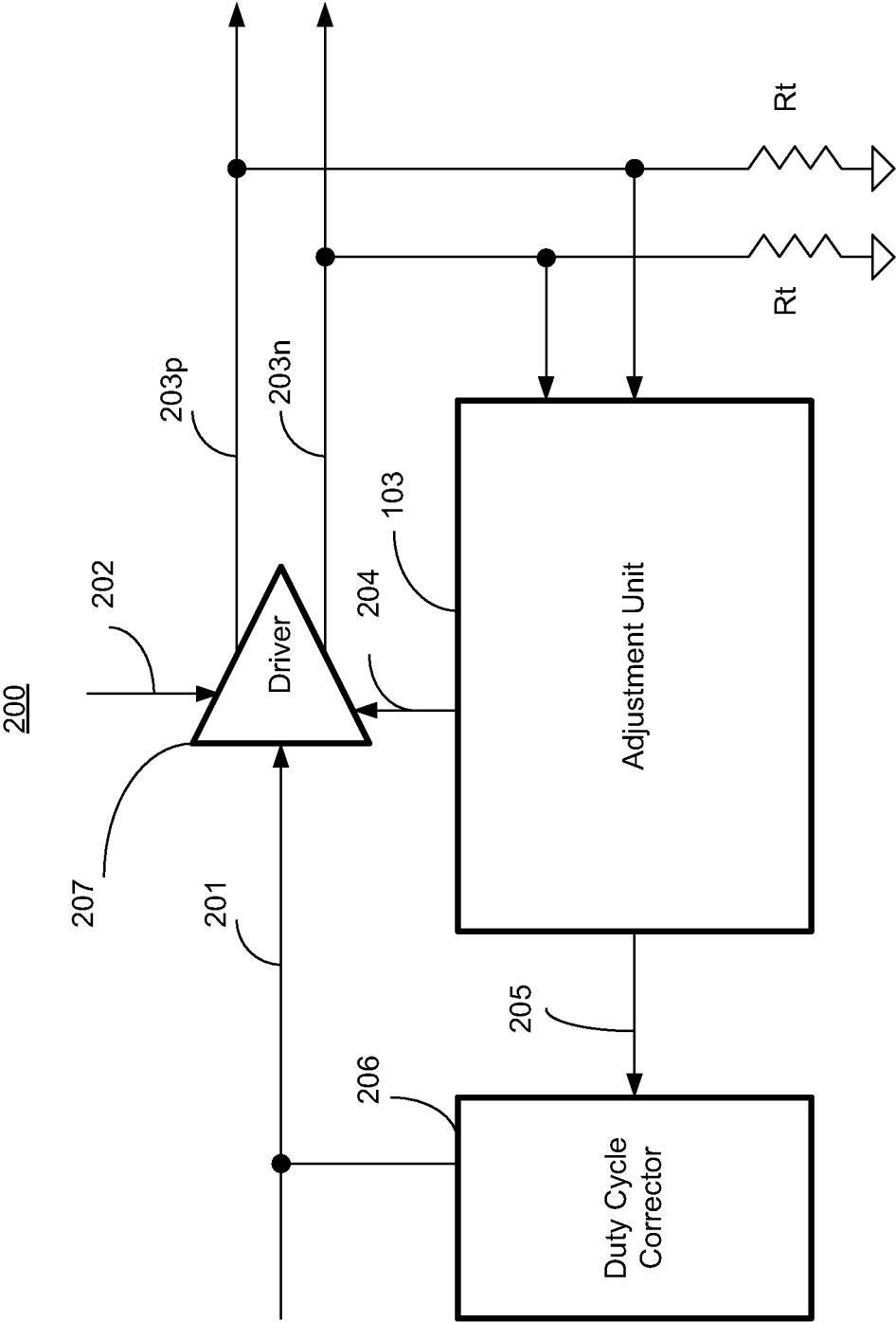
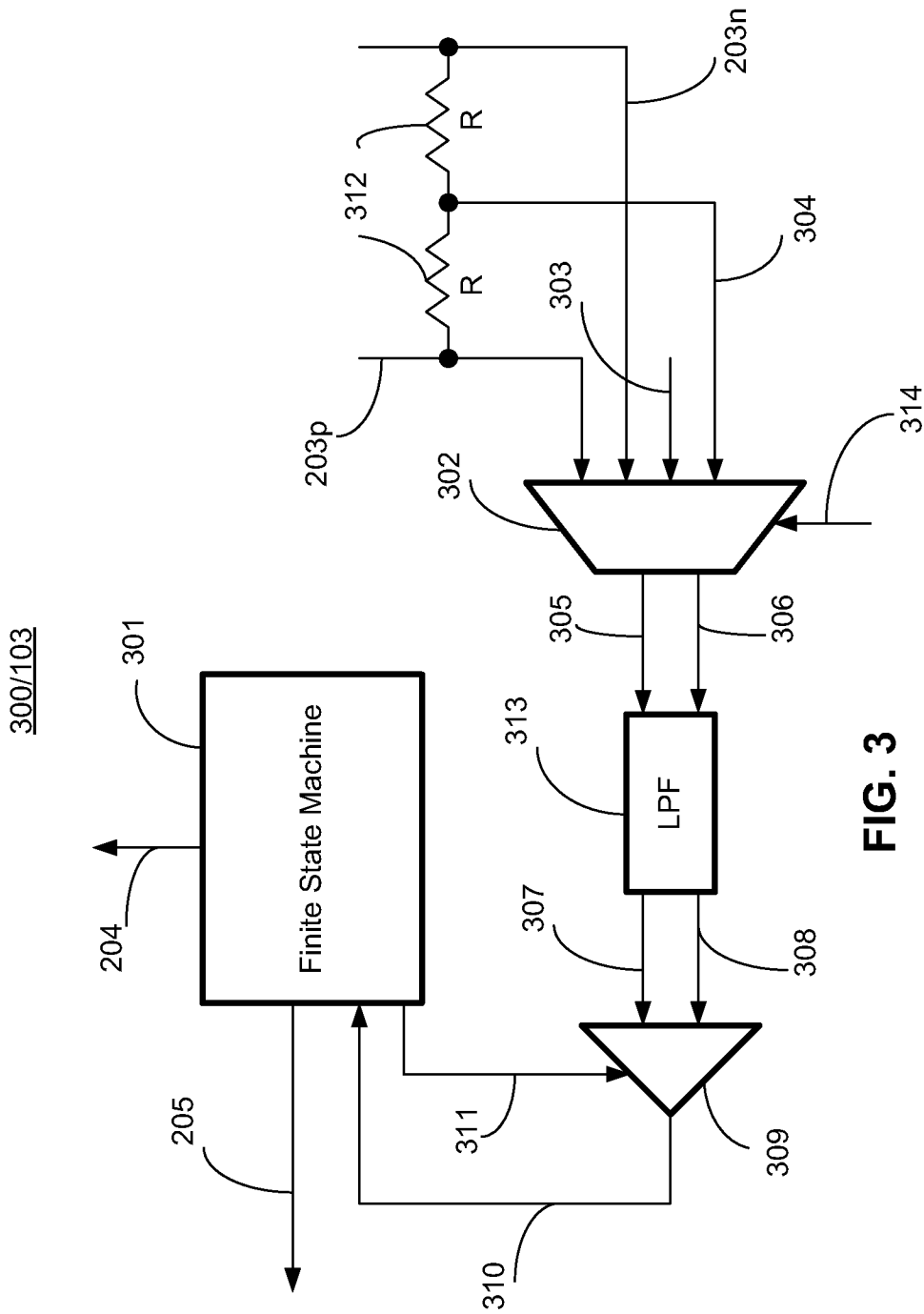


FIG. 2



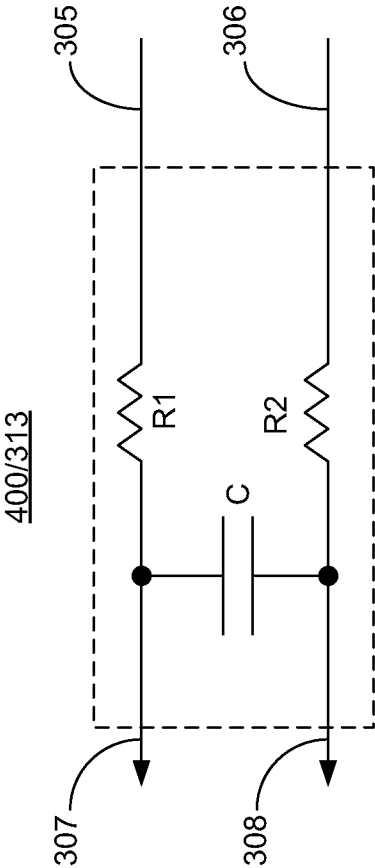


FIG. 4A

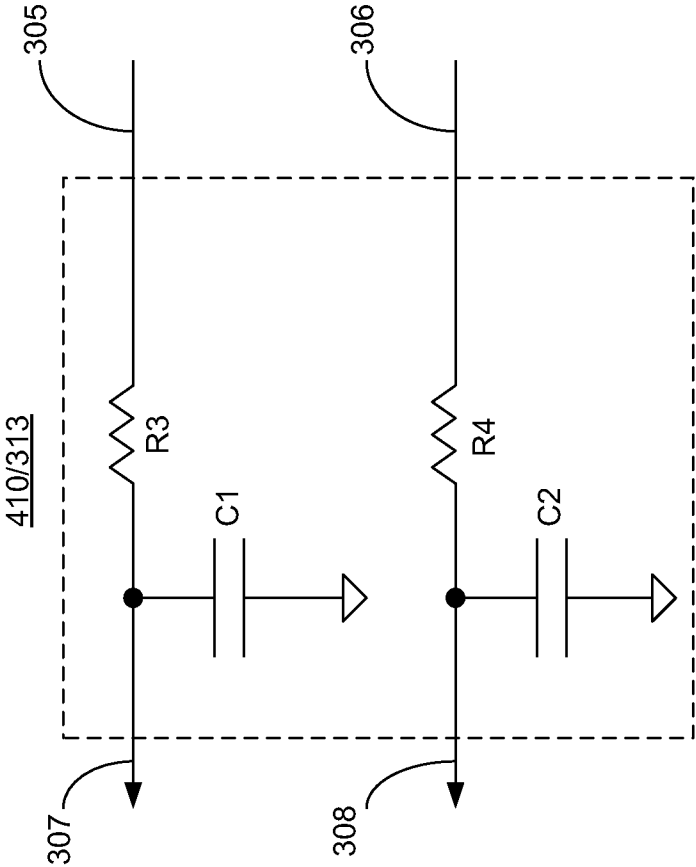


FIG. 4B

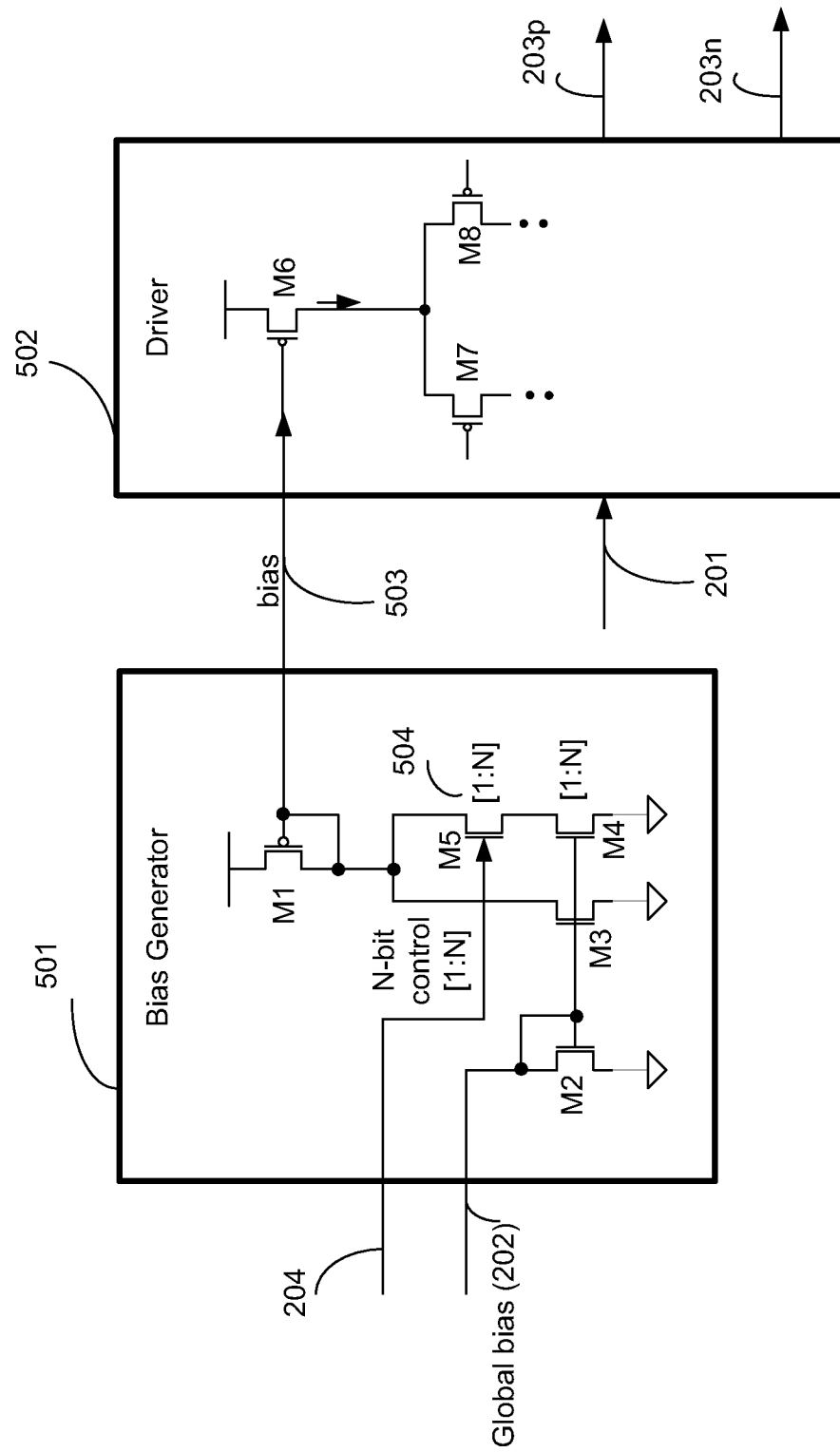
500/207

FIG. 5

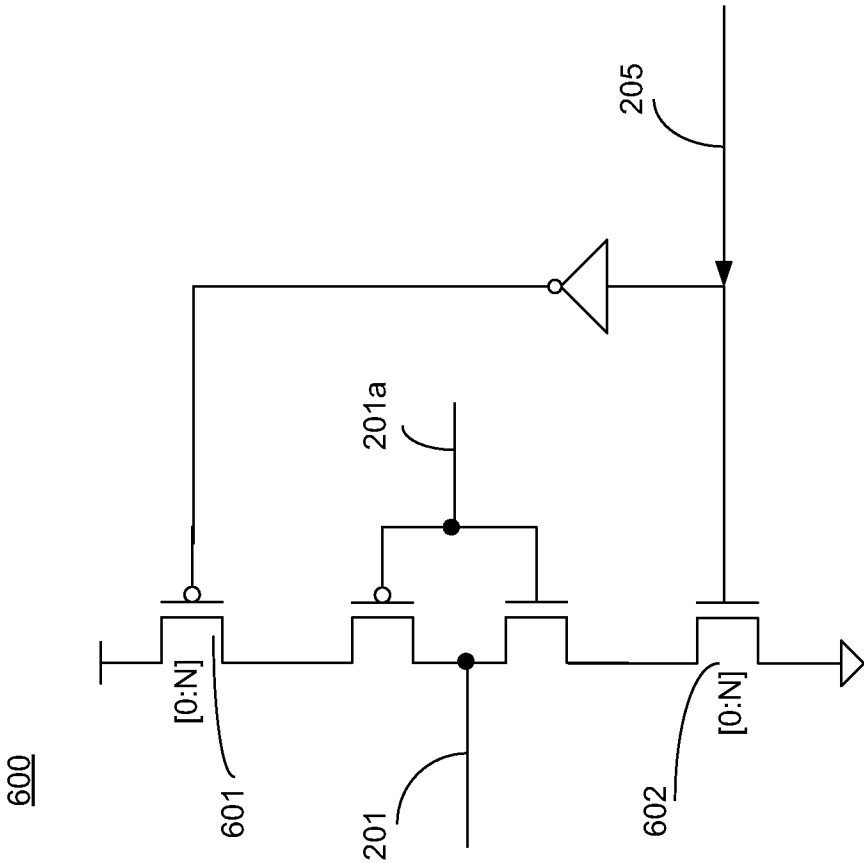
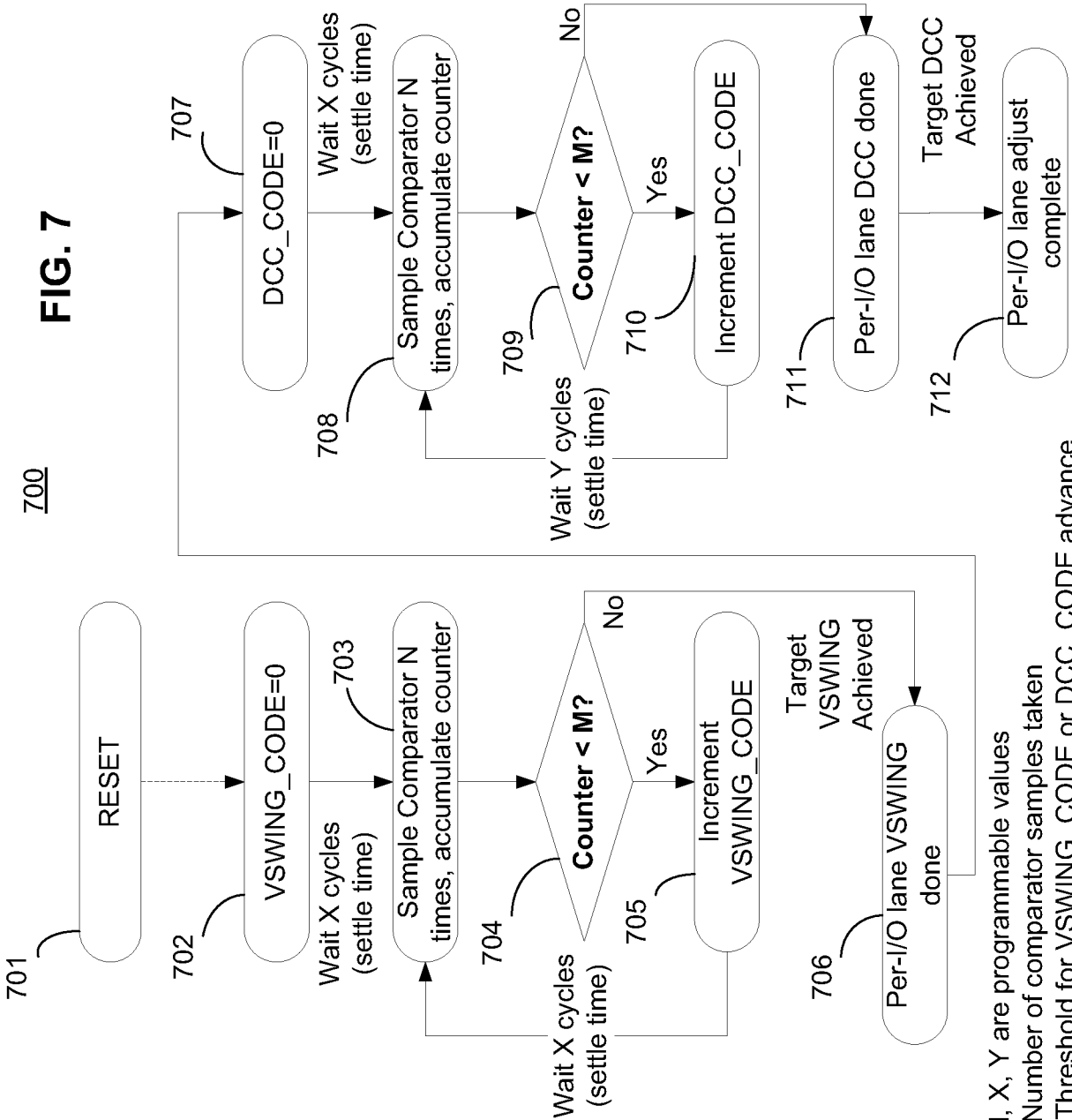


FIG. 6



- N, M, X, Y are programmable values
- N = Number of comparator samples taken
- M = Threshold for VSWING_CODE or DCC_CODE advance
- X = Number of wait cycles needed to let new Vswing value settle
- Y = Number of wait cycles needed to let new Duty-Cycle value settle

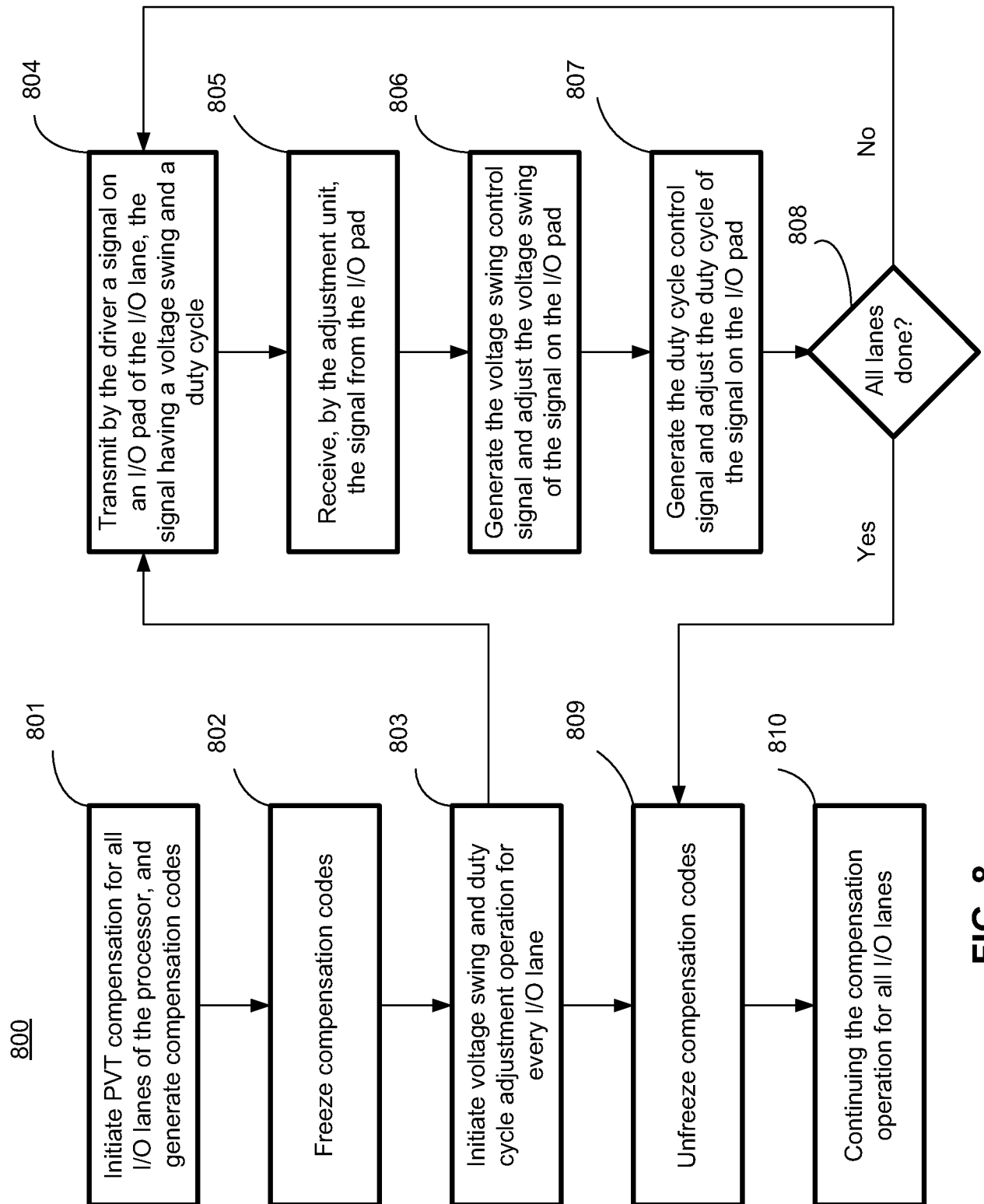


FIG. 8

950

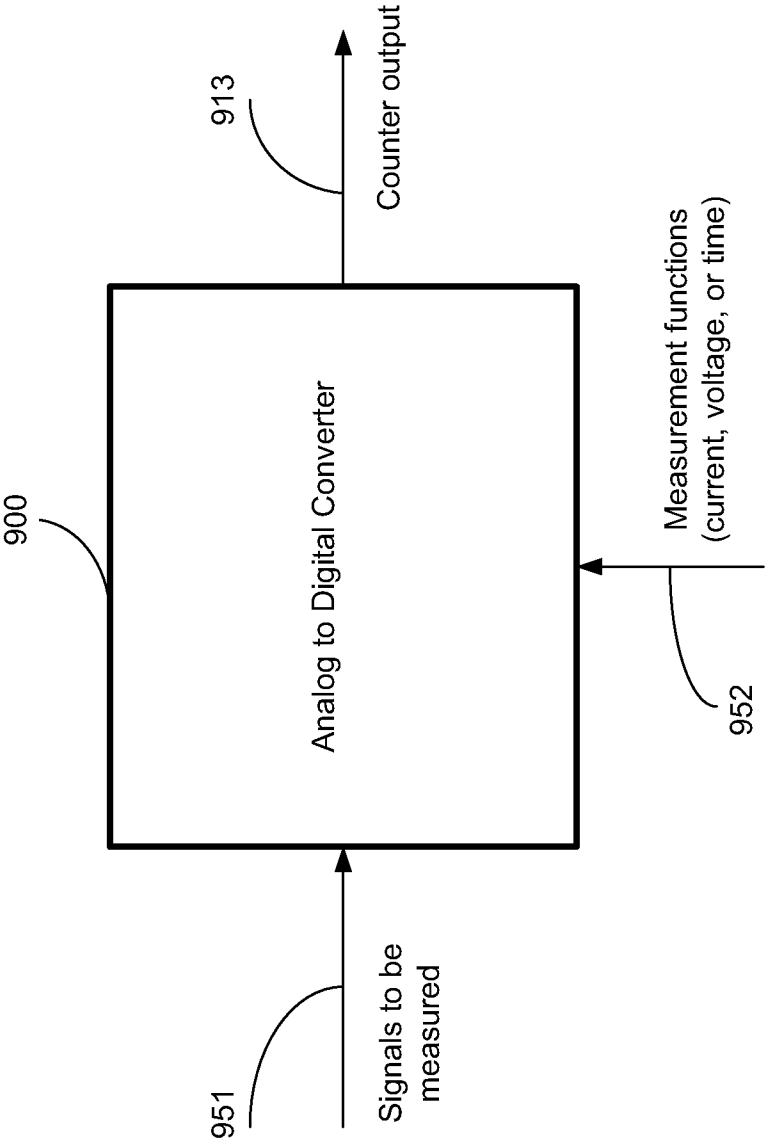


FIG. 9A

900

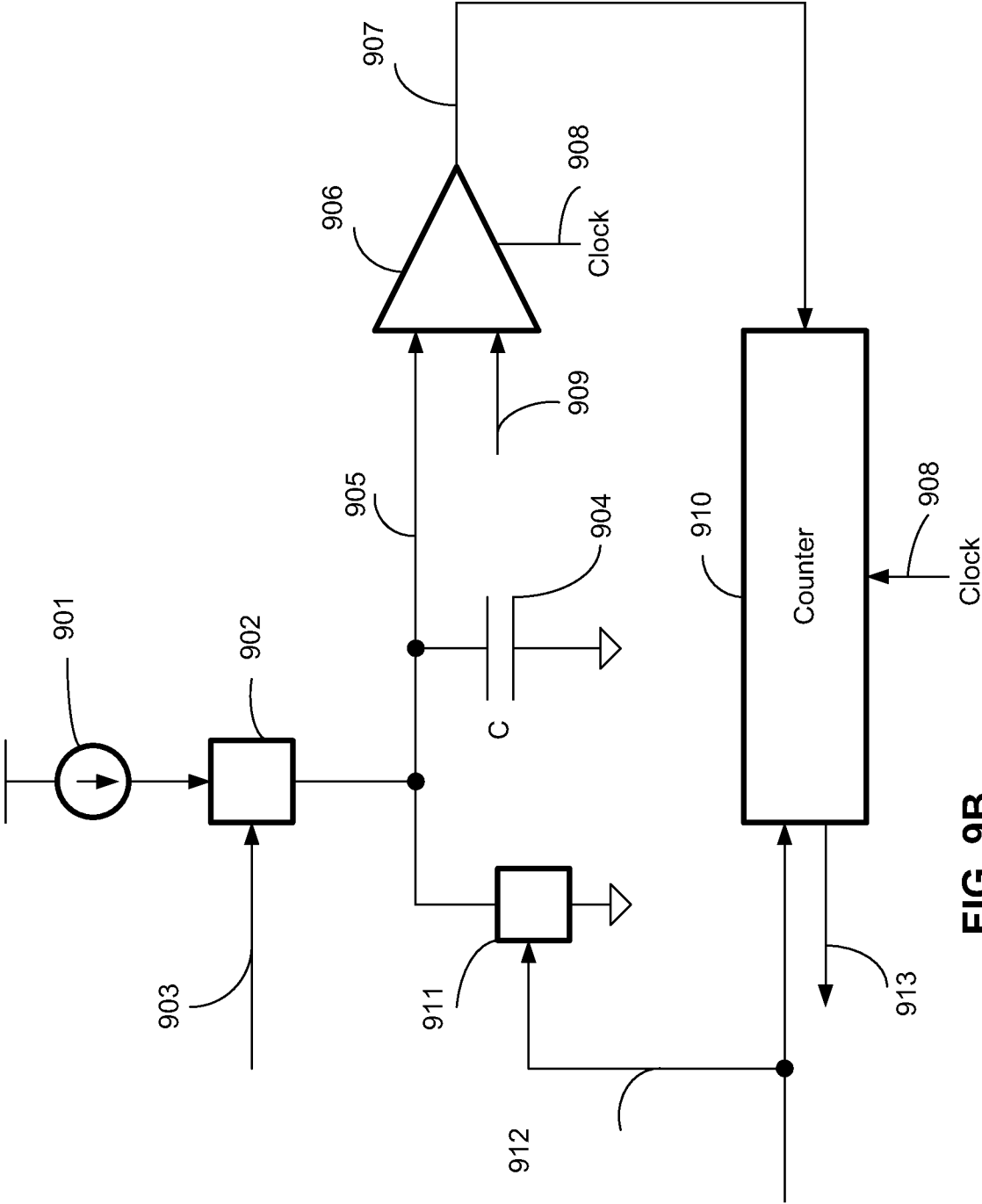
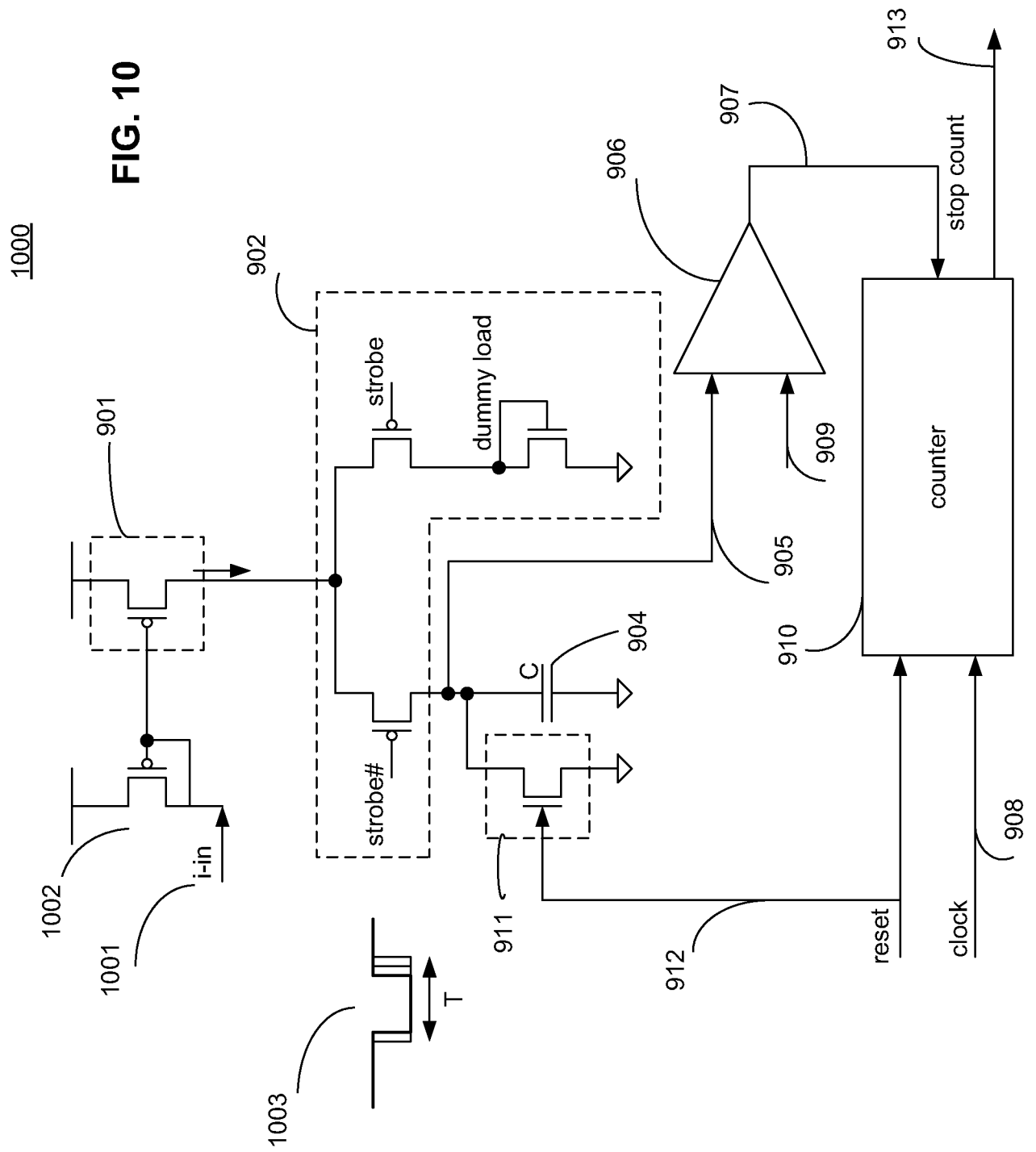


FIG. 9B

FIG. 10



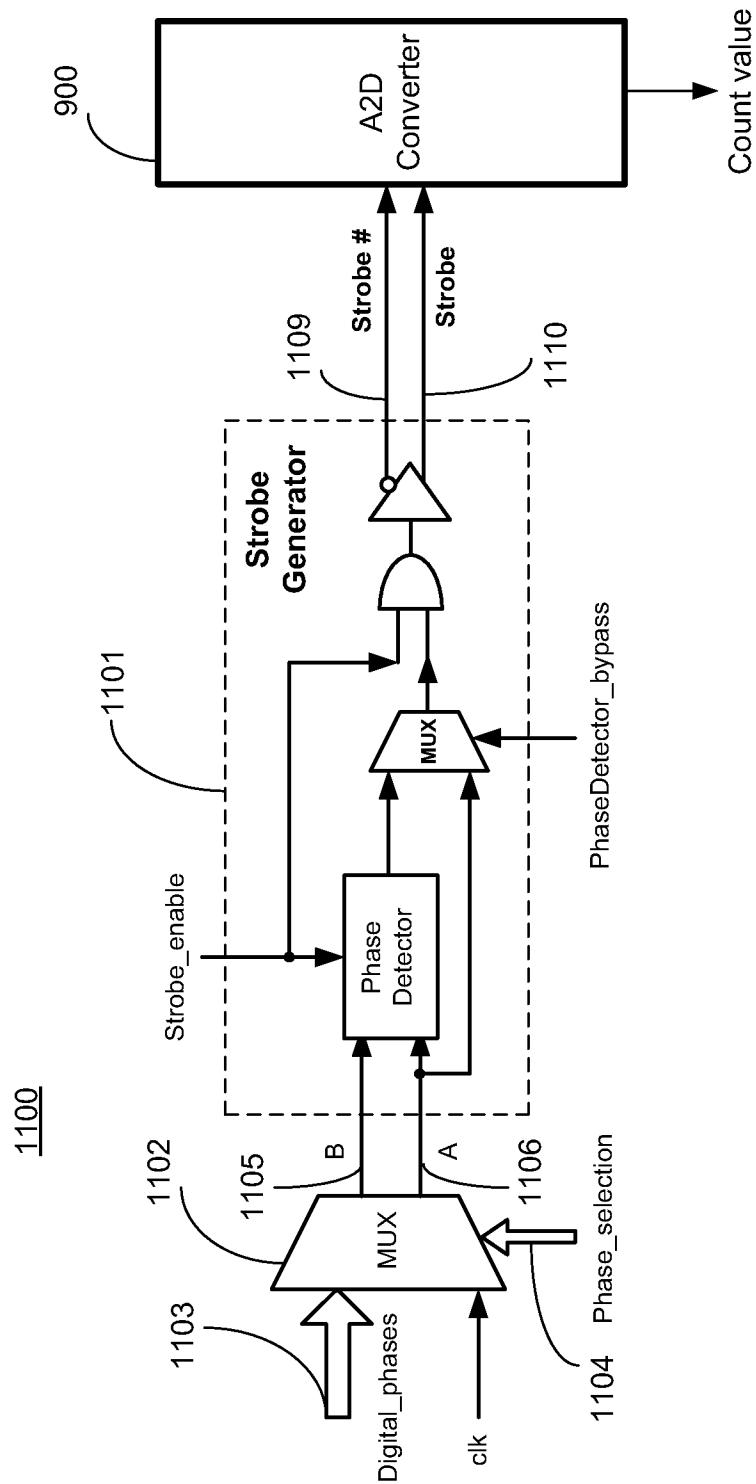


FIG. 11

1200

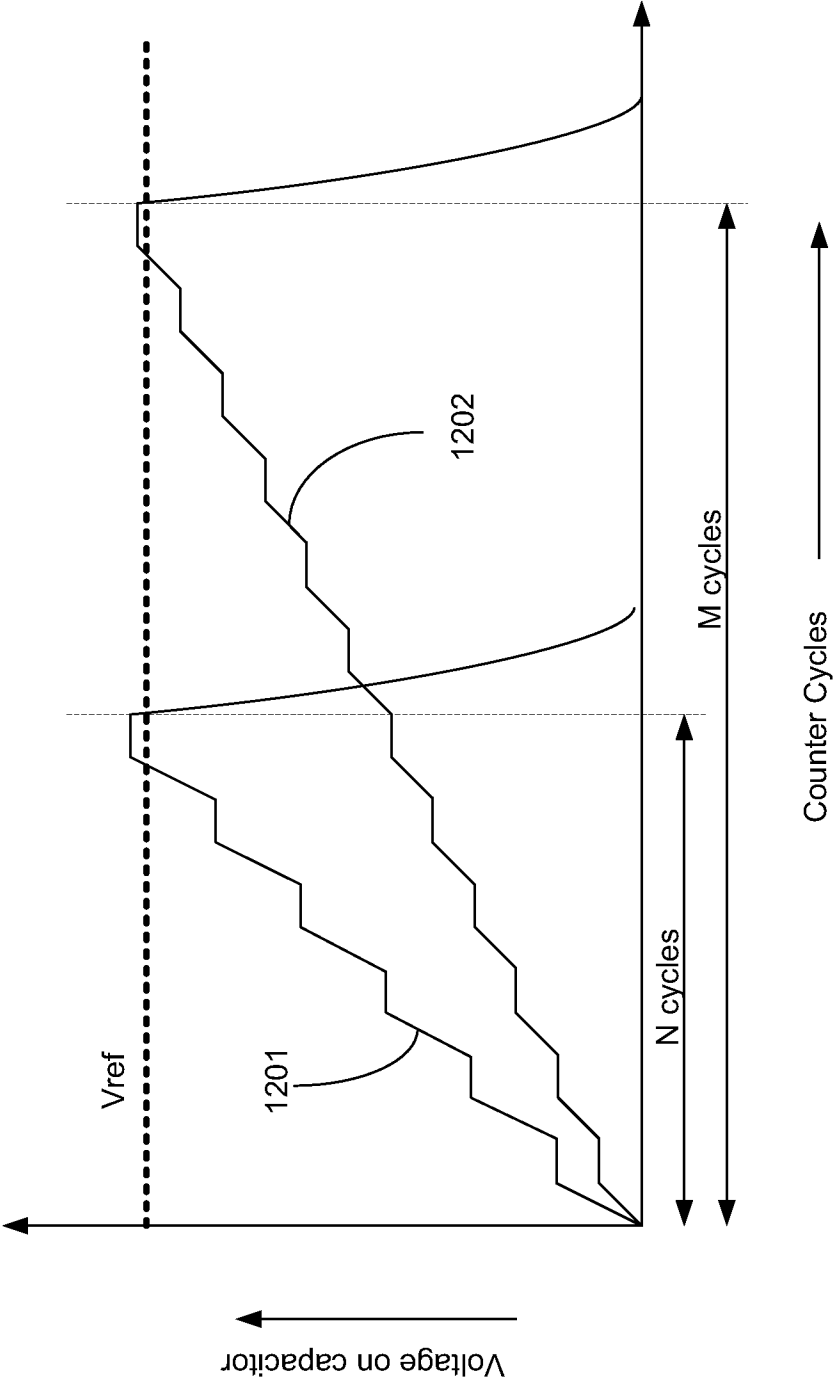


FIG. 12

