GRAPHIC DISPLAY SYSTEM

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ABSTRACT

Incremental plotting instructions are received from a computer for bringing about a point-plotting display on a cathode-ray tube. Plotting inputs increment a counter means for accumulating a total representing cathode-ray tube deflection, with the cathode-ray tube being coupled to the counter means via a digital-to-analog converter means. Inputs to the digital-to-analog converter means are positionable relative to the counter stages for changing the scale of the display. Also, a write-through frame is positionable relative to a stored image for selecting a portion of a given display for subsequent presentation. The offset position of the frame is stored in an offset register by means of a digital servomechanism system. A function of the complement of the offset is added to the aforementioned counter means for offsetting a subsequent display.

38 Claims, 16 Drawing Figures
GRhAPHIC DISPLAY SYSTEM

BACKGROUND OF THE INVENTION

Digital computers generate and process a massive amount of data which oftentimes is more intelligible to the user in a graphic plotted form, e.g., as a graph, a curve, drawing, or the like. A successful scheme for presenting graphic information provides incremental plotting instructions to a mechanical plotter which moves in fixed increments along two orthogonal axes. For each increment, an instruction also causes a plotting pen to write, or not to write, on a plotting surface. The inertia of mechanical plotters limits the rate of incrementing to about 400 steps per second and the rate of changing the pen state to about 10 changes per second. Most often, the plotting information is stored by a computer on magnetic tape. The tape is then played back off-line at a data rate compatible with the mechanical plotter. This rate is very slow compared to the speed of the computer itself.

Cathode-ray tubes, on the other hand, are much faster and, for the purpose of recording incremental digital computer outputs, a bistable rect view- ing storage tube is advantageously employed. Such a tube will almost indefinitely display plotting information once delivered thereto. Modern storage tube technology indicates that dot-writing speeds of 4 microseconds are within reach. With a total writing rate of 250 kilocharacters per second, a storage tube is potentially more than a thousand times faster than a mechanical plotter. However, of course, the storage tube does not as easily deliver a hard copy of the desired plot, and moreover, the hard copy plot of a mechanical plotter is much larger than the screen of a cathode-ray tube storage tube. Thus, both types of output devices have their advantages, and furthermore, these devices may be employed together for obtaining an "advanced" look at one or more plots before the same information is slowly delivered to a mechanical plotter.

Cathode-ray tubes and even storage cathode-ray tubes have been employed heretofore to provide a graphic display of computer information. However, prior systems are frequently not flexible enough for selecting and providing a display of a given plot from a massive amount of stored data. For example, it may be desired to implement a small part of totally available incremental plotting instructions for displaying in magnified fashion a portion of the total available information. The present invention enables the selection of, and magnification of, a given display derived from a portion of the data available.

SUMMARY OF THE INVENTION

According to the present invention, a graphic display system includes counter means responsive to successive increments of plotting inputs for accumulating a total indicative of desired deflection in an analog display. The analog display is coupled to the counter means by way of a digital-to-analog converter, and means adjust the connection of the converter relative to stages of the counter means. Adjustment in a first sense in the direction of less significant bit portions expands the scale of the analog display. Adjustment in the opposite sense compresses the scale of the analog display.

A write-through cursor is developed by counting the output of a signal generator or a clock in the aforementioned counter means and providing a related count to an offset register. The signal generator or clock is continuously enabled until the count accumulated in the offset register compares with a selected offset. A write-through frame is supplied in analog fashion to the display concurrently with the cursor.

To provide a subsequent display selected by the cursor and frame, a function of the complement of the contents of the offset register is added to the counter means together with a second repetition of incremental plotting inputs. A subsequent presentation will be blown up or magnified according to the selectable frame size, and successive reploting through several steps of diminishing plot scale can be accomplished in this manner to provide a "zoom" feature.

The analog display is preferably a bistable storage tube which retains a plot almost indefinitely after having once received the input information. The plot is erased prior to the presentation of a subsequent plot having a different scale, i.e., before the presentation of a subsequent, more magnified plot.

It is accordingly an object of the present invention to provide an improved graphic display system.

It is a further object of the present invention to provide an improved graphic display system for expanding or compressing the scale of the display to provide a magnified or demagnified presentation.

It is a further object of the present invention to provide an improved graphic display system for providing a presentation corresponding to a predetermined portion or sector of a previous display, and with size selection thereof.

It is a further object of the present invention to provide an improved graphic display system for providing a presentation corresponding to a predetermined portion or sector of a previous display in which the location of and magnification of such sector is selectable by means of an adjustable cursor.

It is another object of the present invention to provide an improved graphic display system for providing a presentation corresponding to a predetermined portion or sector of a previous display in which the location of or magnification of such sector is selectable by means of an adjustable cursor, said cursor being provided with a write-through frame for selecting a display sector size.

It is another object of the present invention to provide an improved graphic display system having "zoom" features for successively enlarging successively selectable display portions.

It is another object of the present invention to provide an improved digital servomechanism system.

The subject matter which I regard as my invention is particularly pointed out and distinctly claimed in the concluding portion of this specification. The invention, however, both as to organization and method of operation, together with further advantages and objects thereof, may best be understood by reference to the following description taken in connection with the accompanying drawings wherein like reference characters refer to like elements.

DRAWINGS

FIG. 1 is a simplified block diagram of a circuit according to the present invention;
FIG. 2 is a flow view of a pair of cathode-ray tube presentations illustrating a sectoring operation according to the present invention;
FIG. 3 is a line scale illustrating a preloading operation according to the present invention;
FIG. 4 is a first illustration of a pair of cathode-ray tube displays illustrating a "zoom" operation of the present invention;
FIG. 5 is a second illustration of a pair of cathode-ray tube displays further illustrating a "zoom" operation of the present invention;
FIG. 6 is an overall block diagram of the circuit according to the present invention;
FIG. 7 is a block diagram of an up-down counter according to the present invention;
FIG. 8 is a diagram of a switching matrix circuit according to the present invention;
FIG. 9 is a schematic diagram of a digital-to-analog converter;
FIG. 10 is a schematic diagram of scale switches employed according to the present invention;
FIG. 11 is a diagram of a compare circuit according to the present invention;
FIG. 12 is a truth table for operation of a compare circuit of which the FIG. 11 circuit is part;
FIG. 13 is a diagram of a Z-axis inhibit circuit according to the present invention; FIG. 14 is a schematic diagram of a frame generator according to the present invention; FIG. 15 is a diagram of a first possible location of a frame relative to a cathode-ray tube presentation; and FIG. 16 is a diagram of a second possible location of a frame relative to a cathode-ray tube presentation according to the present invention.

DETAILED DESCRIPTION

Referring to FIG. 1, a simplified block diagram of the graphic display system according to the present invention, a computer 10 provides digital incremental plotting inputs for incrementing a plotting apparatus in two orthogonal directions. Only one such direction will be considered for simplicity of explanation, it being understood that substantially the same explanation would apply with respect to either orthogonal axis. The plotting inputs characteristically comprise a series of pulses which, if supplied to a mechanical plotter, would move the plotting mechanism stepwise in a given position of the computer output indicated at 12, and applied to an up-down binary counter 14. This counter, as indicated, is capable of counting in either direction according to a signal applied thereto by the computer. The computer also supplies an output at 16 to summing point 18 controlling the Z-axis of a bistable storage cathode-ray tube.

As computer incremental outputs are delivered at 12, the up-down counter 14 attains a total accumulation numerically indicative of the deflection in a given axis, say the X-axis, desired for the display. Outputs 20 from the up-down counter are provided from successively more significant binary bit positions in the counter and are connected via switching means 22 to provide inputs for digital-to-analog converter 24. The switching of stages 22 is controlled by a present scale latches 26, selected by pushbutton scale switches 28. Switching means 22 also includes connections 30 at the right hand end of up-down counter 14 for coupling the most significant bit stages of up-down counter 14 to Z-axis inhibit circuit 32.

Switching means 22 operates to connect the 10 inputs of digital-to-analog converter 24 to 10 selected outputs of up-down counter 14. All of the inputs of the digital-to-analog converter 24 are changed at the same time so that for switching in a first sense, all inputs to the digital-to-analog converter can be obtained from successively less significant bit positions or stages of the up-down counter, and for movement of switching means 22 in the opposite direction, the input to the digital-to-analog converter can be connected to successively more significant bit positions or stages of the up-down counter. At the same time, connections 30 make contact with the most significant bit positions or stages which do not, in a given switching position, provide inputs to the digital-to-analog converter 24.

The digital-to-analog converter converts the binary digital information to an analog voltage for application to summing point 34 of deflection means of storage CRT 36, for example the X deflection means thereof. When switch 22 moves the 10 inputs of the digital-to-analog converter to more significant bit positions, the effect is one of providing compressed information to the digital-to-analog converter. Thus, only the more significant portion of the count in the counter will move the analog display, and the relative display value of each bit will be less than if the switch were in a lower position. If the switching means 22 is moved in the opposite sense, whereby less significant bit positions are applied as an input to the digital-to-analog converter, the less significant portions of the accumulated count affect the digital-to-analog converter to a greater extent, and as a result, an expanded or magnified display is produced on the storage CRT 36.

In a given example, up-down counter 14 has a capacity of counting 8,192 incremental inputs accumulated in binary fashion. That is, counter 14 is provided with 13 stages. However, the 10 inputs to the digital-to-analog converter indicate that this converter is capable of providing only 1,024 analog levels. Then, so long as the up-down counter does not exceed a count of 1,024, the digital-to-analog converter will receive this information and provide a full-scale plot on storage CRT 36 representing thereof. If switching means 22 is moved to the right from the position shown, so that terminal 38 is joined to output connection 40 of the up-down counter, then 8,192 counts in the counter will be compressed into the 1,024 levels of the digital-to-analog converter. If, on the other hand, switching means 22 is moved to the left so that terminal 38 connects to output terminal 42 of the up-down counter, then 256 counts or increments in the counter will be expanded into the same analog range as the 1,024 levels of the digital-to-analog converter. It will be noted, that in the last-mentioned position the left two inputs to digital-to-analog converter will not be connected directly to the up-down counter. The information obtained is, however, the detailed information available from the computer and provides enough levels in the digital-to-analog converter for establishing an adequately detailed plot on the storage CRT.

If the digital-to-analog converter 24 is connected to the up-down counter 14 at the position shown in the drawing, that is, the less significant 10 stages thereof, or at some other position short of the maximum capacity of the counter, and a larger number of incremental inputs than this is received by the up-down counter, then the digital inputs to the digital-to-analog converter 24 will repeat themselves resulting in "wrap around" on the display. For this reason, connections 30 of switching means 22 operate Z-axis inhibit circuit 32 so that the storage CRT 36 is responsive only to the 10 least significant bits in the up-down counter which are selected by switching means 22. For larger total counts, the CRT beam is inhibited, even though the lower bit positions still contain information.

Thus, magnification and demagnification in the presentation is achieved through operation of switching means 22 via scale switches 28 and present scale latches 26. Between changes of scale, the storage CRT should be erased and a replot of digital incremental deflecting instructions is requested from the computer. The result is illustrated in FIG. 2 wherein the first display for a first setting of switching means 22 is indicated on the left, and a second display for a second position of switching means 22 (and a different offset) is indicated on the right. The plot on the left, for instance, is a graph of a curve on X and Y coordinates. A detailed sector is selected as hereinafter more fully described, and the size of the new plot is selected by scale switches 28. When the information is replotted from the computer, the presentation may be as indicated at the right, indicating in magnified fashion a portion of the curve which may be of particular interest.

There are two modes of operation for the system according to the present invention, a plotting mode during which a given presentation is written and stored on a storage cathode-ray tube, and a "frame" mode in which the information already stored and viewed on the cathode-ray tube screen is overlaid with a "write-through" cursor mode. This frame is positionable and variable in size for selecting a portion of the stored plot for reploting upon the screen of the storage cathode-ray tube. In the system according to the present invention, the "ready" mode is generally identified rather than the aforementioned plotting mode. In the ready mode, the computer is informed that it may send incremental digital information to the system according to the present invention for providing a plot. The initiation of transmittal of this information is generally from the computer or computer control or interface. In the "frame" mode, the system according to the present invention informs the computer that the system is busy, and no further incremental plotting information should be sent.

The particular sector which may be of interest in the given display is selected by "offsetting" in the "frame" mode of operation. Information in the form of a plot that has been pro-
vided on the face of the storage CRT 36, and a cursor with a frame attached is "written through" the stored display. Consider FIG. 2 wherein a frame 44 is movable with respect to the CRT presentation for selecting the given sector of interest. The position of the cursor is considered to be at the lower left-hand corner of the frame 44 and is displayed on the face of the CRT 36, and a cursor with a frame attached is "written through" the stored display at point 12. At the up-down counter 14, and to the right of the CRT 36. If the frame 44 is located over the top of the Christmas tree, repplotting of the information as indicated at the right in FIG. 4 provides a presentation of the information previously surrounded by the frame. Now let us assume that a further expansion of the repplotting of the information is desired as indicated in FIG. 5. Now, frame 44 is adjusted to coincide with the star at the top of the Christmas tree, and this information is repplotted to provide an enlarged view thereof as indicated at the right in FIG. 5. This zooming feature allows rough selection of a particular part of the compressed plot and then subsequent enlargement until the particular detail of interest is displayed on the CRT.

Now, returning to FIG. 1, let us assume that information for the plot at the left-hand side of FIG. 4 has been entered in up-down counter 14 and plotted on storage CRT 36. Offset switches 46 are adjusted until frame 44 coincides with the top part of the Christmas tree. Likewise, scale switches 28 are adjusted until the frame 44 has the size encompassing the area to be repploted. Thus the position of frame 44 in FIG. 4 is selected by offset switches 46 and 512 bits of the size of the frame is selected by scale switches 28 such that it encompasses the area of interest. The scale now selected will ordinarily not necessarily be smaller than that selected for the original plot. The size of the frame 44, as illustrated in FIG. 2, for example, is determined at this time by frame generator 56 which can generate waveforms of varying size for presenting a write-through frame of varying dimension. The analog frame output of frame generator 56 is controlled by compare circuit 58 which compares the setting of the scale switches 28 as transferred to present scale latches 26, with the setting at the time the overall Christmas tree of FIG. 4 was plotted, as remembered by last scale latches 60. If the difference in the scales is such that the frame would be one-eighth as large as the overall plot, then the frame generator 56 is directed accordingly.

Last scale latches 60 control a divider 52 which divides down the clock output presented to offset register 50. Of course, offset register 59 keeps accumulating until comparator 54 indicates the contents are the same as that of offset switches 46. However, up-down counter 14 receives a greater number of counts. It receives a number of counts appropriate to move the cursor frame appropriately for the previous display, i.e., with respect to the overall Christmas tree presentation at the left in FIG. 4. Last scale latches 60 control the divider 52 in order to cause appropriate movement for the cursor frame with movement of offset switches 46. To employ a specific example, each fine adjustment of offset switches 46 is equivalent to 32 counts outside of 8,192. If the previous display, i.e., the overall Christmas tree, was an 8K display, i.e., one during which the switching means 22 was set so that contact 38 made connection with up-down counter terminal 40, then each fine adjustment of offset switches 46 needs to adjust the cursor frame by an amount equal to one two-hundred-fifty-sixth of the display. If the switching means 22 had been located to the left by one bit position, the amount of cursor adjustment for fine adjustment of offset switches 46 would be equal to one hundred-twenty-eighth of the display. The division of the counts entering the offset register maintains the correct ratios so that the frame moves appropriately as remembered by the previous scale latches 60 relative to the previously selected display. Now, when the plot at the right-hand side of FIG. 4 is desired, the plotting incremental information is again received from computer 10, with the complement plus one from the offset register having been entered in up-down counter 14. It is seen that the repplotting procedure is referenced to the previous plot so that successive selections and magnifications can be accomplished.

Thus, referring to FIG. 5, the plot at the left-hand side is the same as the plot at the right-hand side of FIG. 4. Offset
switches 46 and scale switches 28 are adjusted so that frame 44 is now positioned over the desired area. Again, the frame size generated by frame generator 56 is controlled by comparison of the present scale latches and the last scale latches in compare circuit 58. Also, the positioning or offset of the frame is accomplished by entering an appropriate serial output from clock 48 into the up-down counter until the offset register, appropriately controlled from the last scale latches via divider 52 in order to accomplish proper cursor positioning relative to the last plot, equals the setting of offset switches 46. Now, the component portion of the number in the offset register is entered in the up-down counter, and information from the counter 10 is replotted to obtain the display indicated at the right in FIG. 5.

FIG. 6 is a more complete diagram of the graphic display system according to the present invention wherein like elements are designated by like reference numerals. Computer interface 11 is of the type conventionally employed to attach XY mechanical plotters, etc., to computers, but is preferably much faster in its operation to accommodate the faster plotting capabilities of the electron beam in a cathode-ray tube. A point or dot display is employed in the illustrated embodiment of the present invention wherein each computer output indicates the incremental direction of movement of the dot. That is, a dot is to be incremented in position. For example, X-axis outputs of the computer interface 11 are L, P, and R, indicating whether the incremented dot position is to the left or to the right, with P being the increment instruction. Pen up and pen down indicates whether a dot is to be written, when the other instructions are received. Thus a write dot instruction is given if P and L or R are received, and the pen down instruction sets a write flip-flop (not shown) in a write state. Similarly, U and D indicate up and down, with P' comprising the increment instruction in the Y direction. For any incremented position, the pen up and pen down directions normally control the operation of a writing pen in the case of a mechanical plotter. In the present circuit, these instructions operate Z-axis control 62 such that Z amplifier 64 provides an appropriate voltage to CRT grid 66 for electron beam writing when a pen down instruction is received and for biasing the electron beam off when a pen up instruction is received.

The instructions U, D, and P' are applied to a Y channel circuit 68 which is substantially identical to the X channel circuit herein illustrated except that some elements can be common to the two circuits, e.g., the scale switches 28, the present scale latches 26, the last scale latches 60, and of course, the storage cathode-ray tube 36 as well as the Z-axis circuitry and portions of the frame generator 56.

The instruction P' from the computer interface 11 comprises a pulse and is applied to up-down counter 14 via OR-gate 70 while the instructions R and L are similarly connected to the up and down controls of up-down counter 14. Up-down counter 14 comprises a series of flip-flop stages R1 through R4. The counter has the property of counting in either direction under the control of instructions L and R. A counter of this general type (and the type employed for register 50) is illustrated in FIG. 7 and comprises a number of flip-flops 72, each receiving an input at C for causing the flip-flop to change state. Each flip-flop produces outputs Q and Q', wherein Q' is the inverse or complement of Q. Output Q is connected via an AND-gate 74 to an OR-gate 76 and from there to the input C of the flip-flop. An up-line 78 and up-gate 74 cause the up-down counter to produce a total in binary fashion wherein each succeeding stage corresponds to a higher order or more significant bit in the binary accumulation. If during the operation of the counter, down-line 82 is energized instead of upline 78, such that the complemented outputs of each flip-flop drive the next stage, then the counter will operate in the reverse direction and count-down. Thus, this counter will accumulate in either direction, on command.

Returning to FIG. 6, the individual noncomplemented outputs of up-down counter stages R1 through R4 are applied to a switching matrix 22', the function of which is to allow the movement of the digital-to-analog converter 24 'along' the up-down counter 14 in response to present position latches 26. Present position latches 26 are each comprised of an inverter which is normally in the zero state, but which may be triggered to the one state by operation of its respective pushbutton switch 28. The P' latches 26 are intercoupled so that only one of these circuits may be "up" (one) at one time. Under the control of pushbuttons 28, these latches select the present scale of the display on cathode-ray storage tube 36. The designations 8K, 4K, 2K, 1K, 500, and 250 indicate division factors for the display. For a P' latch position of 1K, i.e., with the 1K present scale latch "up," no scale modification is operating, and 1,024 increments in up-down counter 14 directly produce 1,024 levels in digital-to-analog converter 24. This corresponds to the position of switching means 22 as specifically illustrated in FIG. 1. If the 4K position is selected, up 4,096 increments in up-down counter produce the 1,024 analog levels. For the 2K position, 2,048 increments produce 1,024 levels. In the 500 position (or the 0.5K position) 512 increments produce 512 analog levels, but cover the same voltage range as the 1,024 levels. For the 250 position (or 0.25K position), 256 increments in counter 14 produce 256 analog levels again covering the full voltage range in the digital-to-analog converter 24, etc. The implementation of the switching matrix is illustrated in FIG. 8.

Referring to FIG. 8, the switching matrix circuit comprises a plurality of AND-gates for connecting up-down counter stages R1 through R4 to the first digit through the 10th digit inputs of the digital-to-analog converter. For example, if the 1K line is energized from the present scale latch, P, for 1K, then AND-gates 84 through 93 will be energized on one lead thereof making possible the connections of up-down counter stages R1 through R4 directly to the first digit through the 10th digit outputs respectively of the switching matrix. This, again, is the switching position specifically illustrated in FIG. 1. However, for example, if the 8K line is energized from the corresponding present scale latch, then AND-gates 94 through 103 will in effect connect up-down counter stages R1 through R4 to the first digit through the 10th digit inputs respectively of the digital-to-analog converter. Other of the scale inputs are similarly effective to move the connections to the digital-to-analog converter "along" the up-down counter stages.

Now, referring to FIG. 9, the digital-to-analog converter 24 is illustrated. The first digit through the 10th digit inputs are each connected to operate one of the gates 108 through 117 respectively. Each of these gates receives respective inputs from current sources 118 through 127, and acts to divert selected currents to line 130, providing the input to operational amplifier 132 having a feedback resistor 134. The current sources respectively provide currents I512, I256, etc., up to I as indicated. Thus, when gate 108 is energized corresponding to the first or least significant digit from switching matrix 22', then the smallest current I512 is delivered to line 130. The current source provides output to an input of feedback resistor 134. Succeeding current sources cause successively larger voltage drops and larger outputs from the operational amplifier, and when added together provide an analog output corresponding to the digital input.

Returning again to FIG. 6, the output of the digital-to-analog converter is connected to one point 34 in addition to the output from frame generator 56. The combined signal is applied to the horizontal deflection plates 136 of cathode-ray storage tube 36 by way of horizontal amplifier 138, the amplification of which is adjustable by a factor of two. In the
plotting mode, i.e., when information is normally received from digital-to-analog converter 24 for presenting information on the screen of the cathode-ray storage tube, the gain of amplifier 138 is at its normal value and not at a double value, which is also available.

The storage tube 36 comprises an envelope 140 having a principal electron gun including a cathode 142, a control grid 66, and a focusing and accelerating structure 144. The electron beam 146 produced by the principal electron gun is deflected horizontally by means of horizontal deflection plates 136 and vertically by means of vertical deflection plates 139. The beam 146 is in general directed towards a storage target 150 disposed on the inner side of glass end plate 148, such storage target including a transparent storage target electrode 150 over which is disposed a photosensitive dielectric 152, suitably an integral layer of P—1-type phosphor. Target electrode 150 is a thin transparent conductive coating such as tin oxide or the like and is connected to the midpoint of a voltage divider disposed between a positive voltage and ground, as well as to an erase generator 153.

The storage tube 36 is additionally provided with one or more flood-type electron guns 154 which are supported inside the envelope 140 adjacent to the ends of the vertical deflection plates 136 and close to the storage target 150. Electrons emitted from a flood gun diverge into a wide beam which is substantially uniformly distributed towards dielectric 152. A plurality of electrodes are also provided on the inner surface of envelope 140 beyond the flood guns. A first electrode 156, connected at the midpoint of a voltage divider, disposed between a positive voltage and ground, acts to provide a more uniform electric field for collimating electrons. A second electrode 158 near the target end of the tube is also connected to the midpoint of a voltage divider between a positive voltage and ground and acts to collimate electrons as well as possibly to collect secondary electrons to a certain extent. The dielectric 152 comprising a phosphor layer is suitably thin and porous, to enable secondary electrons emitted from the electron beam bombarded side of phosphor to be transmitted through the phosphor and collected by the target electrode 150. A storage tube and target of this type is set forth and claimed in U.S. Pat. No. 3,293,473 to Robert H. Anderson, issued Dec. 20, 1966, entitled, "Thin, Porous Storage Phosphor Layer," and assigned to the assignee of the present invention. The storage target may alternatively be of the raised collector type as set forth and claimed in the copending application of Roger A. Frankland, entitled, "Cathode Ray Storage Tube and Method of Manufacture," filed Feb. 28, 1967, Ser. NO. 619,904, and which is also assigned to the assignee of the present invention.

During operation of the tube, the tube potentials are such that beam 146 has a relatively high velocity for writing and is capable of producing secondary electrons when it strikes storage dielectric 152. Secondary electrons are then suitably collected by target electrode 150 in which case an elemental area of target can be driven positive or "written" as the result of the secondary emission. A written area is retained at a relatively positive potential after beam 146 has passed such elemental area because of the function of flood guns 154. Flood guns 154 produce relatively low-velocity electrons which strike the target but which ordinarily have insufficient velocity for writing information. When the electrons from flood guns 154 strike areas of the target upon which a positive charge has not been written, these flood electrons tend to maintain such areas at the relatively high potential of the flood guns. This is one stable potential level of the target. However, the flood gun electrons are attracted by positive elemental areas and obtain a high velocity with respect to these areas for producing continued secondary emission therefrom. Therefore these areas are maintained relatively positive or near the potential of target electrode 150. This latter potential comprises the second stable potential level of the target. The target thus has bistable properties and is capable of retaining information written thereon, with the flood beam of electrons deriving target areas toward one of two stable potentials depending upon the information written thereon with beam 146. Since the dielectric 152 comprises a phosphor, the storage tube is of the direct viewing type, and a waveform or the like once written thereon can be retained almost indefinitely by the storing action of the flood guns. Thus, the target need not be "refreshed" or continuously written with waveform information, but the desired presentation of plectron need be delivered only twice to the storage tube 36.

For erasing the storage target, an erase signal is supplied from erase generator 153. This signal, applied to target electrode 150, comprises a positive-going pulse immediately followed by a negative-going pulse. The positive portion of the signal fades the target positive, that is, causes the entire target to attain a positive state of secondary emission corresponding to the written bistable state of the target. The negative-going portion of the signal returns the entire target to a negative or nonwritten condition. This erase procedure is preferred because it results in uniform erasure wherein the entire target ends up at substantially the same potential. In the system according to the present invention, the erase generator 153 is operated to produce the aforementioned signal for erasing the target presentation when it is desired to present new information from the computer, or when it is desired to present the same information on a different scale, that is, with a different degree of magnification.

Since the system according to the present invention provides a series of incremented levels from the digital-to-analog converter 24, the result is a point display or a dot display wherein a waveform, graph, or the like, is established on the face of the cathode-ray tube phosphor dielectric in the form of a series of dots. Each time the digital-to-analog converter steps to a new level, a dot may be written on the screen of the cathode ray tube, i.e., on the phosphor dielectric 152, providing a previous pen-down signal has been received by Z-axis control 62 to provide an input for the Z-amplifier 64 appropriate for causing electron beam 146 to bombard the target at the location of such point. A sufficient number of levels are generated by digital-to-analog converter 24 so that in all but the most magnified displays the dots are not discernible, but construct a substantially solid line viewable on the CRT.

A control lead 160 also provides an input to Z-axis control 62 to AND-gate 162 from the first digit input to the digital-to-analog converter. Assuming a ready-to-plot control signal, as indicated by the FF (ready) designated input to AND-gate 162, the cathode ray tube will write a dot at a digit or least significant bit supplied to the digital-to-analog converter changes. That is, the cathode ray tube will not continue to write a dot unless the input to the digital-to-analog converter from switching matrix 22 changes, so that the dot would be located at a new position. The rewriting of a dot in the same position is unnecessary because the dot will be stored by the bistable storage action of the CRT as hereinbefore described, and since the rewriting of the dot may cause spreading of the observed image. Indicated connection 160 may be AC coupled.

The Z-axis control 62 also receives an input from Z-axis inhibit circuit 32 as well as an input marked FF (frame). The FF (frame) signal disables the pen up and pen down instructions insofar as they affect writing on the CRT during the time a write-through frame is provided. The Z-axis inhibit circuit prevents multiple images by rejecting a writing input for all but predetermined lower order digits from the up-down counter 144. Z-axis inhibit circuit 32 is further illustrated in FIG. 13.

Referring to FIG. 13, the outputs of up-down counter stages Rn, Rm, Rl, Rb, and Rp are applied as inputs to AND-gates 164, 166, 168, 170, and 172, respectively. The AND gates also receive inputs from the present scale latches indicating of the scale selected by the scale switches. The —500 signal, indicating second stage designated present scale latch 26 is in an "up" position, is applied to AND-gate 164. The 500 signal is in inverse or complemented form. Also, the complemented version of the output of a present scale latch, —1K, is
applied to both AND-gates 164 and 166, while the \(-2K\) signal is applied to AND-gates 164, 166, and 168. Also, the signal \(-2K\) is applied to AND-gates 164, 166, 168, and 170. The \(-2K\) signal is applied to all the AND gates.

The output of AND-gates 164, 166, 168, 170, and 172 and forms the Z-axis inhibit signal applied to Z-axis control 62 in FIG. 6. It is noted each of the gates 164, 166, 168, 170, and 172 as well as gate 174 produce an inverting output. Gates 164, 166, 168, 170, and 172 normally energize gate 174 so that the latter normally provides a negative or down output which is connected to Z-axis control 62 in FIG. 6 for enabling normal operation thereof. Now, if a present scale latch is up or energized in the 2K position, for example, then only the \(-2K\) lead will be down in FIG. 13, and since this lead is connected to gates 164, 166, and 168, it will not be possible for any of these three gates to become energized. However, since all but the \(R_{13}\) and \(R_{14}\) inputs to gates 170 and 172 are energized, if either of these outputs is present from the up-down counter, the output of gate 170 or gate 172 will drop, disabling gate 174. The output of gate 174 will then rise for inhibiting the Z-axis control 62. Thus, the electron beam 146 in tube 36 will be prevented from writing a dot should a bit be present in either stage \(R_{13}\) or \(R_{14}\) of the up-down counter, when the 2K scale is selected. This means that a 2K sector, which has been selected by operating the full screen of the cathode-ray tube, will not be obscured by the writing of other 2K sectors from the total digital information available.

Only the digits from stages \(R_{1}\) through \(R_{11}\) provide input switching matrix 22', and if the number in up-down counter 14 exceeds 2,048 bits, then the beam is blanked. Thus, only the lower order 2,048 bits in up-down counter 14 are effective for producing a plot, and as the number in the up-down counter exceeds a count of 2,048 bits, the additional information from the computer is ignored, inasmuch as a count in either stage \(R_{14}\) or \(R_{15}\) inhibits electron beam 146. The Z-axis inhibit circuit operates similarly when other scales are selected. Outputs from up-down counter stages \(R_{14}\) and \(R_{15}\) are also applied to cause inhibition of writing, particularly in the frame mode. Thus, any accumulation in the up-down counter in excess of a count of 8,192 will produce an output from \(R_{14}\) and/or \(R_{15}\). The outputs of stages \(R_{14}\) and \(R_{15}\) may be applied to inhibit frame generator 56 by means not shown.

The last scale latches 60 suitably comprise flip-flops of the same general type as the present scale latches 26, but rather than receiving a pushbutton input, each of the last scale latches receives an input from the corresponding present scale latch. The last scale latches are interconnected, so that only one is on at a time. However, the last scale latches 60 do not automatically assume the position of present scale latches 26.

The present scale latches 26 change in accordance with the information from present scale latches 26 only upon enablement by command on lead 176 from the P or pulse output from computer interface 11. Upon the transmission of plotting information from the computer interface, the last scale latches 60 assume the condition of P scale latches 26.

An AND-gate 174 receives the outputs of present scale latches 26, and the setting of present scale latches 26 will be saved in register 178 when the latter receives a hold input. Later, upon receiving a recall input, the contents of register 178 is reinserted into present scale latches 26. Register 178 is employed for saving the state of a previous plot as hereinafter more fully described.

Offset switches 46 comprise a coarse control switch comprising sections or wafers marked c, and a fine control switch comprising sections or wafers marked F. The F switch sections are controlled together by one control, and the C switch sections are suitably controlled by a second control. Each of these switches is otherwise identical and is further illustrated in FIG. 10. As can be seen, the switch comprises four sections, 180, 182, 184, and 186 ganged together and each having 16 contacts. Selected of the contacts are connected together and to the voltage, \(v\), such that in selected switch positions this voltage is applied to the stages of comparator 54. The arrangement is such that the switches select a binary coded input to the stages of comparator 54, wherein section 180 provides the lowest order digit. For the zero setting of the switch, none of the sections provide an output to any of the comparator stages. For a one setting, section 180 provides an input to the first comparator stage. For position 2, switch section 182 provides an input to the second comparator stage. For position 3, both sections 180 and 182 provide inputs to their respective corresponding comparator stages, and so on, in binary fashion. Since each switch has 16 positions, a total of 256 combinations are possible, with the F switch providing the fine setting, and the c switch providing the coarse setting.

The comparator circuit 54, in FIG. 6, comprises a binary adder wherein each stage adds the output of a switch section, and the digit stored in a stage of offset register 50. Each comparator stage provides a sum output applied to OR-gate 188, and a carry output c to the next adder stage. The combined comparator thus adds the contents of the switches 46 to the contents of the offset register 50 and provides all the sum digit outputs to OR-gate 188. OR-gate 188 operates clock 48 through an AND-gate 190, also receiving a command FF (frame) so that the OR-gate functions only for write-through frame operation. The output of the switches is negative with respect to the output of the offset register so that the comparator will produce no output, that is, all binary zeros, when the contents of the switches are equal (in absolute value) to the contents of the offset register. The clock 48 is enabled whenever the comparator has an output other than zero.

Let us assume the mechanical switches produce an output equal to the binary number 121 (122nd position since position one equals zero). We will assign a minus to this number since the switches in effect produce the inverse thereof. That is, the switches are considered to be set to a \(-121\). The input from the offset register 50 must be \(+121\) for a result of zero. If the contents of the offset register are too low, say \(+115\), the clock 48 is enabled, and the absence of a carry output, c, from the comparator 54 causes the offset register to accumulate in an up direction. At the same time, counter 14 receives pulses from clock 48 and is similarly caused to accumulate positively. On the other hand, if the accumulation in offset register 50 is too high, clock 48 will provide an input to offset register 50 and up-down counter 14, with the carry \(R_{14}\) of the offset register 50 and counter 14 to count negatively until the output of the accumulator is zero. The circuit operates as a digital servomechanism for providing a series of pulses from clock 48 to up-down counter 14 until the error between offset register 50 and switches 46 is reduced to zero. Comparator 54 is thus the error-sensing device.

The output from clock 48 is applied directly to up-down counter 14 through OR-gate 70, but is applied indirectly to offset register 50. The output of the first, or \(R_{14}\), stage of the up-down counter is provided as an input to a divider 52. This divider also provides a counter formed of successive flip-flop stages. As will be appreciated, subsequent stages of the divider 52 provide a divided number of counts to OR-gate 194 as compared to the number of pulses applied to up-down counter 14 via OR-gate 70. The particular division is selected by means of the outputs of last scale latches 60 which select one of a plurality of AND-gates 196 coupling the divider outputs to OR-gate 194. The OR-gate 194 operates a one-shot circuit 198, the output of which is applied to offset register 50 through AND-gate 200 when an FF (frame) command enables gate 200. Thus, in the frame mode of operation, a division factor exists between the count accumulated by the up-down counter 14 and the count accumulated by register 50. This division factor is determined by the scale of the previous plot as remembered by last scale latches 60. This last scale figure applies to the plot which is ordinarily observed on the screen of the cathode-ray tube during frame operation, since this plot would have been just previously stored in the storage tube.
During the cursor frame operation, switches 46 select the offset of the cursor frame in absolute values relative to the digital input information. However, one wishes to view the positioning of the cursor frame relative to the presentation on the CRT screen. The last scale latches remember the scale of the presentation plotted on the CRT screen and divide and then insert information entered into the offset register appropriately. Each adjustment of the fine switch is equivalent to 32 counts of the 8,192 usable count range of counter 14. If the stored display was an 8K display, then each adjustment of the fine switch needs to move the cursor frame by one two-hundred-fifty-sixth of the display. The full scale range of the digital-to-analog converter in the frame mode is 512 counts, as hereinafter will become more evident. Therefore, if the last scale latches are positioned to the scale of 8K, then only a division factor of 2 is required for information entered into the offset register. This division is acquired by energizing the output of the R1 up-down counter stage into the offset register 50. Then, two counts will be entered in up-down counter 14 for every one in the offset register, and the cursor frame will be moved one two-hundred-fifty-sixth of its full screen range. For a previous scale of 4K, each adjustment of the fine switch needs to adjust the cursor by one one-hundred-twenty-eighth of the display. For 2K previous scale, each adjustment of the fine switch needs to move the cursor by an amount equal to one sixty-fourth of the display, and so on.

In going from a frame mode into another plotting mode, the complement of the contents of offset register 50 plus one is entered into up-down counter 14 by gates 202. Since each adjustment of the fine switch in effect changes the contents of up-down counter 14 by 32 counts, then the output of the offset register needs only to be entered in stages R1 through R8 of the up-down counter or the higher order stages beyond count of 32. The contents of the offset register 50 are transferred into the up-down counter when going frame a frame mode to a ready mode, where ready means ready to plot. The contents of the up-down counter are entered in parallel fashion in stages R1 through R4 of the counter, or “jam transferred” therein. The transfer is under the control of the one-shot circuit 204 which provides an output pulse when going from frame to ready mode. The leading edge of the output pulse operates gates 202 to cause the transfer. This output pulse is also applied directly to stages R1 through R4 and R12. This direct application of the output of the one-shot circuit places a one in stages R1 through R4 and R12. Then the trailing edge of the output of one-shot circuit 204 causes an input to be applied to the up-down counter through gate 70. Therefore, the complement added to the up-down counter by gates 202 is increased by one as is necessary to properly preload the counter 14. The stages of R1 through R4 are preloaded to one so that the addition of one returns each of these stages to zero. Actually the addition of one at stage R4 then adds a carry into a stage R8 concluding the complement plus one operation. R14 and R12 also return to zero.

It may sometimes be desirable to store the contents of offset register 50 so the plot at a particular scale can be recalled at a later time. It is observed that the digital information supplied from the computer interface for each record is substantially the same, while only the scale and offset differ. If it is desirable to save a scale, a hold command stores the contents of offset register 50 in a storage register 206. Later, when the same scale and offset are to be employed again to recover a desired presentation of the plot, a recall command is given to storage register 206 and the information is again transferred into up-down counter 14 as well as back into offset register 50. As hereinbefore noted, the same hold and recall commands operate the storage register 178 for similarly remembering and recalling the scale.

During frame operation, that is when the cursor with a frame mode is attached to the CRT, the cursor is represented on the CRT screen, a frame generator 56 produces a frame in analog fashion starting with the cursor offset at the lower left-hand corner thereof. That is to say, during frame operation, digital-to-analog converter 24 deflects a cursor to a point on the CRT screen, and then analog voltages are added for deflecting the electron beam through a frame trace. Frame generator 56 adds appropriate deflection voltages at summing point 34 so that the horizontal deflection will be appropriate for forming the frame. Of course, the frame generator also provides waveform outputs to the Y channel for causing appropriate deflection for application to the vertical plates of the CRT. FIG. 14 is a block diagram of the frame generator.

Referring to FIG. 14, capacitors 208 and 210 are normally clamped to zero volts by high clamp circuits 212 and 214, respectively. A free-running trigger generator 216 generates pulses at times T0, T1, etc., at regular spaced intervals. Each of these pulses triggers a flip-flop circuit 218 to provide an output at Q for operating gate 220. Gate 220 connects a current source 222 to the ungrounded end of capacitor 208. The direction of current 21 is such as to charge capacitor 208 in a negative direction, as indicated by waveforms 224 until the voltage at the ungrounded end of the capacitor reaches a voltage set by low clamp circuit 226. At this time, low clamp circuit 226 operates a flip-flop 228 which produces an output Q for turning on gate 220. Current 21 from current source 232 charges capacitor 210 in a negative direction as indicated by waveform 234, until the voltage on the capacitor reaches the value set by low clamp circuit 226. Low clamp circuit 236 resets flip-flop circuit 218 to its original condition, which opens gate 220 causing current source 233 to charge capacitor 208 back towards ground as controlled by high clamp circuit 212. As the voltage on capacitor 208 reaches ground, high clamp circuit 212 resets flip-flop 228 opening gate 230. Thereupon, current source 233 charges capacitor 210 back towards ground. The waveforms at 224 and 234 are appropriate for generating a frame 44 starting and finishing at the location identified by the designation T0, T1. The voltage at the ungrounded end of capacitor 210 is applied through resistor 238 and an inverting amplifier 240 to summing point 34 for X deflection amplifier 138 in FIG. 6. Similarly, the voltage at capacitor 208 is applied to resistor 242 and an inverting ampli- fier 244 to a summing node for a Y amplifier in Y channel 68. The inversion of the waveforms produces the frame orientation indicated at 44.

High clamp circuits 212 and 214 also provide outputs on leads 246 and 248, respectively, leading to OR-gate 250, the output of which is applied to Z amplifier 64 in FIG. 6. If either one of the capacitors is at other than zero volts, a high clamp circuit provides an output for enabling a storage tube and permitting the beam to write, with a somewhat reduced control voltage as applied to control grid 66. The beam current density at this time is such and the speed of charging and discharging capacitors 208 and 210 is maintained constant such that the beam does not bistably write information on the screen of the storage tube. The frame will thus be seen, visible on the storage tube, and may be moved around with the scale pushbutton switches 28 and by the offset switches 46 during the frame mode of operation without storing the frame. The electron beam during display of the frame in this manner does not deposit sufficient charge at any location on the storage dielectric so that a stored positive condition would be retained. Thus the terminology, "write through" is applied to the frame. It should also be noted that OR-gate 250 enables the Z amplifier 64 only while the frame is moving and not between frame generations. The frame is repeatedly generated by repetitive pulses T0, T1, etc., which should have a period greater than the time between T0 and T1.

The amplitude of the waveform 224 and 234 and therefore the size of the frame on the cathode-ray tube presentation is adjustable by means of control circuit 252. Control circuit 252 includes a voltage divider 254 disposed between ground and the negative voltage along which connected to a plurality of gates 256. These gates operate in pairs, connecting a given point on the voltage divider to a low clamp circuits 226 and 236. The gates are under the control of compare circuit 58 in FIG. 6 which detects the size of the present setting of the scale.
switches as registered by present scale latches 26, where the previous setting of the scale switches when the plot in view was stored is indicated by last scale latches 60. For example, if the new scale is of the size one thirty-second of the previous scale, then the top two gates 256 will be energized connecting the low clamp circuits 236 and 232 to appropriate points on the voltage divider 254 so that the amplitude of the waveforms 224 and 234 will be appropriately low for generating a small frame on the screen of the cathode ray tube. As can be seen, the size is adjustable between 1/32X and 2X, wherein the latter designation indicates a frame size larger than the previous presentation. In the latter instance, the whole frame would not appear on the cathode-ray tube screen, but a part can be made to appear.

The control circuit 252 is operated by compare circuit 58 in FIG. 6. A portion of this compare circuit is also illustrated in FIG. 11. In the FIG. 11 circuit, a combination of gates is illustrated for operating the lower two gates 256 in FIG. 14, that is the gates for producing a 2X frame. Designated present scale latches 26, and last scale latches 60, are connected as illustrated. That is, a 4K last scale latch and an 8K present scale latch provide inputs to AND-gate 258, while a 2K last scale latch and a 4K present scale latch provide inputs to the second AND-gate 260. Similarly, a 1K last scale latch and a 2K present scale latch provide inputs to AND-gate 262, a 500K last scale latch and a 1K present scale latch provide inputs to AND-gate 264, and a 250 last scale latch and a 500K present scale latch provide inputs to AND-gate 266. The outputs of AND-gates 258, 260, 262, 264, and 266 are connected to operate 2X gates 256 through OR-gate 268. It will be seen that if one of the present scale latches 26 is up, indicating a two times multiplication factor in scale as compared with the last scale latch 60 which is up, then the 2X gate will be energized.

A similar connection of AND gates and an OR gate is provided for each pair of gates 256 in FIG. 14. I.e., in order to operate the 1X gates 256 in FIG. 14, the present scale latches must indicate the same scale as the last scale latches. Similarly, for the 1/2X gates to be operated, the present scale latches must indicate a scale one-half of the last scale, whatever these values may be. A truth table for the operation of the compare circuit 58 is given in FIG. 12. Each intersection where a multiplication factor is found represents an AND gate and all identical multiplication factors provide inputs to the same OR gate and operate similarly designated gates in the control circuit 252 in FIG. 14.

It is of advantage to position the cursor off screen as well as on screen as long as the frame is visible in the cathode ray tube presentation. To obtain this flexibility, that part of the up-down counter 14 attached to the digital-to-analog converter 24 is half filled at the start of the frame mode. This is accomplished by placing a one digit in stage R0 of the up-down counter in the frame mode as indicated in FIG. 6. At this time, the switching matrix is also controlled so that only up-down counter states R1 through R4 are (or can be) connected to the digital-to-analog converter 24. Thus, a count of 512 effectively added to the up-down counter would then position the cursor half way across the presentation or in the middle of the screen, a count of 1,024 being required for producing 1,024 levels and normal full screen deflection in the CRT. The output voltage of the digital-to-analog converter 24 for full screen deflection is taken to be 1 volt, so, the count of 512 produces a half volt output from the digital-to-analog converter. To connect the resulting reference of the cursor, a −0.5 volt is added to the digital-to-analog converter output at summing point 34 whereby the cursor is returned to the left-hand side of the screen (the lower left-hand corner considering both axes). The location of the cursor would now be indicated at 270 in FIG. 15 relative to the presentation on the cathode ray tube screen 273. The upward movement of the cursor relative to the screen by then providing an input from clock 48 to the switching matrix 22 is indicated at 272 in FIG. 15. By doubling the gain of amplifier 138 in the frame mode, it is possible to extend the coverage of the cursor to the full screen area (as well as beyond) as indicated at 274 in FIG. 16.

The on screen range of the cursor is seen to be 512 counts of the up-down counter 14 in the frame mode, rather than 1,024 counts. It will be appreciated that movement of the cursor off the screen may bring a corner of the frame or a part of the frame on the screen, or the like, and then meaningfully indicate a part of data, which may be unseen, and which it may be desired to display upon the next replot, for example.

The control change between the ready mode and the frame mode is accomplished by pushbuttons 276 and 278, respectively connected for operating flip-flop 280. In the ready mode, wherein the system is ready for incremental plotting pulses from computer interface 11, information from offset register 50 is "jam transferred" into up-down counter 14 under the control of one-shot circuit 204, and a one is added to the up-down counter 14. The Z-axis control is also enabled via AND-gate 162 so that a dot may be stored on the screen of the CRT when the switching matrix receives information and changes in its least significant bit position.

When the frame button 278 is pushed, flip-flop 280 changes to its opposite state, and performs a number of functions. AND-gate 190 is energized so as to complete a servo mechanism for entering counts in the up-down counter 14 from clock 48, for the purpose of positioning the cursor. AND-gate 200 is energized so that the proper ratio of counts is entered in up-down counter 14 and offset register 50. AND-gate 192 is enabled so that the carry outputs from comparator 54 may control the counting direction of offset register 50 and up-down counter 14. Further, a one is entered into the tenth bit position of the up-down counter. The Z-axis of control 62 is inhibited. At the same time, the flip-flop 280 provides an output to switching matrix 22 so that during the frame mode only the 10 least significant bit stages of the up-down counter are connected to the digital-to-analog converter. As hereinbefore mentioned, −0.5 volts is added to the output of the digital-to-analog converter and amplifier 138 is controlled to have a times-two gain. Frame generator 56 is also enabled so that an analog "write-through" frame is generated.

Considering operation of the system according to the present invention with respect to FIG. 6, block diagram, one of the pushbuttons 28 is depressed as to write as a desired scale for the digital incremental information to be received from the computer. The switching matrix 22 will be set thereby as to switch appropriate output circuits from up-down counter 14 into digital-to-analog converter 24 to provide a scale of the corresponding size. Depending upon the scale selected, certain of the outputs of up-down counter 14 are connected to inhibit the writing of electron beam 146 through the active area of Z-axis inhibit circuit 32. To avoid "multiple exposures," only the range of counts from zero up to the maximum selected by the switching matrix will operate the digital-to-analog converter. All higher order bits (those not connected to the digital-to-analog converter) must be zero for the Z-axis circuitry to allow CRT beam to turn on. Thus, the up-down counter 14 may subsequently range from zero through its usual 8,192 count range, although the low order bits selected by the switching matrix may be present as the up-down counter counts through this entire range, only while the lower order bits are present by themselves will the beam be permitted to write. Thus, other "sectors" of the input information are ignored unless, of course, the scale pushbuttons are set to 8K.

The ready pushbutton is pressed for changing the state of the flip-flop 280 and, as a consequence, a pulse is produced by one-shot circuit 204. The complement of the contents of offset register 50 are added to stages R4 through R0 of up-down counter 14, and a one is added thereto via gate 70. Any offset previously determined may thereby be added to the up-down counter so that the sector of information displayed on the cathode-ray tube will be preselected portion. This is accomplished because of the preloading of the complement plus one.
into the up-down counter 14. Then the sector of interest will "spill over" into the lower order portion of the switching matrix 12 at which time no Z-axis inhibition takes place via circuit 32. The computer interface, having detected the ready signal, will inform the computer that the graphic display system is ready to receive serial digital information in the nature of incremental plotting inputs. The information, so far as the X plotting axis is concerned, consists of a series of pulses from computer interface terminal P together with left or right instructions. As the information is incrementally delivered, the up-down counter 14 counts through the entire plot as stored in the computer memory, and at the same time delivers information to the digital-to-analog converter 24 causing the cathode-ray tube beam 146 to move through the designated positions and store the plot. After the information from the computer memory has been delivered once, the plot will be stored on the screen of the CRT. The delivery of information as indicated by a first pulse on terminal P on the computer interface also sets the last scale latches 60 to record the scale at which the present plot was stored. Of course, Z-axis signals also enable the plot, in combination with X- and Y-axis signals. It is noted that during plotting, the cathode ray tube stores a dot only as the information from the up-down counter 14 changes by registering change in the lowest order bit delivered to the digital-to-analog converter 24. If new information is not received from the computer interface, a dot is not written. It should be noted, however, that the Z-axis control 62 receives an enabling input both from the X channel and the Y channel, so that if the stored information increments in either orthogonal direction, a new dot may be written.

Now that the plot has been written, it may be desired to select a certain sector thereof for presentation in magnified form, or even demagnified form. The frame pushbutton is now depressed, changing flip-flop 280 to its opposite state. As a consequence, gates 190, 192 and 200 are enabled. Also frame generator 56 is enabled, and a −0.5 volts is added to the input to X amplifier 138, the gain of which is changed by X2. At the same time, the switching matrix is controlled to connect stages R1 through R5 of up-down counter 14 to the digital-to-analog converter 24, and a one is added to stage R5, in effect filling the up-down counter half full.

If, in passing from the ready or plotting mode to the frame mode, the same scale is selected by depressing one of the pushbuttons 28, then a frame, 44 in FIGS. 2, 4, and 5 will surround the entire stored display. This also assumes that switches 46 have not been changed. If offset switches are rotated, the frame, including a cursor reference which is assumed to be at the lower left-hand corner thereof, will move with respect to the stored display. If a different pushbutton 28 is selected, the frame 44 is changed in size accordingly, by action of compare circuit 58 which compares the present selected scale with the scale selected when the stored plot was plotted. If the setting of offset switches 46 is changed, clock 48 is enabled to provide a series of pulses for causing up-down counter 14 and offset register 50 to count. The counts in counter 14 and register 50 are not the same, because divider 52 causes offset register 50 to count to a smaller number. The number to which counter 14 meanwhile counts will be appropriate for moving the cursor frame on the scale of the stored plot, as a consequence of the control of the divided output entered into register 50, the division factor being controlled by last scale latches 60. When the count in offset register 50 reaches a total equaling that selected by the offset switches 46, clock 46 is no longer enabled.

When a sector of interest in the stored plot has been selected within the frame 44, and the ready button is depressed for admitting the incremental plotting information from the computer interface, erase generator 153 is energized to erase the previous plot on the storage cathode ray tube screen. At this time, again, the complement of information from the offset register 50 is "jam-transferred" into the up-down counter 14 and this amount is increased by one. The offset register has remembered and provided the offset. Therefore, all information from the computer will be ignored except for the sector previously preselected by the frame. Thus, the displayed information is always referred to the previously stored display, and information may be successively "zoomed" until an area of particular interest is located and magnified to the degree desired. It is to be understood that the above description is illustrative of the application of the principles of the invention. Numerous variations may be devised by those skilled in the art which will embody the principles of the invention and fall within the spirit and scope thereof.

I claim:

1. A graphic display system comprising: display storage tube means, means for receiving digital input data and providing an output to said display storage tube means for providing a stored plot on said storage tube means in accordance with said digital input data, means for providing a nonstored cursor indication on said storage tube means superimposed on said plot including means for adjusting size and position information to which selected size and movement of said cursor indication are related, said cursor being defined by a charge image on said storage tube means of sufficiently low voltage that it is not stored, and means for presenting a new stored display in response to said digital input data and to the size and position information to which the cursor indication was related, said new stored display comprising the region of the previous plot selected by said cursor indication.

2. The system according to claim 1 including means for remembering the position of a cursor indication for selecting the second stored display according to the remembered position.

3. The system according to claim 1 wherein said display storage means comprises a bistable cathode ray storage tube provided with a writing gun for writing a display and flood gun means for causing bistable storage through selective secondary emission at the phosphor screen of said cathode-ray tube, said cursor indication being written by said writing gun at a sufficiently high rate and at a sufficiently low intensity so that storage of said cursor indication does not occur.

4. A graphic display system for providing a plot in response to digital incremental plotting instructions comprising: digital counter means responsive to successive plotting inputs for incrementing an accumulated analog display means responsive to said counter means for providing a stored display in accordance with said plotting inputs, signal generator means and means for selectively providing an output from said signal generator means for incrementing said digital counter means for providing a cursor upon said display means relative to stored information, and means for controlling the input to said counter means from said signal generator means, said means for controlling comprising means for selecting the position of said cursor and a digital servomechanism for providing the output of said signal generator means to said counter means until it reaches a function of the cursor position selected by the means for selecting the position of said cursor.

5. The system according to claim 4 wherein said digital servomechanism comprises a register for receiving at least a portion of the input provided by said signal generator means to said counter means, and a comparator means for comparing the contents of said register with the contents of said means for selecting the position of said cursor.

6. The system according to claim 5 including a divider between said signal generator means and said register, and means for controlling the division factor of said divider according to the scale of the display stored by said display means.
7. The system according to claim 6 further including means for remembering the scale size of the stored plot and controlling said divider means thereby so that cursor movement will be at the scale of the stored plot.

8. The system according to claim 7 including means for generating a frame attached to said cursor of selectable scale size, and means for adjusting the size of said frame by comparison between the selected scale size thereof and the scale remembered by said means for remembering the size of the stored plot.

9. The system according to claim 4 wherein said servomechanism means includes a register for remembering a function of the accumulated input provided to said counter means in order to position said cursor, and means for subsequently loading a function of the contents of said register into said counter means for a subsequent plot of incremental plotting inputs for selecting the plotting of a portion of the information according to the position selected by said means for selecting the position of said cursor.

10. The system according to claim 9 wherein said register accumulates a submultiple of the input provided said counter means by said signal generator means according to the scale size of plotted information, and wherein the function of contents of the register loaded into the counter means comprises the complement of the contents of said register plus one.

11. A graphic display system comprising:

an up-down counter for receiving serial digital plotting inputs from a computer for accumulating a total representative of the position of a point at which storage is to take place on an analog display,

digital-to-analog converter for receiving information from said up-down counter for providing an output having a level representative of the count in said up-down counter, a bistable cathode ray storage tube having first deflection means responsive to said analog output for producing deflection of an electron writing beam thereof to provide a stored pot,

a switching matrix between said up-down counter and said digital-to-analog converter for switching the digital outputs into said converter according to a switchably selected scale, wherein a scale having a greater division factor selects successive higher order digits from said up-down counter while having a lower division factor selects successive lower order digit outputs of said up-down counter, and means for inhibiting said electron beam of said cathode ray storage tube, said means for inhibiting being controlled by higher order digit stages of said up-down counter not selected by said switching matrix for application to said digital-to-analog converter so that only lower order contents of said up-down counter will produce an analog output and not repetitions of lower order digits for a greater accumulation in said up-down counter.

12. The system according to claim 11 further including a clock signal generator for selectively providing an input to said up-down counter after the plot of digital information from said computer by said cathode ray storage tube, said clock signal generator having the function of providing a write-through cursor frame on said cathode ray storage tube, means for controlling said clock signal generator including a register comprising a second counter for also receiving selected signals from said clock signal generator, switching means for selecting the offset position of said cursor frame, and a comparator for comparing the contents of said register with said switching means and enabling said clock signal generator only when said contents are not the same, said comparator also controlling the direction of accumulation in said register and said up-down counter so that said register accumulates a count in a direction for equaling the setting of said switching means,
said digital-to-analog converter providing the positional information from said up-down counter to said storage tube for locating said cursor frame relative to a stored plot, and an analog frame generator for deflecting said electron beam from the cursor position to provide a frame relative to stored information.

13. The system according to claim 12 further including a divider means for selecting outputs of the clock signal generator for application to said register, and a plurality of last scale latches for remembering the scale selected for the stored plot, which latches operate said divider means so that the cursor frame is positionable by said offset switches with accurate relation to the stored plot.

14. The system according to claim 12 further including means for storing the setting of said switching matrix and said register and for resetting said switching matrix and said register on command as well as entering a function of the complement of the stored setting of said register to said counter.

15. The system according to claim 12 further including a plurality of gates for transferring the complement of the information in said register into said up-down counter for accomplishment of the positioning of a new plot, and means for adding one to the contents of said up-down counter, said complement plus one being thereby added to incremental serial plotting inputs received from the computer identical to the inputs received for the last plot, wherein the cathode ray tube electron beam is inhibited by said inhibiting means except for part of the plotting instructions corresponding to the cursor position as selected by said offset switches.

16. The system according to claim 12 wherein said cathode-ray storage tube is also provided with a second deflection means for electron beam deflection orthogonal to the first deflection means, and a similarly connected up-down counter, switching matrix, digital-to-analog converter, register, comparator, and offset switches for causing deflection of said electron beam in the orthogonal direction.

17. The system according to claim 16 wherein said frame generator provides a pair of waveforms coupled to orthogonal deflection means for providing a rectangular frame on the screen of the cathode-ray storage tube, the amplitude of said waveforms being selected according to scale size selected therefor in comparison to a remembered previous scale size for a stored plot, said waveforms moving said electron beam at a speed fast enough to prevent storage of said frame for a selected beam intensity during the presentation of said frame.

18. A graphic display system for providing a plot in response to digital incremental plotting instructions, wherein said digital counter means responsive to successive plotting inputs for incrementing an accumulated total, display means for providing a plot in response to said total, means for simultaneously changing the successive digits operating said display means in a first sense providing a digital sequence from less significant bit positions for expanding the scale of the display and in the second sense providing digital information from more significant bit positions for compressing the scale of the display, means for blanking said display for digital counts accumulated in excess of those selected by said means for simultaneously changing said digits, and means for adding a digital input to said counter means for changing the portion of the incremental plotting input which does not inhibit said display for selection of a portion of said display.

19. The system according to claim 18 wherein said means for adding an input to said counter means for changing the portion of said display comprises means for positioning a cursor relative to a display.

20. The system according to claim 11 further including a clock signal generator for selectively providing an input to said up-down counter after the plot of digital information from said computer by said cathode-ray storage tube, said clock signal generator having the function of providing a write-through cursor frame on said cathode-ray storage tube,
means for controlling said clock signal generator,
a register comprising a second counter for also receiving
said signals from said clock signal generator,
and an analog frame generator for deflecting said electron
beam from the cursor position to provide a frame relative
to stored information,
said digital-to-analog converter providing the positional
information from said up-down counter to said storage tube
for locating said cursor frame relative to a stored plot.
21. The system according to claim 20 further including a di-
vider means for selecting outputs of the clock signal generator
for application to said register,
and a plurality of last scale latches for remembering the scale
selected for the stored plot, which latches operate
said divider means so that the cursor frame is positionable
by said offset switches with accurate relation to the stored
plot.
22. The system according to claim 20 further including means
for storing the setting of said switching matrix and said re-
ister and for resetting said switching matrix and said re-
ister on command as well as entering a function of the com-
plement of the stored setting of said register to said counter.
23. The system according to claim 20 further including a plurality
of gates for transferring the complement of the informa-
tion in said register into said up-down counter for accom-
plishment of the positioning of a new plot, and means for ad-
ding to the contents of said up-down counter, said com-
plement plus one being added to incremental serial
plotting inputs received from the computer identical to the in-
puts received for the last plot, wherein the cathode-ray tube
electron beam is inhibited by said inhibiting means except for
part of the plotting instructions corresponding to the cursor
position.
24. The system according to claim 20 wherein said cathode-
ray storage tube is also provided with a second deflection
means for electron beam deflection orthogonal to the first
deflection means, and a similarly connected up-down counter,
switching matrix, digital-to-analog converter, and register for
causing deflection of the electron beam in the orthogonal
direction.
25. The system according to claim 24 wherein said frame
generator provides a pair of waveforms coupled to orthogonal
deflection means for providing a rectangular frame on the
screen of the cathode-ray storage tube, the amplitude of the
waveforms being selected according to the scale size selected
therefor in comparison to a remembered previous scale size
for a stored plot, said waveforms moving said electron beam at
a speed fast enough to prevent storage of said frame for a
selected beam intensity during the presentation of said frame.
26. A graphic display system for providing a plot in response
to digital incremental plotting instructions comprising:
digital counter means responsive to successive plotting in-
puts for incrementing an accumulated total,
digital-to-analog converter means coupled to plural stages
of said counter means, corresponding to plural bit posi-
tions of successively different numerical significance, for
transforming the count accumulated into an analog value
suitable for causing deflection of an analog display,
means for simultaneously changing the coupling of said con-
verter relative to the stages of said counter in a first sense
providing a digital input for said converter from less sig-
nificant bit positions for expanding the scale of the analog
display, and in a second sense providing a digital input for
said converter from more significant bit positions for
compressing the scale of said analog display,
signal generator means for selectively providing a cursor
input to which said counter means is responsive,
offset selection means for selecting the location of said cur-
sor relative to the display,
an offset register also responsive to said cursor input from
said signal generator means,
and comparator means responsive to said offset selection
means and said offset register for controlling said signal
generator means to provide an output for incrementing
said counter means and said offset register until said off-
set register receives a count selected by said offset selec-
tion means.
27. The system according to claim 26 further including means
for transferring a function of the complement of the count
accumulated by said offset register into said counter
means to provide an offset preload relative to repeated incre-
mental plotting inputs.
28. The system according to claim 27 including means for
dividing the cursor input from said signal generator means as
applied to said offset register according to the scale size
selected by said means for simultaneously changing the
coupling for the previously plotted display.
29. The system according to claim 26 further including a frame
generator means for providing analog values for said
analog display in addition to those provided by said digital-to-
analog converter means, said additional analog values causing
the presentation of a frame surrounding a portion of the
analog display.
30. The system according to claim 29 wherein said means for
simultaneously changing the coupling also adjusts said ad-
ditional analog values for adjusting the size of said frame rela-
tive to a stored display.
31. A digital servomechanism system for providing a
predetermined number of pulse outputs comprising:
a signal pulse generator,
means for selecting the number of pulses to be produced by
said servomechanism means, said means for selecting
comprising a plurality of switching means controlling bi-
nary bits of a selected quantity, said means for selecting
providing a binary output related to a function of the
desired number of pulse outputs,
a register counter for receiving at least a portion of the out-
put of said signal pulse generator and accumulating the
total thereof,
and comparator means responsive to said register counter
and said selecting means for controlling said pulse
generator for continuing operation thereof only so long as
the contents of said register counter disagrees with said
selecting means,
said comparator means comprising an adder having stages
thereof connected to stages of said register counter,
said selecting means also providing corresponding inputs to
the stages of said adder,
said comparator means further including means connecting
the sum outputs of each of said adder stages to operate
said signal pulse generator,
and means responsive to carry output from said adder for
controlling the direction of accumulation in said register
counter.
32. A graphic display system for providing a plot in response
to digital incremental plotting instructions comprising:
digital counter means responsive to successive plotting in-
puts for incrementing an accumulated total,
analog display means responsive to said counter means for
providing a stored display in accordance with said
plotting inputs,
signal generator means and means for selectively providing
an output from said signal generator means for incre-
menting said digital counter means for providing a cursor
upon said display means relative to stored information,
and means for presenting a new stored display in response
to digital incremental plotting instructions, with said
digital counter means again being responsive to succes-
vive plotting inputs as well as being responsive to informa-
tion representative of said cursor, wherein said last-men-
tioned means includes means for remembering the posi-
tion of said cursor.
33. The system according to claim 32 wherein said means for
remembering comprises a register for receiving at least a
portion of the input provided by said signal generator means
said counter means.
34. The system according to claim 33 including a divider between said signal generator means and said register, and means for controlling the division factor of said divider according to the scale of the display stored by said display means.

35. The system according to claim 34 further including means for remembering the scale size of the stored plot and controlling said divider means thereby so that cursor movement will be at the scale of the stored plot.

36. The system according to claim 35 including means for generating a frame attached to said cursor of selectable scale size, and means for adjusting the size of said frame by comparison between the selected scale size thereof and the scale remembered by said means for remembering the scale size of the stored plot.

37. The system according to claim 33 including means for subsequently loading a function of the contents of said register into said counter means for a subsequent plot in response to plotting instructions for selecting the plotting of a portion of the input information according to the position of said cursor.

38. The system according to claim 37 wherein said register accumulates a submultiple of the input provided by means means by said signal generator means according to the scale size of plotted information, and wherein the function of contents of the register loaded into the counter means comprises the complement of the contents of said register plus one.

* * * * *

Inventor(s) WALTER A. PETERSEN

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 4, line 75, after "plot" delete "that".
Col. 5, line 61, "sealed" should be --scaled--.
Col. 7, line 13, "counter" should be --computer--.
Col. 9, line 75, "deriving" should be --driving--.
Col. 11, line 68, "c" should be --C--.
Col. 12, line 1, "v" should be --V--.
Col. 12, line 14, "c" should be --C--.
Col. 12, line 72, "lathes" should be --latches--.
Col. 13, line 36, "frame" (first occurrence) should be --from--.
Col. 14, line 1, "CRT" should be --CRT--.
Col. 18, claim 3, line 42, "rage" should be --rate--.
Col. 19, claim 9, line 19, before "information" insert --input--.
Col. 19, claim 11, line 41, "pot" should be --plot--.
Col. 19, claim 11, line 47, after "while" insert --a scale--.

Signed and sealed this 8th day of August 1972.

(SEAL)
Attest:

EDWARD M. FLETCHER, JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents
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