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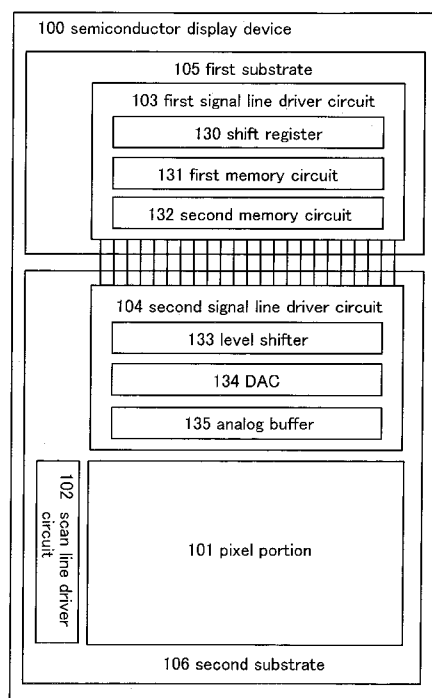
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[Continued on next page]

(54) Title: SEMICONDUCTOR DISPLAY DEVICE

FIG. 2



(57) Abstract: A semiconductor display device comprising a pixel portion and a signal line driver circuit comprising a first circuit, a second circuit configured to control timing of the sampled serial video signals by the first circuit, and a third circuit configured to perform signal processing on the parallel video signals, wherein the second circuit comprises a first semiconductor element formed over a first substrate, the first semiconductor element including a first semiconductor layer, wherein the third circuit comprises a second semiconductor element formed over a second substrate, the second semiconductor element including a second semiconductor layer, wherein the pixel portion comprises a third semiconductor element formed over the second substrate, the third semiconductor element including a third semiconductor layer, wherein the first semiconductor layer comprises silicon or germanium, and wherein each the second semiconductor layer and the third semiconductor layer has a wider bandgap than the first semiconductor layer.

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DESCRIPTION

SEMICONDUCTOR DISPLAY DEVICE

5 TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor display device including a driver circuit.

10 BACKGROUND ART

[0002]

A semiconductor display device in which a transistor including amorphous silicon is provided in a pixel portion has advantages of high productivity and low cost because the semiconductor display device is applicable to a glass substrate of the fifth generation (1200 mm long × 1300 mm wide) or higher generations. Further, in the semiconductor display device, a driver circuit such as a scan line driver circuit for selecting a pixel or a signal line driver circuit for supplying a video signal to the selected pixel is required to operate at high speed. Therefore, the driver circuit is formed using crystalline silicon such as single crystal silicon, which has higher mobility than amorphous silicon.

[0003]

In general, an IC chip including a driver circuit formed using a single crystal silicon wafer or the like is mounted in the periphery of a pixel portion formed using amorphous silicon by a tape automated bonding (TAB) method, a chip on glass (COG) method, or the like.

[0004]

Patent Document 1 cited below discloses a technique by which a driver circuit formed in the form of an IC chip using silicon is mounted on a panel. Patent Document 2 discloses a technique in which a driver circuit formed over a glass substrate is divided into thin rectangular shapes and mounted on a substrate provided with a pixel portion.

[Reference]

[Patent Document]

[0005]

[Patent Document 1] Japanese Published Patent Application No. 2007-286119

[Patent Document 2] Japanese Published Patent Application No. H7-014880

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DISCLOSURE OF INVENTION

[0006]

A driver circuit such as a signal line driver circuit or a scan line driver circuit is required to have not only high operation speed but also high withstand voltage. In particular, in the case of a semiconductor display device in which AC voltage is applied to a pixel, such as a liquid crystal display device, a circuit on an output side of a signal line driver circuit needs to have a withstand voltage of at least approximately more than ten and several volts. Therefore, the structure of a semiconductor element such as a transistor or a capacitor included in the signal line driver circuit needs to be designed so that the above level of withstand voltage is obtained, for example, by increasing the thickness of a gate insulating film and an insulating film interposed between electrodes thereof.

[0007]

However, not all semiconductor elements included in the signal line driver circuit are required to have the above level of withstand voltage. For example, a circuit distant from the output side of the signal line driver circuit, such as a shift register, only needs to withstand a voltage of approximately 3 V at most. As for a semiconductor element used in the shift register, high-speed operation is more important than high withstand voltage to secure high quality of a display image of the semiconductor display device. In order to realize high-speed operation, it is preferable that the semiconductor element be miniaturized and the thickness of the insulating films thereof be reduced.

[0008]

However, the same process is employed to manufacture a semiconductor element which needs to have high withstand voltage and a semiconductor element which needs to operate at high speed. It is necessary to employ a complicated process in order to manufacture semiconductor elements having different structures through the

same process, which results in a reduction in yield and an increase in cost. Therefore, in practice, the structure of the semiconductor element which needs to operate at high speed has to be designed in accordance with the structure of the semiconductor element which needs to have high withstand voltage. Accordingly, a reduction in the area occupied by the driver circuit is hindered, and it is difficult to secure high operation speed and to suppress power consumption.

[0009]

In view of the above problems, an object of the present invention is to provide a semiconductor display device including a driver circuit whose high-speed operation and high withstand voltage are secured without making the manufacturing process complicated. Another object of the present invention is to provide a semiconductor display device including a driver circuit whose power consumption is suppressed and whose high withstand voltage is secured without making the manufacturing process complicated. Another object of the present invention is to provide a semiconductor display device including a driver circuit whose occupation area is reduced and whose high withstand voltage is secured without making the manufacturing process complicated.

[0010]

In order to achieve the above object, in an embodiment of the present invention, a circuit which needs to have high withstand voltage is formed using a semiconductor having a wider bandgap and lower intrinsic carrier density than silicon or germanium. As an example of such a semiconductor, an oxide semiconductor whose bandgap is approximately more than twice as wide as that of silicon can be given. Further, a circuit which does not need to have such high withstand voltage is formed using a crystalline semiconductor including silicon, germanium, or the like. The semiconductor display device is manufactured by connecting the above two circuits.

[0011]

As semiconductors having a wider bandgap and lower intrinsic carrier density than silicon or germanium, an oxide semiconductor, silicon carbide, gallium nitride, and the like can be given. The bandgap of an oxide semiconductor, the bandgap of silicon carbide, and the bandgap of gallium nitride are 3.0 eV to 3.5 eV, 3.26 eV, and 3.39 eV, respectively, which are approximately three times as wide as that of silicon. The wide

bandgaps of these semiconductors are advantageous in terms of improvement in withstand voltage of a semiconductor element such as a transistor, a reduction in loss of power, and the like. According to an embodiment of the present invention, with the use of the above-described semiconductor having a wide bandgap in the circuit which
5 needs to have high withstand voltage, a semiconductor element having resistance to intermediate voltage, that is, intermediate withstand voltage can be manufactured.

[0012]

According to an embodiment of the present invention, the circuit which does not need to have such high withstand voltage can be formed using a semiconductor and
10 a process different from those of the circuit which needs to have high withstand voltage. Therefore, in the circuit which does not need to have such high withstand voltage, a semiconductor element can be manufactured so as to have resistance to low voltage, that is, low withstand voltage, to operate at high speed, and to be miniaturized with the thickness of an insulating film thereof reduced.

[0013]

That is, according to an embodiment of the present invention, semiconductor elements having structures most suitable for characteristics needed for circuits can be separately manufactured without making the process complicated.

[0014]

In this specification, the low voltage means a voltage of lower than or equal to 5 V, preferably lower than or equal to 3 V, further preferably lower than or equal to 1.8 V; the low withstand voltage means resistance to the low voltage. The intermediate voltage means a voltage of higher than 5 V and approximately lower than or equal to 20 V; the intermediate withstand voltage means resistance to the intermediate voltage.

[0015]

Specifically, in a signal line driver circuit, a circuit that controls the timing of sampling serially input video signals, such as a shift register, needs to have high operation speed rather than high withstand voltage. On the other hand, a circuit that performs signal processing on video signals converted to parallel signals, such as a level
30 shifter, a buffer, or a DA converter (DAC), needs to have high withstand voltage rather than high operation speed. Therefore, in the signal line driver circuit of an embodiment of the present invention, the circuit that controls the timing of sampling

video signals has low withstand voltage and the circuit that performs signal processing on video signals converted to parallel signals has intermediate withstand voltage. The signal line driver circuit is formed by connecting the circuit having the low withstand voltage and the circuit having the intermediate withstand voltage.

5 [0016]

As for a circuit such as a memory circuit or a sampling circuit, which samples and temporarily holds video signals for conversion of serially input video signals to parallel signals, the level of withstand voltage needed for the circuit is determined as appropriate depending on whether the video signals are analog signals or digital signals.

10 In the case of digital video signals, the withstand voltage of the above circuit is not necessarily high because the circuit needs to operate at high speed owing to an increase in the number of bits. In contrast, in the case of analog video signals, which tend to have higher voltage than digital video signals, the above circuit preferably has the intermediate withstand voltage.

15 [0017]

An oxide semiconductor is a metal oxide having semiconductor characteristics, and has mobility approximately as high as microcrystalline or polycrystalline silicon and uniform element characteristics which is a characteristic of amorphous silicon. As the oxide semiconductor, a four-component metal oxide such as an
20 In-Sn-Ga-Zn-O-based oxide semiconductor, a three-component metal oxide such as an In-Ga-Zn-O-based oxide semiconductor, an In-Sn-Zn-O-based oxide semiconductor, an In-Al-Zn-O-based oxide semiconductor, a Sn-Ga-Zn-O-based oxide semiconductor, an Al-Ga-Zn-O-based oxide semiconductor, or a Sn-Al-Zn-O-based oxide semiconductor, a two-component metal oxide such as an In-Zn-O-based oxide semiconductor, a
25 Sn-Zn-O-based oxide semiconductor, an Al-Zn-O-based oxide semiconductor, a Zn-Mg-O-based oxide semiconductor, a Sn-Mg-O-based oxide semiconductor, an In-Mg-O-based oxide semiconductor, or an In-Ga-O-based oxide semiconductor, an In-O-based oxide semiconductor, a Sn-O-based oxide semiconductor, a Zn-O-based oxide semiconductor, or the like can be used. In this specification, for example, an
30 In-Sn-Ga-Zn-O-based oxide semiconductor means a metal oxide including indium (In), tin (Sn), gallium (Ga), and zinc (Zn), and there is no particular limitation on the stoichiometric composition ratio. In addition, the above oxide semiconductor may

include silicon.

[0018]

Moreover, the oxide semiconductor can be represented by the chemical formula, $\text{InMO}_3(\text{ZnO})_m$ ($m > 0$, m is not necessarily a natural number). Here, M represents one or more metal elements selected from Ga, Al, Mn, and Co.

[0019]

With the above structure, according to an embodiment of the present invention, a semiconductor display device including a driver circuit whose high-speed operation and high withstand voltage are secured without making the manufacturing process complicated can be provided. With the above structure, according to an embodiment of the present invention, a semiconductor display device including a driver circuit whose power consumption is suppressed and whose high withstand voltage is secured without making the manufacturing process complicated can be provided. With the above structure, according to an embodiment of the present invention, a semiconductor display device including a driver circuit whose occupation area is reduced and whose high withstand voltage is secured without making the manufacturing process complicated can be provided.

BRIEF DESCRIPTION OF DRAWINGS

[0020]

In the accompanying drawings:

FIG. 1A is a block diagram illustrating a structure of a semiconductor display device, and FIGS. 1B and 1C are cross-sectional views of semiconductor elements;

FIG. 2 is a block diagram illustrating a structure of a semiconductor display device;

FIG. 3 is a diagram illustrating a structure of a first signal line driver circuit;

FIG. 4 is a diagram illustrating a structure of a second signal line driver circuit;

FIG. 5 is an external view of a semiconductor display device;

FIG. 6 is a circuit diagram of a level shifter;

FIG. 7 is a circuit diagram of a DAC;

FIG. 8 is a circuit diagram of a buffer;

FIG. 9 is a circuit diagram illustrating a configuration of a pixel portion;

FIG. 10 is a block diagram illustrating a structure of a semiconductor display device;

FIG. 11 is a block diagram illustrating a structure of a semiconductor display device;

5 FIGS. 12A to 12C are cross-sectional views of semiconductor elements;

FIGS. 13A to 13C are views illustrating embodiments of connection between terminals;

FIGS. 14A and 14B are views illustrating embodiments of mounting;

FIG. 15 is a cross-sectional view of a pixel of a liquid crystal display device;

10 FIG. 16A is a top view and FIG. 16B is a cross-sectional view of a panel;

FIG. 17 is a perspective view illustrating a structure of a liquid crystal display device;

FIGS. 18A to 18D are views of electronic devices;

FIG. 19 is a circuit diagram illustrating a configuration of a pixel portion; and

15 FIG. 20 is a circuit diagram illustrating a configuration of a pixel portion.

BEST MODE FOR CARRYING OUT THE INVENTION

[0021]

Embodiments and an example of the present invention will be described below
20 in detail with reference to the accompanying drawings. Note that the present invention is not limited to the following description and it is easily understood by those skilled in the art that the modes and details can be variously changed without departing from the spirit and scope of the present invention. Therefore, the present invention is not construed as being limited to the description of the embodiments and the example
25 below.

[0022]

The semiconductor display device of the present invention includes the following in its category: liquid crystal display devices, light-emitting devices in which a light-emitting element typified by an organic light-emitting diode (OLED) is provided
30 in each pixel, digital micromirror devices (DMDs), plasma display panels (PDPs), field emission displays (FEDs), and other semiconductor display devices in which a circuit element using a semiconductor film is provided in a driver circuit.

[0023]

(Embodiment 1)

FIG. 1A is a block diagram illustrating an example of a structure of a semiconductor display device according to an embodiment of the present invention. A semiconductor display device 100 illustrated in FIG. 1A includes a pixel portion 101 where a display element is provided in each pixel, and driver circuits that control the operation of the pixel portion 101.

[0024]

In FIG. 1A, the driver circuits correspond to a scan line driver circuit 102, a first signal line driver circuit 103, and a second signal line driver circuit 104. Specifically, the scan line driver circuit 102 selects a pixel included in the pixel portion 101. The first signal line driver circuit 103 and the second signal line driver circuit 104 supply a video signal to the pixel selected by the scan line driver circuit 102.

[0025]

The first signal line driver circuit 103 includes a circuit that controls the timing of sampling serially input video signals and needs to have high operation speed rather than high withstand voltage. On the other hand, the second signal line driver circuit 104 includes a circuit that performs signal processing on video signals converted to parallel signals and needs to have high withstand voltage rather than high operation speed.

[0026]

In an embodiment of the present invention, the first signal line driver circuit 103 which can operate even with low withstand voltage includes a first semiconductor element manufactured using a crystalline semiconductor such as a polycrystalline or single crystal semiconductor including silicon, germanium, or the like. In addition, the first signal line driver circuit 103 including the first semiconductor element is formed over a first substrate 105 such as a semiconductor substrate or a glass substrate having an insulating surface. The first semiconductor element can operate at high speed by reducing the thickness of an insulating film thereof. Further, the element size of the first semiconductor element can be reduced.

[0027]

In an embodiment of the present invention, the second signal line driver circuit

104 having intermediate withstand voltage includes a second semiconductor element manufactured using a semiconductor having a wider bandgap and lower intrinsic carrier density than silicon or germanium. With the use of a semiconductor having a wide bandgap, the second semiconductor element can have resistance to intermediate voltage, that is, intermediate withstand voltage. In addition, the second signal line driver circuit 104 including the second semiconductor element is formed over a second substrate 106 such as a glass substrate having an insulating surface.

[0028]

Note that as examples of a wide-gap semiconductor having a wider bandgap and lower intrinsic carrier density than silicon, a compound semiconductor such as silicon carbide (SiC) or gallium nitride (GaN), an oxide semiconductor including a metal oxide such as zinc oxide (ZnO), and the like can be given. Among them, the oxide semiconductor is advantageous in that it can be formed by a sputtering method or a wet method (such as a printing method) and has high mass productivity. In addition, the oxide semiconductor film can be formed even at room temperature, whereas the process temperature of silicon carbide and the process temperature of gallium nitride are approximately 1500 °C and approximately 1100 °C, respectively. Therefore, the oxide semiconductor can be formed over a glass substrate which is inexpensively available and it is possible to stack a semiconductor element formed using an oxide semiconductor over an integrated circuit including a semiconductor which does not have resistance enough to withstand heat treatment at a high temperature of 1500 °C to 2000 °C. Furthermore, a larger substrate can be used. Accordingly, among the wide-gap semiconductors, the oxide semiconductor particularly has an advantage of high mass productivity. In addition, in the case where a crystalline oxide semiconductor is to be obtained in order to improve the performance of a transistor (e.g., field-effect mobility), the crystalline oxide semiconductor can be easily obtained by heat treatment at 450 °C to 800 °C (preferably at 250 °C to 800 °C).

[0029]

In the following description, the case where an oxide semiconductor having the above advantages is used as the semiconductor having a wide bandgap is given as an example.

[0030]

Note that FIG. 1A illustrates the case where the pixel portion 101 and the scan line driver circuit 102 are formed over the second substrate 106 together with the second signal line driver circuit 104 as an example; however, an embodiment of the present invention is not limited to this structure.

[0031]

In the case where the first substrate 105 provided with the first signal line driver circuit 103 is a substrate having an insulating surface, the pixel portion 101 may be formed over the first substrate 105 together with the first signal line driver circuit 103. Further, the scan line driver circuit 102 may be formed over the first substrate 105 together with the first signal line driver circuit 103. However, in the case where the pixel portion 101 or the scan line driver circuit 102 operates with intermediate voltage and if a semiconductor element in the pixel portion 101 or the scan line driver circuit 102 can be manufactured using a semiconductor having a wide bandgap in a manner similar to that of the second semiconductor element, the following structure is preferable for security of the withstand voltage of the pixel portion 101 or the scan line driver circuit 102: the pixel portion 101 or the scan line driver circuit 102, and the second signal line driver circuit 104 are formed over the second substrate 106 as illustrated in FIG. 1A.

[0032]

Further, the first signal line driver circuit 103 and the second signal line driver circuit 104 are connected to each other. There is no particular limitation on the connection method, and a known method such as a chip on glass (COG) method, a wire bonding method, or a tape automated bonding (TAB) method can be used. Alternatively, a chip on film (COF) method, a tape carrier package (TCP) method by which a circuit is mounted on a TAB tape, or the like may be used. Further, a connection position is not limited to the position illustrated in FIG. 1A as long as electrical connection is possible. In addition, a controller, a CPU, a memory, or the like may be formed separately and connected.

[0033]

FIG. 5 is an example of an external view of the semiconductor display device according to an embodiment of the present invention. In the semiconductor display

device in FIG. 5, the first substrate 105 provided with the first signal line driver circuit 103 is mounted on a TAB tape 160 as an example. In the semiconductor display device in FIG. 5, the pixel portion 101, the scan line driver circuit 102, and the second signal line driver circuit 104 are formed over the second substrate 106. Further, through the TAB tape 160, the first signal line driver circuit 103 formed over the first substrate 105 is connected to the second signal line driver circuit 104 formed over the second substrate 106.

[0034]

Note that the semiconductor display device of an embodiment of the present invention includes, in its category, a panel in which driver circuits such as the first signal line driver circuit 103, the second signal line driver circuit 104, and the scan line driver circuit 102 are connected to the pixel portion 101; and a module in which an IC including a controller, a CPU, a memory, or the like is mounted on the panel.

[0035]

Next, an example of a cross section of the first semiconductor element in the case where the first substrate 105 is a substrate having an insulating surface is illustrated in FIG. 1B. FIG. 1B illustrates an example in which an n-channel transistor 110, a p-channel transistor 111, and a capacitor 112 are manufactured over the first substrate 105 as the first semiconductor elements.

[0036]

The transistor 110 includes a semiconductor film 113 which is a polycrystalline or single crystal semiconductor film including silicon or germanium, an insulating film 116 over the semiconductor film 113, and a gate electrode 117 which overlaps with the semiconductor film 113 with the insulating film 116 positioned therebetween. The transistor 111 includes a semiconductor film 114 which is a polycrystalline or single crystal semiconductor film including silicon or germanium, the insulating film 116 over the semiconductor film 114, and a gate electrode 118 which overlaps with the semiconductor film 114 with the insulating film 116 positioned therebetween. The capacitor 112 includes a semiconductor film 115 which is a polycrystalline or single crystal semiconductor film including silicon or germanium, the insulating film 116 over the semiconductor film 115, and an electrode 119 which overlaps with the semiconductor film 115 with the insulating film 116 positioned therebetween.

[0037]

In the case where the semiconductor film 114 is formed using single crystal silicon and the insulating film 116 is formed using silicon oxide, for example, the thickness of the insulating film 116 is preferably greater than or equal to 1 nm and less than or equal to 20 nm, further preferably greater than or equal to 5 nm and less than or equal to 10 nm.

[0038]

Note that the structures of the first semiconductor elements are not limited to those illustrated in FIG. 1B. The first semiconductor elements can be manufactured using a semiconductor film or the like formed over a silicon wafer, a silicon-on-insulator (SOI) substrate, or an insulating surface.

[0039]

An SOI substrate can be manufactured using, for example, UNIBOND (registered trademark) typified by Smart Cut (registered trademark), epitaxial layer transfer (ELTRAN) (registered trademark), a dielectric separation method, plasma assisted chemical etching (PACE), separation by implanted oxygen (SIMOX), or the like.

[0040]

A semiconductor film of silicon formed over a substrate having an insulating surface may be crystallized by a known technique. As the known technique of crystallization, a laser crystallization method using a laser beam and a crystallization method using a catalytic element are given. Alternatively, a crystallization method using a catalytic element and a laser crystallization method may be combined. In the case of using a substrate having high heat resistance such as a quartz substrate, any of the following crystallization methods may be combined: a thermal crystallization method using an electrically heated oven, a lamp annealing crystallization method using infrared light, a crystallization method using a catalytic element, and a high temperature annealing method at approximately 950 °C.

[0041]

The first semiconductor elements manufactured by the above method may be transferred to a separately prepared first substrate having flexibility such as a plastic substrate. The semiconductor elements can be transferred to another substrate by a

variety of methods. Examples of the transfer method include a method in which a metal oxide film is provided between the substrate and the semiconductor element, and the metal oxide film is embrittled by crystallization so that the semiconductor element is separated off and transferred; a method in which an amorphous silicon film including hydrogen is provided between the substrate and the semiconductor element, and the amorphous silicon film is removed by laser beam irradiation or etching so that the semiconductor element is separated off from the substrate and transferred; and a method in which the substrate provided with the semiconductor element is removed by mechanical cutting or etching using a solution or a gas so that the semiconductor element is cut off from the substrate and transferred.

[0042]

FIG. 1C illustrates an example of a cross section of the second semiconductor element. FIG. 1C illustrates an example in which a transistor 120 and a capacitor 121 are manufactured over the second substrate 106 as the second semiconductor elements.

[0043]

The transistor 120 includes a gate electrode 122, an insulating film 123 over the gate electrode 122, an active layer 124 which includes an oxide semiconductor and overlaps with the gate electrode 122 with the insulating film 123 positioned therebetween, and a source electrode 125 and a drain electrode 126 over the active layer 124. The transistor 120 may further include an insulating film 127 which covers the active layer 124, the source electrode 125, and the drain electrode 126. FIG. 1C illustrates the case where the transistor 120 is a bottom-gate transistor and has a channel-etched structure in which part of the active layer 124 is etched between the source electrode 125 and the drain electrode 126, as an example.

[0044]

The capacitor 121 includes an electrode 128, the insulating film 123 over the electrode 128, and an electrode 129 which overlaps with the electrode 128 with the insulating film 123 positioned therebetween.

[0045]

Note that the semiconductor element means a circuit element including a semiconductor film and includes, in its category, any circuit element such as a diode, a resistor, and an inductor in addition to a transistor and a capacitor described above.

[0046]

In the case where the insulating film 123 is formed using silicon oxide, for example, the thickness of the insulating film 123 is preferably greater than or equal to 50 nm and less than or equal to 400 nm, further preferably greater than or equal to 100 nm and less than or equal to 200 nm.

[0047]

Next, FIG. 2 illustrates an example of a more specific structure of the semiconductor display device 100 illustrated in FIG. 1A. In the semiconductor display device 100 illustrated in FIG. 2, the first signal line driver circuit 103 includes a shift register 130, a first memory circuit 131, and a second memory circuit 132. The second signal line driver circuit 104 includes a level shifter 133, a DAC 134, and an analog buffer 135.

[0048]

FIG. 3 illustrates an example of a more specific structure of the first signal line driver circuit 103 illustrated in FIG. 2. FIG. 4 illustrates an example of a more specific structure of the second signal line driver circuit 104 illustrated in FIG. 2. Note that FIG. 3 and FIG. 4 illustrate the structures of the first signal line driver circuit 103 and the second signal line driver circuit 104, respectively, with which a 4-bit video signal is applied. In this embodiment, the first signal line driver circuit and the second signal line driver circuit each have a structure with which a 4-bit video signal can be applied as an example; however, the present invention is not limited to this structure. The first signal line driver circuit and the second signal line driver circuit can be formed in accordance with the number of bits of a video signal set by a practitioner.

[0049]

In the first signal line driver circuit 103 in FIG. 3, the first memory circuit 131 includes a plurality of memory element groups each having four memory elements 140 corresponding to the each of the 4-bit signal. The second memory circuit 132 includes a plurality of memory element groups each having four memory elements 141 corresponding to the each of the 4-bit signal. The video signal output from the second memory circuit 132 is supplied to a plurality of terminals 142.

[0050]

In the second signal line driver circuit 104 in FIG. 4, the video signal supplied

to a plurality of terminals 143 is supplied to the level shifter 133. The level shifter 133 includes a plurality of level shifter groups each having four level shifters 144 corresponding to the each of the 4-bit signal. The DAC 134 includes a plurality of DACs 145 corresponding to the 4-bit video signal. The analog buffer 135 includes a plurality of buffers 146, and at least one of the buffers 146 corresponds to one DAC 145.

[0051]

Next, operation of the semiconductor display device 100 illustrated in FIG. 2, FIG. 3, and FIG. 4 will be described. In the first signal line driver circuit 103, a clock signal and a start pulse signal are input to the shift register 130. The shift register 130 generates timing signals, pulses of which are sequentially shifted, in response to the clock signal and the start pulse signal, and outputs the timing signals to the first memory circuit 131. The order of the appearance of the pulses of the timing signals can be switched in accordance with a scan direction switching signal.

[0052]

When the timing signal is input to the first memory circuit 131, video signals are sampled in accordance with the pulses of the timing signals, and are sequentially written to the memory elements 140 of the first memory circuit 131. In other words, the video signals which are serially input to the first signal line driver circuit 103 are written in parallel to the first memory circuit 131. The video signals written to the first memory circuit 131 are held.

[0053]

The video signals may be sequentially written to the plurality of memory elements 140 included in the first memory circuit 131; alternatively, a so-called division driving may be performed in which the plurality of memory elements 140 included in the first memory circuit 131 is divided into some groups, and the video signals are input to each group in parallel. Note that the number of memory elements included in each group in this case is referred to as the number of divisions. For example, in the case where the memory elements are divided into groups such that each group has four memory elements 140, division driving is performed with four divisions.

[0054]

The time until the completion of writing of the video signal to the first memory

circuit 131 is referred to as a line period.

[0055]

When one line period is completed, in a retrace period, the video signals held in the first memory circuit 131 are written to the second memory circuit 132 all at once and held in accordance with a pulse of a latch signal input to the second memory circuit 132. Video signals for the next line period are sequentially written to the first memory circuit 131 which has finished transmitting the video signals to the second memory circuit 132, in response to timing signals from the shift register 130. In the second round of the one line period, the video signals written to and held in the second memory circuit 132 are output from the terminal 142 of the first signal line driver circuit 103 and supplied to the terminal 143 of the second signal line driver circuit 104.

[0056]

In the second signal line driver circuit 104, the voltage amplitude of the video signals from the first signal line driver circuit 103 is increased in each of the plurality of level shifters 144 in the level shifter 133, and then transmitted to the DAC 134. In the DAC 134, the input video signals are converted from digital signals to analog signals in each of the plurality of DACs 145. Then, the analog video signals are transmitted to the analog buffer 135. The video signals transmitted from the DAC 134 are transmitted from each of the plurality of buffers 146 included in the analog buffer 135 to the pixel portion 101 through signal lines.

[0057]

In the scan line driver circuit 102, selection of pixels included in the pixel portion 101 is performed for each line. The video signals transmitted from the second signal line driver circuit 104 to the pixel portion 101 through the signal lines are input to pixels in a line selected by the scan line driver circuit 102.

[0058]

Note that another circuit which can output signals of which pulses are sequentially shifted may be used instead of the shift register 130.

[0059]

In the semiconductor display device 100 illustrated in FIG. 2, FIG. 3, and FIG. 4, the withstand voltage of the shift register 130, the first memory circuit 131, and the second memory circuit 132 included in the first signal line driver circuit 103 is not

necessarily high. In order to secure a high-quality display image on the pixel portion 101, it is more important for the shift register 130, the first memory circuit 131, and the second memory circuit 132 to have high operation speed than to have high withstand voltage. On the other hand, the level shifter 133, the DAC 134, and the analog buffer 135 included in the second signal line driver circuit 104 have intermediate withstand voltage.

[0060]

According to an embodiment of the present invention, in the first signal line driver circuit 103 which does not need to have such high withstand voltage can be formed using a semiconductor and a process different from those of the second signal line driver circuit 104 which needs to have high withstand voltage. Thus, since the thickness of an insulating film in the first signal line driver circuit 103 which does not need to have such high withstand voltage can be made smaller than that in the second signal line driver circuit 104, the first signal line driver circuit 103 can operate at high speed and the first semiconductor element can be miniaturized. Moreover, in the second signal line driver circuit 104 which needs to have high withstand voltage, the thickness of an insulating film is made larger than that in the first signal line driver circuit 103; thus, the second semiconductor element can have high withstand voltage. That is, according to an embodiment of the present invention, semiconductor elements having structures most suitable for characteristics needed for circuits can be separately manufactured without making the process complicated.

[0061]

In this manner, according to an embodiment of the present invention, a semiconductor display device including a driver circuit whose high-speed operation and high withstand voltage are secured without making the manufacturing process complicated can be provided. According to an embodiment of the present invention, a semiconductor display device including a driver circuit whose power consumption is suppressed and whose high withstand voltage is secured without making the manufacturing process complicated can be provided. According to an embodiment of the present invention, a semiconductor display device including a driver circuit whose occupation area is reduced and whose high withstand voltage is secured without making the manufacturing process complicated can be provided.

[0062]

(Embodiment 2)

In this embodiment, specific configurations of a level shifter, a DAC, and a buffer used in a second signal line driver circuit will be described.

5 [0063]

FIG. 6 illustrates an example of a level shifter including an n-channel transistor. The level shifter illustrated in FIG. 6 includes a bootstrap circuit as a base. Specifically, the level shifter illustrated in FIG. 6 includes bootstrap circuits 600a to 600c, a transistor 601, and a transistor 602.

10 [0064]

A drain electrode and a gate electrode of the transistor 602 are connected to a node supplied with a high-level power supply potential VDD1, and a source electrode of the transistor 602 is connected to a drain electrode of the transistor 601. A potential of an input signal IN to be input to the level shifter is supplied to a gate electrode of the transistor 601, and a source electrode of the transistor 601 is connected to a node supplied with a low-level power supply potential VSS.

[0065]

The bootstrap circuit 600a includes a transistor 603a, a transistor 604a, a transistor 605a, a transistor 606a, a transistor 607a, and a capacitor 608a. A gate electrode of the transistor 603a is connected to the node supplied with the power supply potential VDD1, a source electrode of the transistor 603a is connected to the source electrode of the transistor 602, and a drain electrode of the transistor 603a is connected to a gate electrode of the transistor 605a. A gate electrode of the transistor 604a is connected to the gate electrode of the transistor 601, a drain electrode of the transistor 604a is connected to a source electrode of the transistor 605a, and a source electrode of the transistor 604a is connected to the node supplied with the power supply potential VSS. A drain electrode of the transistor 605a is connected to the node supplied with the power supply potential VDD1. A gate electrode of the transistor 606a is connected to the gate electrode of the transistor 604a, and a drain electrode of the transistor 606a is connected to a source electrode of the transistor 607a, and a source electrode of the transistor 606a is connected to the node supplied with the power supply potential VSS. A gate electrode of the transistor 607a is connected to the gate electrode of the transistor

605a, and a drain electrode of the transistor 607a is connected to the node supplied with the power supply potential VDD1. One electrode of the capacitor 608a is connected to the gate electrode of the transistor 605a, and the other electrode of the capacitor 608a is connected to the source electrode of the transistor 605a.

5 [0066]

The bootstrap circuit 600b includes a transistor 603b, a transistor 604b, a transistor 605b, a transistor 606b, a transistor 607b, and a capacitor 608b. The bootstrap circuit 600c includes a transistor 603c, a transistor 604c, a transistor 605c, a transistor 606c, a transistor 607c, and a capacitor 608c.

10 [0067]

The connection relation of the semiconductor elements included in the bootstrap circuit 600b and the bootstrap circuit 600c is similar to that in the bootstrap circuit 600a. That is, the transistor 603a corresponds to the transistor 603b and the transistor 603c, the transistor 604a corresponds to the transistor 604b and the transistor 604c, the transistor 605a corresponds to the transistor 605b and the transistor 605c, the transistor 606a corresponds to the transistor 606b and the transistor 606c, the transistor 607a corresponds to the transistor 607b and the transistor 607c, and the capacitor 608a corresponds to the capacitor 608b and the capacitor 608c. Note that a source electrode of the transistor 603b is connected to the source electrode of the transistor 607a and the drain electrode of the transistor 606a. A source electrode of the transistor 603c is connected to a source electrode of the transistor 607b and a drain electrode of the transistor 606b. In the bootstrap circuit 600b, a node supplied with a high-level power supply potential VDD2 is used instead of the node supplied with the power supply potential VDD1. In the bootstrap circuit 600c, a node supplied with a high-level power supply potential VDD3 is used instead of the node supplied with the power supply potential VDD1. The potential of a source electrode of the transistor 607c and a drain electrode of the transistor 606c is output as an output signal OUT of the level shifter.

[0068]

30 The terms "source electrode" and "drain electrode" included in a transistor interchange with each other depending on the polarity of the transistor or the levels of potentials supplied to the respective electrodes. In general, in an n-channel transistor,

an electrode to which a lower potential is supplied is called a source electrode, and an electrode to which a higher potential is supplied is called a drain electrode. Further, in a p-channel transistor, an electrode to which a lower potential is supplied is called a drain electrode, and an electrode to which a higher potential is supplied is called a source electrode. In this specification, for convenience, the connection relation of the transistor is described assuming that the source electrode and the drain electrode are fixed in some cases; actually, the names of the source electrode and the drain electrode interchange with each other depending on the relation between the potentials.

[0069]

Note that the term "connection" in this specification means electrical connection and corresponds to the state in which current, voltage, or potential can be supplied, applied, or conducted. Accordingly, a connection state means not only a state of direct connection but also a state of indirect connection through a circuit element such as a wiring, a resistor, a diode, or a transistor so that current, voltage, or potential can be supplied, applied, or conducted.

[0070]

In this specification, even when a circuit diagram illustrates independent components connected to each other, there is a case where one conductive film has functions of a plurality of components such as the case where part of a wiring also functions as an electrode. The term "connection" also means such a case where one conductive film has functions of a plurality of components.

[0071]

Next, operation of the level shifter illustrated in FIG. 6 will be described.

[0072]

When the potential of the input signal IN is set to a high level, the transistors 601, 604a, 606a, 604b, 606b, 604c, and 606c are turned on. In addition, the low-level power supply potential VSS is supplied to the source electrodes of the transistors 601, 604a, and 606a. Thus, the transistor 603a is turned on, so that the low-level power supply potential VSS is supplied to the drain electrode of the transistor 603a and the transistors 605a and 607a are turned off. Accordingly, the low-level power supply potential VSS is supplied to the source electrode of the transistor 603b through the transistor 606a. Since the high-level power supply potential VDD2 is supplied to a

gate electrode of the transistor 603b, the transistor 603b is turned on when the power supply potential VSS is supplied to the source electrode thereof. Thus, the low-level power supply potential VSS is supplied to a drain electrode of the transistor 603b, so that the transistors 605b and 607b are turned off. Accordingly, the low-level power supply potential VSS is supplied to the source electrode of the transistor 603c through the transistor 606b. Since the high-level power supply potential VDD3 is supplied to a gate electrode of the transistor 603c, the transistor 603c is turned on when the power supply potential VSS is supplied to the source electrode thereof. Thus, the low-level power supply potential VSS is supplied to a drain electrode of the transistor 603c, so that the transistors 605c and 607c are turned off. Then, the low-level power supply potential VSS is supplied to the source electrode of the transistor 607c through the transistor 606c, and this potential is output as the output signal OUT.

[0073]

Next, when the potential of the input signal IN is set to a low level, the transistors 601, 604a, 606a, 604b, 606b, 604c, and 606c are turned off. Since the high-level power supply potential VDD1 is supplied to the source electrode of the transistor 603a through the transistor 602, the potential of the drain electrode of the transistor 603a is raised. Thus, the transistors 605a and 607a are turned on. Then, the transistor 603a is turned off since a gate voltage thereof is lower than a threshold voltage thereof. Current flows through the transistor 605a and the potential of the source electrode thereof is raised. Since the capacitor 608a is connected between the source electrode and the gate electrode of the transistor 605a, the potential of the gate electrode of the transistor 605a is raised along with the potential of the source electrode thereof and becomes higher than the power supply potential VDD1. Similarly, the potential of the source electrode of the transistor 607a is raised to the level of the power supply potential VDD1.

[0074]

Since the high-level power supply potential VDD1 is supplied to the source electrode of the transistor 603b through the transistor 607a, the potential of the drain electrode of the transistor 603b is raised. Thus, the transistors 605b and 607b are turned on. Then, the transistor 603b is turned off since a gate voltage thereof is lower than a threshold voltage thereof. Current flows through the transistor 605b and the

potential of the source electrode thereof is raised. Since the capacitor 608b is connected between the source electrode and a gate electrode of the transistor 605b, the potential of the gate electrode of the transistor 605b is raised along with the potential of the source electrode thereof and becomes higher than the power supply potential VDD2.

5 Similarly, the potential of the source electrode of the transistor 607b is raised to the level of the power supply potential VDD2.

[0075]

Since the high-level power supply potential VDD2 is supplied to the source electrode of the transistor 603c through the transistor 607b, the potential of the drain
10 electrode of the transistor 603c is raised. Thus, the transistors 605c and 607c are turned on. Then, the transistor 603c is turned off since a gate voltage thereof is lower than a threshold voltage thereof. Current flows through the transistor 605c and the potential of the source electrode thereof is raised. Since the capacitor 608c is connected between the source electrode and a gate electrode of the transistor 605c, the
15 potential of the gate electrode of the transistor 605c is raised along with the potential of the source electrode thereof and becomes higher than the power supply potential VDD3. Similarly, the potential of the source electrode of the transistor 607c is raised to the level of the power supply potential VDD3. Accordingly, the potential of the output signal OUT is the power supply potential VDD3.

20 [0076]

The power supply potential VDD1 is set to the same level as a power supply potential of a first signal line driver circuit having low withstand voltage, the power supply potential VDD3 is set to the same level as a power supply potential supplied to the buffer, and the power supply potential VDD2 is set to a level between the power
25 supply potential VDD1 and the power supply potential VDD3; thus, the level can be shifted so that the amplitude of the output signal OUT is increased.

[0077]

The configuration and operation of the level shifter described above are examples, and an embodiment of the present invention is not limited to the above
30 description.

[0078]

Next, FIG. 7 illustrates an example of a DAC including an n-channel transistor.

The DAC illustrated in FIG. 7 is a CDAC including transistors 501 to 510 which function as switching elements and capacitors 511 to 516. In this embodiment, the DAC has a structure with which a 4-bit video signal can be applied as an example; however, an embodiment of the present invention is not limited to this structure. The DAC can be formed in accordance with the number of bits of a video signal set by a practitioner.

[0079]

The transistors 501 and 502 function as switching elements for initializing the amount of electric charge accumulated in the capacitors 511 to 516. The transistors 503 to 510 function as switching elements for controlling supply of power supply potentials to the capacitors 511 to 516.

[0080]

Specifically, a gate electrode of the transistor 503 is connected to a terminal 527, a source electrode of the transistor 503 is connected to one electrode of the capacitor 511, and a drain electrode of the transistor 503 is connected to a node supplied with a power supply potential VL. A gate electrode of the transistor 504 is connected to a terminal 526, a source electrode of the transistor 504 is connected to the one electrode of the capacitor 511, and a drain electrode of the transistor 504 is connected to a node supplied with a power supply potential VH. A gate electrode of the transistor 505 is connected to a terminal 525, a source electrode of the transistor 505 is connected to one electrode of the capacitor 512, and a drain electrode of the transistor 505 is connected to the node supplied with the power supply potential VL. A gate electrode of the transistor 506 is connected to a terminal 524, a source electrode of the transistor 506 is connected to the one electrode of the capacitor 512, and a drain electrode of the transistor 506 is connected to the node supplied with the power supply potential VH. A gate electrode of the transistor 507 is connected to a terminal 523, a source electrode of the transistor 507 is connected to one electrode of the capacitor 514, and a drain electrode of the transistor 507 is connected to the node supplied with the power supply potential VL. A gate electrode of the transistor 508 is connected to a terminal 522, a source electrode of the transistor 508 is connected to the one electrode of the capacitor 514, and a drain electrode of the transistor 508 is connected to the node supplied with the power supply potential VH. A gate electrode of the transistor 509 is connected to a

terminal 521, a source electrode of the transistor 509 is connected to one electrode of the capacitor 515, and a drain electrode of the transistor 509 is connected to the node supplied with the power supply potential VL. A gate electrode of the transistor 510 is connected to a terminal 520, a source electrode of the transistor 510 is connected to the one electrode of the capacitor 515, and a drain electrode of the transistor 510 is connected to the node supplied with the power supply potential VH.

[0081]

A gate electrode of the transistor 501 is connected to a terminal Res2, a source electrode of the transistor 501 is connected to the node supplied with the power supply potential VL, and a drain electrode of the transistor 501 is connected to the other electrode of the capacitor 511, the other electrode of the capacitor 512, and one electrode of the capacitor 513. A gate electrode of the transistor 502 is connected to a terminal Res1, a source electrode of the transistor 502 is connected to a node supplied with a power supply potential VB, and a drain electrode of the transistor 502 is connected to the other electrode of the capacitor 513, the other electrode of the capacitor 514, the other electrode of the capacitor 515, and one electrode of the capacitor 516. The other electrode of the capacitor 516 is supplied with a power supply potential VG. Thus, the potential of the drain electrode of the transistor 502 is output as an output signal.

[0082]

Next, operation of the DAC illustrated in FIG. 7 will be described.

[0083]

Firstly, initialization is performed. In the initialization, high-level potentials are supplied to the terminal Res1, the terminal Res2, the terminal 521, the terminal 523, the terminal 525, and the terminal 527, so that the transistors 501, 502, 503, 505, 507, and 509 are turned on. Low-level potentials are supplied to the terminal 520, the terminal 522, the terminal 524, and the terminal 526, so that the transistors 504, 506, 508, and 510 are turned off. Accordingly, the power supply potential VL is supplied to both of the pairs of electrodes of the capacitors 511 and 512; a potential difference between the power supply potential VL and the power supply potential VB is applied between the electrodes of the capacitors 513, 514, and 515; and a potential difference between the power supply potential VB and the power supply potential VG is applied

between the electrodes of the capacitor 516.

[0084]

Next, digital-analog conversion is performed. First, low-level potentials are supplied to the terminal Res1 and the terminal Res2, so that the transistors 501 and 502 are turned off. Then, potentials of the corresponding bits of the video signal are supplied to the terminals 520 to 527. Specifically, a potential of a first bit is supplied to the terminal 520, and a potential with an inverted phase thereof is supplied to the terminal 521. A potential of a second bit is supplied to the terminal 522, and a potential with an inverted phase thereof is supplied to the terminal 523. A potential of a third bit is supplied to the terminal 524, and a potential with an inverted phase thereof is supplied to the terminal 525. A potential of a fourth bit is supplied to the terminal 526, and a potential with an inverted phase thereof is supplied to the terminal 527.

[0085]

Thus, switching of the transistors 503 to 510 is controlled in accordance with the potentials of the corresponding bits of the video signal. Then, the power supply potential VL or the power supply potential VH is supplied to the one electrodes of the capacitors 511, 512, 514, and 515 through the transistors that are turned on among the transistors 503 to 510. With the above configuration, the capacitors 511 to 516 are charged with and discharged of electric charge in accordance with the potentials of the corresponding bits of the video signal, and then get into a steady state. After that, the potential of the drain electrode of the transistor 502 is determined by the amount of electric charge and the capacitance of the capacitors 511 to 516, and is output from the DAC as a potential of the output signal.

[0086]

The configuration and operation of the DAC described above are examples, and an embodiment of the present invention is not limited to the above description.

[0087]

Next, FIG. 8 illustrates an example of a buffer including an n-channel transistor. The buffer illustrated in FIG. 8 is a source follower circuit including a transistor 530 and a transistor 531.

[0088]

Specifically, a gate electrode of the transistor 530 is connected to a terminal

532, a source electrode of the transistor 530 is connected to a terminal 533, and a drain electrode of the transistor 530 is connected to a node 536 supplied with a high-level power supply potential. A gate electrode of the transistor 531 is connected to a terminal 534, a source electrode of the transistor 531 is connected to a node 535
5 supplied with a low-level power supply potential, and a drain electrode of the transistor 531 is connected to the terminal 533.

[0089]

The output signal of the DAC is supplied to the terminal 532. Further, the terminal 533 is connected to a signal line extended to a pixel portion. The operation of
10 the transistor 531 is controlled by a potential supplied to the terminal 534 so that constant drain current is obtained, and the transistor 531 functions as a constant current source. Note that the above drain current does not necessarily flow constantly, and the current flow may be stopped when there is no change in the potential of the signal line.

[0090]

15 The configuration and operation of the buffer described above are examples, and an embodiment of the present invention is not limited to the above description.

[0091]

This embodiment can be implemented in combination with the above embodiment as appropriate.

20 [0092]

(Embodiment 3)

In this embodiment, a specific structure of a pixel portion will be described by taking a liquid crystal display device which is one of semiconductor display devices of the present invention as an example.

25 [0093]

FIG. 9 illustrates a configuration of a pixel portion 301 including a plurality of pixels 300, as an example. In FIG. 9, each of the pixels 300 includes at least one of signal lines S1 to Sx and at least one of scan lines G1 to Gy. In addition, the pixel 300 includes a transistor 305 which functions as a switching element, a liquid crystal element 306, and a capacitor 307. The liquid crystal element 306 includes a pixel electrode, a counter electrode, and liquid crystals to which voltage between the pixel electrode and the counter electrode is applied.

[0094]

The transistor 305 controls whether a potential of the signal line, that is, a potential of a video signal is supplied to the pixel electrode of the liquid crystal element 306. A predetermined potential is supplied to the counter electrode of the liquid crystal element 306. In addition, the capacitor 307 includes a pair of electrodes; one electrode (first electrode) is connected to the pixel electrode of the liquid crystal element 306, and a predetermined potential is supplied to the other electrode (second electrode).

[0095]

Note that FIG. 9 illustrates the case where one transistor 305 is used as a switching element in the pixel 300; an embodiment of the present invention is not limited to this structure. A plurality of transistors may be used as switching elements.

[0096]

Next, operation of the pixel portion 301 illustrated in FIG. 9 will be described.

[0097]

First, when the scan lines G1 to Gy are sequentially selected, the transistors 305 in the pixels 300 including the selected scan lines are turned on. Then, when a potential of the video signal is supplied to the signal lines S1 to Sx, the potential of the video signal is supplied to the pixel electrodes of the liquid crystal elements 306 through the transistors 305 which are turned on, respectively.

[0098]

In the liquid crystal element 306, the alignment of liquid crystal molecules is changed in accordance with the level of the voltage applied between the pixel electrode and the counter electrode, whereby transmittance is changed. Consequently, the transmittance of the liquid crystal element 306 is controlled by the potential of the video signal, so that grayscale display can be performed.

[0099]

Next, when the selection of the scan lines is completed, the transistors 305 are turned off in the pixels 300 including the selected scan lines. The liquid crystal element 306 holds the voltage applied between the pixel electrode and the counter electrode, whereby the grayscale display is maintained.

[0100]

In the liquid crystal display device, so-called AC driving in which the polarity of voltage applied to the liquid crystal element 306 is inverted at a predetermined timing is performed in order to prevent deterioration of the liquid crystals called burn-in. Specifically, AC driving can be performed in such a manner that the polarity of the potential of the video signal input to each of the pixels 300 is inverted with the use of the potential of the counter electrode as a reference. Further, change in the potential supplied to the signal line is increased by the AC driving; thus, a potential difference between a source electrode and a drain electrode of the transistor 305 which functions as a switching element is increased. Accordingly, deterioration of characteristics such as a shift in threshold voltage is easily caused in the transistor 305. Furthermore, in order to maintain the voltage held in the liquid crystal element 306, the transistor 305 needs to have low off-state current even when the potential difference between the source electrode and the drain electrode is large.

[0101]

Unless otherwise specified, in the case of an n-channel transistor, off-state current in this specification is current which flows between a source electrode and a drain electrode when a potential of the drain electrode is higher than that of the source electrode and that of a gate electrode while the potential of the gate electrode is less than or equal to zero when a reference potential is the potential of the source electrode.

Alternatively, in the case of a p-channel transistor, off-state current in this specification is current which flows between a source electrode and a drain electrode when a potential of the drain electrode is lower than that of the source electrode and that of a gate electrode while the potential of the gate electrode is greater than or equal to zero when a reference potential is the potential of the source electrode.

[0102]

In an embodiment of the present invention, a semiconductor such as an oxide semiconductor having a wider bandgap and lower intrinsic carrier density than silicon or germanium is used for the transistor 305, whereby the withstand voltage of the transistor 305 can be increased.

[0103]

Further, an oxide semiconductor (purified OS) purified by reduction of impurities such as moisture or hydrogen which serves as an electron donor (donor) is an

intrinsic (i-type) semiconductor or a substantially i-type semiconductor. Therefore, use of the above oxide semiconductor for the transistor 305 enables the off-state current of the transistor 305 to be significantly reduced.

[0104]

5 Specifically, the hydrogen concentration of the purified oxide semiconductor, which is measured by secondary ion mass spectrometry (SIMS), is lower than or equal to $5 \times 10^{19} / \text{cm}^3$, preferably lower than or equal to $5 \times 10^{18} / \text{cm}^3$, further preferably lower than or equal to $5 \times 10^{17} / \text{cm}^3$, still further preferably less than $1 \times 10^{16} / \text{cm}^3$. In addition, the carrier density of the oxide semiconductor film, which can be measured by
10 Hall effect measurement, is lower than $1 \times 10^{14} / \text{cm}^3$, preferably lower than $1 \times 10^{12} / \text{cm}^3$, further preferably lower than $1 \times 10^{11} / \text{cm}^3$. Furthermore, the bandgap of the oxide semiconductor is greater than or equal to 2 eV, preferably greater than or equal to 2.5 eV, further preferably greater than or equal to 3 eV. With the use of the oxide semiconductor film which is purified by sufficiently reducing the concentration of
15 impurities such as moisture or hydrogen, off-state current of the transistor can be reduced.

[0105]

The analysis of the hydrogen concentration of the oxide semiconductor film is described here. The hydrogen concentrations of the oxide semiconductor film and a
20 conductive film are measured by SIMS. It is known that it is difficult to obtain accurate data in the proximity of a surface of a sample or in the proximity of an interface between stacked films formed using different materials by the SIMS in principle. Thus, in the case where distribution of the hydrogen concentration of the film in a thickness direction is analyzed by SIMS, an average value in a region where
25 the film is provided, the value is not greatly changed, and almost the same value can be obtained is employed as the hydrogen concentration. Further, in the case where the thickness of the film is small, a region where almost the same value is obtained cannot be found in some cases owing to the influence of the hydrogen concentration of an adjacent film. In this case, the maximum value or the minimum value of the hydrogen
30 concentration of a region where the film is provided is employed as the hydrogen concentration of the film. Furthermore, in the case where a mountain-shaped peak

having the maximum value and a valley-shaped peak having the minimum value do not exist in the region where the film is provided, the value of the inflection point is employed as the hydrogen concentration.

[0106]

5 Various experiments can actually prove low off-state current of the transistor including the purified oxide semiconductor film as an active layer. For example, even an element having a channel width of $1 \times 10^6 \mu\text{m}$ and a channel length of $10 \mu\text{m}$ can have the characteristic of an off-state current (drain current in the case where voltage between a gate electrode and a source electrode is 0 V or less) of less than or equal to the measurement limit of a semiconductor parameter analyzer, that is, less than or equal to 1×10^{-13} A, in a range of 1 V to 10 V of voltage (drain voltage) between the source electrode and a drain electrode. In this case, it can be found that off-state current density corresponding to a value obtained by dividing the off-state current by the channel width of the transistor is less than or equal to $100 \text{ zA}/\mu\text{m}$. In addition, in an experiment, a circuit where a capacitor is connected to a transistor (whose gate insulating film has a thickness of 100 nm) and electric charge flowing in or out of the capacitor is controlled by the transistor was used. When a purified oxide semiconductor film is used for a channel formation region of the transistor, the off-state current density of the transistor was measured on the basis of change in the amount of electric charge in the capacitor per unit time. It was found that a lower off-state current density of $10 \text{ zA}/\mu\text{m}$ to $100 \text{ zA}/\mu\text{m}$ was obtained in the case where the voltage between the source electrode and the drain electrode of the transistor was 3 V. Therefore, the off-state current density of the transistor including the purified oxide semiconductor film as an active layer can be lower than or equal to $10 \text{ zA}/\mu\text{m}$, preferably lower than or equal to $1 \text{ zA}/\mu\text{m}$, further preferably lower than or equal to $1 \text{ yA}/\mu\text{m}$, depending on the voltage between the source electrode and the drain electrode. Accordingly, the transistor including the purified oxide semiconductor film as an active layer has much lower off-state current than a transistor including crystalline silicon.

[0107]

30 In addition, a transistor including a purified oxide semiconductor shows almost no temperature dependence of off-state current. This is because the conductivity type

is made to be as close to an intrinsic type as possible by removing impurities serving as electron donors (donors) in the oxide semiconductor to purify the oxide semiconductor, so that the Fermi level is located in a center of the forbidden band. This also results from the fact that the oxide semiconductor has an energy gap of 3 eV or more and includes extremely few thermally excited carriers. In addition, the source electrode and the drain electrode are in a degenerated state, which is also a factor for showing no temperature dependence. The transistor is mostly operated by carriers injected into the oxide semiconductor from the degenerated source electrode and the carrier density has no dependence on temperature; therefore, the off-state current has no dependence on temperature.

[0108]

By increasing the withstand voltage of the transistor 305, reliability of the liquid crystal display device can be increased. Moreover, by reducing the off-state current of the transistor 305, change in transmittance in the liquid crystal display device can be prevented from being recognized.

[0109]

This embodiment can be implemented in combination with any of the above embodiments as appropriate.

[0110]

(Embodiment 4)

In this embodiment, an example in which the semiconductor display device 100 has a structure different from that in FIG. 2 will be described.

[0111]

FIG. 10 illustrates an example of a structure of the semiconductor display device 100 of an embodiment of the present invention. In the semiconductor display device 100 illustrated in FIG. 10, the first signal line driver circuit 103 includes the shift register 130, the first memory circuit 131, and the second memory circuit 132 as in the case of FIG. 2. In the semiconductor display device 100 illustrated in FIG. 10, the second signal line driver circuit 104 does not include the DAC 134 and the analog buffer 135 and includes a level shifter 133 and a digital buffer 152, which is different from the case of FIG. 2.

[0112]

Next, operation of the semiconductor display device 100 illustrated in FIG. 10 will be described. The operation of the first signal line driver circuit 103 is similar to that in the case of FIG. 2 and thus the description in Embodiment 1 can be referred to. Note that in FIG. 10, a video signal written to and held in the second memory circuit 132 is output from the first signal line driver circuit 103 and transmitted to the level shifter 133 in the second signal line driver circuit 104. The level shifter 133 increases the voltage amplitude of the input video signal and outputs the increased signal. The video signal output from the level shifter 133 is transmitted from the digital buffer 152 to the pixel portion 101 through a signal line.

[0113]

In the scan line driver circuit 102, selection of pixels included in the pixel portion 101 is performed for each line. The video signal transmitted from the second signal line driver circuit 104 to the pixel portion 101 through the signal line is input to pixels in a line selected by the scan line driver circuit 102.

[0114]

Note that another circuit which can output a signal of which pulse is sequentially shifted may be used instead of the shift register 130.

[0115]

In the semiconductor display device 100 illustrated in FIG. 10, not an analog video signal but a digital video signal is input to the pixel portion 101. Therefore, grayscale display can be performed in the pixel portion 101 by an area ratio grayscale method or a time ratio grayscale method, for example. An area ratio grayscale method is a driving method in which one pixel is divided into a plurality of subpixels and the subpixels are driven on the basis of corresponding bits of a video signal so that grayscale display is performed. Further, a time ratio grayscale method is a driving method in which the ratio of periods during which a pixel displays a bright image and a dark image is controlled so that grayscale display is performed.

[0116]

In the semiconductor display device 100 illustrated in FIG. 10, the withstand voltage of the shift register 130, the first memory circuit 131, and the second memory circuit 132 included in the first signal line driver circuit 103 is not necessarily high. In order to secure a high-quality display image on the pixel portion 101, it is more

important for the shift register 130, the first memory circuit 131, and the second memory circuit 132 to have high operation speed than to have high withstand voltage. On the other hand, the level shifter 133 and the digital buffer 152 included in the second signal line driver circuit 104 have intermediate withstand voltage.

5 [0117]

FIG. 11 illustrates another example of a structure of the semiconductor display device 100 of an embodiment of the present invention. In the semiconductor display device 100 illustrated in FIG. 11, the first signal line driver circuit 103 does not include the first memory circuit 131 and the second memory circuit 132 and includes the shift register 130, which is different from the case of FIG. 2. Further, in the semiconductor display device 100 illustrated in FIG. 11, the second signal line driver circuit 104 includes a sampling circuit 150 and an analog memory circuit 151 instead of the DAC 134, which is different from the case of FIG. 2.

[0118]

15 Next, operation of the semiconductor display device 100 illustrated in FIG. 11 will be described. In the first signal line driver circuit 103, a clock signal and a start pulse signal are input to the shift register 130. The shift register 130 generates a timing signal, a pulse of which is sequentially shifted, in response to the clock signal and the start pulse signal, and outputs the timing signal. The order of the appearance of the pulse of the timing signal can be switched in accordance with a scan direction switching signal.

20 [0119]

Then, the voltage amplitude of the timing signal output from the first signal line driver circuit 103 is increased in the level shifter 133 of the second signal line driver circuit 104, and then the timing signal is transmitted to the sampling circuit 150. In the sampling circuit 150, an analog video signal is sampled in accordance with the input timing signal. In other words, the video signals serially input to the second signal line driver circuit 104 are written in parallel by the sampling circuit 150. The video signals written by the sampling circuit 150 are held. When all video signals for one line period are sampled, the sampled video signals are output to the analog memory circuit 151 all at once and held in accordance with a latch signal. The video signals held in the analog memory circuit 151 are input from the analog buffer 135 to the pixel

portion 101 through signal lines.

[0120]

Note that in this embodiment, an example in which the video signals for one line period are sampled in the sampling circuit 150, and then all the sampled video signals are input to the analog memory circuit 151 in a lower stage all at once is described; however, an embodiment of the present invention is not limited to this structure. In the sampling circuit 150, every time a video signal for each pixel is sampled, the sampled video signal may be input to the signal line, without waiting for the one line period to finish.

[0121]

In addition, video signals may be sampled sequentially in corresponding pixels, or so-called division driving in which pixels in one line are divided into several groups and video signals are sampled in each pixel in one group at the same time may be performed.

[0122]

Then, when the video signals are input to the pixel portion 101 from the analog memory circuit 151, the sampling circuit 150 can sample video signals for the next line period at the same time.

[0123]

In the scan line driver circuit 102, selection of pixels included in the pixel portion 101 is performed for each line. The video signals transmitted from the second signal line driver circuit 104 to the pixel portion 101 through the signal lines are input to pixels in a line selected by the scan line driver circuit 102.

[0124]

Note that another circuit which can output a signal of which pulse is sequentially shifted may be used instead of the shift register 130.

[0125]

In the semiconductor display device 100 illustrated in FIG. 11, an analog video signal is input to the pixel portion 101. Therefore, grayscale display can be performed in the pixel portion 101 in a manner similar to that in the case of FIG. 2.

[0126]

In the semiconductor display device 100 illustrated in FIG. 11, the withstand

voltage of the shift register 130 included in the first signal line driver circuit 103 is not necessarily high. In order to secure a high-quality display image on the pixel portion 101, it is more important for the shift register 130 to have high operation speed than to have high withstand voltage. On the other hand, the level shifter 133, the sampling circuit 150, the analog memory circuit 151, and the analog buffer 135 included in the second signal line driver circuit 104 have intermediate withstand voltage.

[0127]

According to an embodiment of the present invention, in the first signal line driver circuit 103 which does not need to have such high withstand voltage can be formed using a semiconductor and a process different from those of the second signal line driver circuit 104 which needs to have high withstand voltage. Thus, since the thickness of an insulating film in the first signal line driver circuit 103 which does not need to have such high withstand voltage can be made smaller than that in the second signal line driver circuit 104, the first signal line driver circuit 103 can operate at high speed and a first semiconductor element can be miniaturized. Moreover, in the second signal line driver circuit 104 which needs to have high withstand voltage, the thickness of an insulating film is made larger than that in the first signal line driver circuit 103; thus, a second semiconductor element can have high withstand voltage. That is, according to an embodiment of the present invention, semiconductor elements having structures most suitable for characteristics needed for circuits can be separately manufactured without making the process complicated.

[0128]

According to an embodiment of the present invention, a semiconductor display device including a driver circuit whose high-speed operation and high withstand voltage are secured without making the manufacturing process complicated can be provided. According to an embodiment of the present invention, a semiconductor display device including a driver circuit whose power consumption is suppressed and whose high withstand voltage is secured without making the manufacturing process complicated can be provided. According to an embodiment of the present invention, a semiconductor display device including a driver circuit whose occupation area is reduced and whose high withstand voltage is secured without making the manufacturing process complicated can be provided.

[0129]

This embodiment can be implemented in combination with any of the above embodiments as appropriate.

[0130]

5 (Embodiment 5)

In this embodiment, structures of second semiconductor elements, which are different from those in FIG. 1C, will be described.

[0131]

FIG. 12A illustrates an example in which a transistor 401 and a capacitor 402
10 which are second semiconductor elements are formed over a second substrate 400.

[0132]

The transistor 401 includes, over the second substrate 400 having an insulating surface, a gate electrode 403, an insulating film 404 over the gate electrode 403, an oxide semiconductor film 405 which overlaps with the gate electrode 403 with the
15 insulating film 404 positioned therebetween and functions as an active layer, a channel protective film 406 over the oxide semiconductor film 405, and a source electrode 407 and a drain electrode 408 over the oxide semiconductor film 405. An insulating film 409 is formed over the oxide semiconductor film 405, the channel protective film 406, the source electrode 407, and the drain electrode 408, and the transistor 401 may include
20 the insulating film 409 as a component.

[0133]

Further, the capacitor 402 includes an electrode 410, the insulating film 404 over the electrode 410, and an electrode 411 over the insulating film 404.

[0134]

25 The channel protective film 406 can be formed by a vapor deposition method such as a plasma CVD method or a thermal CVD method, or a sputtering method. In addition, the channel protective film 406 is preferably formed using an inorganic material including oxygen (such as silicon oxide, silicon oxynitride, or silicon nitride oxide). An inorganic material including oxygen is used for the channel protective film
30 406, whereby a structure can be provided in which oxygen is supplied to at least a region of the oxide semiconductor film 405 in contact with the channel protective film 406 and oxygen deficiency serving as a donor is reduced to satisfy the stoichiometric

composition ratio even when the oxygen deficiency is caused by heat treatment for reducing moisture or hydrogen in the oxide semiconductor film 405. Therefore, a channel formation region can be made i-type or substantially i-type, and variation in electric characteristics of the transistor 401 caused by oxygen deficiency is reduced; accordingly, the electric characteristics can be improved.

[0135]

Note that a channel formation region corresponds to a region of a semiconductor film, which overlaps with a gate electrode with a gate insulating film positioned therebetween.

[0136]

The transistor 401 may further include a back-gate electrode over the insulating film 409. The back-gate electrode is formed so as to overlap with the channel formation region of the oxide semiconductor film 405. The back-gate electrode may be electrically insulated and in a floating state, or may be in a state where the back-gate electrode is supplied with a potential. In the latter case, the back-gate electrode may be supplied with a potential at the same level as the gate electrode 403, or may be supplied with a fixed potential such as a ground potential. By controlling the level of the potential supplied to the back-gate electrode, it is possible to control the threshold voltage of the transistor 401.

[0137]

FIG. 12B illustrates an example in which a transistor 421 and a capacitor 422 which are second semiconductor elements and have structures different from those in FIG. 12A are formed over the second substrate 400.

[0138]

The transistor 421 includes, over the second substrate 400 having an insulating surface, a gate electrode 423, an insulating film 424 over the gate electrode 423, a source electrode 427 and a drain electrode 428 over the insulating film 424, and an oxide semiconductor film 425 which overlaps with the gate electrode 423 with the insulating film 424 positioned therebetween, is in contact with the source electrode 427 and the drain electrode 428, and functions as an active layer. An insulating film 429 is formed over the oxide semiconductor film 425, the source electrode 427, and the drain electrode 428, and the transistor 421 may include the insulating film 429 as a

component.

[0139]

Further, the capacitor 422 includes an electrode 430, the insulating film 424 over the electrode 430, and an electrode 431 over the insulating film 424.

5 [0140]

The transistor 421 may further include a back-gate electrode over the insulating film 429. The back-gate electrode is formed so as to overlap with a channel formation region of the oxide semiconductor film 425. Further, the back-gate electrode may be electrically insulated and in a floating state, or may be in a state where the back-gate electrode is supplied with a potential. In the latter case, the back-gate electrode may be supplied with a potential at the same level as the gate electrode 423, or may be supplied with a fixed potential such as a ground potential. By controlling the level of the potential supplied to the back-gate electrode, it is possible to control the threshold voltage of the transistor 421.

15 [0141]

FIG. 12C illustrates an example in which a transistor 441 and a capacitor 442 which are second semiconductor elements and have structures different from those in FIG. 12A and FIG. 12B are formed over the second substrate 400.

[0142]

20 The transistor 441 includes, over the second substrate 400 having an insulating surface, a source electrode 447 and a drain electrode 448, an oxide semiconductor film 445 which is over the source electrode 447 and the drain electrode 448 and functions as an active layer, an insulating film 444 over the oxide semiconductor film 445, and a gate electrode 443 which overlaps with the oxide semiconductor film 445 with the insulating film 444 positioned therebetween. An insulating film 449 is formed over the gate electrode 443, and the transistor 441 may include the insulating film 449 as a component.

[0143]

30 Further, the capacitor 442 includes an electrode 450, the insulating film 444 over the electrode 450, and an electrode 451 over the insulating film 444.

[0144]

Note that it is found that an oxide semiconductor film formed by sputtering or

the like includes a large amount of impurities such as moisture or hydrogen. Moisture or hydrogen easily forms a donor level and thus serve as an impurity in the oxide semiconductor. Thus, heat treatment is performed on an oxide semiconductor film in a nitrogen atmosphere, an oxygen atmosphere, ultra dry air, or a rare gas (such as argon or helium) atmosphere in order to reduce impurities such as moisture or hydrogen in the oxide semiconductor film and to purify the oxide semiconductor film. It is preferable that the content of water in the gas be less than or equal to 20 ppm, preferably less than or equal to 1 ppm, and further preferably less than or equal to 10 ppb. The above heat treatment is preferably performed at higher than or equal to 500 °C and lower than or equal to 850 °C (or lower than or equal to a strain point of a glass substrate), further preferably higher than or equal to 550 °C and lower than or equal to 750 °C. Note that this heat treatment is performed at a temperature not exceeding the allowable temperature limit of the substrate to be used. An effect of elimination of moisture or hydrogen by heat treatment is confirmed by thermal desorption spectroscopy (TDS).

[0145]

This embodiment can be implemented in combination with any of the above embodiments as appropriate.

[0146]

(Embodiment 6)

In this embodiment, a method for connecting terminals in the case where a first substrate is directly mounted on a second substrate will be described.

[0147]

FIG. 13A is a cross-sectional view of a portion where a first substrate 900 and a second substrate 901 are connected to each other by a wire bonding method. The first substrate 900 is attached on the second substrate 901 with an adhesive 903. The first substrate 900 is provided with a first semiconductor element 906. Further, the first semiconductor element 906 is electrically connected to a pad 907 which is formed to be exposed on a surface of the first substrate 900 and functions as a terminal. A terminal 904 is formed over the second substrate 901 in FIG. 13A, and the pad 907 and the terminal 904 are connected to each other through a wire 905.

[0148]

Next, FIG. 13B is a cross-sectional view of a portion where a first substrate and a second substrate are connected to each other by a flip-chip method. In FIG. 13B, a solder ball 913 is connected to a pad 912 which is formed to be exposed on a surface of a first substrate 910. Thus, a first semiconductor element 914 formed on the first substrate 910 is electrically connected to the solder ball 913 through the pad 912. Further, the solder ball 913 is connected to a terminal 916 formed over a second substrate 911.

[0149]

Note that the solder ball 913 and the terminal 916 can be connected by various methods such as thermocompression bonding or thermocompression bonding with vibration by ultrasonic waves. The mechanical strength of the connection portion or the efficiency of diffusion or the like of heat generated in the second substrate 911 may be increased by providing an underfill between the first substrate 910 and the second substrate 911 so that a space between solder balls is filled after pressure bonding. The underfill is not necessarily used; however, the provision of the underfill can prevent a connection defect due to a stress caused by a mismatch between thermal expansion coefficients of the first substrate 910 and the second substrate 911. When thermocompression bonding is performed by application of ultrasonic waves, occurrence of a connection defect can be suppressed as compared to the case where only thermocompression bonding is performed. The thermocompression bonding by application of ultrasonic waves is particularly effective when the number of connection portions is more than approximately 300.

[0150]

The flip-chip method, by which a relatively wide pitch can be secured between pads as compared to by a wire bonding method even when the number of pads to be connected is increased, is suitable for the case of connecting a large number of terminals.

[0151]

Note that the solder ball may be formed by a droplet discharge method in which dispersion liquid where metal nanoparticles are dispersed is discharged.

[0152]

Next, FIG. 13C is a cross-sectional view of a portion where a first substrate and

a second substrate are connected to each other with the use of an anisotropic conductive resin. In FIG. 13C, a pad 922 which is formed to be exposed on a surface of a first substrate 920 is electrically connected to a first semiconductor element 924 formed on the first substrate 920. Further, the pad 922 is connected to a terminal 926 formed over a second substrate 921 through an anisotropic conductive resin 927.

[0153]

Note that the connection method is not limited to the methods illustrated in FIGS. 13A to 13C. Connection may be performed by a combination of a wire bonding method and a flip-chip method.

[0154]

This embodiment can be implemented in combination with any of the above embodiments as appropriate.

[0155]

(Embodiment 7)

In this embodiment, a method for mounting a first substrate will be described.

[0156]

FIGS. 14A and 14B are each a perspective view of a semiconductor display device in which a chip-like first substrate is mounted on a second substrate.

[0157]

In the semiconductor display device illustrated in FIG. 14A, a pixel portion 6002, a scan line driver circuit 6003, and a second signal line driver circuit 6007 are provided between a second substrate 6001 and a counter substrate 6006. Further, a first substrate 6004 provided with a first signal line driver circuit is directly mounted on the second substrate 6001.

[0158]

Specifically, the first signal line driver circuit formed over the first substrate 6004 is attached to the second substrate 6001 and electrically connected to the second signal line driver circuit 6007. Further, a power supply potential, a variety of signals, and the like are supplied through an FPC 6005 to the pixel portion 6002, the scan line driver circuit 6003, the second signal line driver circuit 6007, and the first signal line driver circuit formed over the first substrate 6004.

[0159]

In the semiconductor display device illustrated in FIG. 14B, a pixel portion 6102, a scan line driver circuit 6103, and a second signal line driver circuit 6107 are provided between a second substrate 6101 and a counter substrate 6106. Further, a first substrate 6104 provided with a first signal line driver circuit is mounted on an FPC 6105 connected to the second substrate 6101. A power supply potential, a variety of signals, and the like are supplied through the FPC 6105 to the pixel portion 6102, the scan line driver circuit 6103, the second signal line driver circuit 6107, and the first signal line driver circuit formed over the first substrate 6104.

[0160]

There is no particular limitation on a method for mounting the first substrate, and a known method such as a COG method, a wire bonding method, or a TAB method can be used. Further, a position where the IC chip is mounted is not limited to the positions shown in FIGS. 14A and 14B as long as electrical connection is possible. In addition, an IC chip including a controller, a CPU, a memory, or the like may be formed and mounted on the second substrate.

[0161]

This embodiment can be implemented in combination with any of the above embodiments.

[0162]

(Embodiment 8)

When a transistor having low off-state current and high reliability is used for a pixel portion of a liquid crystal display device according to an embodiment of the present invention, high visibility and high reliability can be obtained. In this embodiment, a structure of a liquid crystal display device according to an embodiment of the present invention will be described.

[0163]

FIG. 15 illustrates an example of a cross-sectional view of a pixel in a liquid crystal display device according to an embodiment of the present invention. A transistor 1401 illustrated in FIG. 15 includes a gate electrode 1402 formed over an insulating surface, a gate insulating film 1403 over the gate electrode 1402, an oxide semiconductor film 1404 which is over the gate insulating film 1403 and overlaps with the gate electrode 1402, and a conductive film 1405 and a conductive film 1406 which

are formed over the oxide semiconductor film 1404 and function as a source electrode and a drain electrode. Further, the transistor 1401 may include an insulating film 1407 formed over the oxide semiconductor film 1404 as a component. The insulating film 1407 is formed so as to cover the gate electrode 1402, the gate insulating film 1403, the oxide semiconductor film 1404, the conductive film 1405, and the conductive film 1406.

[0164]

An insulating film 1408 is formed over the insulating film 1407. An opening is provided in part of the insulating film 1407 and the insulating film 1408, and a pixel electrode 1410 is formed so as to be in contact with the conductive film 1406 in the opening.

[0165]

Further, a spacer 1417 for controlling a cell gap of a liquid crystal element is formed over the insulating film 1408. An insulating film is etched to have a desired shape, so that the spacer 1417 can be formed. The cell gap may also be controlled by dispersing a filler over the insulating film 1408.

[0166]

An alignment film 1411 is formed over the pixel electrode 1410. Further, a counter electrode 1413 is provided in a position that faces the pixel electrode 1410, and an alignment film 1414 is formed on the side of the counter electrode 1413 which is close to the pixel electrode 1410. The alignment film 1411 and the alignment film 1414 can be formed using an organic resin such as polyimide or polyvinyl alcohol. Alignment treatment such as rubbing is performed on their surfaces in order to align liquid crystal molecules in a certain direction. Rubbing can be performed by rolling a roller wrapped with cloth of nylon or the like while pressure is applied on the alignment film so that the surface of the alignment film is rubbed in a certain direction. Note that it is also possible to form the alignment films 1411 and 1414 that have alignment characteristics with the use of an inorganic material such as silicon oxide by an evaporation method, without alignment treatment.

[0167]

Furthermore, a liquid crystal 1415 is provided in a region which is surrounded by a sealant 1416 between the pixel electrode 1410 and the counter electrode 1413.

Injection of the liquid crystal 1415 may be performed by a dispenser method (dripping method) or a dipping method (pumping method). Note that a filler may be mixed in the sealant 1416.

[0168]

5 The liquid crystal element formed using the pixel electrode 1410, the counter electrode 1413, and the liquid crystal 1415 may overlap with a color filter through which light in a particular wavelength region can pass. The color filter may be formed over a substrate (counter substrate) 1420 provided with the counter electrode 1413. The color filter can be selectively formed by photolithography after application of an
10 organic resin such as an acrylic-based resin in which pigment is dispersed on the substrate 1420. Alternatively, the color filter can be selectively formed by etching after application of a polyimide-based resin in which pigment is dispersed on the substrate 1420. Further alternatively, the color filter can be selectively formed by a droplet discharge method such as ink jetting.

15 [0169]

 A light-blocking film which can block light may be formed between the pixels so that disclination due to disorder of alignment of the liquid crystal 1415 between pixels is prevented from being observed. The light-blocking film can be formed using an organic resin including black pigment such as carbon black or titanium lower oxide.
20 Alternatively, a film of chromium can be used as the light-blocking film.

[0170]

 The pixel electrode 1410 and the counter electrode 1413 can be formed using a transparent conductive material such as indium tin oxide including silicon oxide (ITSO), indium tin oxide (ITO), zinc oxide (ZnO), indium zinc oxide (IZO), or zinc oxide to
25 which gallium is added (GZO), for example. Note that in this embodiment, an example in which a transmissive liquid crystal element is manufactured using a light-transmitting conductive film for the pixel electrode 1410 and the counter electrode 1413 is described; however, an embodiment of the present invention is not limited to this structure. The liquid crystal display device according to an embodiment of the
30 present invention may be a semi-transmissive liquid crystal display device or a reflective liquid crystal display device.

[0171]

Although a liquid crystal display device of a twisted nematic (TN) mode is described in this embodiment, other liquid crystal display devices of a vertical alignment (VA) mode, an optically compensated birefringence (OCB) mode, an in-plane switching (IPS) mode, a multi-domain vertical alignment (MVA) mode, and the like may be employed.

[0172]

Alternatively, liquid crystals exhibiting a blue phase for which an alignment film is unnecessary may be used. A blue phase is one of liquid crystal phases, which is generated just before a cholesteric phase changes into an isotropic phase when temperature of cholesteric liquid crystals is increased. Since the blue phase is generated within only a narrow range of temperature, a liquid crystal composition in which a chiral agent is mixed at 5 wt% or more is used for the liquid crystal 1415 in order to improve the temperature range. The liquid crystal composition including liquid crystals exhibiting a blue phase and a chiral agent has a short response time of greater than or equal to 10 μ sec and less than or equal to 100 μ sec and is optically isotropic; therefore, alignment treatment is not necessary and viewing angle dependence is small.

[0173]

Next, the appearance of a panel of a liquid crystal display device according to an embodiment of the present invention will be described with reference to FIGS. 16A and 16B. FIG. 16A is a top view of a panel in which a second substrate 4001 and a counter substrate 4006 are attached to each other with a sealant 4005. FIG. 16B is a cross-sectional view along dashed line A-A' in FIG. 16A.

[0174]

The sealant 4005 is provided so as to surround a pixel portion 4002, a scan line driver circuit 4004, and a second signal line driver circuit 4020 which are provided over the second substrate 4001. Further, the counter substrate 4006 is provided over the pixel portion 4002, the scan line driver circuit 4004, and the second signal line driver circuit 4020. Thus, the pixel portion 4002, the scan line driver circuit 4004, and the second signal line driver circuit 4020 are sealed together with a liquid crystal 4007 by the second substrate 4001, the sealant 4005, and the counter substrate 4006.

[0175]

A first substrate 4021 provided with a first signal line driver circuit 4003 is mounted in a region which is over the second substrate 4001 and different from the region surrounded by the sealant 4005. FIG. 16B illustrates a transistor 4009 which corresponds to a first semiconductor element included in the first signal line driver circuit 4003, as an example.

[0176]

A plurality of transistors is included in the pixel portion 4002, the scan line driver circuit 4004, and the second signal line driver circuit 4020 which are formed over the second substrate 4001. FIG. 16B illustrates a transistor 4010 included in the pixel portion 4002 and a transistor 4022 included in the second signal line driver circuit 4020, as examples. The transistor 4010 and the transistor 4022 correspond to second semiconductor elements including an oxide semiconductor.

[0177]

A pixel electrode 4030 included in a liquid crystal element 4011 is electrically connected to the transistor 4010. A counter electrode 4031 of the liquid crystal element 4011 is formed over the counter substrate 4006. A portion where the pixel electrode 4030, the counter electrode 4031, and the liquid crystal 4007 overlap with one another corresponds to the liquid crystal element 4011.

[0178]

A spacer 4035 is provided to control a distance (cell gap) between the pixel electrode 4030 and the counter electrode 4031. Note that FIG. 16B illustrates the case where the spacer 4035 is formed by patterning an insulating film, as an example; however, a spherical spacer may be used.

[0179]

A variety of signals and potentials which are applied to the first signal line driver circuit 4003, the second signal line driver circuit 4020, the scan line driver circuit 4004, and the pixel portion 4002 are supplied from a connection terminal 4016 through lead wirings 4014 and 4015. The connection terminal 4016 is electrically connected to a terminal of an FPC 4018 through an anisotropic conductive film 4019.

[0180]

Note that for the second substrate 4001, the counter substrate 4006, and the

first substrate 4021, glass, ceramics, or plastics can be used. Plastics include, in its category, a fiberglass-reinforced plastic (FRP) plate, a polyvinyl fluoride (PVF) film, a polyester film, an acrylic resin film, and the like. In addition, a sheet having a structure in which an aluminum foil is sandwiched between PVF films can be used.

5 [0181]

Note that a substrate placed in a direction in which light is extracted through the liquid crystal element 4011 is formed using a light-transmitting material such as a glass plate, plastic, a polyester film, or an acrylic film.

[0182]

10 FIG. 17 is an example of a perspective view illustrating a structure of a liquid crystal display device according to an embodiment of the present invention. The liquid crystal display device illustrated in FIG. 17 includes a panel 1601 in which a liquid crystal element is formed between a second substrate and a counter substrate, a first diffusion plate 1602, a prism sheet 1603, a second diffusion plate 1604, a light
15 guide plate 1605, a reflection plate 1606, a light source 1607, a circuit board 1608, and a first substrate 1611.

[0183]

The panel 1601, the first diffusion plate 1602, the prism sheet 1603, the second diffusion plate 1604, the light guide plate 1605, and the reflection plate 1606 are
20 sequentially stacked. The light source 1607 is provided at an end portion of the light guide plate 1605. Light from the light source 1607 is diffused inside the light guide plate 1605 and is uniformly delivered to the panel 1601 with the help of the first diffusion plate 1602, the prism sheet 1603, and the second diffusion plate 1604.

[0184]

25 Although the first diffusion plate 1602 and the second diffusion plate 1604 are used in this embodiment, the number of diffusion plates is not limited to this. The number of diffusion plates may be one, or may be three or more. The diffusion plate is provided between the light guide plate 1605 and the panel 1601. Therefore, the diffusion plate may be provided only on the side closer to the panel 1601 than the prism
30 sheet 1603, or may be provided only on the side closer to the light guide plate 1605 than the prism sheet 1603.

[0185]

Further, the cross section of the prism sheet 1603 is not limited to a sawtooth shape illustrated in FIG. 17. The prism sheet 1603 may have a shape with which light from the light guide plate 1605 can be concentrated on the panel 1601 side.

[0186]

5 The circuit board 1608 is provided with a circuit which generates various signals input to the panel 1601, a circuit which processes the signals, or the like. In FIG. 17, the circuit board 1608 and the panel 1601 are connected to each other through a COF tape 1609. Further, the first substrate 1611 is connected to the COF tape 1609 by a chip on film (COF) method.

10 [0187]

FIG. 17 illustrates an example in which the circuit board 1608 is provided with a control circuit which controls driving of the light source 1607 and the control circuit and the light source 1607 are connected to each other through an FPC 1610. Note that the above control circuit may be formed over the panel 1601; in this case, the panel 1601 and the light source 1607 are connected to each other through an FPC or the like.

15 [0188]

Although FIG. 17 illustrates an edge-light type light source and the light source 1607 is provided at an end of the panel 1601 as an example, the liquid crystal display device of an embodiment of the present invention may be a direct-below type in which the light source 1607 is provided directly below the panel 1601.

20 [0189]

This embodiment can be implemented in combination with any of the above embodiments as appropriate.

[0190]

25 (Embodiment 9)

In this embodiment, a specific structure of a pixel portion will be described by taking a light-emitting device which is one of semiconductor display devices of the present invention as an example.

[0191]

30 FIG. 19 is a circuit diagram of a pixel portion in a light-emitting device in which a light-emitting element typified by an organic light-emitting diode (OLED) is provided in each pixel. The pixel portion in FIG. 19 includes a plurality of signal lines

S1 to Sx, a plurality of power supply lines V1 to Vx, and a plurality of scan lines G1 to Gy. Each of the plurality of pixels 310 has at least one of the signal lines S1 to Sx, one of the power supply lines V1 to Vx, and one of the scan lines G1 to Gy.

[0192]

5 Each of the pixels 310 includes a light-emitting element 313, a switching transistor 311 that controls input of a video signal to the pixel 310, and a driving transistor 312 that controls the amount of current supplied to the light-emitting element 313. A gate electrode of the switching transistor 311 is connected to one of the scan lines G1 to Gy. One of a source electrode and a drain electrode of the switching
10 transistor 311 is connected to one of the signal lines S1 to Sx. The other of the source electrode and the drain electrode of the switching transistor 311 is connected to a gate electrode of the driving transistor 312. One of a source electrode and a drain electrode of the driving transistor 312 is connected to one of the power supply lines V1 to Vx. The other of the source electrode and the drain electrode of the driving transistor 312 is
15 connected to a pixel electrode of the light-emitting element 313. Further, the pixel 310 includes a storage capacitor 314. One electrode of the storage capacitor 314 is connected to one of the power supply lines V1 to Vx. The other electrode of the storage capacitor 314 is connected to the gate electrode of the driving transistor 312.

[0193]

20 The light-emitting element 313 includes an anode, a cathode, and an electroluminescent layer provided between the anode and the cathode. One of the anode and the cathode is used as a pixel electrode, and the other of the anode and the cathode is used as a counter electrode. When the anode is connected to the source electrode or the drain electrode of the driving transistor 312, the anode is the pixel
25 electrode and the cathode is the counter electrode. On the other hand, when the cathode is connected to the source electrode or the drain electrode of the driving transistor 312, the cathode is the pixel electrode and the anode is the counter electrode.

[0194]

30 Voltage is applied to the counter electrode of the light-emitting element 313 and the power supply line from the power source. The value of the voltage difference between the counter electrode and the power supply line is kept such that forward bias voltage is applied to the light-emitting element when the driving transistor 312 is turned

on.

[0195]

When the switching transistor 311 is turned on by a pulse of a selection signal input to the scan line, the voltage of the video signal input to a signal line is applied to the gate electrode of the driving transistor 312. The gate voltage of the driving transistor 312 (voltage difference between the gate electrode and the source electrode) is determined in accordance with the voltage of the input video signal. Then, drain current of the driving transistor 312 which flows in accordance with the gate voltage is supplied to the light-emitting element 313, so that the light-emitting element 313 emits light.

[0196]

In the case where an image is displayed in a specific area, a selection signal having a pulse is sequentially input only to scan lines included in pixels in the area. Then, a video signal having image data is input only to signal lines included in the pixels in the area, so that the image can be displayed in the specific area.

[0197]

The structure of the pixel 310 illustrated in FIG. 19 is just an example of the pixel included in the semiconductor display device of an embodiment of the present invention, and an embodiment of the present invention is not limited to the configuration of the pixel illustrated in FIG. 19.

[0198]

Note that in the light-emitting device, grayscale display may be performed by a time ratio grayscale method in which time during which a pixel displays white for one frame period is controlled, or by using a video signal having analog image data. Since the response time of a light-emitting element is shorter than that of a liquid crystal element or the like, the light-emitting element is more suitable for a time ratio grayscale method than the liquid crystal element. Specifically, in the case of displaying by a time ratio grayscale method, one frame period is divided into a plurality of subframe periods. Then, in accordance with video signals, the light-emitting element in the pixel is brought into a light-emitting state or a non-light-emitting state in each subframe period. With the above structure, the total length of a period during which the pixel actually in a light-emitting state in one frame period can be controlled by the video

signals, so that grayscale display can be performed.

[0199]

This embodiment can be implemented in combination with any of the above embodiments as appropriate.

5 [0200]

(Embodiment 10)

In this embodiment, a specific structure of a pixel portion will be described by taking an electrophoretic display device called electronic paper or digital paper, which is one of semiconductor display devices of the present invention, as an example.

10 [0201]

A display element which can control grayscale by voltage application and has a memory property is used for an electrophoretic display device. Specifically, as the display element used for the electrophoretic display device, a non-aqueous electrophoretic display element; a display element that employs a polymer dispersed liquid crystal (PDLC) method, in which liquid crystal droplets are dispersed in a high molecular material between two electrodes; a display element that includes a chiral nematic liquid crystal or a cholesteric liquid crystal between two electrodes; a display element that includes charged fine particles between two electrodes and employs a particle-moving method in which the charged fine particles are moved through fine particles by using an electric field; or the like can be used. Further, examples of a non-aqueous electrophoretic display element include a display element in which dispersion liquid where charged fine particles are dispersed is sandwiched between two electrodes; a display element in which dispersion liquid where charged fine particles are dispersed is provided over two electrodes between which an insulating film is sandwiched; a display element in which twisting balls having hemispheres that are colored in different colors and charged differently are dispersed in a solvent between two electrodes; and a display element which includes microcapsules where a plurality of charged fine particles are dispersed in a solution, between two electrodes.

[0202]

30 FIG. 20 illustrates a circuit diagram of a pixel portion 321 of an electrophoretic display device, as an example. The pixel portion 321 includes a plurality of pixels 320. The pixel portion 321 includes a plurality of signal lines S1 to Sx and a plurality of scan

lines G1 to Gy. Each of the plurality of pixels 320 has at least one of the signal lines S1 to Sx and one of the scan lines G1 to Gy.

[0203]

Each of the pixels 320 includes a transistor 325, a display element 326, and a storage capacitor 327. A gate electrode of the transistor 325 is connected to one of the scan lines G1 to Gy. One of a source electrode and a drain electrode of the transistor 325 is connected to one of the signal lines S1 to Sx, and the other of the source electrode and the drain electrode of the transistor 325 is connected to a pixel electrode of the display element 326.

[0204]

Note that in FIG. 20, the storage capacitor 327 is connected in parallel to the display element 326 such that voltage applied between the pixel electrode and a counter electrode of the display element 326 is held; in the case where the memory property of the display element 326 is high enough to maintain display, the storage capacitor 327 is not necessarily provided.

[0205]

Note that FIG. 20 illustrates a configuration of an active-matrix pixel portion in which one transistor functioning as a switching element is provided in each pixel; however, the electrophoretic display device according to an embodiment of the present invention is not limited to this configuration. A plurality of transistors may be provided in each pixel. Further, other than transistors, an element such as a capacitor, a resistor, or a coil may be connected.

[0206]

As described above, the structure of the display element 326 depends on the kind of the electrophoretic display device. For example, in the case of an electrophoretic display device including microcapsules, the display element 326 includes a pixel electrode, a counter electrode, and microcapsules to which voltage is applied by the pixel electrode and the counter electrode. One of the source electrode and the drain electrode of the transistor 325 is connected to the pixel electrode.

[0207]

In the microcapsules, positively charged white pigment such as titanium oxide and negatively charged black pigment such as carbon black are sealed together with a

dispersion medium such as oil. Voltage is applied between the pixel electrode and the counter electrode in accordance with the voltage of a video signal applied to the pixel electrode, and the black pigment and the white pigment are drawn to a positive electrode side and a negative electrode side, respectively. Thus, binary grayscale display can be performed.

[0208]

In the case of an electrophoretic display device, display of intermediate grayscale can be performed with the use of a digital image processing technique such as an error diffusion method or a dither method.

[0209]

Note that voltage needed to change the grayscale levels of the display element used in an electrophoretic display device tends to be higher than that needed for a liquid crystal element used in a liquid crystal display device or a light-emitting element such as an organic light-emitting element used in a light-emitting device. Therefore, the potential difference between the source electrode and the drain electrode of the transistor 325 in a pixel which is used as a switching element is large when a video signal is written; as a result, off-state current is increased and disturbance of display is likely to occur owing to fluctuation of the potential of the pixel electrode. Moreover, since the potential difference between the source electrode and the drain electrode is increased, the transistor 325 is easily deteriorated. According to an embodiment of the present invention, however, an oxide semiconductor is used for a channel formation region of the transistor 325, whereby the off-state current thereof can be significantly reduced and the withstand voltage thereof can be increased. Accordingly, display can be prevented from being disturbed by the off-state current. According to an embodiment of the present invention, variation in the threshold voltage of the transistor 325 due to degradation over time can be reduced, so that reliability of the electrophoretic display device can be increased.

[0210]

This embodiment can be implemented in combination with any of the above embodiments.

[Example]

[0211]

With the use of a semiconductor display device according to an embodiment of the present invention, an electronic device having high reliability or an electronic device capable of displaying a high-quality image can be provided.

[0212]

5 The semiconductor display device according to an embodiment of the present invention can be used for display devices, laptop computers, or image reproducing devices provided with recording media (typically, devices which reproduce the content of recording media such as digital versatile discs (DVDs) and have displays for displaying the reproduced images). Further, the electronic devices for which the
10 semiconductor display device according to an embodiment of the present invention can be used are as follows: mobile phones, portable game machines, portable information terminals, electronic book readers, video cameras, digital still cameras, goggle-type displays (head mounted displays), navigation systems, audio reproducing devices (such as car audio systems and digital audio players), copiers, facsimiles, printers,
15 multifunction printers, automated teller machines (ATMs), vending machines, and the like. Specific examples of these electronic devices are illustrated in FIGS. 18A to 18D.

[0213]

FIG. 18A illustrates a portable game machine including a housing 7031, a
20 housing 7032, a display portion 7033, a display portion 7034, a microphone 7035, a speaker 7036, an operation key 7037, a stylus 7038, and the like. The semiconductor display device according to an embodiment of the present invention can be used for the display portion 7033 or the display portion 7034. By using the semiconductor display device according to an embodiment of the present invention for the display portion 7033
25 or the display portion 7034, the portable game machine can have high reliability and display a high-quality image. Although the portable game machine illustrated in FIG. 18A has the two display portions 7033 and 7034, the number of display portions included in the portable game machine is not limited to this.

[0214]

30 FIG. 18B illustrates a mobile phone including a housing 7041, a display portion 7042, an audio-input portion 7043, an audio-output portion 7044, an operation key 7045, a light-receiving portion 7046, and the like. Light received in the light-receiving

portion 7046 is converted to electrical signals, whereby external images can be loaded. The semiconductor display device according to an embodiment of the present invention can be used for the display portion 7042. By using the semiconductor display device according to an embodiment of the present invention for the display portion 7042, the mobile phone can have high reliability and display a high-quality image.

[0215]

FIG. 18C illustrates a portable information terminal including a housing 7051, a display portion 7052, an operation key 7053, and the like. In the portable information terminal illustrated in FIG. 18C, a modem may be incorporated in the housing 7051. The semiconductor display device according to an embodiment of the present invention can be used for the display portion 7052. By using the semiconductor display device according to an embodiment of the present invention for the display portion 7052, the portable information terminal can have high reliability and display a high-quality image.

[0216]

FIG. 18D illustrates a display device including a housing 7011, a display portion 7012, a support 7013, and the like. The semiconductor display device according to an embodiment of the present invention can be used for the display portion 7012. By using the semiconductor display device according to an embodiment of the present invention for the display portion 7012, the display device can have high reliability and display a high-quality image. Note that a display device includes all display devices for displaying information, such as display devices for personal computers, for receiving television broadcast, and for displaying advertisement, in its category.

[0217]

This example can be implemented in combination with any of the above embodiments as appropriate.

This application is based on Japanese Patent Application serial no. 2010-080661 filed with Japan Patent Office on March 31, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor display device comprising:

a pixel portion; and

5 a signal line driver circuit comprising a first circuit, a second circuit, and a third circuit,

wherein the first circuit is configured to sample serial video signals and to convert the serial video signals to parallel video signals,

wherein the second circuit is configured to control timing of the sampled serial video signals by the first circuit,

10 wherein the third circuit is configured to perform signal processing on the parallel video signals,

wherein the second circuit comprises a first semiconductor element formed over a first substrate, the first semiconductor element including a first semiconductor layer,

15 wherein the third circuit comprises a second semiconductor element formed over a second substrate, the second semiconductor element including a second semiconductor layer,

wherein the pixel portion comprises a third semiconductor element formed over the second substrate, the third semiconductor element including a third semiconductor layer,

20 wherein the first semiconductor layer comprises silicon or germanium, and

wherein each the second semiconductor layer and the third semiconductor layer has a wider bandgap than the first semiconductor layer.

25 2. The semiconductor display device according to claim 1,

wherein the first circuit includes a fourth semiconductor element formed over the first substrate, and

wherein the fourth semiconductor element comprises silicon or germanium.

30 3. The semiconductor display device according to claim 1,

wherein the first circuit includes a fifth semiconductor element formed over the second substrate, and

wherein the fifth semiconductor element comprises the semiconductor.

4. The semiconductor display device according to claim 1,

5 wherein a withstand voltage of the second semiconductor element is more than 10V higher than that of the first semiconductor element.

5. The semiconductor display device according to claim 1,

10 wherein a withstand voltage of the second semiconductor element is higher than 5 V and approximately lower than or equal to 20 V.

6. The semiconductor display device according to claim 1,

wherein each the first to third semiconductor element is a transistor.

7. The semiconductor display device according to claim 1,

15 wherein the semiconductor is an oxide semiconductor.

8. The semiconductor display device according to claim 7,

wherein the oxide semiconductor is an In-Ga-Zn-O-based oxide semiconductor.

9. A semiconductor display device comprising:

20 a pixel portion;

a scan line driver circuit; and

a signal line driver circuit comprising a first circuit, a second circuit, and a third circuit,

25 wherein the first circuit is configured to sample serial video signals and to convert the serial video signals to parallel video signals,

wherein the second circuit is configured to control timing of the sampled serial video signals by the first circuit,

30 wherein the third circuit is configured to perform signal processing on the parallel video signals,

wherein the second circuit comprises a first semiconductor element formed over a first substrate, the first semiconductor element including a first semiconductor

layer,

wherein the third circuit comprises a second semiconductor element formed over a second substrate, the second semiconductor element including a second semiconductor layer,

5 wherein the pixel portion comprises a third semiconductor element formed over the second substrate, the third semiconductor element including a third semiconductor layer,

wherein the first semiconductor layer comprises silicon or germanium, and

10 wherein each the second semiconductor layer and the third semiconductor layer has a wider bandgap than the first semiconductor layer.

10. The semiconductor display device according to claim 9,

wherein the first circuit includes a fourth semiconductor element formed over the first substrate, and

15 wherein the fourth semiconductor element comprises silicon or germanium.

11. The semiconductor display device according to claim 9,

wherein the first circuit includes a fifth semiconductor element formed over the second substrate, and

20 wherein the fifth semiconductor element comprises the semiconductor.

12. The semiconductor display device according to claim 9,

wherein a withstand voltage of the second semiconductor element is more than 10V higher than that of the first semiconductor element.

25

13. The semiconductor display device according to claim 9,

wherein a withstand voltage of the second semiconductor element is higher than 5 V and approximately lower than or equal to 20 V.

30

14. The semiconductor display device according to claim 9,

wherein each the first to third semiconductor element is a transistor.

15. The semiconductor display device according to claim 9,
wherein the semiconductor is an oxide semiconductor.

5 16. The semiconductor display device according to claim 15,
wherein the oxide semiconductor is an In-Ga-Zn-O-based oxide semiconductor.

17. A semiconductor display device comprising:
a pixel portion;
a shift register;
10 a memory circuit;
a D/A converter circuit; and
a level shifter,
wherein the shift register comprises a first semiconductor element formed over
a first substrate, the first semiconductor element including a first semiconductor layer,
15 wherein the level shifter comprises a second semiconductor element formed
over a second substrate, the second semiconductor element including a second
semiconductor layer,
wherein the pixel portion comprises a third semiconductor element formed
over the second substrate, the third semiconductor element including a third
20 semiconductor layer,
wherein the first semiconductor layer comprises silicon or germanium, and
wherein each the second semiconductor layer and the third semiconductor layer
has a wider bandgap than the first semiconductor layer.

25 18. The semiconductor display device according to claim 17,
wherein the D/A converter circuit includes a fourth semiconductor element
formed over the first substrate, and
wherein the fourth semiconductor element comprises silicon or germanium.

30 19. The semiconductor display device according to claim 17,
wherein the D/A converter circuit includes a fifth semiconductor element
formed over the second substrate, and

wherein the fifth semiconductor element comprises the semiconductor.

20. The semiconductor display device according to claim 17,
wherein a withstand voltage of the second semiconductor element is more than
5 10V higher than that of the first semiconductor element.

21. The semiconductor display device according to claim 17,
wherein a withstand voltage of the second semiconductor element is higher
than 5 V and approximately lower than or equal to 20 V.

10

22. The semiconductor display device according to claim 17,
wherein each the first to third semiconductor element is a transistor.

15

23. The semiconductor display device according to claim 17,
wherein the semiconductor is an oxide semiconductor.

24. The semiconductor display device according to claim 23,
wherein the oxide semiconductor is an In-Ga-Zn-O-based oxide semiconductor.

20

25. The semiconductor display device according to claim 17,
wherein the memory circuit is configured to sample serial video signals and to
convert the serial video signals to parallel video signals.

FIG. 1A

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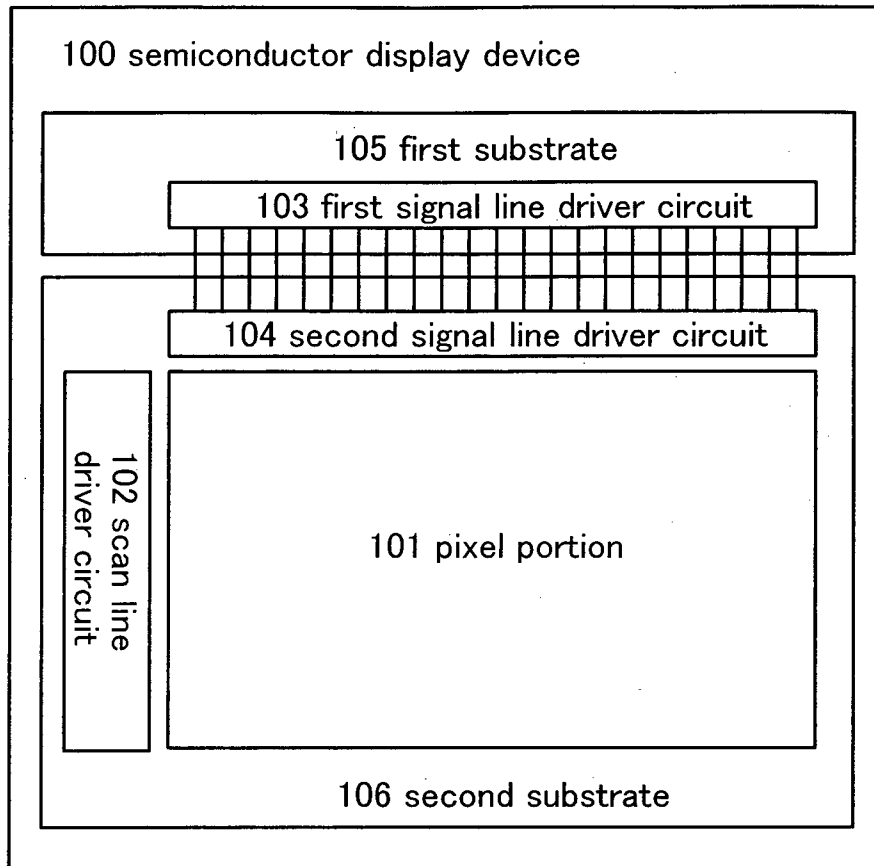


FIG. 1B

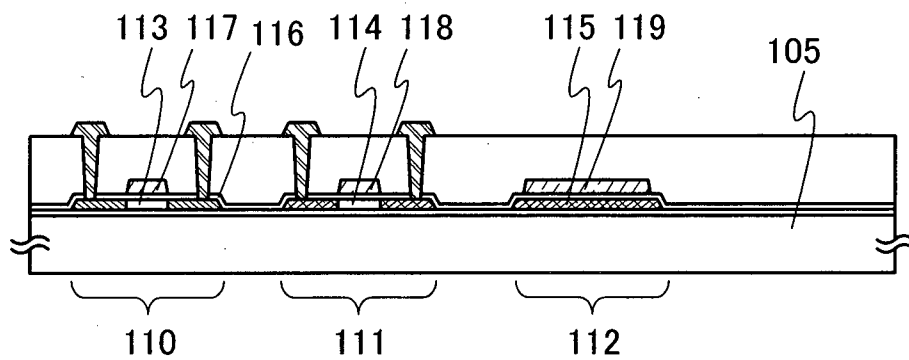


FIG. 1C

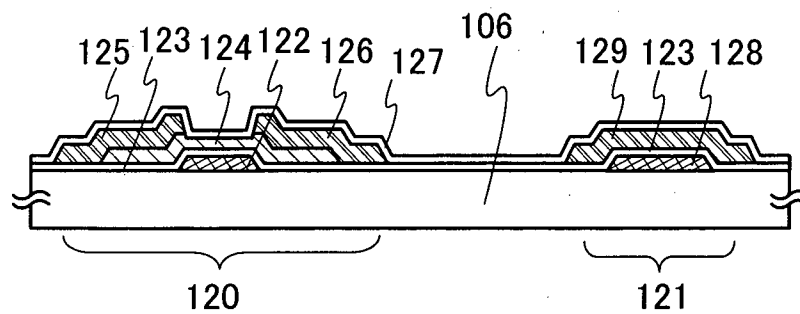


FIG. 2

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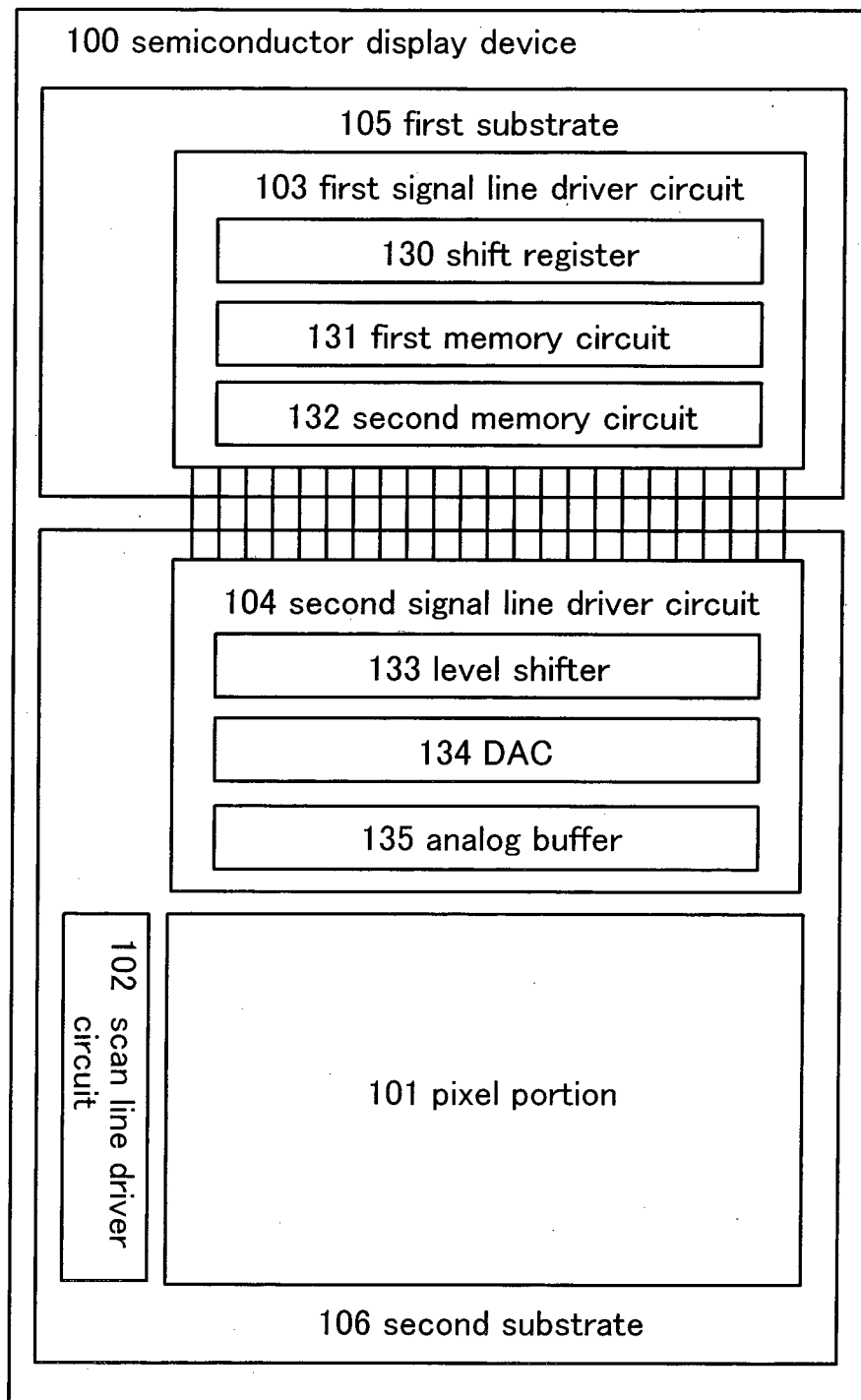


FIG. 3

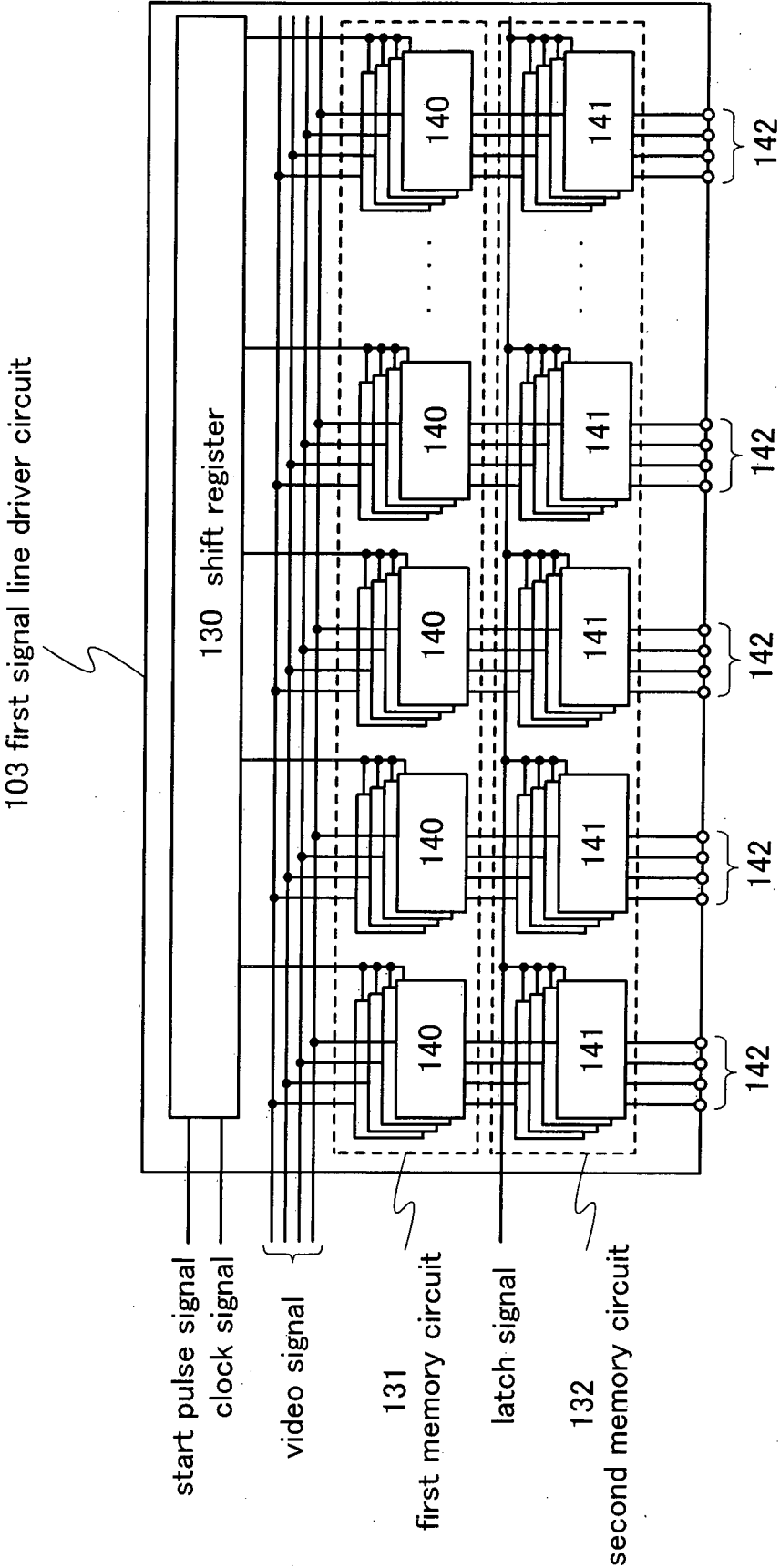


FIG. 4

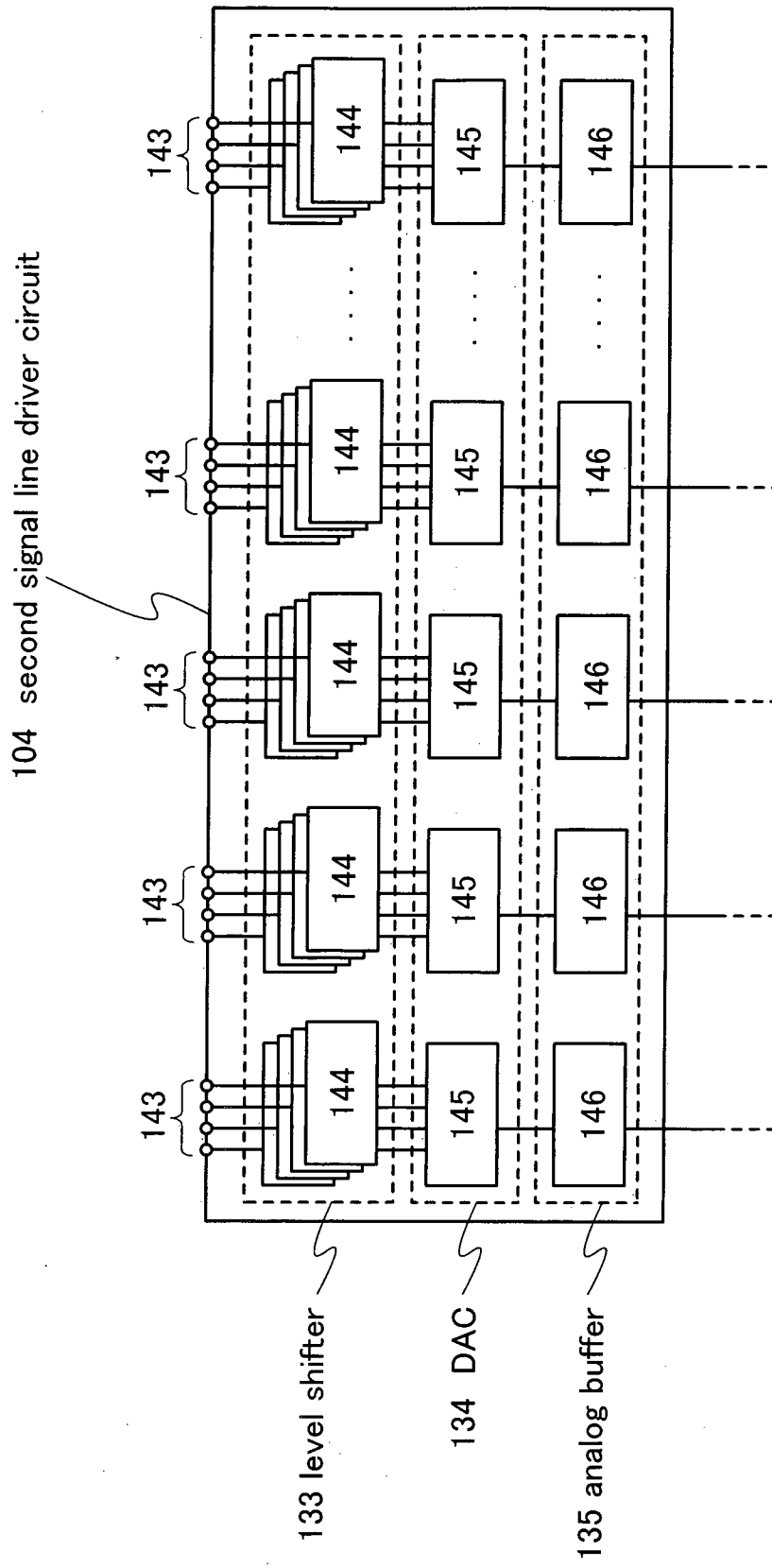
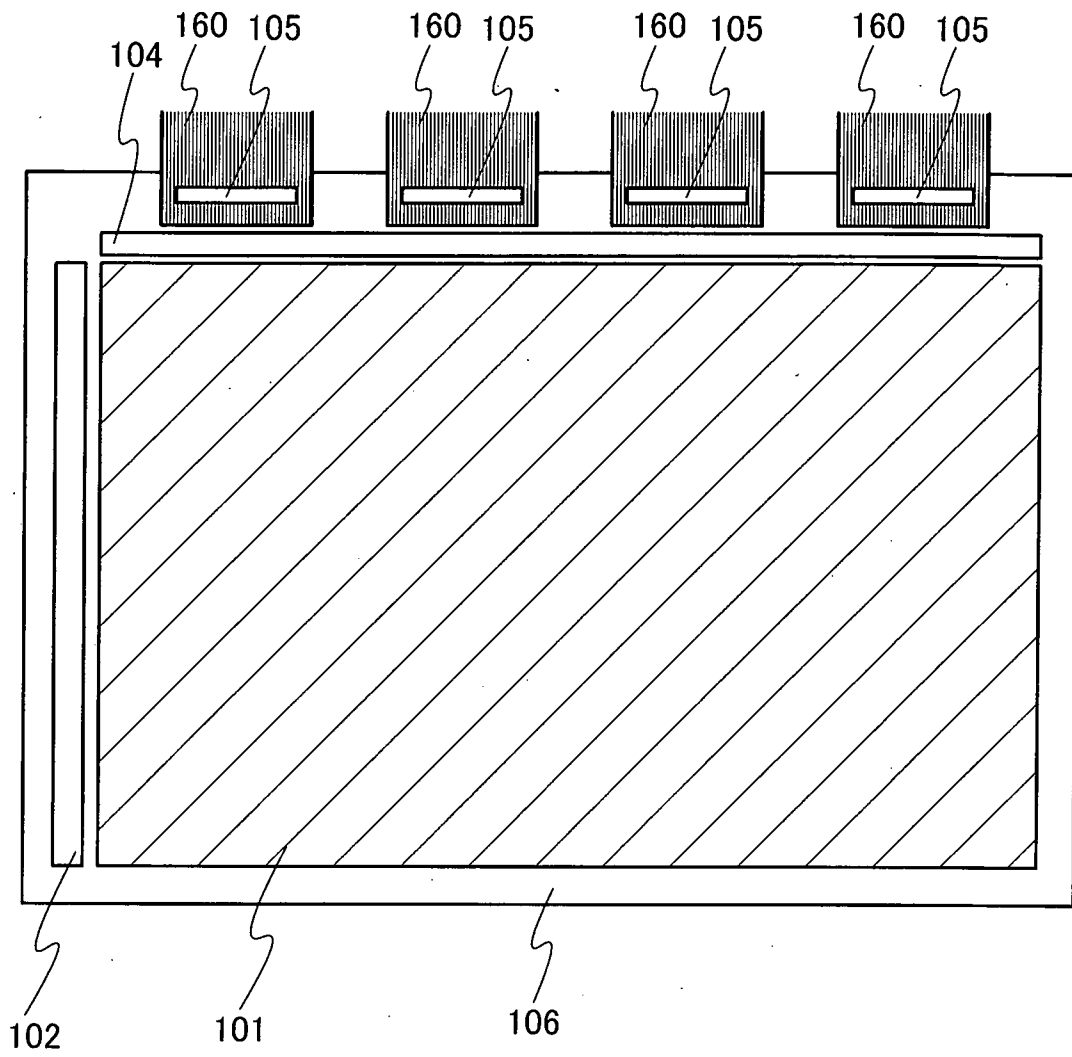


FIG. 5

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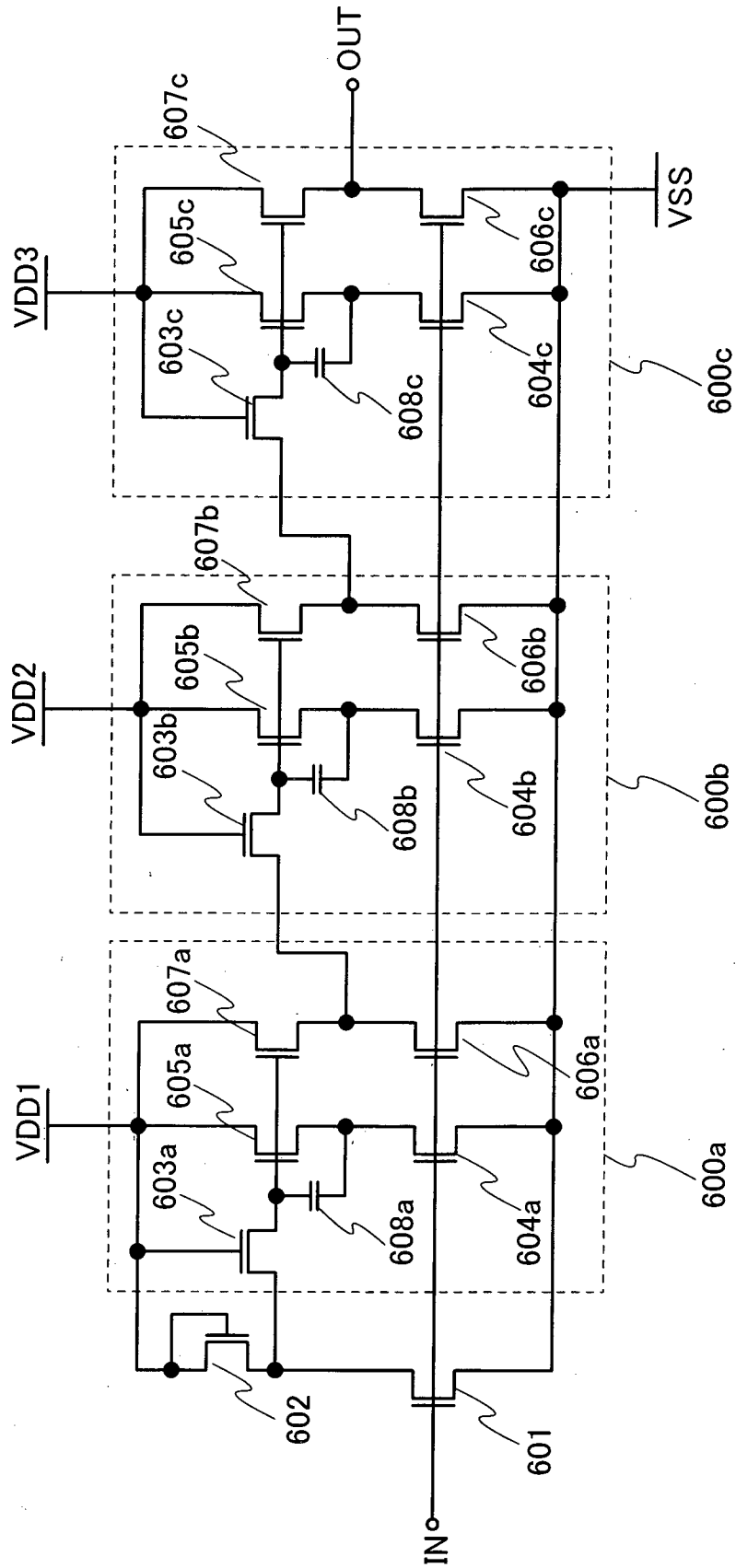


FIG. 6

FIG. 7

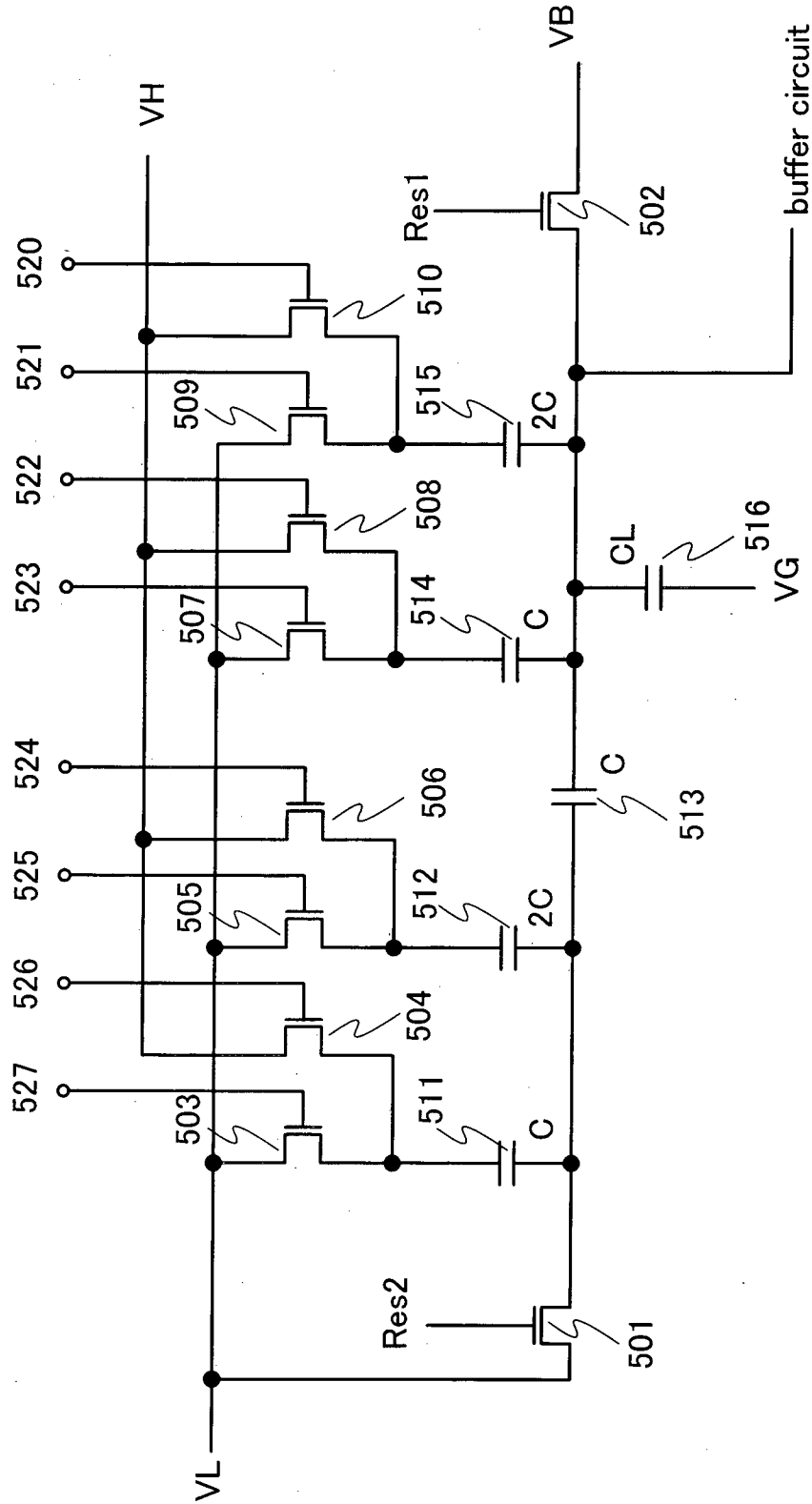
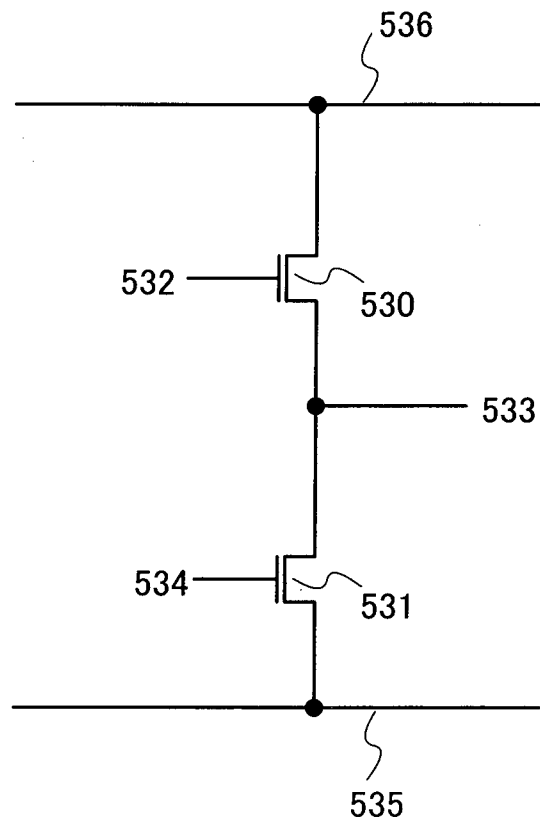


FIG. 8

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FIG. 9

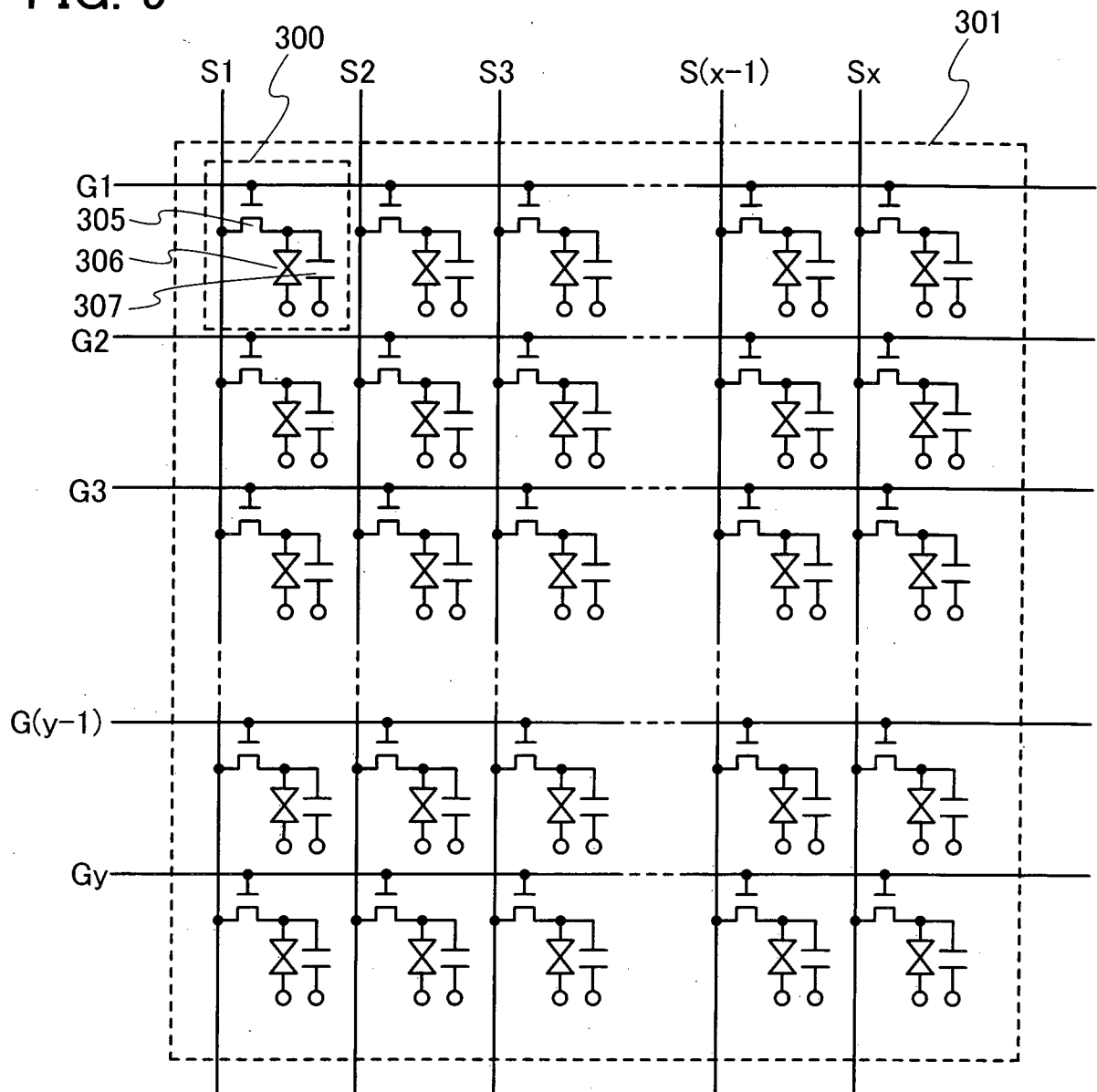
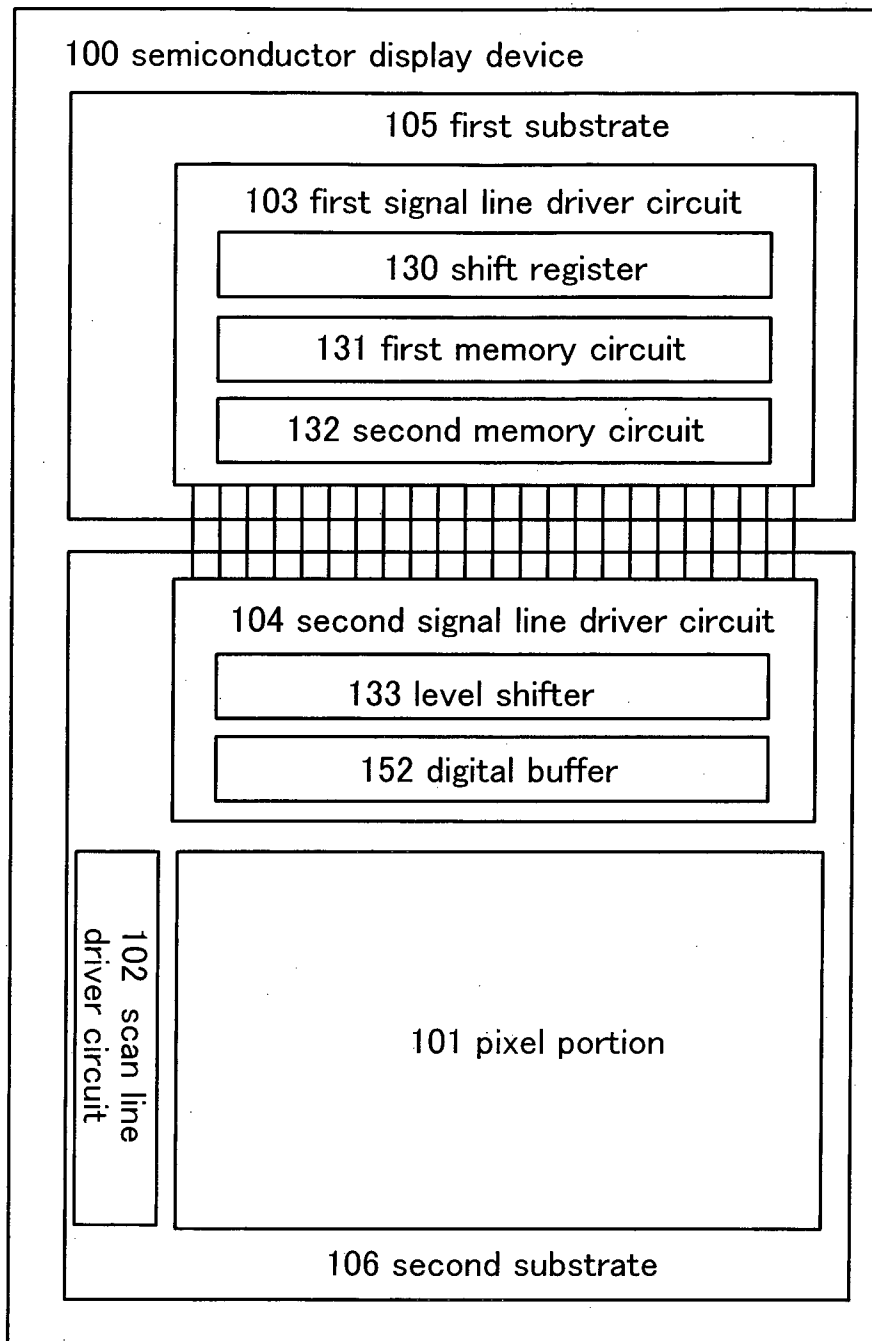
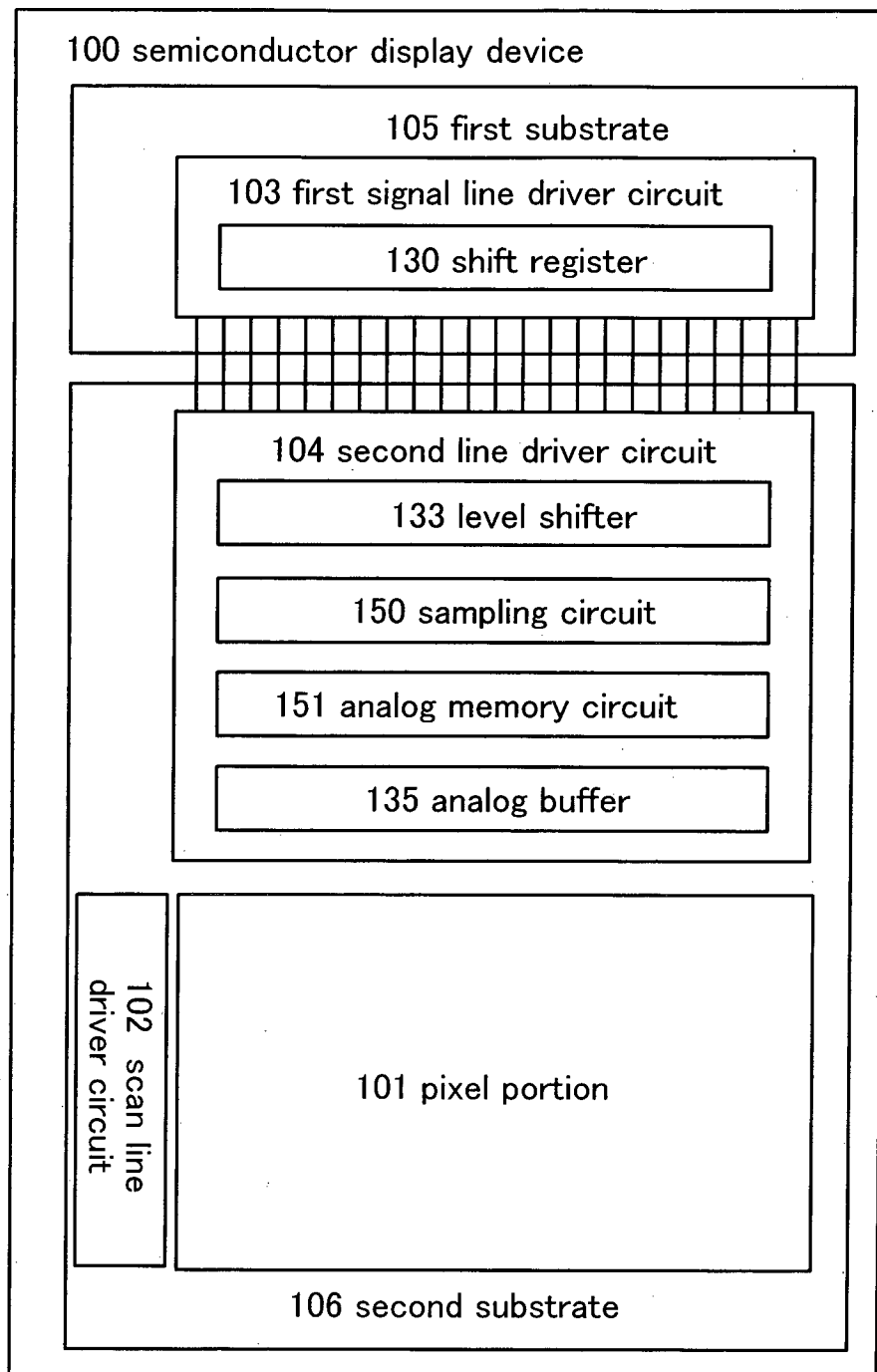


FIG. 10



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FIG. 11



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FIG. 12A

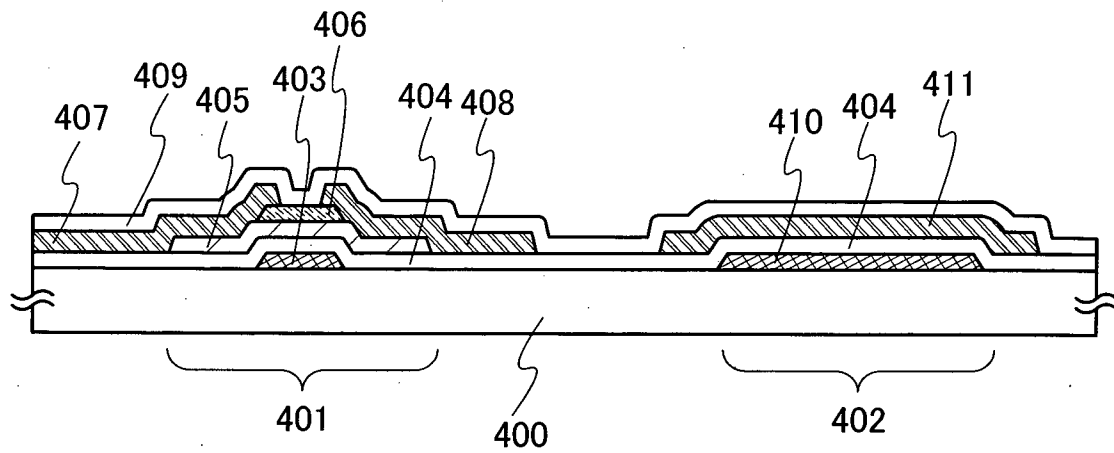


FIG. 12B

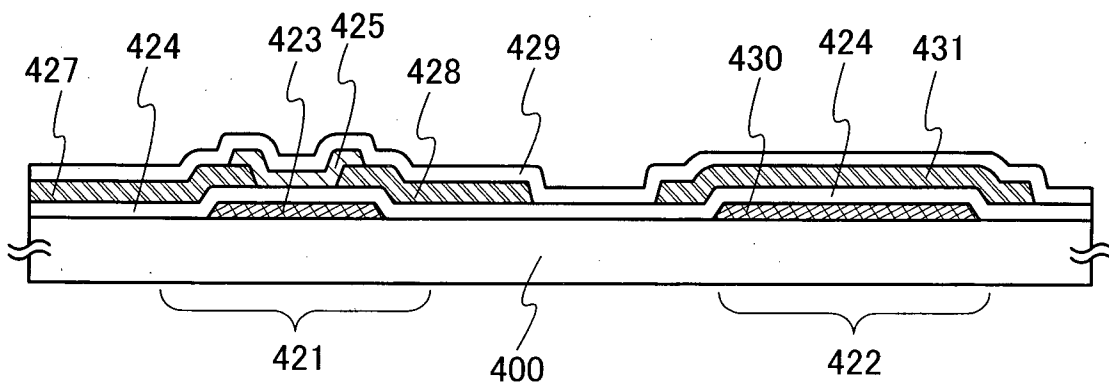


FIG. 12C

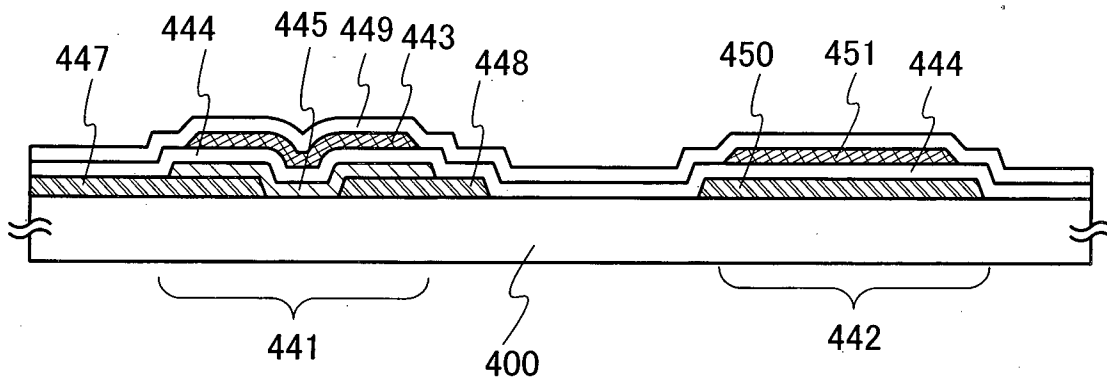


FIG. 13A

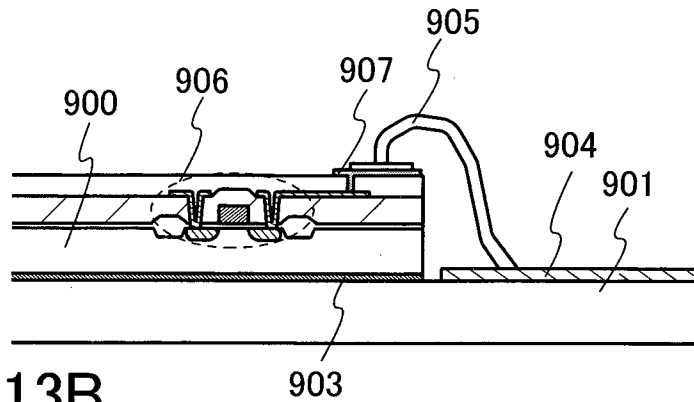


FIG. 13B

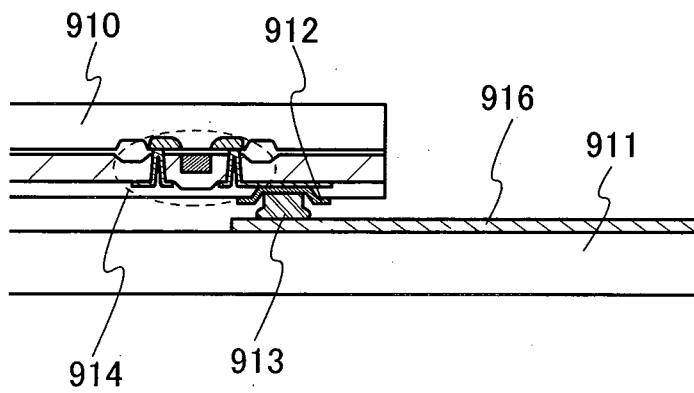
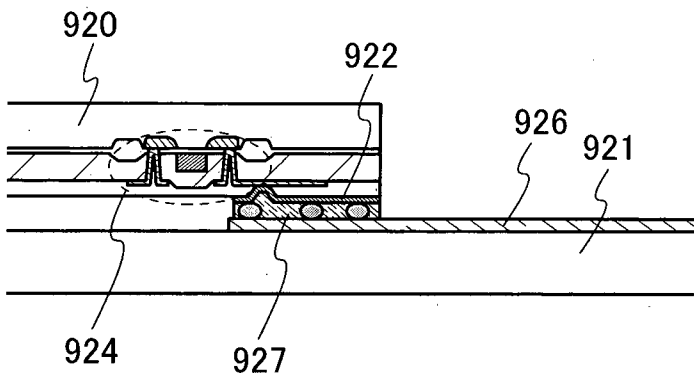


FIG. 13C



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FIG. 14A

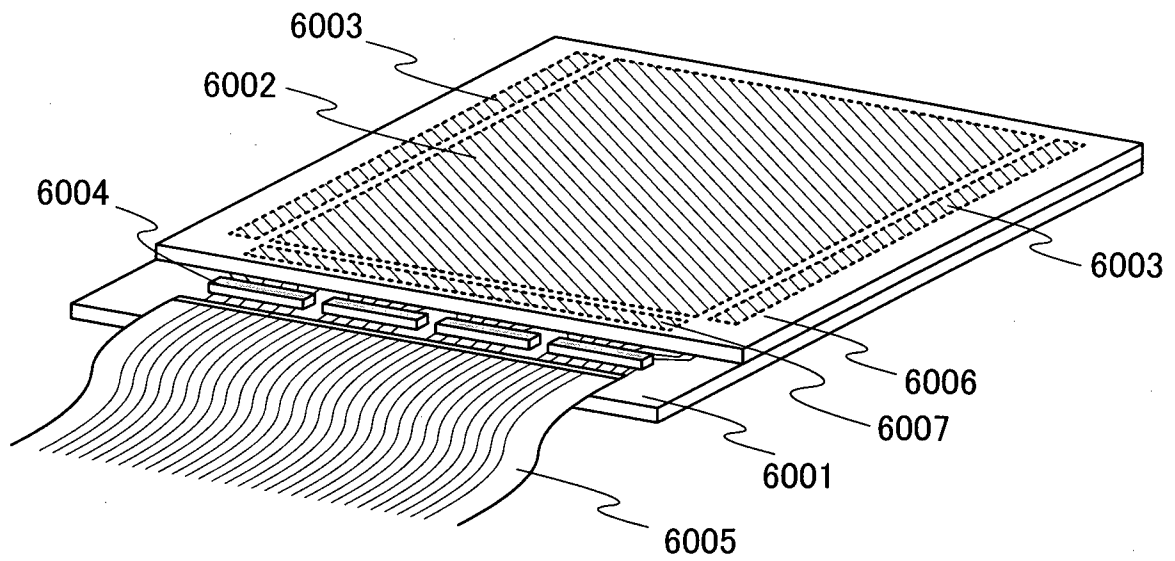


FIG. 14B

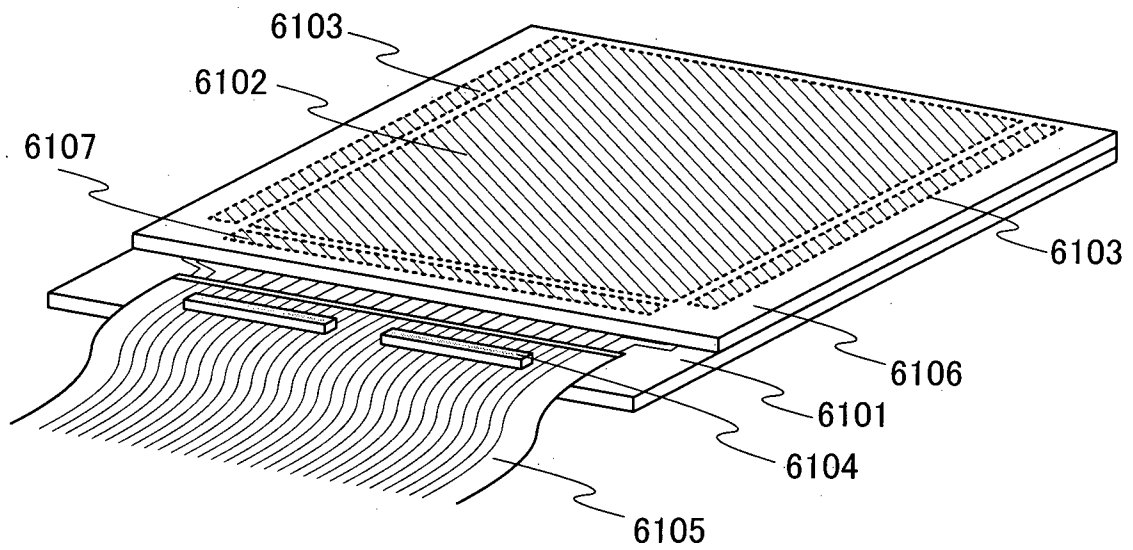


FIG. 15

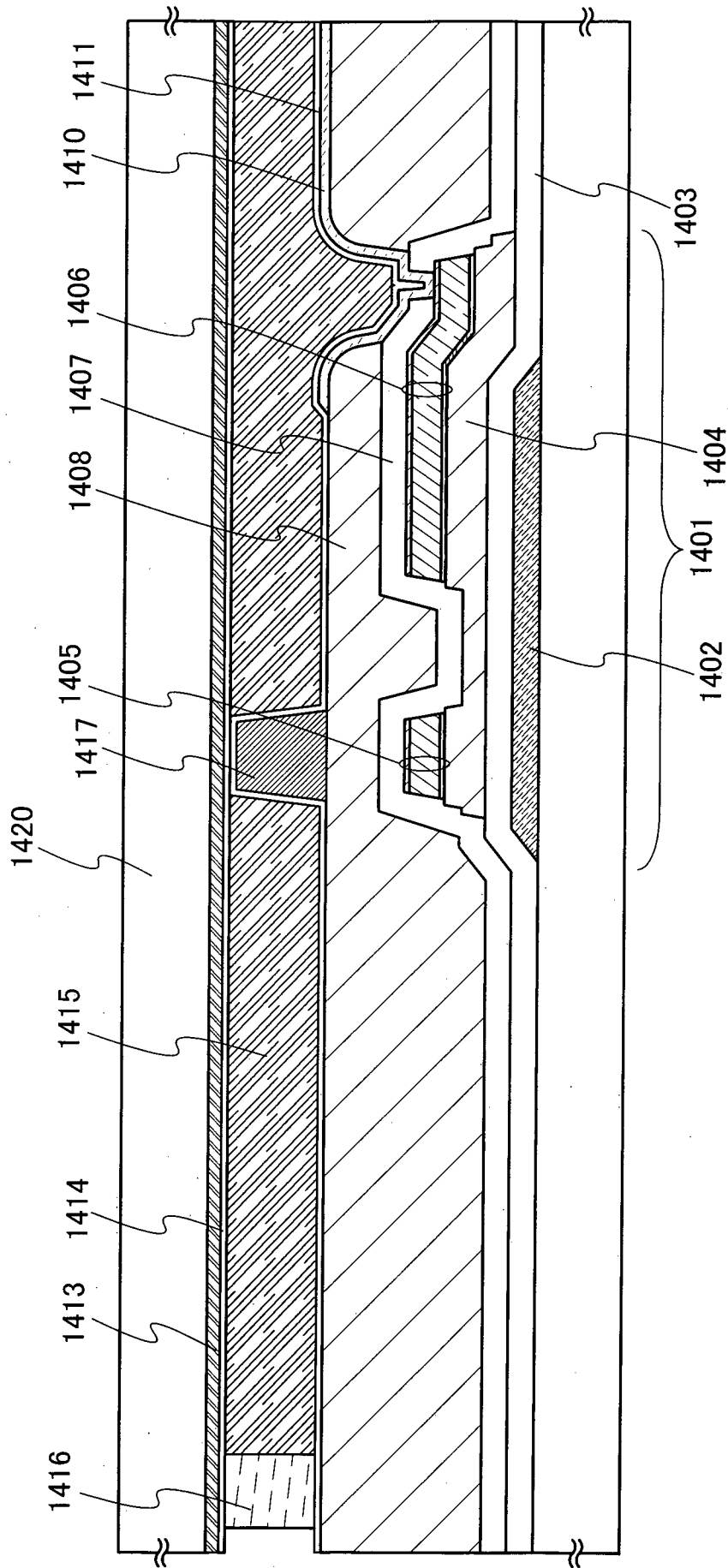


FIG. 16A

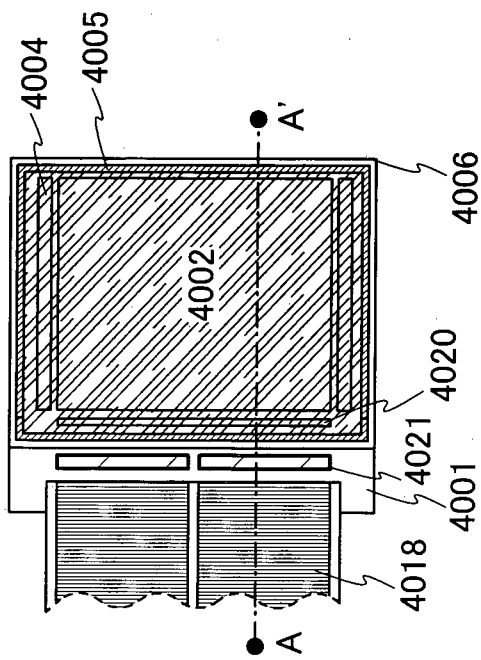
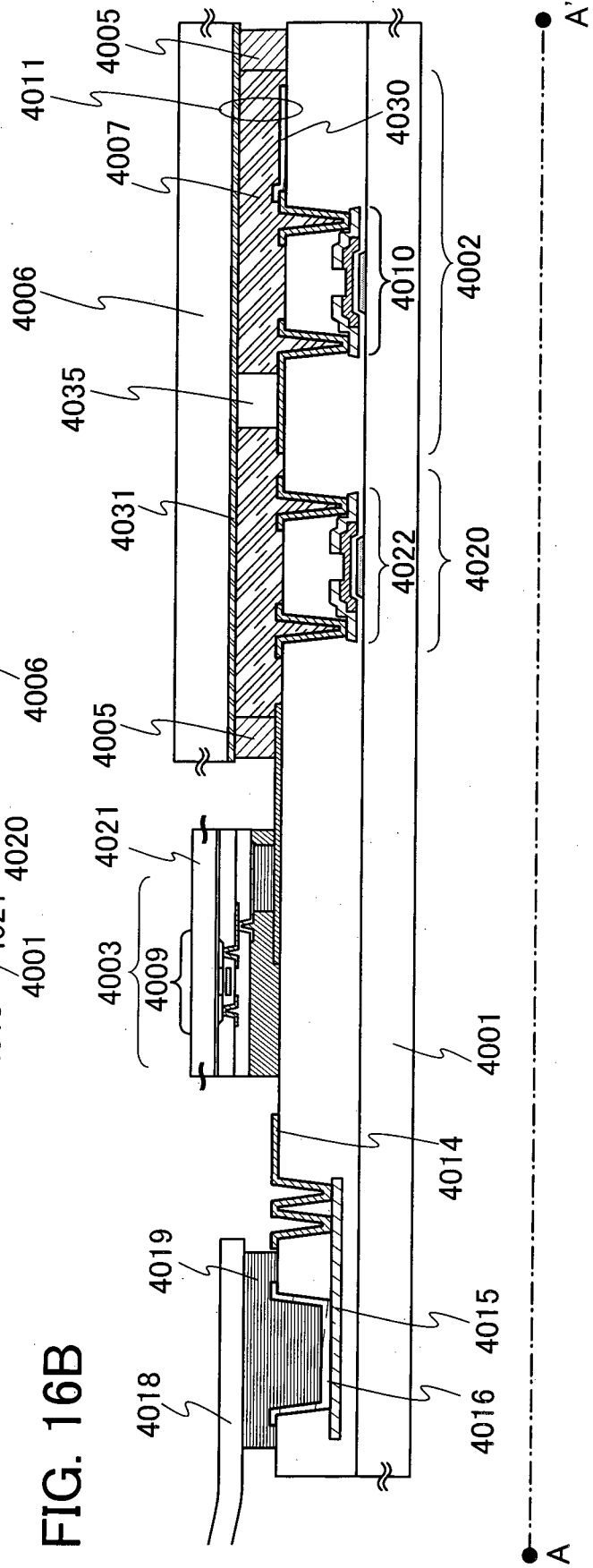


FIG. 16B



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FIG. 17

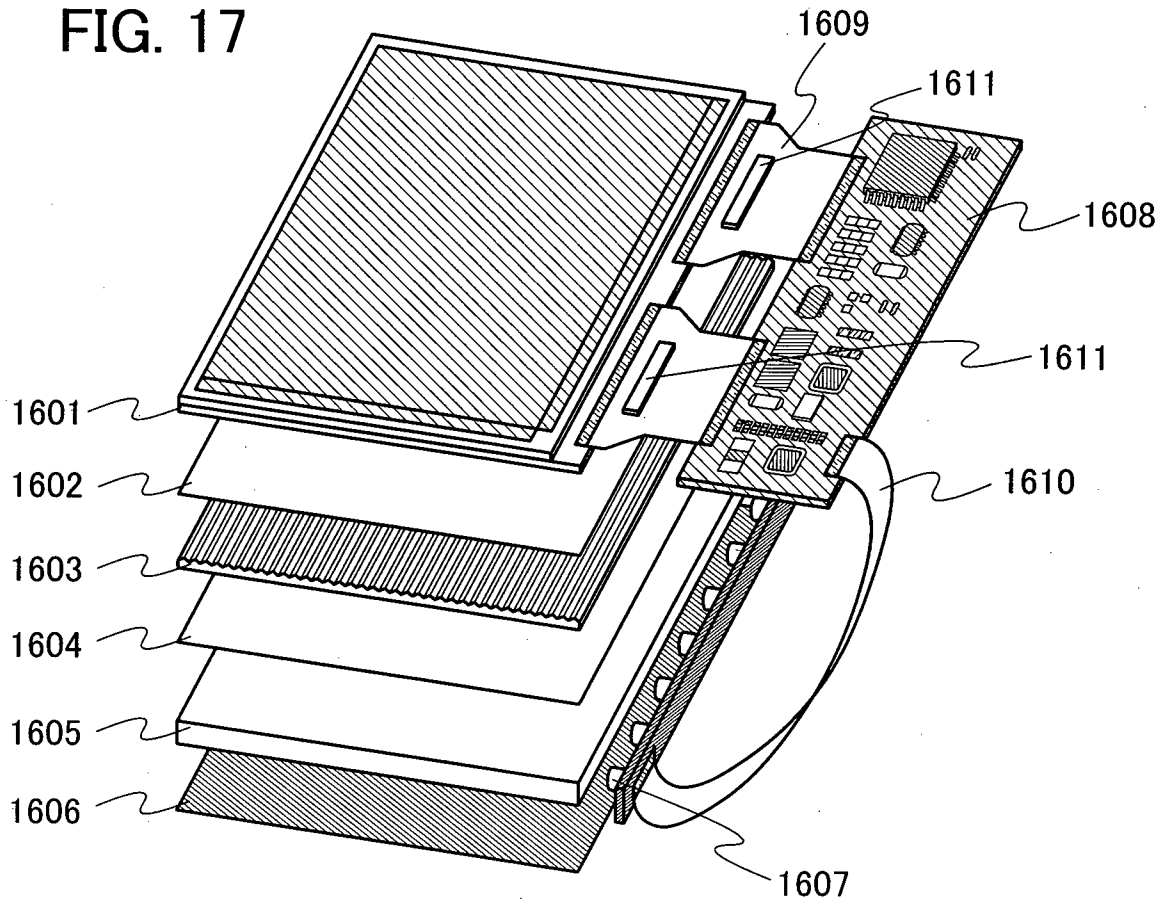


FIG. 18A

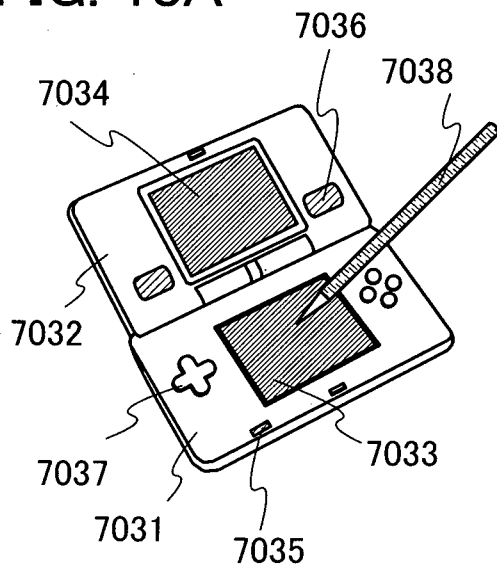


FIG. 18B

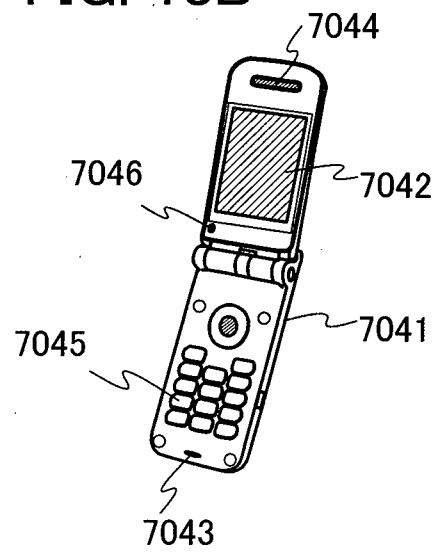


FIG. 18C

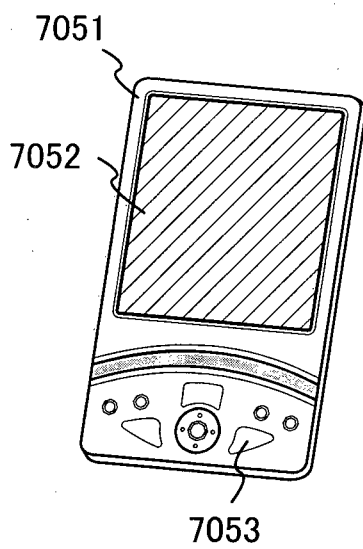


FIG. 18D

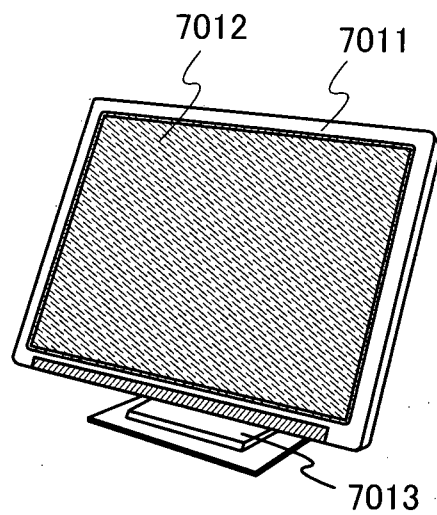


FIG. 19

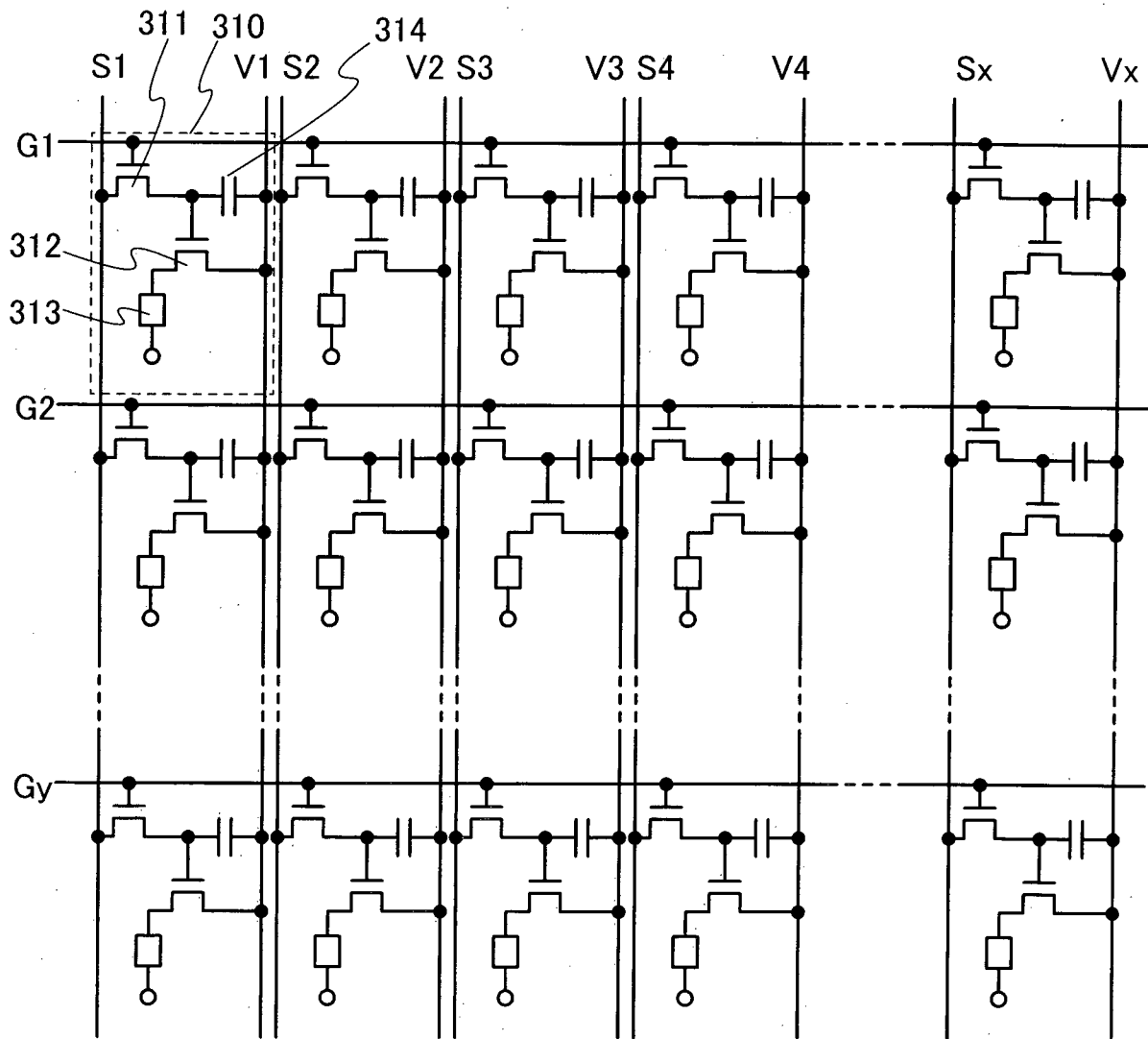
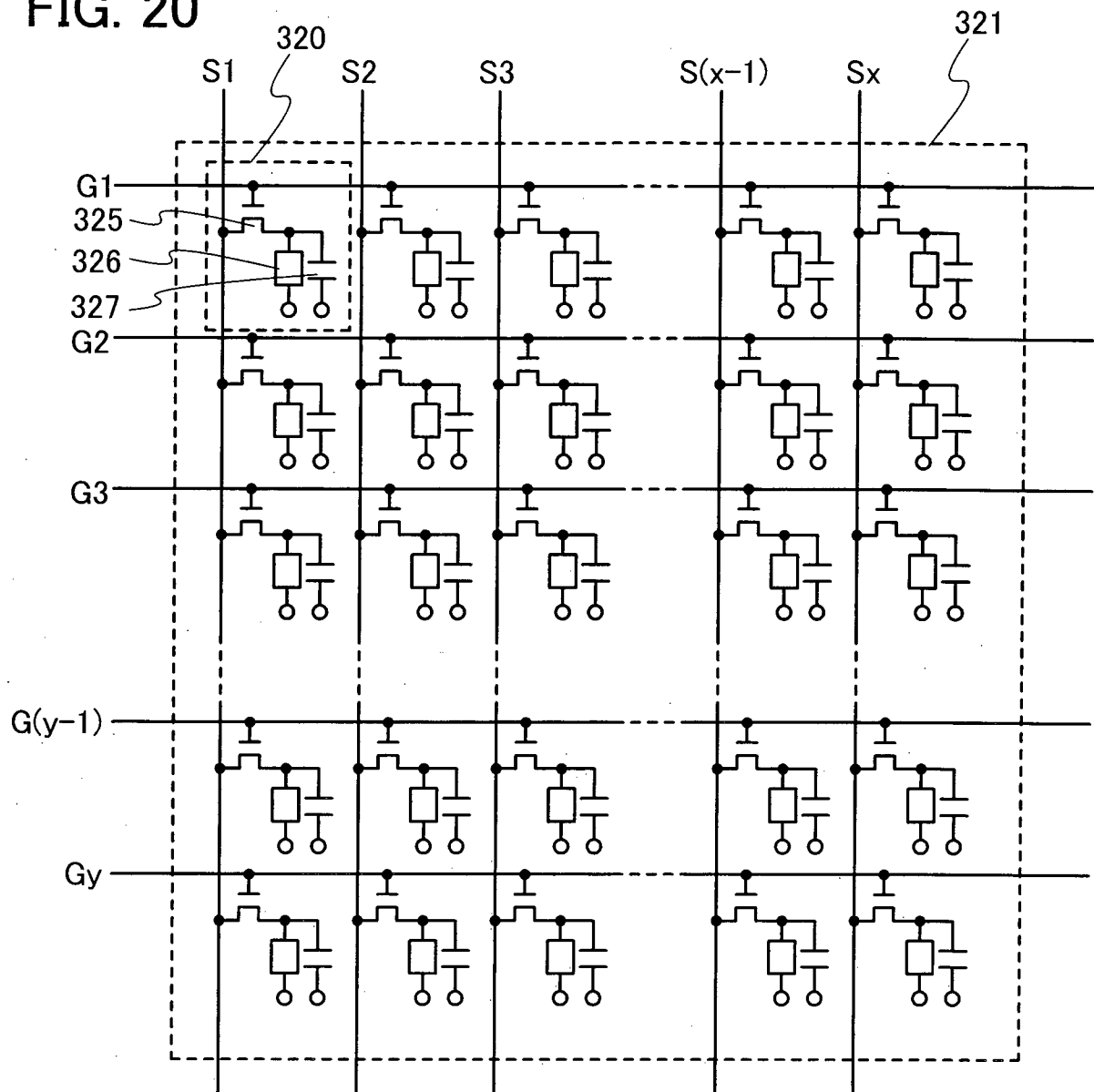


FIG. 20



EXPLANATION OF REFERENCE

100: semiconductor display device, 101: pixel portion, 102: scan line driver circuit, 103: first signal line driver circuit, 104: second signal line driver circuit, 105: first substrate, 106: second substrate, 110: transistor, 111: transistor, 112: capacitor, 113: semiconductor film, 114: semiconductor film, 115: semiconductor film, 116: insulating film, 117: gate electrode, 118: gate electrode, 119: electrode, 120: transistor, 121: capacitor, 122: gate electrode, 123: insulating film, 124: active layer, 125: source electrode, 126: drain electrode, 127: insulating film, 128: electrode, 129: electrode, 130: shift register, 131: memory circuit, 132: memory circuit, 133: level shifter, 134: DAC, 135: analog buffer, 140: memory element, 141: memory element, 142: terminal, 143: terminal, 144: level shifter, 145: DAC, 146: buffer, 150: sampling circuit, 151: analog memory circuit, 152: digital buffer, 160: TAB tape, 300: pixel, 301: pixel portion, 305: transistor, 306: liquid crystal element, 307: capacitor, 310: pixel, 311: switching transistor, 312: driving transistor, 313: light-emitting element, 314: storage capacitor, 320: pixel, 321: pixel portion, 325: transistor, 326: display element, 327: storage capacitor, 400: second substrate, 401: transistor, 402: capacitor, 403: gate electrode, 404: insulating film, 405: oxide semiconductor film, 406: channel protective film, 407: source electrode, 408: drain electrode, 409: insulating film, 410: electrode, 411: electrode, 421: transistor, 422: capacitor, 423: gate electrode, 424: insulating film, 425: oxide semiconductor film, 427: source electrode, 428: drain electrode, 429: insulating film, 430: electrode, 431: electrode, 441: transistor, 442: capacitor, 443: gate electrode, 444: insulating film, 445: oxide semiconductor film, 447: source electrode, 448: drain electrode, 449: insulating film, 450: electrode, 451: electrode, 501: transistor, 502: transistor, 503: transistor, 504: transistor, 505: transistor, 506: transistor, 507: transistor, 508: transistor, 509: transistor,

510: transistor, 511: capacitor, 512: capacitor, 513: capacitor, 514: capacitor, 515: capacitor, 516: capacitor, 520: terminal, 521: terminal, 522: terminal, 523: terminal, 524: terminal, 525: terminal, 526: terminal, 527: terminal, 530: transistor, 531: transistor, 532: terminal, 533: terminal, 534: terminal, 535: node, 536: node, 600a: bootstrap circuit, 600b: bootstrap circuit, 600c: bootstrap circuit, 601: transistor, 602: transistor, 603a: transistor, 603b: transistor, 603c: transistor, 604a: transistor, 604b: transistor, 604c: transistor, 605a: transistor, 605b: transistor, 605c: transistor, 606a: transistor, 606b: transistor, 606c: transistor, 607a: transistor, 607b: transistor, 607c: transistor, 608a: capacitor, 608b: capacitor, 608c: capacitor, 900: first substrate, 901: second substrate, 903: adhesive, 904: terminal, 905: wire, 906: first semiconductor element, 907: pad, 910: first substrate, 911: second substrate, 912: pad, 913: solder ball, 914: first semiconductor element, 916: terminal, 920: first substrate, 921: second substrate, 922: pad, 924: first semiconductor element, 926: terminal, 927: conductive resin, 1401: transistor, 1402: gate electrode, 1403: gate insulating film, 1404: oxide semiconductor film, 1405: conductive film, 1406: conductive film, 1407: insulating film, 1408: insulating film, 1410: pixel electrode, 1411: alignment film, 1413: counter electrode, 1414: alignment film, 1415: liquid crystal, 1416: sealant, 1417: spacer, 1420: substrate, 1601: panel, 1602: diffusion plate, 1603: prism sheet, 1604: diffusion plate, 1605: light guide plate, 1606: reflection plate, 1607: light source, 1608: circuit board, 1609: COF tape, 1610: FPC, 1611: first substrate, 4001: second substrate, 4002: pixel portion, 4003: first signal line driver circuit, 4004: scan line driver circuit, 4005: sealant, 4006: counter substrate, 4007: liquid crystal, 4009: transistor, 4010: transistor, 4011: liquid crystal element, 4014: wiring, 4015: wiring, 4016: connection terminal, 4018: FPC, 4019: anisotropic conductive film, 4020: second signal line driver circuit, 4021: first substrate,

4022: transistor, 4030: pixel electrode, 4031: counter electrode, 4035: spacer, 6001: second substrate, 6002: pixel portion, 6003: scan line driver circuit, 6004: first substrate, 6005: FPC, 6006: counter substrate, 6007: second signal line driver circuit, 6101: second substrate, 6102: pixel portion, 6103: scan line driver circuit, 6104: first substrate, 6105: FPC, 6106: counter substrate, 6107: second signal line driver circuit, 7011: housing, 7012: display portion, 7013: support, 7031: housing, 7032: housing, 7033: display portion, 7034: display portion, 7035: microphone, 7036: speaker, 7037: operation key, 7038: stylus, 7041: housing, 7042: display portion, 7043: audio-input portion, 7044: audio-output portion, 7045: operation key, 7046: light-receiving portion, 7051: housing, 7052: display portion, and 7053: operation key.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/055559

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L29/786(2006.01) i, G09F9/30(2006.01) i, G09G3/20(2006.01) i,
G09G3/30(2006.01) i, G09G3/36(2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, G09F9/30, G09G3/20, G09G3/30, G09G3/36

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 5-045668 A (SANYO ELECTRIC CO LTD) 1993.02.26, [0077]-[0086], Fig.2 (No Family)	1-17, 19-25
Y	JP 2007-123861 A (SEMICONDUCTOR ENERGY LAB) 2007.05.17, [0144], Fig.16 & US 2007/0072439 A1 & EP 1770788 A2 & CN 1941299 A	1-17, 19-25
A	JP 2010-003910 A (TOSHIBA MOBILE DISPLAY KK) 2010.01.07, Full text; All drawings (No Family)	1-17, 19-25

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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“&” document member of the same patent family

Date of the actual completion of the international search

18.05.2011

Date of mailing of the international search report

31.05.2011

Name and mailing address of the ISA/JP

Japan Patent Office

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/055559

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 18
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
The feature of claim 18 is not referred to in the description. Therefore, claim 18 is not supported by the description as required by Article 6 PCT.

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.