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(54) Title: INTEGRATED CLIP AND LEAD AND METHOD OF MAKING A CIRCUIT

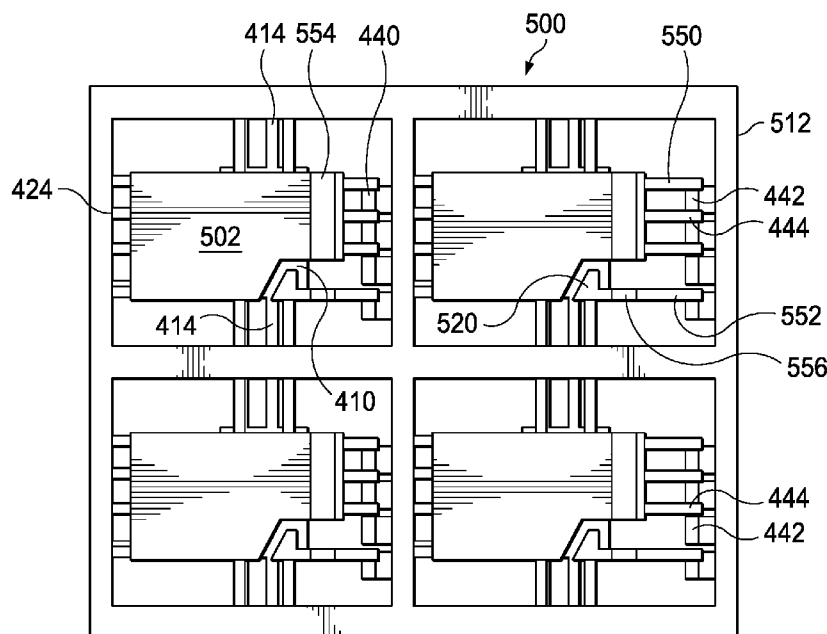


FIG. 7

(57) Abstract: A circuit includes a conductive clip (502) coupled to at least one component in the circuit. At least one lead portion (552) is located on an end of the clip. The circuit further includes a first lead frame having at least one opening sized (444) to receive the at least one lead portion (552). The at least one lead portion (552) is received in the at least one opening (444), and the at least one lead portion (552) is an external conductor of the circuit.



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Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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INTEGRATED CLIP AND LEAD AND METHOD OF MAKING A CIRCUIT

BACKGROUND

[0001] Some integrated circuits have no-lead packages, such as quad-flat no-leads (QFN) and dual-flat no-leads (DFN) devices that physically and electrically couple integrated circuits to printed circuit boards. Flat no-lead devices, also known as micro leadframe (MLF) and small-outline no-leads (SON) devices, are based on a surface-mount technology that connects integrated circuits to the surfaces of printed circuit boards without through-holes in the printed circuit boards. In some examples, flat no-lead packages are near chip scale plastic encapsulated packages, typically fabricated with a planar copper lead frame substrate. Perimeter lands on the package provide electrical coupling to the printed circuit board. The lands serve as contacts and may be referred to as leads internal to the integrated circuit, but the leads do not extend beyond the boundaries of the integrated circuit package.

[0002] Some integrated circuits and other electronic devices have conductive clips that are coupled to electronic components within the circuits and devices. The clips may be on a first plane, and the leads or contacts for the circuits and devices may be on a second plane. The clips are soldered or otherwise electrically and/or mechanically bonded to the leads, which yields additional resistance between the devices and the external contacts of the integrated circuit. The bond also provides a weak spot in the circuits and devices. For example, the bonds are susceptible to cracking and other failures, which may render the circuits and devices inoperable.

SUMMARY

[0003] A circuit includes a conductive clip coupled to at least one component in the circuit. At least one lead portion is located on an end of the clip. The circuit further includes a first lead frame having at least one opening sized to receive the at least one lead portion. The at least one lead portion is received in the at least one opening, and the at least one lead portion is an external conductor of the circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a side cross sectional view of a portion of a device, showing the bonding between a clip and a lead.

[0005] FIG. 2 is a top isometric view of the whole device of FIG. 1, showing the bonding between the clip and the lead.

[0006] FIG. 3 is an expanded, cutaway view of the bond between the clip and the lead of FIGS. 1 and 2, showing the location of a crack in the bond.

[0007] FIG. 4 is a top plan view of an example of a first lead frame.

[0008] FIG. 5 is a top plan view of an example of a second lead frame.

[0009] FIG. 6 is a cutaway, elevation view showing an example of the tabs on the lead frame of FIG. 4.

[0010] FIG. 7 is a top plan view of the lead frames of FIGS. 4 and 5 after they have been placed together.

[0011] FIG. 8 is a side elevation view of the clips of FIG. 5 attached to the leads after a swaging process.

[0012] FIG. 9 is a side, cutaway view of a structure containing a first FET device and a second FET device.

[0013] FIG. 10 is a flow chart of an example method of manufacturing the structure of FIG. 9.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0014] FIG. 1 is a side cross sectional view of a portion of an electronic device 100, showing the bonding between a clip 102 and a lead 104. Examples of the device 100 include an integrated circuit in a quad-flat no-leads (QFN) or a dual-flat no-leads (DFN) package. The clip 102 is a conductive material, such as copper that is coupled to at least one electronic component (not shown in FIG. 1) within a circuit or integrated circuit. In some embodiments, the clip 102 is electrically coupled to the source or drain of at least one field effect transistor (FET). The lead 104 is also a conductive material and serves as a lead for the device 100 to couple the device 100 to other electronic devices. For example, the lead 104 may electronically and mechanically couple the device 100 to a conductor on a printed circuit board.

[0015] The device 100 is incased in a mold 106 that is applied by conventional molding techniques. The lead 104 has a surface 107 that is not encased by the mold 106 and serves as a conductive land for the device 100. During assembly of the device 100 to a printed circuit board (not shown), the surface 107 is set on a bonding material, such as solder on the surface of a printed circuit board. After curing the bonding material, the device 100 is electrically and mechanically coupled to the printed circuit board without the use of through holes in the printed

circuit board.

[0016] The clip 102 and the lead 104 are on different planes, so the clip 102 has an angled portion 108 that brings an end 110 of the clip 102 to the plane of the lead 104. The end 110 of the clip 102 is located proximate a surface 114 of the lead 104 and is mechanically and electrically coupled to the surface 114 at a bonded region 115 by a bonding compound 116. In some embodiments, the bonding compound 116 is solder or a conductive epoxy that commonly bonds clips and leads together.

[0017] FIG. 2 is a top isometric view of an example of the device 100 of FIG. 1. The clip 102 is electrically coupled to electronic components, which are transistors Q1 and Q2 in the embodiment of FIG. 2. The transistor Q1 is also electrically and mechanically coupled to a clip 200. For example, the clip 102 may be coupled to the source of the transistor Q1 and the clip 200 may be coupled to the drain of the transistor Q1. The clip 200 may be electrically coupled to a lead that is not shown in FIG. 2 that couples the drain of the transistor Q1 to external circuits or devices. The gate of the transistor Q1 is coupled to a clip 202, which is bonded to a lead 204 by bonding material 208. The clip 102 is electrically and mechanically bonded to the source of the transistor Q2.

[0018] The bonds between the clip 102 and the lead 104 (and the clip 202 and the lead 204) present some electrical and mechanical problems. Referring to the bond between the clip 102 and the lead 104, the bond creates a relatively high resistance between the clip 102 and the lead 104. For example, resistances are in the following locations: the clip 102; the contact between the clip 102 and the bonding material 116; the bonding material 116; the contact between the bonding material 116 and the lead 104; and the lead 104. These resistances are in series and may be greater than the resistance of the material of the clip 102 and the lead 104, which may be low resistance copper. Accordingly, the bonding of the clip 102 to the lead 104 may provide a relatively high resistance between electronic components coupled to the clip 102 and the lead 104, which may negatively impact the functions of these components.

[0019] Mechanically, the bond between the clip 102 and the lead 104 is a weak spot in the device 100 and is susceptible to cracking or other failures. FIG. 3 is an expanded, cutaway view of the bonded region 115 between the clip 102 and the lead 104 of FIGS. 1 and 2, showing the location of a crack 300 in the bonding material 116. The crack 300 may be caused by stresses, such as stressing due to expansion and contraction as a result of temperature changes or other

factors that stress the bonding material 116, the clip 102 and/or the lead 104. The crack 300 is located in the bonding material 116, so it may increase the resistance in the bond material 116 and exacerbate the above-described problems with high resistance between the clip 102 and the lead 104. In some situations, the crack 300 may cause a complete disconnection between the clip 102 and the lead 104, which may lead to a failure of the device 100.

[0020] The devices described herein overcome the above-described problems associated with the bond between a clip and a lead by forming or fabricating a clip and a lead as a single device rather than two devices that are bonded together. FIG. 4 is a top plan view of a first lead frame 400. FIG. 5 is a top plan view of a second lead frame 500. The lead frames 400 and 500 are portions of dual FET devices in which the FETs are electrically coupled in series and physically arranged side by side. The use of dual FET devices is an example of the many applications in which clips may be fabricated into leads as described herein.

[0021] The first lead frame 400 has multiple portions 402. Each of the portions 402 constitutes a single device having dual FETs, which are referred to herein as a first FET and a second FET. In the example of FIG. 4, the first lead frame 400 has four portions 402, but any number of portions 402 may exist. The portions 402 are bounded by a frame 406 that supports components within the portions 402 and connects the portions 402 to one another.

[0022] In the example of FIG. 4, the first lead frame 400 has a first clip or conductor 410 on which a node of the first FET is fabricated. In the examples described herein, the drain of the first FET is fabricated onto the surface 412 of the first conductor 410. Multiple retainers 414 connect the first conductor 410 to the frame 402 and serves to maintain the first conductor 410 in a fixed position relative to the frame 402 during fabrication. Later processes in fabrication cut the retainers 414, so they serve as conductors to couple the first FET to other circuits and/or electronic components.

[0023] A second clip or conductor 420 has a surface 422 on which the source of the second FET is fabricated. Multiple retainers 424 connect the second conductor 420 to the frame 402 and serves to maintain the second conductor 420 in a fixed position relative to the frame 402 during fabrication. As with the first conductor 410, the retainers 424 are cut during later fabrication processes and serve as conductors to couple the second FET to other circuits and/or electronic components. A third clip or conductor 430 couples to the gate of the second FET. A retainer 434 connects the third conductor 430 to the frame 402 and serves the same function as the

retainers 414 and 424.

[0024] Multiple retainers 440 extend from the frame 402 and serve to receive portions of the second lead frame 500 as described in greater detail below. The retainers 440 include multiple tabs 442 separated by spaces 444, in which portions of the second lead frame 500 are received into the spaces 444 as described in greater detail below.

[0025] FIG. 6 is a cutaway, elevation view showing an example of the retainers 440 of FIG. 4. In the example of FIG. 6, portions of the second lead frame 500 are filling the spaces 444 between the tabs 442. The tabs 442 have extended portions 600 that extend beyond the height of the second lead frame 500. In the example of FIG. 6, the extended portions 600 are pointed or substantially triangular. The extended portions 600 provide metal to fill spaces between the tabs 442 and the second lead frame 500 during a swaging process.

[0026] Referring again to FIG. 5, the second lead frame 500 has a first clip or conductor 502 with a surface 504. The surface 504 is a top surface of the device containing the FETs; and, in some embodiments, it is an external surface of the device. The first conductor 502 has a surface (not shown in FIG. 5) that is opposite the surface 504 on which both the source of the first FET and the drain of the second FET are fabricated. The second lead frame 500 has multiple retainers 510 that connect the first conductor 502 to a frame 512. The frame 512 functions in the same manner as the frame 402 of FIG. 4. A second clip or conductor 520 couples to the gate of the first FET. The second conductor 520 is maintained in a fixed location relative to the frame 512 by a retainer 522.

[0027] The first conductor 502 has multiple leads 550 extending from a body portion and the second conductor 520 has a lead 552 extending from a body portion. The leads 550 and 552 are sometimes referred to as lead portions. The leads 550 are connected to the first conductor 502 by a transition 554, and the lead 552 is connected to the second conductor 520 by a transition 556. The transitions 554 and 556 lower the leads 550 and 552 to a plane or planes lower than a plane on which the body portions of the first conductor 502 and the second conductor 520 are located. The leads 550 and 552 are integrally formed with other components in the first conductor 502.

[0028] During fabrication, the materials for the sources, gates and drains of the FETs are fabricated onto the conductors of the lead frames 400 and 500. For example, the components of the FETs may be fabricated onto or be electrically coupled to the conductors 410, 420 and 430. An example of the layers in the FETs is described further below. The second lead frame 500

may then be placed onto the first lead frame 400, and solder bonds or other bonds may be cured to form the FETs.

[0029] FIG. 7 is a top plan view of the lead frames 400 and 500 of FIGS. 4 and 5 after they have been placed together. FIG. 7 is a top view in which the second lead frame 500 has been placed on top of the first lead frame 400. As shown in FIG. 7, the leads 550 of the first conductor 502 and the lead 552 of the second conductor 520 are received into the spaces 444 of the retainers 440. The placement of the leads 550 and 552 within the retainers 440 is shown by the elevation view of FIG. 6. The solder and/or other bonding materials in the FETs are cured after the leads 550 and 552 are received in the spaces 444.

[0030] At this point of fabrication, the bonding materials within the FETs are cured, and the lead frames 400 and 500 need to be encased with a molding compound before singulation. The leads 550 and 552 are secured to the retainers 440 before molding, which secures the leads 550 and 552 in a secure location during the molding and singulation processes. FIG. 8 shows the retainers 440 attached to the leads 550 and 552 after a swaging process. With additional reference to FIG. 6, the swaging process has crushed or deformed the top portions 600 of the retainers 440 into the leads 550 and 552, which secures the leads 550 and 552 in fixed locations. Accordingly, the leads 550 and 552 are on a lower plane than the conductors 502 and 520 (FIG. 5), and they will not move when the pressures associated with molding are applied to the lead frames 400 and 500. Other techniques may be applied to secure the leads 550 and 552 to the first retainers 440, such as caulking and other bonding techniques.

[0031] FIG. 9 is a side, cutaway view of a structure 900 containing a first FET device 902 and a second FET device 904. The view of the structure 900 does not show molding compound, but it would extend between top surfaces 908 and bottom surfaces 910 of the FET devices 902 and 904. Each of the FET devices 902 and 904 has two FETs, which are the aforementioned first FET 914 and the second FET 916. The devices are singulated along singulation lines 920 that pass through the retainers 440. Accordingly, the singulation breaks any electrical contact between the first lead frame 400 and the second lead frame 500, so that the leads 550 and 552 (not shown in FIG. 9) do not electrically contact the second lead first lead frame 400. After singulation, the ends of the leads 550 and 552 are exposed and serve as electrical conductors for their respective devices 902 and 904.

[0032] FIG. 10 is a flow chart 1000 of an example method of manufacturing a device with two

lead frames as described above. Step 1002 includes fabricating at least one electronic component between a portion of a first lead frame and a portion of a second lead frame. The first lead frame has a lead portion. Step 1004 includes attaching the lead portion of the first lead frame to the second lead frame. Step 1006 includes singulating the at least one component. The lead portion is a lead of the electronic component subsequent to singulating.

[0033] The devices described above are fabricated with dual transistors for illustration purposes. In other embodiments, the devices are fabricated with other components, such as single transistors. The integrally formed leads (described above) reduce the electrical resistance from the leads to the components and increase the thermal conductivity. For example, the integrally formed leads enable the efficient transfer of heat, without conducting the heat through bonding materials.

[0034] While some examples of integrated circuits have been described in detail herein, modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A circuit comprising:
a conductive clip coupled to at least one component in the circuit;
at least one lead portion located on an end of the clip; and
a first lead frame having at least one opening sized to receive the at least one lead portion;
wherein the at least one lead portion is received in the at least one opening; and
wherein the at least one lead portion is an external conductor of the circuit.
2. The circuit of claim 1, wherein the conductive clip is at least a portion of a second lead frame.
3. The circuit of claim 2, wherein the first lead frame is at least partially on a first plane, and wherein the second lead frame is at least partially on a second plane.
4. The circuit of claim 1, wherein the at least one lead portion is secured within the at least one opening by a swaging process.
5. The circuit of claim 1, wherein the at least one lead portion is secured within the at least one opening by a bonding compound.
6. The circuit of claim 1 further comprising a plurality of tabs defining the boundaries of the at least one opening.
7. The circuit of claim 6, wherein the tabs have extended portions during fabrication, and wherein the extended portions are crushed during fabrication, and wherein the crushing secures the at least one lead portion in the at least one opening.
8. The circuit of claim 6, wherein the tabs are swaged to secure the at least one lead portion in the at least one opening.
9. The circuit of claim 6, wherein the tabs are bonded with a bonding material to secure the at least one lead portion in the at least one opening.
10. The circuit of claim 1, wherein the conductive clip is coupled to a first node of at least one transistor.
11. The circuit of claim 10, wherein the first lead frame is coupled to a second node of the at least one transistor.
12. The circuit of claim 1, wherein a source of a first transistor and the drain of a second

transistor are fabricated onto the conductive clip.

13. The circuit of claim 12, wherein the drain of the second transistor and the source of the second transistor are fabricated onto the first lead frame.

14. The circuit of claim 12, wherein the gate of the first transistor is coupled to the conductive clip.

15. A method of fabricating a circuit, the method comprising:

fabricating at least one electronic component between a portion of a first lead frame and a portion of a second lead frame, the first lead frame having a lead portion;

attaching the lead portion of the first lead frame to the second lead frame; and

singulating individual components from the first lead frame and the second lead frame, wherein the lead portion is a lead of the electronic component subsequent to singulating.

16. The method of claim 15, wherein the singulating cuts the attachment between the at least one conductive clip and the first lead frame.

17. The method of claim 15, further comprising encasing at least the lead portion in a mold compound before singulation.

18. The method of claim 17, wherein the at least a portion of the lead portion extends from the mold compound after singulation.

19. The method of claim 15, wherein attaching includes swaging the lead portion of the first lead frame to the second lead frame.

20. A circuit comprising:

a conductive clip coupled to at least a first node of a transistor;

at least one lead portion located on an end of the clip and integrally formed with the clip;
and

a lead frame having at least one opening sized to receive the at least one lead portion, wherein a second node of the transistor is coupled to the lead frame;

wherein the at least one lead portion is received in the at least one opening; and

wherein the at least one lead portion is an external conductor of the circuit.

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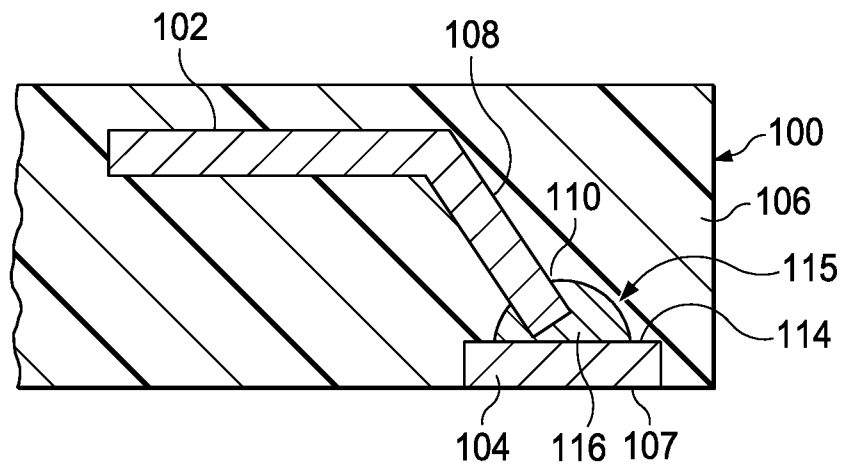


FIG. 1

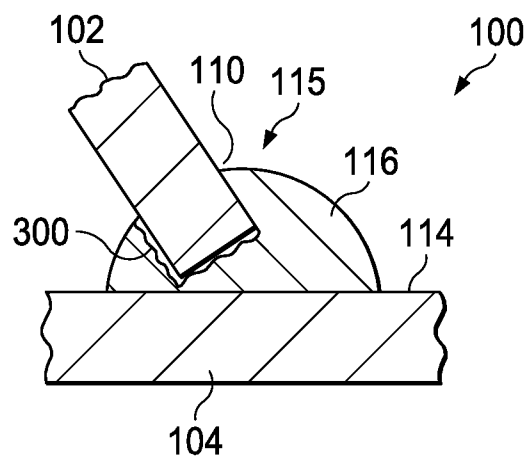


FIG. 3

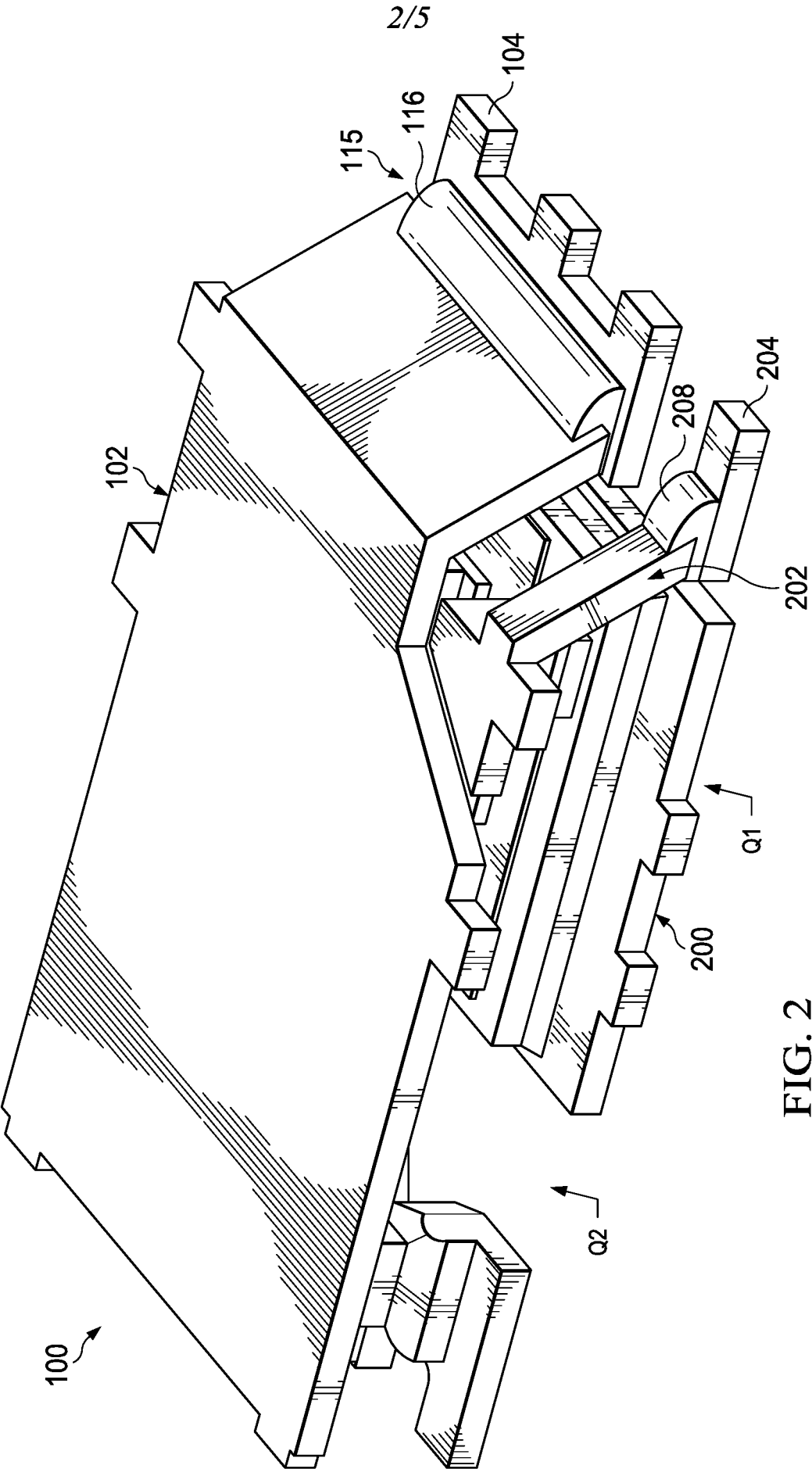
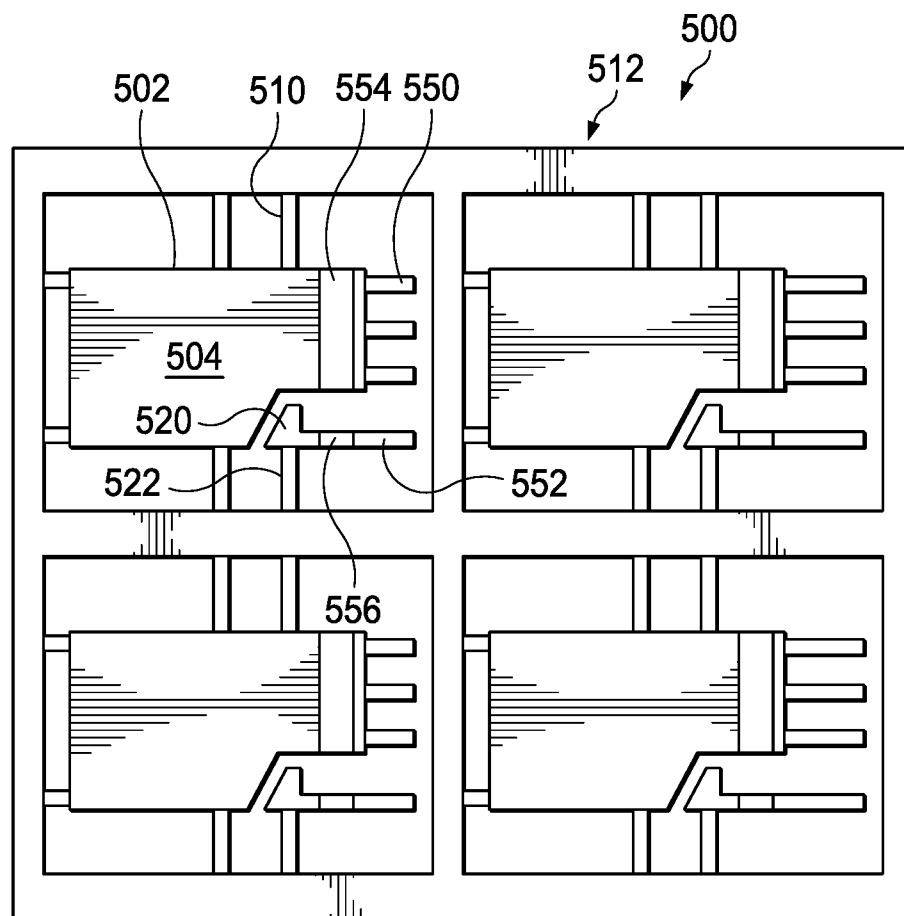
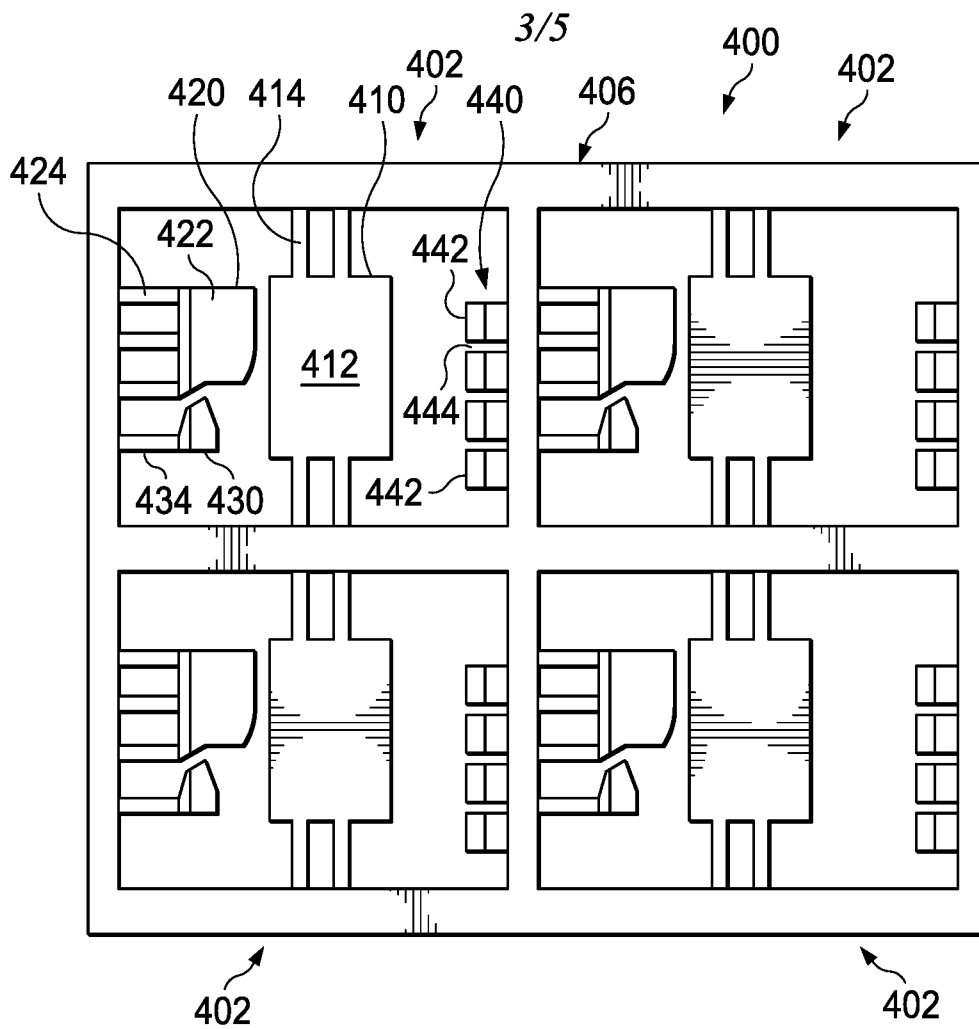


FIG. 2



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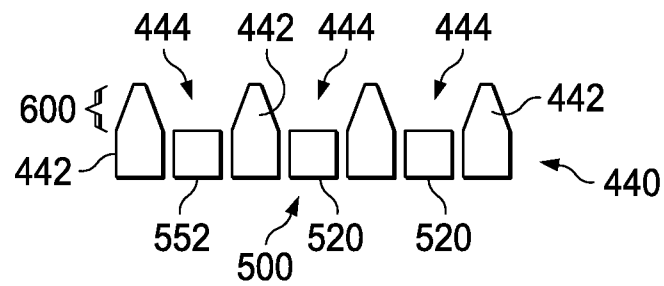


FIG. 6

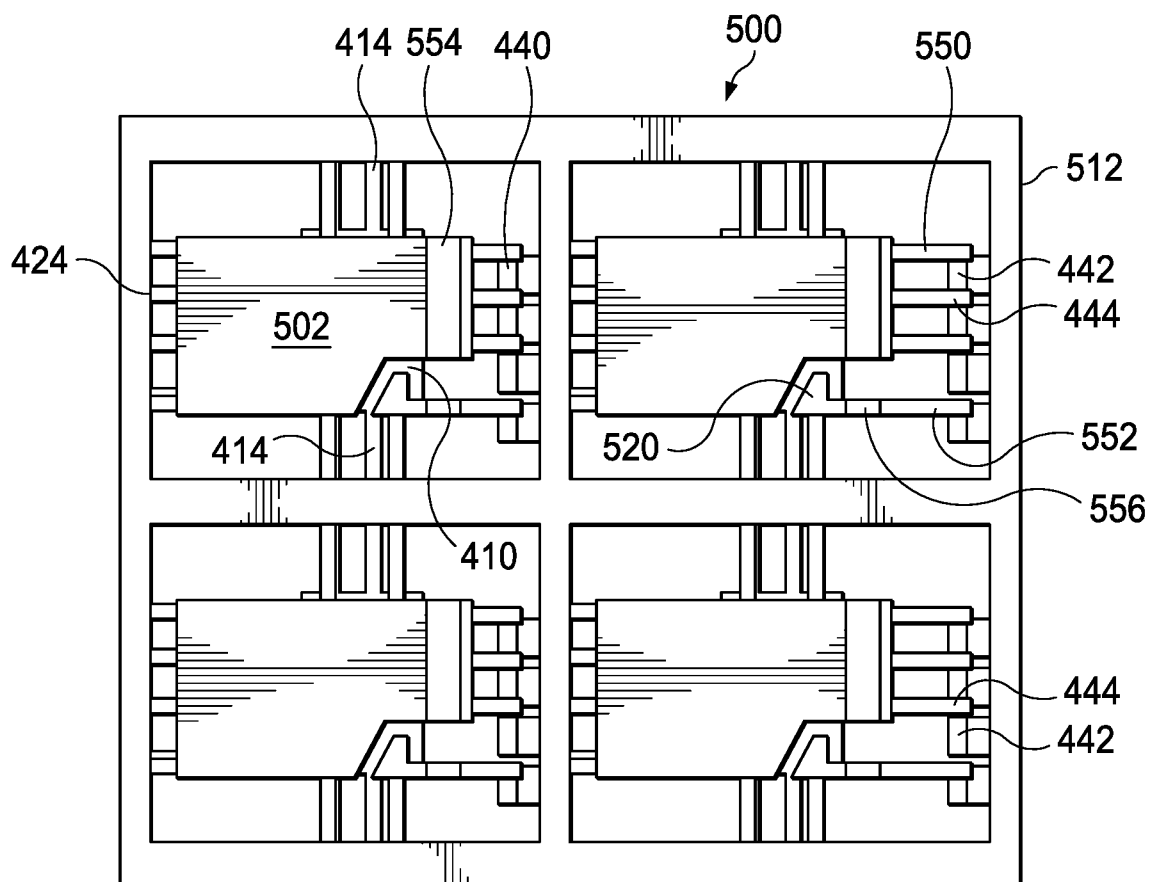


FIG. 7

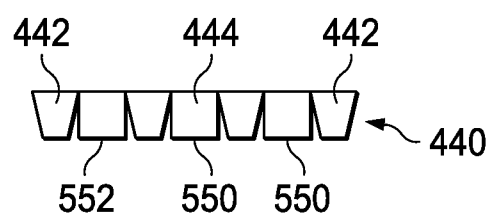
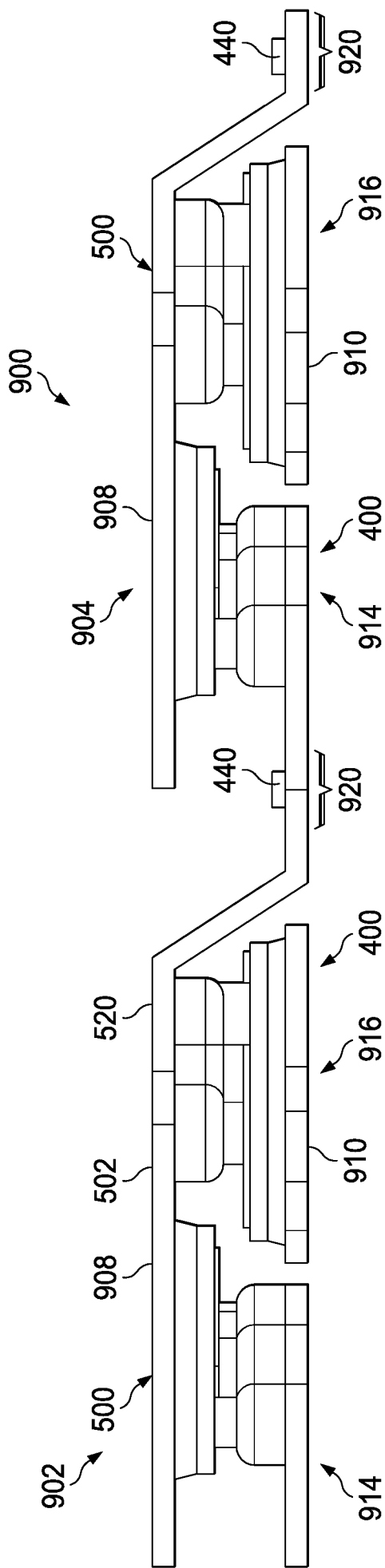


FIG. 8



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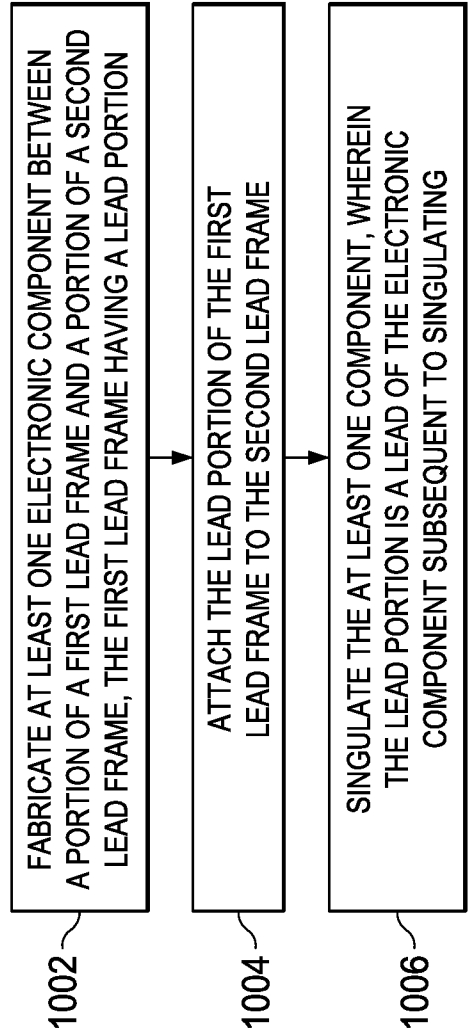


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/031873

A. CLASSIFICATION OF SUBJECT MATTER <i>H01L 23/495 (2006.01)</i> <i>H01L 27/00 (2006.01)</i> <i>H01L 21/60 (2006.01)</i>		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H01L 23/00, 23/02, 23/495, 27/00, 27/14, 21/00, 21/02, 21/60		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007/0215996 A1 (RALF OTREMBA) 20.09.2007	1-20
A	US 2012/0292754 A1 (INTERNATIONAL RECTIFIER CORPORATION) 22.11.2012	1-20
A	US 2009/0189266 A1 (YONG LIU et. al.) 30.07.2009	1-20
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Date of the actual completion of the international search	Date of mailing of the international search report	
22 August 2016 (22.08.2016)	01 September 2016 (01.09.2016)	
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer O. Gudkova Telephone No. 8 499 240 25 91	