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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 4 :		(11) International Publication Number:
G05F 7/00, H03K 17/64, 17/66	A1	WO 88/ 00370
		(43) International Publication Date: 14 January 1988 (14.01.88)

(21) International Application Number: PCT/US87/01591

(22) International Filing Date: 1 July 1987 (01.07.87)

(31) Priority Application Number: 880,765

(32) Priority Date: 1 July 1986 (01.07.86)

(33) Priority Country: US

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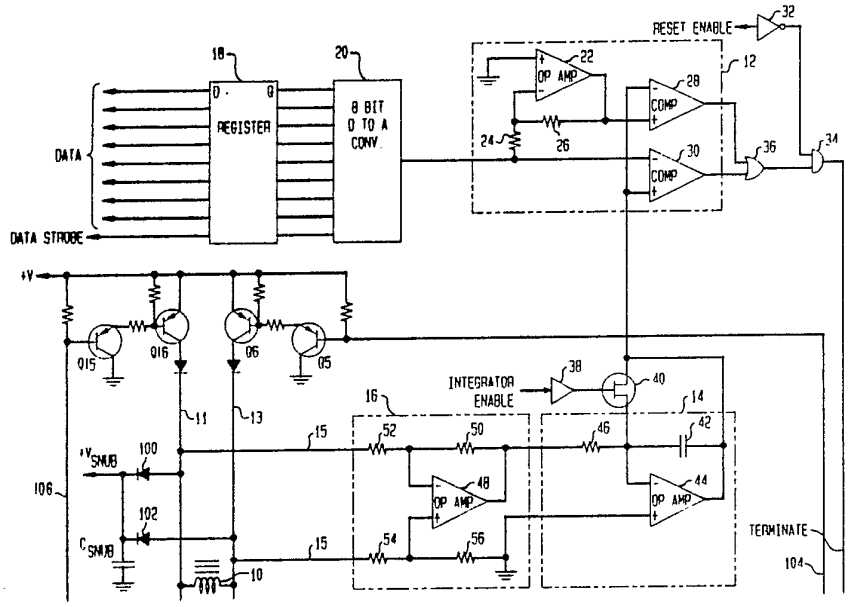
(81) Designated States: DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, NO.

Published
With international search report.

(54) Title: METHOD AND APPARATUS FOR CONTROLLING THE AMOUNT OF MAGNETIC FLUX IMPARTED TO A FERRIMAGNETIC LOAD

(57) Abstract

A device-implemented method for driving a ferrimagnetic load (10), such as a phase shifter in an antenna array, which precisely meters the amount of magnetic flux imparted to the load (10) by sensing the voltage applied to a winding and integrating the sensed voltage over time. The time integrated voltage is proportional to the magnetic flux imparted to the load (10) and is constantly compared to a preprogrammed value stored in a memory (18). When the sensed voltage reaches the preprogrammed value, the voltage is removed from the load (10) so that a metered amount of magnetic flux, proportional to the preprogrammed value, remains in the load (10). The load (10) is initially reset by delivering current in one direction through its winding until saturation is reached. The load (10) is set with a metered amount of magnetic flux by delivering current in the opposite direction through the winding. A current sensing circuit (68) senses the point at which the load (10) becomes saturated during the reset cycle and also senses current flow through the winding during the set cycle in order to prevent a current overload.



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METHOD AND APPARATUS FOR CONTROLLING THE AMOUNT OF MAGNETIC FLUX IMPARTED TO A FERRIMAGNETIC LOAD

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention broadly relates to a device for changing the current flow through a ferrimagnetic load so as to affect the magnetic flux imparted to the load, and deals more particularly with a device-implemented method for driving a phase shifter for an antenna array in which the magnetic flux imparted to the phase shifter is precisely metered.

2. Description of Related Art

Phase shifters are used as primary components in electronically controlled array antennas. An array antenna contains many individual radiating elements. By properly controlling the phase of each element, the resulting beam of the antenna can be steered electronically. By using a so-called reciprocal phase shifter, the same antenna can be used as a receiving antenna with a steerable beam.

Ferrite phase shifters employed in array antennas are formed by placing ferrite materials in a section of a waveguide. The ferrite phase shifter can be either a reciprocal or non-reciprocal device depending upon its configuration. In a reciprocal phase shifter, phase shifting is accomplished by changing the magnetic permeability of the ferrite through changing the externally applied DC magnetic field. Non-reciprocal ferrite phase shifters provide a shift in microwave phase dependent upon the amount of remanent magnetism in the ferrimagnetic element. A coil of wire, forming an inductive load, is normally used to alter the strength of the magnetic field in a reciprocal phase shifter. The strength of the field in a non-reciprocal phase shifter is a function of voltage across its toroidal winding versus the period of time that the voltage is applied.

In the past, the strength of the magnetic field was controlled by controlling the time period for which the voltage was applied to the coil. In order to accomplish this, the switching speeds of the control element were required to be extremely fast and it was also necessary that the applied voltage be controlled very precisely. U.S. Patents 3,947,776 and 4,469,961, respectively issued March 30, 1976 and September 4, 1984, exemplify prior approaches for driving inductive loads, such as phase shifters, which rely on extremely fast switching times. Specifically, the arrangements in these prior patents relate to reciprocal-type phase shifters for establishing and then sustaining a current flow by reducing the drive voltage. These previous systems were less than completely satisfactory in terms of their speed and accuracy because of

variables which affect the switching time, such as variations in rise time, voltage drops on the power supply and temperature variations.

The present invention is directed toward overcoming the above-mentioned deficiencies.

SUMMARY OF THE INVENTION

According to the present invention, a device-implemented method is provided for driving a ferrimagnetic load, such as a non-reciprocal ferrite phase shifter, in an antenna array by precisely metering the amount of magnetic flux imparted to the load. The voltage applied across its winding is sensed by a differential amplifier and is integrated over time by an integrating amplifier and capacitor. The time integrated voltage is proportional to the magnetic flux imparted to the load and is continuously compared to a preprogrammed value stored in a memory. When the time integrated voltage reaches the preprogrammed value, the voltage is removed from the winding so that a metered amount of magnetic flux, proportional to the preprogrammed value, remains in the load. The load is initially reset by delivering current in one direction through the winding until the load is saturated. A current sensing circuit determines when the load has become saturated and removes voltage from the winding when the saturation point is reached. The load is set by delivering current through the winding in the opposite direction. Current is driven through the winding by a pair of bridged drivers which include MOSFET's. The differential amplifier and integrating amplifier

function in a manner which takes into consideration variations in voltage rise time, voltage drops on the power supplies and temperature variations.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

Figures 1 and 2, taken together, form a detailed schematic diagram of a circuit for driving a ferrimagnetic load, which forms the preferred embodiment of the present invention; and

Figure 3 is a plan view showing how Figures 1 and 2 are to be arranged for proper viewing.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figures 1 and 2, the present invention broadly relates to a device-implemented method for driving an inductive load and particularly a ferrimagnetic load, such as the coil 10 of a nonreciprocal type ferrite phase shifter. The phase shifter is used in an incorporating radar or communiations system, and more particularly an antenna array, comprising a plurality of individual radiating elements. The phase shift imparted to each radiating element is dependent upon the quantity of gauss contained in the magnetic field of the phase shifter. The strength of the field in the ferrite is a function of the voltage across the coil 10 and the period of time that this voltage is applied.

The coil 10 is coupled across a pair of lines 11, 13 and is "driven" by a pair of bridged drivers comprising transistors Q5, Q6, Q15 and Q16. These drivers are referred to as being "bridged" because the coil 10 is connected between the two sets of drivers, i.e. one side of coil 10 is connected via line 13 to drivers Q5, Q6 while the other side of the coil 10 is connected via line 11 to transistors Q15, Q16. These drivers respectively deliver current alternately through the coil 10 in opposite directions. Transistor Q5 has its base connected with a control line 104 and is operative to control the base electrode of transistor Q6. The collector-to-emitter path of the transistors Q6 and Q16 are connected between a positive source of voltage and the coil 10. Transistor Q15 has its base connected to a control line 106 and is operative to control the base electrode of transistor Q16.

Transistors Q15 and Q16 cooperate with a switching transistor Q3 and a Baker-clamped driver generally indicated within the broken line 98. The Baker-clamped driver 98 broadly includes a pair of transistors Q1 and Q2 which control the gate of transistor Q3, and is controlled by a negative enable signal received on line 108.

Similarly, transistors Q5 and Q6 operate in concert with a switching transistor Q13 and a Baker-clamped driver, generally indicated within the broken line 66. The Baker-clamped driver 66 includes a pair of transistors Q11, Q12 as well as resistors 76, 77, 78, 80 and 82, capacitors 74 and diodes 70, 72. The Baker clamp driver 66 is

essentially identical in all respects to driver 98 and is controlled by a positive enable signal received on line 110. The driver 66 is connected to and controls the gate of transistor Q13. Transistors Q3 and Q13 are MOSFET's which by their nature have a particularly fast switching time. The source-to-drain path of each of the transistors Q3, Q13 are connected with each other and with a current sensing circuit 68 which functions to sense the magnitude of current flowing through the coil 10. The current sensing circuit 68 includes an operational amplifier 86, a zener diode 88 and resistors 92, 96. Resistor 90 completes the current path for diode 88. The op-amp 86 is configured as a comparator so as to compare the voltage on its non-inverting input, which is proportional to the flow of current through coil 10, with a reference voltage on its inverting input. The output of the comparator 86 is delivered through an OR gate 84 to the reset inputs of a pair of flip-flops 58,60. The set inputs of flip-flops 58 and 60 are connected with the incorporating communications system (not shown) which controls the antenna in its transmit and receive modes. The $\overline{Q}$ output of flip-flop 58 is delivered on line 110 as a positive enabling signal to the Baker clamp driver 66, and is also delivered through resistor 61 and through transistor Q14 as an enabling signal to the base of transistor Q15, on line 106. In a similar manner, the $\overline{Q}$ output of flip-flop 60 is delivered as a negative enabling signal on line 108 to the Baker-clamped driver 98, and is also delivered through resistor 63 and through transistor Q4 and line 104 to the base of transistor Q5.

Means generally indicated within the broken line 16 are provided for sensing the magnitude of voltage applied across the coil 10. The voltage sensing means 16 is connected across the coil 10 by means of lines 15. The voltage sensing means 16 comprises an op-amp 48 and resistors 50, 52, 54, 56. The output of the voltage sensor 16 is delivered to an integrator 14 which functions to integrate the sensed voltage over time. The integrator 14 comprises an operational amplifier 44, a resistor 46 and a capacitor 42 connected in feedback between the output of the op-amp 44 and its inverting input. The integrator 14 is controlled by a switch in the nature of a FET 40 which receives an enabling signal from the incorporating communications system through an amplifier 38.

The time integrated voltage value output by the integrator 14 is delivered to the inverting and non-inverting inputs respectively of a pair of comparators 28 and 30. Op-amp 22 and resistors 24, 26 invert the voltage applied to the non-inverting input of comparator 28. Comparators 28, 30, along with an op-amp 22 and resistors 24 and 26, form a "window comparator" which functions to compare or "threshold" the time integrated voltage value provided by the integrator 14 with a reference value when the coil 10 is being set either in a transmit or receive mode. This reference value is defined by a multibit digital data word which is received from a suitable source such as a memory (not shown). In the present example, the data word comprises eight bits which are loaded from the source (memory) into a register 18 upon receipt at the register 18 of a data strobe signal from the incorporating communication system. A D/A converter 20 converts the digital data to an analog signal which is

delivered to the non-inverting and inverting inputs respectively of the comparators 28,30. In regard to the input to comparator 28, the voltage is inverted as discussed above. The outputs of the comparators 28,30 are delivered through an OR gate 36 to one input of an AND gate 34. The second input to the AND gate 34 is formed by a reset enable signal received from the incorporating communications system which is inverted by an inverter 32. The output of the AND gate 34 is delivered through the other input of OR gate 84 to the reset inputs of flip-flops 58, 60.

Having generally described the components of the circuit, a more detailed description will now be given with reference to its operation. In connection with the present description, it will be assumed that the phase shifter of which the coil 10 forms a part is of the non-reciprocal type in which the phase shift applied to an incoming or received signal is different from that applied to an outgoing, transmitted signal. It is thus necessary to "set" the ferrite with the appropriate amount of magnetic flux very quickly between the transmit and receive cycles. The data word loaded into the register 18 is preprogrammed and may be, for example, non-linear. This data word corresponds to a voltage value to be integrated across the coil 10 during the transmit and receive cycles. This value may be the same for both the transmit and receive cyles but of opposite polarity. In other words, the value represented by this data word is proportional to the magnitude of magnetic flux imparted to the ferrite by the coil 10.

Initially, before a metered amount of flux is imparted to the ferrite from the coil 10, the coil 10 is reset by driving it into saturation. By driving the coil 10 into saturation, the initial value of the magnetic flux is known and this flux remains in the ferrite after the current is turned off. The reset cycle will be described later in more detail. Assume now that the ferrite has been reset and it is desired to set the ferrite in preparation for a transmit cycle. Digital data is delivered from a central bus of the incorporating communications system and is latched into the register 18. As mentioned above, the data word stored in register 18 corresponds to the voltage to be integrated across the coil 10 and is thus proportional to the amount of phase shift to be set in the ferrite. The D/A converter 20 converts the digital data to an analog, DC voltage signal which is delivered to the input of the window comparator 12. The op-amp 22 provides its complements to the comparators 28, 30 which form an absolute value peak detector. At this point, the integrator enabling signal from the incorporating communications system controls the FET switch 40 so as to discharge the capacitor 42 until the output of the integrator 14 is zero. A positive start command signal received at the set input of flip-flop 58 causes the $\overline{Q}$ output to drive the common base buffer transistor Q14 and the Baker-clamped driver 66. The enabling signal, delivered from transistor Q14 through line 106 to transistor Q15, turns on the latter. With transistor Q15 on, its emitter-follower drives the power transistor Q16 which forms one-half of the positive side of the bridge. The Baker-clamped driver 66 provides a voltage at the base of transistor Q12 which is sufficient to drive the power MOSFET Q13 which forms one part of the

other side of the bridge. A circuit is thus completed which connects the coil 10 across the power supply, +V, -V, which can be traced as follows: from +V through transistor Q16, coil 10, MOSFET Q13 and transistor Q12 to -V. The voltages denoted by +V and -V are selected in accordance with switching time requirements of the application. +Vcc is a voltage appropriate to the logic devices employed.

The voltage sensor 16 outputs a voltage which is the absolute sum of the voltage on lines 11 and 13 referenced to ground. This absolute voltage is delivered to the integrator 14 which commences charging the capacitor 42. The integrator 14 supplies an output signal to the window comparator 12 which is a voltage/time product, i.e. the voltage applied across the coil 10 as a function of time. The comparator 12 compares the voltage time product supplied by the integrator 14 with the DC signal supplied by the D/A converter 20. When the voltage time product exceeds the value of the DC voltage signal supplied by the D/A converter 20, a signal is delivered through one of the comparators 28, 30 and OR gate 36 to one input of AND gate 34. At this point, the second input to AND gate 34 consisting of the reset enable signal is high, consequently a high signal is output from the AND gate 34 which functions to reset the flip-flop 58 through OR gate 84 connected by the line labled TERMINATE. The enabling signal output from the flip-flop 58 is removed, thereby turning off the bridge. During this turn-off phase, the positive side of the bridge turns off slowly but the output of the Baker-clamped driver 66 drops quickly. The emitter follower of transistor Q12 removes the stored charge on the

gate of the MOSFET 13 causing the latter to turn off quickly to leave a precisely metered amount of flux in the ferrite core of the phase shifter. Variables such as rise time, voltage variations in the power supply and temperature variations are taken into consideration by the voltage sensor 16 and the integrator 14. In the invention, the voltage across the coil 10 is not required to be constant over time as in prior techniques but an integration of voltage over time is used. Therefore, the amount of flux applied to the ferrimagnetic load by the coil is independent of the above-mentioned variations. The back EMF spike produced across the coil 10 is dissipated into a snubbing capacitor C_{snub} via diodes 100, 102. The accumulated charge on C_{snub} is removed by an external shunt regulator, V_{snub}.

During the reset mode, a high reset enable signal is inverted to a low signal by inverter 32, thereby disabling the output of AND gate 34. With AND gate 34 disabled, the window comparator 12 is likewise disabled, thus the flip-flops 58, 60 cannot be reset by the output of AND gate 34. In the reset mode, a start signal is delivered to the set input of one of the flip-flops 58, 60. For example, if a start signal is delivered to the set input of flip-flop 58, the positive side of the bridge will be turned on resulting in current flow in one direction through the coil 10. The current through the coil 10 increases until the voltage across resistor 96 (R_{sense}) exceeds a reset reference voltage on the inverting input of comparator 86. When this latter-mentioned reset reference voltage is exceeded, a signal is delivered from the output of comparator 86 through OR gate 84 to the reset input of flip-flop 58, the reset reference voltage on the inverting

input of comparator 86 is such as to assure that the current through coil 10 during the reset cycle is sufficient to saturate the ferrite. This voltage is determined by resistors 92 and 94 which provide a voltage divider. It should be noted here that the current sensor 68 functions as a protective circuit to limit the magnitude of current flowing through the coil 10, even during the set cycle with the window comparator 12 enabled.

In order to set the ferrite in preparation for a receive mode, the start signal is delivered to the set input of flip-flop 60, rather than flip-flop 58. In response to a negative start signal, an output signal is delivered on line 108 to the Baker-clamped driver 98, and through the buffering transistor Q4 to the base of transistor Q5. Transistor Q5 drives transistor Q6 so that current flows from -V through transistors Q2, Q3, the coil 10 and transistor Q6 to +V.

Having thus described the invention, it is recognized that those skilled in the art may make various modifications or additions to the preferred embodiment chosen to illustrate the invention without departing from the spirit and scope of the present contribution to the art. Accordingly, it is to be understood that the protection sought and to be afforded hereby should be deemed to extend to the subject matter claimed and all equivalents thereof fairly within the scope of the invention.

CLAIMS

What is claimed is:

1. An apparatus for controlling the amount of magnetic energy imparted to a ferrimagnetic material, wherein a source of electrical power is applied to a load device (10) which generates magnetic energy and which applies said magnetic energy to said ferrimagnetic material, said apparatus controlling said source of electrical power and characterized in that it comprises:

sensing means (16) for sensing the voltage across said load device (10) and for producing an output voltage signal proportional to the sensed voltage;

integration means (14) responsive to said sensing means (16) for integrating said output voltage signal as a function of time and for producing a time integrated voltage signal;

reference means (18, 20) for generating a reference signal proportional to a preselected amount of magnetic energy to be imparted to said ferrimagnetic material;

comparison means (12) for comparing said time integrated voltage signal with said reference signal; and

control means (58, 60) responsive to said comparison means (12) for controlling the application of electrical power to said load device (10).

2. An apparatus according to Claim 1, characterized in that said integration means includes capacitive means (42) for accumulating a charge proportional to the time that the output voltage signal is applied thereto.

3. An apparatus according to any preceding claim, characterized in that said reference means (18, 20) receives a multibit digital reference word representative of said preselected amount of magnetic energy, and includes storage means (18) for storing said digital reference word, and converting means (20) for converting said multibit digital data reference word into an analog reference signal for output to said comparison means (12).

4. An apparatus according to any preceding claim, characterized in that said apparatus further comprises a second sensing means (68) for sensing the current flowing through said load device (10); and further characterized in that said control means (58,60) is responsive to said second sensing means (68) for controlling the application of electrical power to said load device (10).

5. An apparatus according to Claim 4, characterized in that said second sensing means (68) delivers a disabling control signal to said control means (58, 60) when the sensed current exceeds a preselected value and further characterized in that said control means (58, 60) terminates the current to the load device (10) in response to said disabling control signal.

6. An apparatus according to any preceding claim, characterized in that said sensing means (16) includes a difference amplifier (48) for measuring the difference in voltage of each side of said load device (10) with respect to a preselected value, said output voltage signal being defined by said voltage difference.

7. An apparatus according to any preceding claim, characterized in that said comparison means (12) compares the time integrated voltage signal with the reference signal and produces a disabling signal when the time integrated voltage signal value reaches the value of said reference signal, said control means (58, 60) being responsive to said disabling signal for controlling the application of the electrical power source to the load device (10).

8. An apparatus according to any preceding claim, characterized in that said apparatus further comprises switch means for selectively coupling said load device (10) with said power source in either of two polarities such that current flows through said load device (10) in either of two opposite directions as switched.

9. An apparatus according to any preceding claim, characterized in that:

said apparatus further comprises switch means for selectively coupling said load device (10) with said power source in either of two polarities such that current flows through said load device (10) in either of first or second, opposite directions as switched;

said switch means couples said source of electrical power to said load device (10) in one polarity such that electrical current may be conducted through said load device (10) in the corresponding first direction until said ferrimagnetic element is substantially saturated;

said switch means couples said source of electrical power to said load device (10) in the second polarity such that electrical current may be conducted

through said load device (10) in the corresponding second direction;

said sensing means (16) senses the value of voltage across said load device (10) while current is being conducted in said second direction and produces said output voltage signal in response;

said integration means integrates said output voltage signal over time, the time integrated voltage signal being proportional to the amount of magnetic flux imparted to said ferrimagnetic material;

said comparison means compares the time integrated voltage signal with the reference signal and in the event that the time integrated voltage signal reaches the value of said reference signal, said comparison means (12) produces a disabling signal; and,

said control means being responsive to said disabling signal to terminate the conduction of electrical current in said second direction.

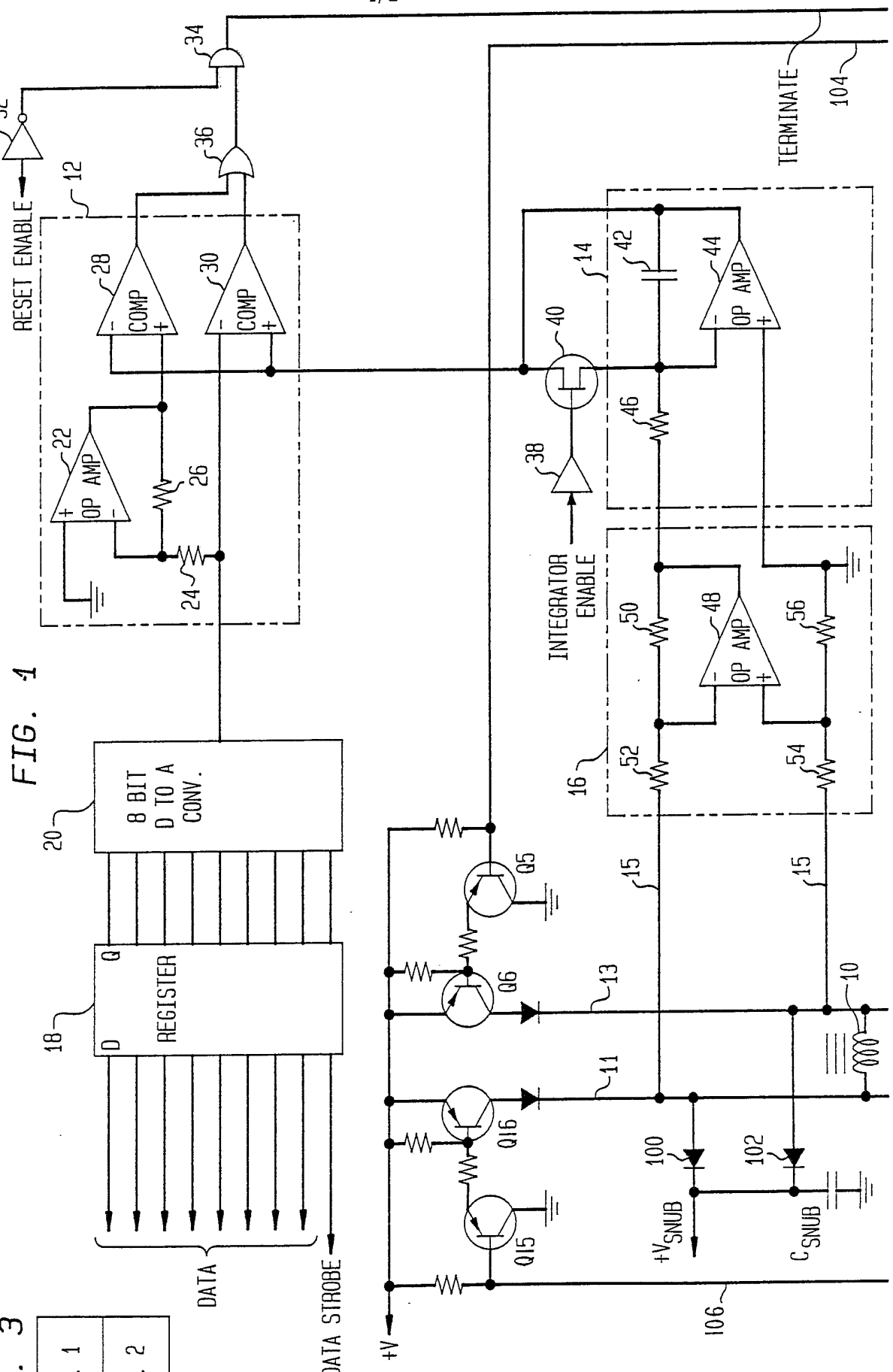


FIG. 1

FIG. 3

FIG. 1	FIG. 2

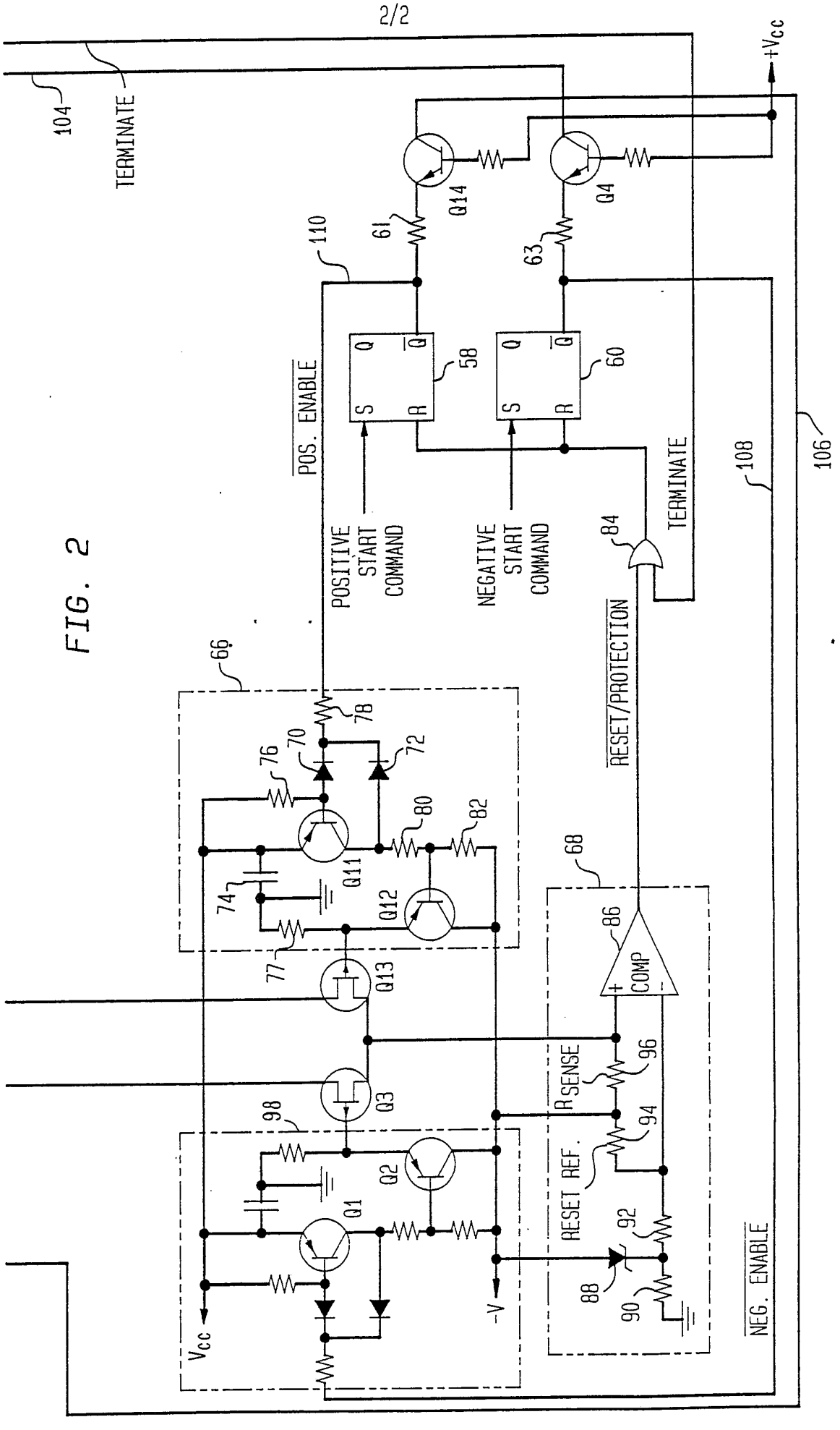

104
TERMINATE
+Vcc
Q14
Q4
61
63
110
POS. ENABLE
58
60
Q
S
R
POSITIVE START COMMAND
NEGATIVE START COMMAND
84
TERMINATE
108
106
RESET/PROTECTION
66
78
70
72
76
80
82
Q11
Q12
74
77
Q13
68
86
COMP
Q3
98
RSENSE
96
94
Q2
Q1
RESET REF.
92
88
90
Vcc
-V
NEG. ENABLE

FIG. 2

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/01591

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) *

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: G 05 F 7/00; H 03 K 17/64; H 03 K 17/66

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	G 05 F; H 03 K

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT *

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No [13]
X	US, A, 3626425 (STRENGLEIN) 7 December 1971, see figures 1,2; abstract; column 1, line 64 - column 2, line 33; column 3, lines 28-44; column 3, line 57 - column 4, line 30	1,3,6,7,8, 9
A	--	2,4,5
X	US, A, 3510675 (JOHNSON et al.) 5 May 1970, see column 1, line 64 - column 2, line 9; column 2, line 40 - column 3, line 23; column 4, lines 68-74	1,2,4,5-9
A	-- US, A, 3521079 (KUCK) 21 July 1970, see column 2, line 56 - column 4, line 72	1-9

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* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
30th September 1987	26 OCT 1987
International Searching Authority	Signature of Authorized Officer
EUROPEAN PATENT OFFICE	M. VAN MOL

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 87/01591 (SA 17954)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 09/10/87

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 3626425	07/12/71	None	
US-A- 3510675	05/05/70	None	
US-A- 3521079	21/07/70	None	