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CA 2817467 C 2015/11/24

(11)(21) **2 817 467**

(12) BREVET CANADIEN / CANADIAN PATENT

(13) **C**

(86) **Date de dépôt PCT/PCT Filing Date:** 2011/06/03
(87) **Date publication PCT/PCT Publication Date:** 2011/11/24
(45) **Date de délivrance/Issue Date:** 2015/11/24
(85) **Entrée phase nationale/National Entry:** 2013/05/09
(86) **N° demande PCT/PCT Application No.:** CN 2011/075252
(87) **N° publication PCT/PCT Publication No.:** 2011/144170
(30) **Priorité/Priority:** 2010/11/10 (CN201010538671.5)

(51) **Cl.Int./Int.Cl.** ***H03M 13/11*** (2006.01)

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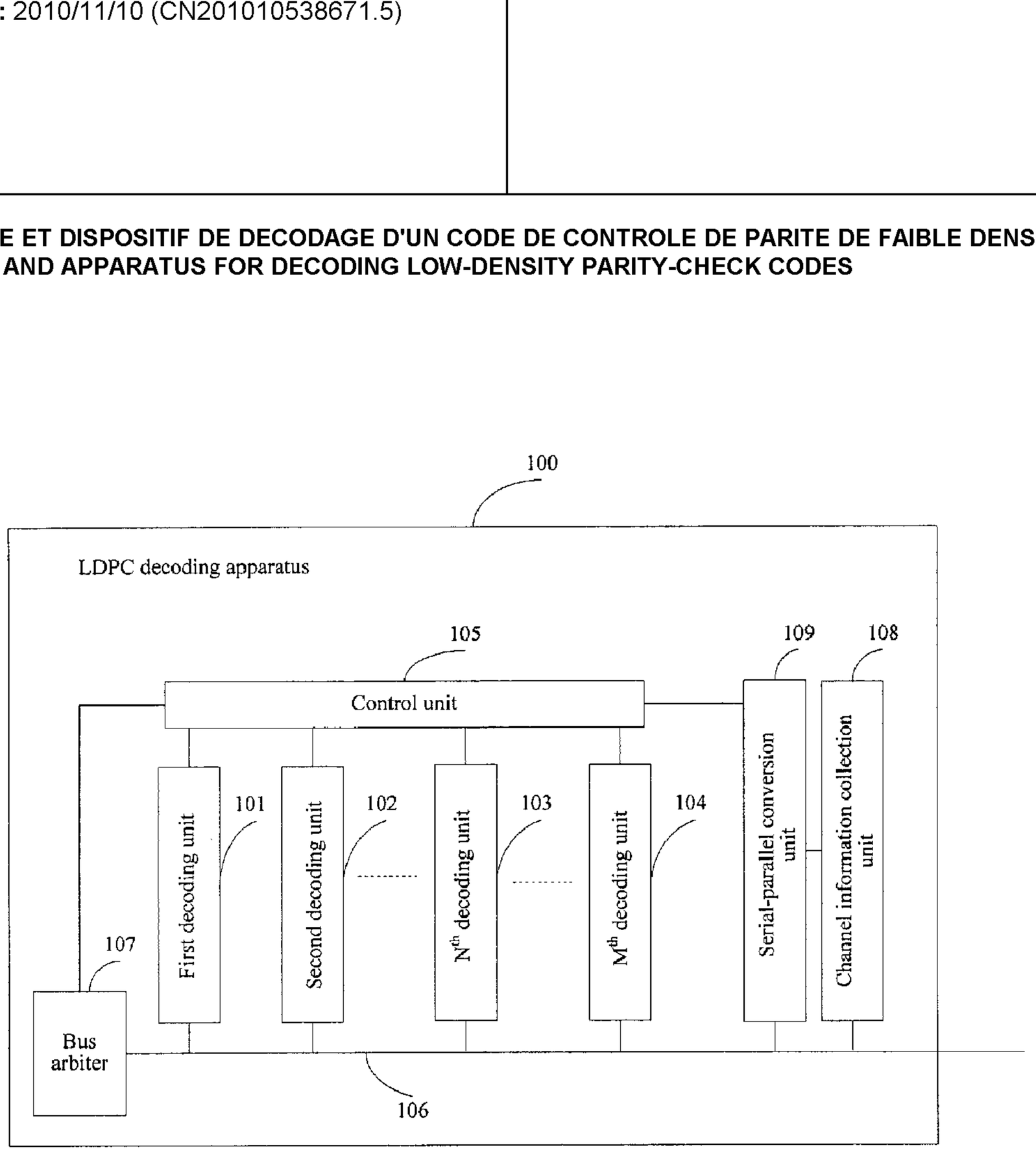
(54) **Titre : PROCEDE ET DISPOSITIF DE DECODAGE D'UN CODE DE CONTROLE DE PARITE DE FAIBLE DENSITE**
(54) **Title: METHOD AND APPARATUS FOR DECODING LOW-DENSITY PARITY-CHECK CODES**



(57) **Abrégé/Abstract:**
A method and an apparatus for decoding low-density parity-check codes are provided. The method includes the following: A first decoding unit performs decoding computation on a first code word from a second time period to an O^{th} time period; a second

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(57) **Abrégé(suite)/Abstract(continued):**
decoding unit performs decoding computation on a second code word from a third time period to an $(O+1)^{th}$ time period; an N^{th} decoding unit performs decoding computation on an N^{th} code word from an $(N+1)^{th}$ time period to an $(N+O-1)^{th}$ time period; and an M^{th} decoding unit performs decoding computation on an M^{th} code word from an $(M+1)^{th}$ time period to an $(M+O-1)^{th}$ time period. Each decoding unit may perform decoding computation in multiple time periods, so that the iteration time of decoding computation is adjusted according to a decoding algorithm and the channel status, and the number of iterations is thereby effectively increased to ensure the decoding performance.

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ABSTRACT

A method and an apparatus for decoding low-density parity-check codes are provided. The method includes the following: A first decoding unit performs decoding computation on a first code word from a second time period to an O^{th} time period; a second decoding unit performs decoding computation on a second code word from a third time period to an $(O+1)^{th}$ time period; an N^{th} decoding unit performs decoding computation on an N^{th} code word from an $(N+1)^{th}$ time period to an $(N+O-1)^{th}$ time period; and an M^{th} decoding unit performs decoding computation on an M^{th} code word from an $(M+1)^{th}$ time period to an $(M+O-1)^{th}$ time period. Each decoding unit may perform decoding computation in multiple time periods, so that the iteration time of decoding computation is adjusted according to a decoding algorithm and the channel status, and the number of iterations is thereby effectively increased to ensure the decoding performance.

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METHOD AND APPARATUS FOR DECODING LOW-DENSITY PARITY-CHECK CODES

FIELD OF THE INVENTION

[0001] The present invention relates to the field of communications technologies, and in particular, to a method and an apparatus for decoding low-density parity-check codes.

BACKGROUND OF THE INVENTION

[0002] A purpose of a communication system is to rapidly, reliably and sometimes securely transmit information from a source to a desination. The source has many forms, such as voice, data, image and video. In the communication system, there are many types of channels for transmitting information, including a mobile communication channel, a satellite communication channel, an optical fiber communication channel, an underwater acoustic communication channel, an infrared communication channel, a copper cable transmitting channel and a data storage channel. Generally, noises and interferences of different levels are usually brought into the channels, thereby lowering the accuracy of the information. In order to resist the noises and interferences, channel coding technologies may be adopted. In brief, the channel coding is to add redundant information to original information at a sending end according to a certain rule, and at a receiving end by using the redundant information, correct errors brought by the channel noises; therefore, the channel coding is also called correction coding.

[0003] Low-density parity-check (Low-density parity-check, LDPC) is a coding and decoding scheme that has the performance close to the Shannon limit and can be implemented.

[0004] The LDPC decoding incluedes three steps, that is, storage, decoding computation and outputting. A first code word is stored and then decoding computation is performed on the first code. The decoding computation of the first code word is ended after a second code word is stored, and the decoding computation of the second code word is then started. The decoding computation time of the first code word is the same as the storage time

of the second code word. Assuming it takes 5000 clock cycles to store a code word and takes 500 clock cycles to finish a decoding iteration in the decoding computation, 10 decoding iterations may be completed, and the performance of the decoding computation is closely related to the number of iterations.

SUMMARY OF THE INVENTION

[0005] Embodiments of the present invention provide a method and an apparatus for decoding low-density parity-check codes, which can significantly improve the decoding performance of the low-density parity-check and increase the number of decoding iteration.

[0006] An embodiment of the present invention provides a method for decoding low-density parity-check codes, where a decoding apparatus includes M decoding units, and M is a natural number greater than 1. The method includes:

storing, by a first decoding unit, a first code word in a first time period;

storing, by a second decoding unit, a second code word in a second time period;

storing, by an N^{th} decoding unit, an N^{th} code word in an N^{th} time period, where N is a natural number that is greater than or equal to 1 and smaller than M;

storing, by an M^{th} decoding unit, an M^{th} code word in an M^{th} time period;

performing, by the first decoding unit, decoding computation on the first code word from the second time period to the O^{th} time period, where O is a natural number greater than 3, wherein when a channel rate is reduced, a value of O is increased, when the channel rate is increased, the value of O is reduced;

performing, by the second decoding unit, decoding computation on the second code word from the third time period to the $(O+1)^{th}$ time period;

performing, by the N^{th} decoding unit, decoding computation on the N^{th} code

word from the $(N+1)^{th}$ time period to the $(N+O-1)^{th}$ time period;

performing, by the M^{th} decoding unit, decoding computation on the M^{th} code word from the $(M+1)^{th}$ time period to the $(M+O-1)^{th}$ time period;

outputting, by the first decoding unit, the decoded first code word in the $(1+O)^{th}$ time period;

outputting, by the second decoding unit, the decoded second code word in the $(2+O)^{th}$ time period;

outputting, by the N^{th} decoding unit, the decoded N^{th} code word in the $(N+O)^{th}$ time period; and

outputting, by the M^{th} decoding unit, the decoded M^{th} code word in the $(M+O)^{th}$ time period.

[0007] An embodiment of the present invention provides an apparatus for decoding low-density parity-check codes, where the decoding apparatus includes M decoding units, and M is a natural number greater than 1. The apparatus includes:

a first decoding unit, configured to store a first code word in a first time period;

a second decoding unit, configured to store a second code word in a second time period;

an N^{th} decoding unit, configured to store an N^{th} code word in an N^{th} time period, where N is a natural number that is greater than or equal to 1 and smaller than M;

an M^{th} decoding unit, configured to store an M^{th} code word in an M^{th} time period;

the first decoding unit, configured to perform decoding computation on the first code word from the second time period to the O^{th} time period, where O is a natural number greater than 3;

the second decoding unit, configured to perform decoding computation on the second code word from the third time period to the $(O+1)^{th}$ time period;

the N^{th} decoding unit, configured to perform decoding computation on the N^{th} code word from the $(N+1)^{th}$ time period to the $(N+O-1)^{th}$ time period;

the M^{th} decoding unit, configured to perform decoding computation on the M^{th} code word from the $(M+1)^{th}$ time period to the $(M+O-1)^{th}$ time period;

the first decoding unit, configured to output the decoded first code word in the $(1+O)^{th}$ time period;

the second decoding unit, configured to output the decoded second code word in the $(2+O)^{th}$ time period;

the N^{th} decoding unit, configured to output the decoded N^{th} code word in the $(N+O)^{th}$ time period;

the M^{th} decoding unit, configured to output the decoded M^{th} code word in the $(M+O)^{th}$ time period; and

a control unit, configured to contol the M decoding units to perform storage, decoding computation and outputting, when a channel rate is reduced, a value of O is increased, when the channel rate is increased, the value of O is reduced.

[0008] In the embodiment of the present invention, the first decoding unit stores the first code word in the first time period; the second decoding unit stores the second code word in the second time period; the N^{th} decoding unit stores the N^{th} code word in the N^{th} time period, where N is a natural number that is greater than or equal to 1 and smaller than M; the M^{th} decoding unit stores the M^{th} code word in the M^{th} time period; the first decoding unit performs decoding computation on the first code word from the second time period to the O^{th} time period, where O is a natural number greater than 3; the second decoding unit performs decoding computation on the second code word from the third time period to the $(O+1)^{th}$ time period; the N^{th} decoding unit performs decoding computation on the N^{th} code word from the

$(N+1)^{th}$ time period to the $(N+O-1)^{th}$ time period; the M^{th} decoding unit performs decoding computation on the M^{th} code word from the $(M+1)^{th}$ time period to the $(M+O-1)^{th}$ time period; the first decoding unit outputs the decoded first code word in the $(1+O)^{th}$ time period; the second decoding unit outputs the decoded second code word in the $(2+O)^{th}$ time period; the N^{th} decoding unit outputs the decoded N^{th} code word in the $(N+O)^{th}$ time period; and the M^{th} decoding unit outputs the decoded M^{th} code word in the $(M+O)^{th}$ time period. Each decoding unit may perform decoding computation in (O-1) time periods. The decoding computation time of the code word is greater than the storage time of the code word, which may increase the number of decoding iterations. Meanwhile, the iteration time of decoding computation may be adjusted according to a decoding algorithm and the channel status. When the channel rate is reduced, the value of O is increased, and thereby the decoding computation time is shortened and the number of decoding iterations is increased to improve the performance of decoding iteration. When the channel rate is increased, the value of O is reduced, to ensure that the decoding iteration can be completed in time. Multiple decoding units may work simultaneously without interfering with each other, and thereby the processing quantity of data is effectively increased, so that the decoding rate may meet the current demand for rapid expansion of the network bandwidth.

BRIEF DESCRIPTION OF THE DRAWING

[0009] To illustrate the technical solutions according to the embodiments of the present invention or in the prior art more clearly, the accompanying drawings for describing the embodiments or the prior art are introduced briefly in the following. Apparently, the accompanying drawings in the following description are only some embodiments of the present invention, and persons of ordinary skill in the art can derive other drawings from the accompanying drawings without creative efforts.

[0010] FIG. 1 is a structural diagram of an apparatus for decoding low-density parity-check codes according to an embodiment of the present invention;

[0011] FIG. 2 is a structural diagram of a first decoding unit according to an embodiment of the present invention;

[0012] FIG. 3 is a structural diagram of a first decoding unit and an N^{th} decoding unit according to an embodiment of the present invention; and

[0013] FIG. 4 is a structural diagram of another apparatus for decoding low-density parity-check codes according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0014] The technical solutions of the present invention will be clearly and completely described in the following with reference to the accompanying drawings. It is obvious that the embodiments to be described are only a part rather than all of the embodiments of the present invention. All other embodiments obtained by persons of ordinary skill in the art based on the embodiments of the present invention without creative effects shall fall within the protection scope of the present invention.

[0015] As shown in FIG. 1, an embodiment of the present invention provides an apparatus 100 for decoding low-density parity-check codes, where the decoding apparatus 100 includes M decoding units, and M is a natural number greater than 1. The apparatus includes:

a first decoding unit 101, configured to store a first code word in a first time period;

a second decoding unit 102, configured to store a second code word in a second time period;

an N^{th} decoding unit 103, configured to store an N^{th} code word in an N^{th} time period, where N is a natural number that is greater than or equal to 1 and smaller than M;

an M^{th} decoding unit 104, configured to store an M^{th} code word in an M^{th} time period;

the first decoding unit 101, configured to perform decoding computation on the first code word from the second time period to the O^{th} time period, where O is a natural number greater than 3;

the second decoding unit 102, configured to perform decoding computation on the second code word from the third time period to the $(O+1)^{th}$ time period;

the N^{th} decoding unit 103, configured to perform decoding computation on the N^{th} code word from the $(N+1)^{th}$ time period to the $(N+O-1)^{th}$ time period;

the M^{th} decoding unit 104, configured to perform decoding computation on the M^{th} code word from the $(M+1)^{th}$ time period to the $(M+O-1)^{th}$ time period;

the first decoding unit 101, configured to output the decoded first code word in the $(1+O)^{th}$ time period;

the second decoding unit 102, configured to output the decoded second code word in the $(2+O)^{th}$ time period;

the N^{th} decoding unit 103, configured to output the decoded N^{th} code word in the $(N+O)^{th}$ time period; and

the M^{th} decoding unit 104, configured to output the decoded M^{th} code word in the $(M+O)^{th}$ time period.

[0016] As shown in FIG. 1, the LDPC decoding apparatus in this embodiment may further include:

a control unit 105, configured to control the M decoding units to perform storage, decoding computation and outputting;

a bus 106, configured to transmit the first code word, the second code word, the N^{th} code word and the M^{th} code word, and input the first code word, the second code word, the N^{th} code word and the M^{th} code word to the M decoding units; and further configured to receive the decoded first code word, the decoded second code word, the decoded N^{th} code word and the decoded M^{th} code word that are output by the M decoding units, and transmit the decoded first code word, the decoded second code word, the decoded N^{th} code word and the decoded M^{th} code word; and

a bus arbiter 107, configured to control the M decoding units to use the bus.

[0017] As shown in FIG. 1, the LDPC decoding apparatus in this embodiment may further include:

a channel information collection unit 108, configured to collect channel information; and

a serial-parallel conversion unit 109, configured to adjust a serial-parallel conversion rate according to the channel information, and input the code word to the bus according to the serial-parallel conversion rate.

[0018] The control unit 105 is further configured to control, according to the serial-parallel conversion rate, the M decoding units to perform storage, decoding computation and outputting.

[0019] The use of the channel information collection unit 108 and the serial-parallel conversion unit 109 enables the LDPC decoding apparatus 100 to be adaptive to a change of the channel rate. For example, previously the channel condition is not good and the data input in parallel is 64 bits, and when the channel information collection unit finds that the channel status turns good, the data input in parallel may be adjusted into 128 bits, so that the throughput of the LDPC decoding apparatus 100 is doubled. Since microwave channels are more greatly influenced by factors such as the environment and the weather, this embodiment may solve the problem and adapt to the microwave channel condition.

[0020] In this embodiment, as shown in FIG. 1, the control unit 105 is connected to each decoding unit, connected to the bus arbiter 107, and connected to the serial-parallel conversion unit 109; and the serial-parallel conversion unit 109 is connected to the channel information collection unit 108. In other embodiments, information exchange between the control unit 105, the bus arbiter 107, the channel information collection unit 108 and the serial-parallel conversion unit 109 is implemented through the bus 106.

[0021] This embodiment may further include a monitoring unit (not shown in the

drowing) configured to: monitor decoding computation of the M decoding units, and if the monitored decoding result is correct, stop the decoding computation. In the embodiment of the present invention, the monitoring unit may be integrated in each decoding unit or integrated in the control unit, and may also act as an independent unit to monitor each decoding unit. The monitoring unit is set to greatly reduce the power consumption of the system, so as to achieve green communication without affecting the decoding performance.

[0022] As shown in FIG. 2, the first decoding unit 101 provided in the embodiment of the present invention includes:

a storing unit 201, configured to store a first code word in a first time period;

a decoding computation unit 202, configured to perform decoding computation on the first code word from the second time period to the O^{th} time period, where O is a natural number greater than 3; and

an output unit 203, configured to output the decoded first code word in the $(1+O)^{th}$ time period.

[0023] Each decoding unit may adopt the foregoing structure.

[0024] The output unit 203 is substantially a storing unit, and generally the storing unit 201 and the output unit 203 of a same decoding unit may not work at the same time. In order to reduce the cost and achieve green communication, the storing unit 201 and the output unit 203 may be integrated into one unit, and implement the storage and the output operation seperately in different time periods.

[0025] In some time periods, the decoding computation unit 202 does not work, and in order to make full use of the precious computing resources, different decoding units may use a same decoding computation unit in different time periods.

[0026] As shown in FIG. 3, a schematic diagram showing that the first decoding unit 101 and the N^{th} decoding unit 103 share the decoding computation unit 303 is given.

[0027] The storing unit and the output unit of the first decoding unit 101 are integrated into one unit, that is, a storage output unit 301, configured to store a first code word in a first time period and output the decoded first code word in the $(1+O)^{th}$ time period.

[0028] The storing unit and the output unit of the N^{th} decoding unit 102 are integrated into one unit, that is, a storage output unit 302, configured to store an N^{th} code word in an N^{th} time period and output the decoded N^{th} code word in the $(N+O)^{th}$ time period.

[0029] In this embodiment, each decoding unit may perform decoding computation in multiple time periods, so that the iteration time of decoding computation may be adjusted according to a decoding algorithm and the channel status, and thereby the number of iterations may be effectively increased to ensure the decoding performance. Multiple decoding units may work simultaneously without interfering with each other, and thereby the processing quantity of data may be effectively increased, so that the decoding rate can meet the current demand for rapid expansion of the network bandwidth.

[0030] As shown in FIG. 4, an embodiment of the present invention provides an apparatus 400 for decoding low-density parity-check codes, where in this embodiment, the decoding apparatus 400 includes four decoding units, including:

a first decoding unit 401, configured to store a first code word in a first time period;

a second decoding unit 402, configured to store a second code word in a second time period;

a third decoding unit 403, configured to store a third code word in a third time period;

a fourth decoding unit 404, configured to store a fourth code word in a fourth time period;

the first decoding unit 401, configured to perform decoding computation on the first code word from the second time period to the O^{th} time period, where O is a natural

number greater than 3;

the second decoding unit 402, configured to perform decoding computation on the second code word from the third time period to the $(O+1)^{th}$ time period;

the third decoding unit 403, configured to perform decoding computation on the third code word from the fourth time period to the $(O+2)^{th}$ time period;

the fourth decoding unit 404, configured to perform decoding computation on the fourth code word from the fifth time period to the $(O+3)^{th}$ time period;

the first decoding unit 401, configured to output the decoded first code word in the $(O+1)^{th}$ time period;

the second decoding unit 402, configured to output the decoded second code word in the $(O+2)^{th}$ time period;

the third decoding unit 403, configured to output the decoded third code word in the $(O+3)^{th}$ time period; and

the fourth decoding unit 404, configured to output the decoded fourth code word in the $(O+4)^{th}$ time period.

[0031] Table 1 shows the working status of the decoding apparatus 400 when O=3.

T	2T	3T	4T	5T
the decoding unit 1 writes	the decoding unit 1 computes	the decoding unit 1 computes	the decoding unit 1 outputs	the decoding unit 1 writes
the decoding unit 2 is idle	the decoding unit 2 writes	the decoding unit 2 computes	the decoding unit 2 computes	the decoding unit 2 outputs
the decoding unit 3 is idle	the decoding unit 3 is idle	the decoding unit 3 writes	the decoding unit 3 computes	the decoding unit 3 computes
the decoding unit 4 is idle	the decoding unit 4 is idle	the decoding unit 4 is idle	the decoding unit 4 writes	the decoding unit 4 computes

6T	7T
the decoding unit 1 computes	the decoding unit 1 computes
the decoding unit 2 writes	the decoding unit 2 computes
the decoding unit 3 outputs	the decoding unit 3 writes
the decoding unit 4 computes	the decoding unit 4 outputs

Table 1

[0032] After the decoding starts, data enters the LDPC decoding unit 1 for storage. After one code word is fully stored, the LDPC decoding computation is performed, and meanwhile the storage of the LDPC decoding unit 2 is performed. After one code word is

fully stored, the LDPC decoding computation is performed, and meanwhile the storage of the LDPC decoding unit 3 is performed... The rest can be deduced in the same manner. After the LDPC decoding unit 4 is fully stored, the LDPC decoding unit 1 completes output of the decoded code word, and can be used for storing an input code word. Through the above cycle operation, the storage and computation of the code words may be performed continuously, which improves the decoding performance and also ensures high data traffic.

[0033] Table 2 shows the working status of the decoding apparatus 400 when O=3. In this embodiment, the decoding unit 1 includes a storing unit 1, the decoding unit 2 includes a storing unit 2, the decoding unit 3 includes a storing unit 3, and the decoding unit 4 includes a storing unit 4; the decoding unit 1 and the decoding unit 3 share a computation unit 1, and the decoding unit 2 and the decoding unit 4 share a computation unit 2. In Table 2, "the storing unit 1 writes" under 1T indicates that the first code word is stored in the first time period, "the storing unit 1 outputs" under 4T indicates that the decoded first code word is output in the fourth time period, "the storing unit 1 is working" under 2T and 3T indicates that the storing unit 1 needs to be used for work such as buffering when the computation unit 1 performs decoding computation, and "the storing unit 3 is working" under 4T and 5T indicates that the storing unit 3 needs to be used for work such as buffering when the computation unit 1 performs decoding computation. It can be seen that the decoding unit 1 uses the computation unit 1 to perform decoding computation in 2T and 3T, and the decoding unit 3 uses the computation unit 1 to perform decoding computation in 4T and 5T; this solution may effectively reduce the hardware resource.

T	2T	3T	4T	5T
the storing unit 1writes	the storing unit 1 is working	the storing unit 1 is working	the storing unit 1 outputs	the storing unit 1 writes
the storing unit 2 is idle	the storing unit 2 writes	the storing unit 2 is working	the storing unit 2 is working	the storing unit 2 outputs
the storing unit 3 is idle	the storing unit 3 is idle	the storing unit 3 writes	the storing unit 3 is working	the storing unit 3 is working

the storing unit 4 is idle	the storing unit 4 is idle	the storing unit 4 is idle	the storing unit 4 writes	the storing unit 4 is working
the computation unit 1 is idle	the computation unit 1 is working	the computation unit 1 is working	the computation unit 1 is working	the computation unit 1 is working
the computation unit 2 is idle	the computation unit 2 is idle	the computation unit 2 is idle	the computation unit 2 is working	the computation unit 2 is working

6T	7T
the storing unit 1 is working	the storing unit 1 is working
the storing unit 2 writes	the storing unit 2 is working
the storing unit 3 outputs	the storing unit 3 writes
the storing unit 4 is working	the storing unit 4 is working
the computation unit 1 is working	the computation unit 1 is working
the computation unit 2 is working	the computation unit 2 is working

Table 2

[0034] In this embodiment, each decoding unit may perform decoding computation in multiple time periods, so that the iteration time of decoding computation may be adjusted according to a decoding algorithm and the channel status, and thereby the number of iterations may be effectively increased to ensure the decoding performance. Multiple decoding units may work simultaneously without interfering with each other, and thereby the processing quantity of data is effectively increased, so that the decoding rate can meet the current demand

for rapid expansion of the network bandwidth.

[0035] An embodiment of the present invention provides a method for decoding low-density parity-check codes, where a decoding apparatus includes M decoding units, and M is a natural number greater than 1. The method includes:

storing, by a first decoding unit, a first code word in a first time period;

storing, by a second decoding unit, a second code word in a second time period;

storing, by an N^{th} decoding unit, an N^{th} code word in an N^{th} time period, where N is a natural number that is greater than or equal to 1 and smaller than M;

storing, by an M^{th} decoding unit, an M^{th} code word in an M^{th} time period;

performing, by the first decoding unit, decoding computation on the first code word from the second time period to the O^{th} time period, where O is a natural number greater than 3;

performing, by the second decoding unit, decoding computation on the second code word from the third time period to the $(O+1)^{th}$ time period;

performing, by the N^{th} decoding unit, decoding computation on the N^{th} code word from the $(N+1)^{th}$ time period to the $(N+O-1)^{th}$ time period;

performing, by the M^{th} decoding unit, decoding computation on the M^{th} code word from the $(M+1)^{th}$ time period to the $(M+O-1)^{th}$ time period;

outputting, by the first decoding unit, the decoded first code word in the $(1+O)^{th}$ time period;

outputting, by the second decoding unit, the decoded second code word in the $(2+O)^{th}$ time period;

outputting, by the N^{th} decoding unit, the decoded N^{th} code word in the $(N+O)^{th}$ time period; and

outputting, by the M^{th} decoding unit, the decoded M^{th} code word in the $(M+O)^{th}$ time period.

[0036] Before the storing, by the first decoding unit, the first code word in the first time period, the method further includes:

Inputting, by a bus, the first code word.

[0037] After the outputting, by the first decoding unit, the decoded first code word in the $(1+O)^{th}$ time period, the method further includes:

Outputting, by the bus, the decoded first code word.

[0038] Before the inputting, by the bus, the first code word, the method further includes:

adjusting, by a serial-parallel conversion unit, a serial-parallel conversion rate according to channel information, and inputting the first code word to the bus according to the serial-parallel conversion rate.

[0039] After the adjusting, by the serial-parallel conversion unit, the serial-parallel conversion rate according to the channel information, and inputting the first code word to the bus according to the serial-parallel conversion rate, the method further includes:

adjusting, by the control unit, the value of O according to the serial-parallel conversion rate.

[0040] The performing, by the first decoding unit, decoding computation on the first code word from the second time period to the O^{th} time period further includes:

monitoring, by a monitoring unit, a decoding result of the first decoding unit, and stopping the decoding computation when the decoding result is correct.

[0041] In this embodiment, each decoding unit may perform decoding computation in multiple time periods, so that the iteration time of decoding computation may adjusted according to a decoding algorithm and the channel status, and thereby the number of iterations may be effectively increased to ensure the decoding performance. Multiple decoding units may work simultaneously without interfering with each other, and thereby the processing quantity of data is effectively increased, so that the decoding rate can meet the current demand for rapid expansion of the network bandwidth. After the initialization of the LDPC decoder is completed, at a same moment, only one decoding unit is in a read status and one decoder unit is in a write status, and other decoder units are in a computation status.

[0042] The apparatus embodiments are merely exemplary. Units described as separate components may be or may not be physically separated. Components shown as units may be or may not be physical units, that is, may be integrated or may be distributed to multiple network units. Some or all of the modules may be selected to achieve the objective of the solution of the embodiment according to actual requirements. Persons of ordinary skill in the art can understand and make implementation without making creative efforts.

[0043] Through the above description of the implementation manners, persons skilled in the art can clearly understand that the implementation manners may be implemented through hardware, or through software plus a necessary universal hardware platform. Based on this understanding, the essence of technical solutions or the part that makes contributions to the prior art can be embodied in the form of a software product. The computer software product may be stored in a computer readable storage medium such as a ROM/RAM, a magnetic disk, or an optical disk, and include several instructions for instructing computer equipment (for example, a personal computer, a server, or network equipment) to perform the methods described in the embodiments of the present invention or in some parts of the embodiment of the present invention.

[0044] Finally, it should be noted that the foregoing embodiments are merely used for describing the technical solutions of the present invention, but not intended to limit the present invention. Although the present invention has been described in detail with reference to the foregoing embodiments, it should be understood by persons of ordinary skill in the art that:

modifications can be made to the technical solutions described in the foregoing embodiments, or equivalent replacements can be made to some technical features in the technical solutions, and such modifications or replacements do not cause the essence of corresponding technical solutions to depart from the scope of the present invention.

CLAIMS:

1. A method for decoding low-density parity-check codes, wherein a decoding apparatus comprises M decoding units, and M is a natural number greater than 1, the method comprising:

storing, by a first decoding unit, a first code word in a first time period;

storing, by a second decoding unit, a second code word in a second time period;

storing, by an N^{th} decoding unit, an N^{th} code word in an N^{th} time period, where N is a natural number that is greater than or equal to 1 and smaller than M;

storing, by an M^{th} decoding unit, an M^{th} code word in an M^{th} time period;

performing, by the first decoding unit, decoding computation on the first code word from the second time period to the O^{th} time period, where O is a natural number greater than 3, wherein when a channel rate is reduced, a value of O is increased, when the channel rate is increased, the value of O is reduced;

performing, by the second decoding unit, decoding computation on the second code word from the third time period to the $(O+1)^{th}$ time period;

performing, by the N^{th} decoding unit, decoding computation on the N^{th} code word from the $(N+1)^{th}$ time period to the $(N+O-1)^{th}$ time period;

performing, by the M^{th} decoding unit, decoding computation on the M^{th} code word from the $(M+1)^{th}$ time period to the $(M+O-1)^{th}$ time period;

outputting, by the first decoding unit, the decoded first code word in the $(1+O)^{th}$ time period;

outputting, by the second decoding unit, the decoded second code word in the $(2+O)^{th}$ time period;

outputting, by the N^{th} decoding unit, the decoded N^{th} code word in the $(N+O)^{th}$ time period; and

outputting, by the M^{th} decoding unit, the decoded M^{th} code word in the $(M+O)^{th}$ time period.

2. The decoding method according to claim 1, wherein

before the storing, by the first decoding unit, the first code word in the first time period, the method further comprises:

inputting, by a bus, the first code word; and

after the outputting, by the first decoding unit, the decoded first code word in the $(1+O)^{th}$ time period, the method further comprises:

outputting, by the bus, the decoded first code word.

3. The decoding method according to claim 2, wherein

before the inputting, by the bus, the first code word, the method further comprises:

adjustting, by a serial-parallel conversion unit, a serial-parallel conversion rate according to channel information, and inputting the first code word to the bus according to the serial-parallel conversion rate.

4. The decoding method according to claim 3, wherein

after the adjusting, by the serial-parallel conversion unit, the serial-parallel conversion rate according to the channel information, and inputting the first code word to the bus according to the serial-parallel conversion rate, the method further comprises:

adjusting, by the control unit, the value of O according to the serial-parallel conversion rate.

5. The decoding method according to claim 1, wherein

the performing, by the first decoding unit, decoding computation on the first code word from the second time period to the O^{th} time period further comprises:

monitoring, by a monitoring unit, a decoding result of the first decoding unit, and stopping the decoding computation when the decoding result is correct.

6. An apparatus for decoding low-density parity-check codes, wherein the decoding apparatus comprises M decoding units, and M is a natural number greater than 1, the apparatus comprising:

a first decoding unit, configured to store a first code word in a first time period;

a second decoding unit, configured to store a second code word in a second time period;

an N^{th} decoding unit, configured to store an N^{th} code word in an N^{th} time period, where N is a natural number that is greater than or equal to 1 and smaller than M;

an M^{th} decoding unit, configured to store an M^{th} code word in an M^{th} time period;

the first decoding unit, configured to perform decoding computation on the first code word from the second time period to the O^{th} time period, where O is a natural number greater than 3;

the second decoding unit, configured to perform decoding computation on the second code word from the third time period to the $(O+1)^{th}$ time period;

the N^{th} decoding unit, configured to perform decoding computation on the N^{th} code word from the $(N+1)^{th}$ time period to the $(N+O-1)^{th}$ time period;

the M^{th} decoding unit, configured to perform decoding computation on the M^{th} code word from the $(M+1)^{th}$ time period to the $(M+O-1)^{th}$ time period;

the first decoding unit, configured to output the decoded first code word in the $(1+O)^{th}$ time period;

the second decoding unit, configured to output the decoded second code word in the $(2+O)^{th}$ time period;

the N^{th} decoding unit, configured to output the decoded N^{th} code word in the $(N+O)^{th}$ time period;

the M^{th} decoding unit, configured to output the decoded M^{th} code word in the $(M+O)^{th}$ time period; and

a control unit, configured to control the M decoding units to perform storage, decoding computation and outputting, when a channel rate is reduced, a value of O is increased, when the channel rate is increased, the value of O is reduced.

7. The decoding apparatus according to claim 6, further comprising:

a bus, configured to transmit the first code word, the second code word, the N^{th} code word and the M^{th} code word, and input the first code word, the second code word, the N^{th} code word and the M^{th} code word to the M decoding units; and further configured to receive the decoded first code word, the decoded second code word, the decoded N^{th} code word and the decoded M^{th} code word that are output by the M decoding units, and transmit the decoded first code word, the decoded second code word, the decoded N^{th} code word and the decoded M^{th} code word; and

a bus arbiter, configured to control the M decoding units to use the bus.

8. The decoding apparatus according to claim 7, further comprising:

a channel information collection unit, configured to collect channel information; and

a serial-parallel conversion unit, configured to adjust a serial-parallel conversion rate according to the channel information, and input the code word to the bus according to the serial-parallel conversion rate,

wherein the control unit is further configured to control, according to the serial-parallel conversion rate, the M decoding units to perform storage, decoding computation and

outputting.

9. The decoding apparatus according to claim 6, wherein

the M decoding units respectively comprise a storing unit, a decoding computation unit and an output unit;

the storing unit is configured to store a code word;

the decoding computation unit is configured to perform decoding computation on the stored code word; and

the output unit is configured to output the code word after the decoding computation.

10. The decoding apparatus according to claim 9, wherein

the storing unit and the output unit of a same decoding unit are one unit used in different time periods.

11. The decoding apparatus according to claim 9, wherein

different decoding units use a same decoding computation unit in different time periods.

12. The decoding apparatus according to claim 6, further comprising:

a monitoring unit, configured to monitor decoding computation of the M decoding units, and if the monitored decoding result is correct, stop the decoding computation.

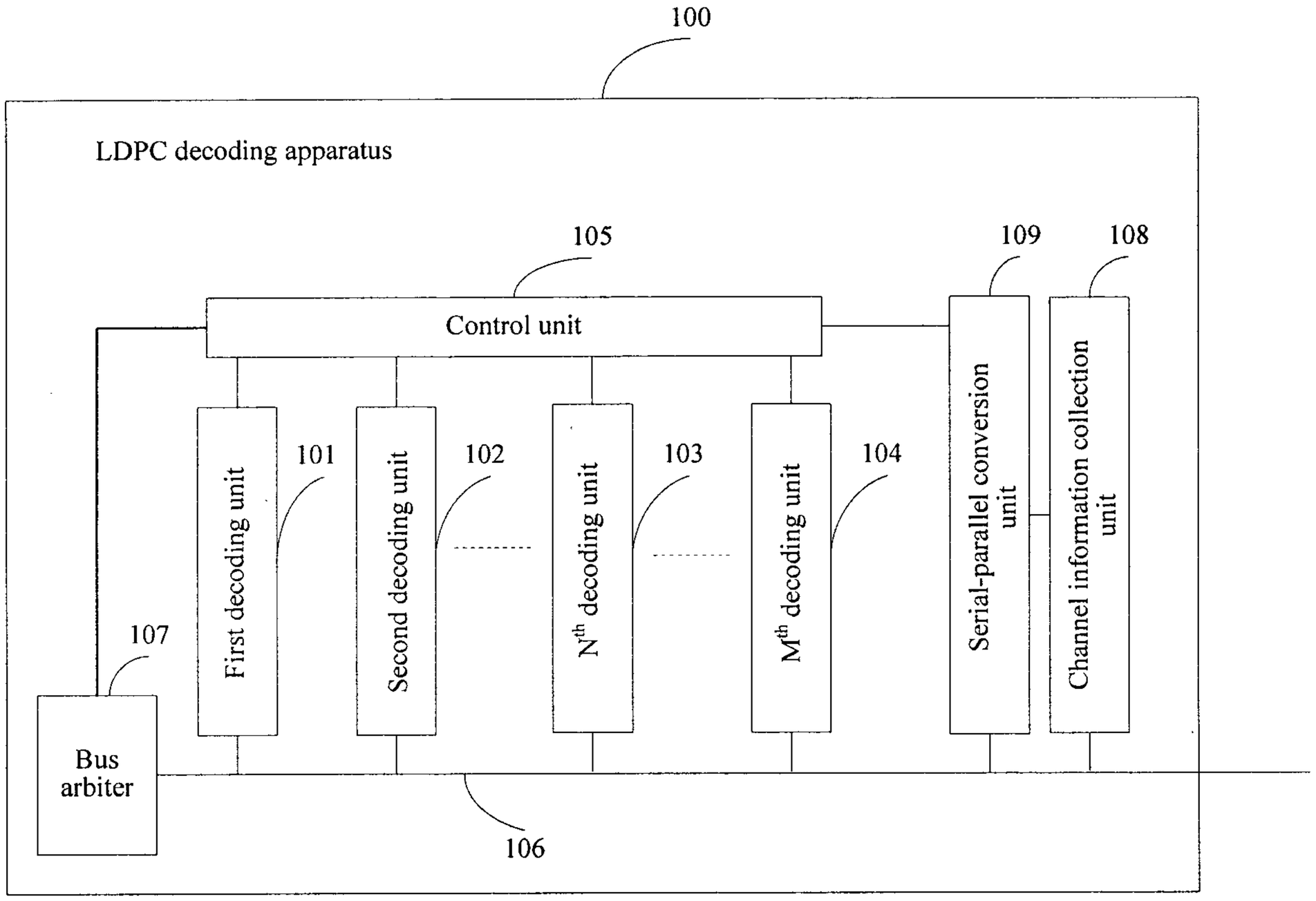

100
LDPC decoding apparatus
105
Control unit
109
Serial-parallel conversion unit
108
Channel information collection unit
First decoding unit
101
Second decoding unit
102
N^th decoding unit
103
M^th decoding unit
104
107
Bus arbiter
106

FIG. 1

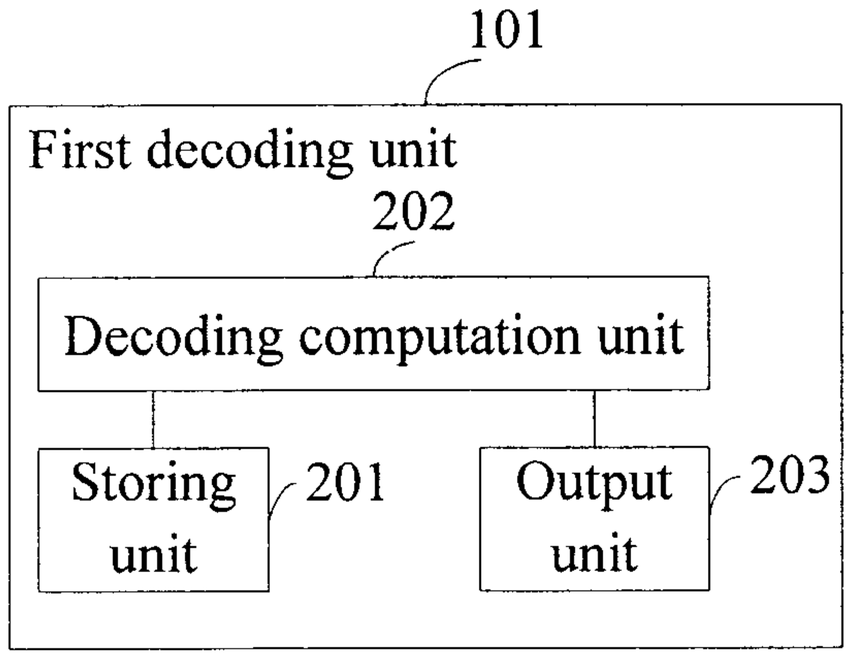

101
First decoding unit
202
Decoding computation unit
Storing unit
201
Output unit
203

FIG. 2

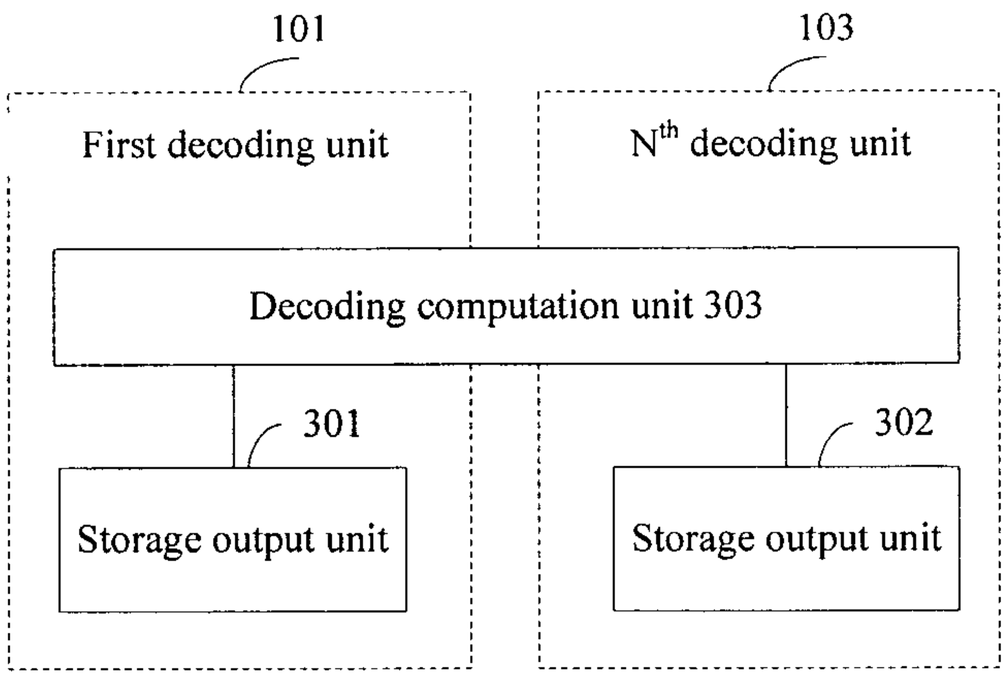

101
103
First decoding unit
N^th decoding unit
Decoding computation unit 303
301
302
Storage output unit
Storage output unit

FIG. 3

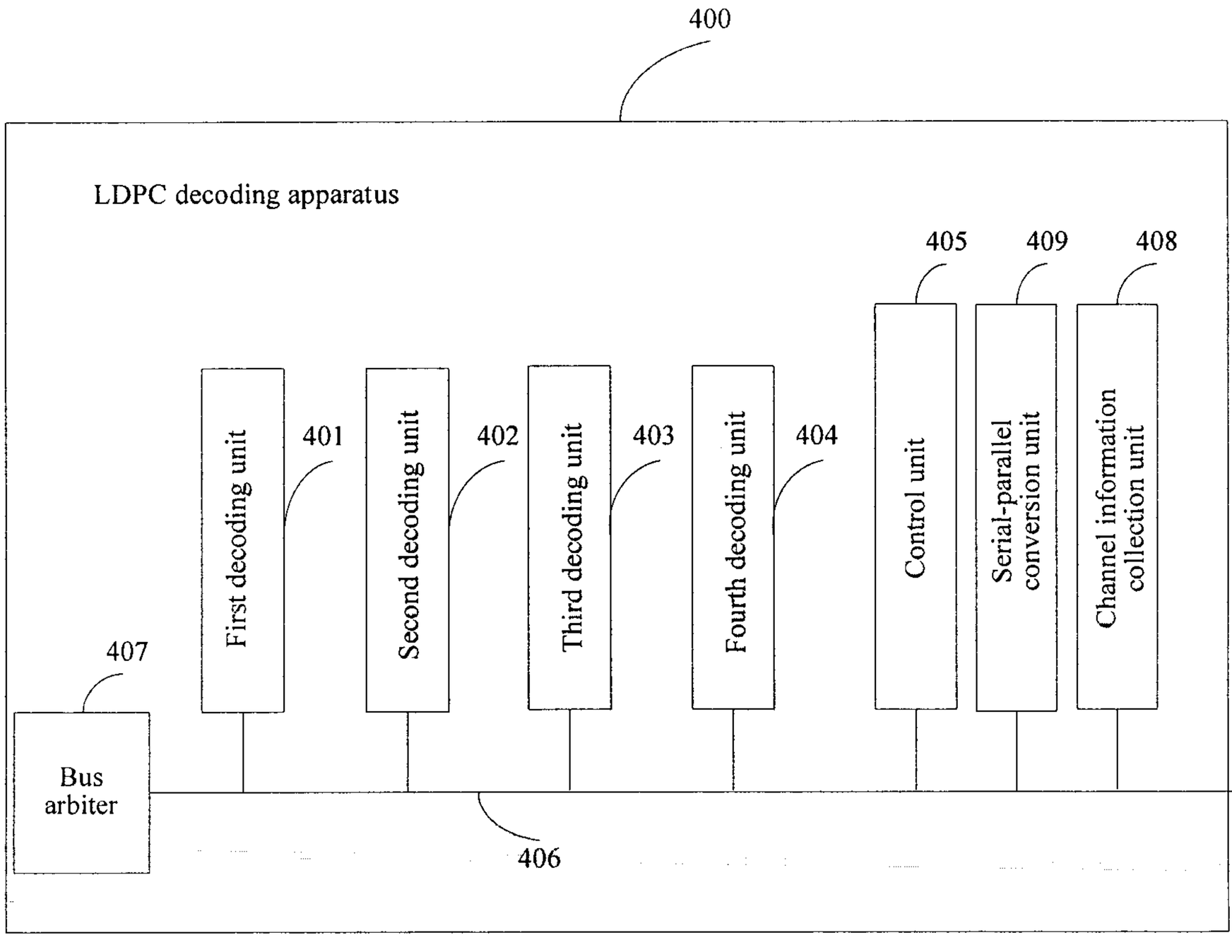
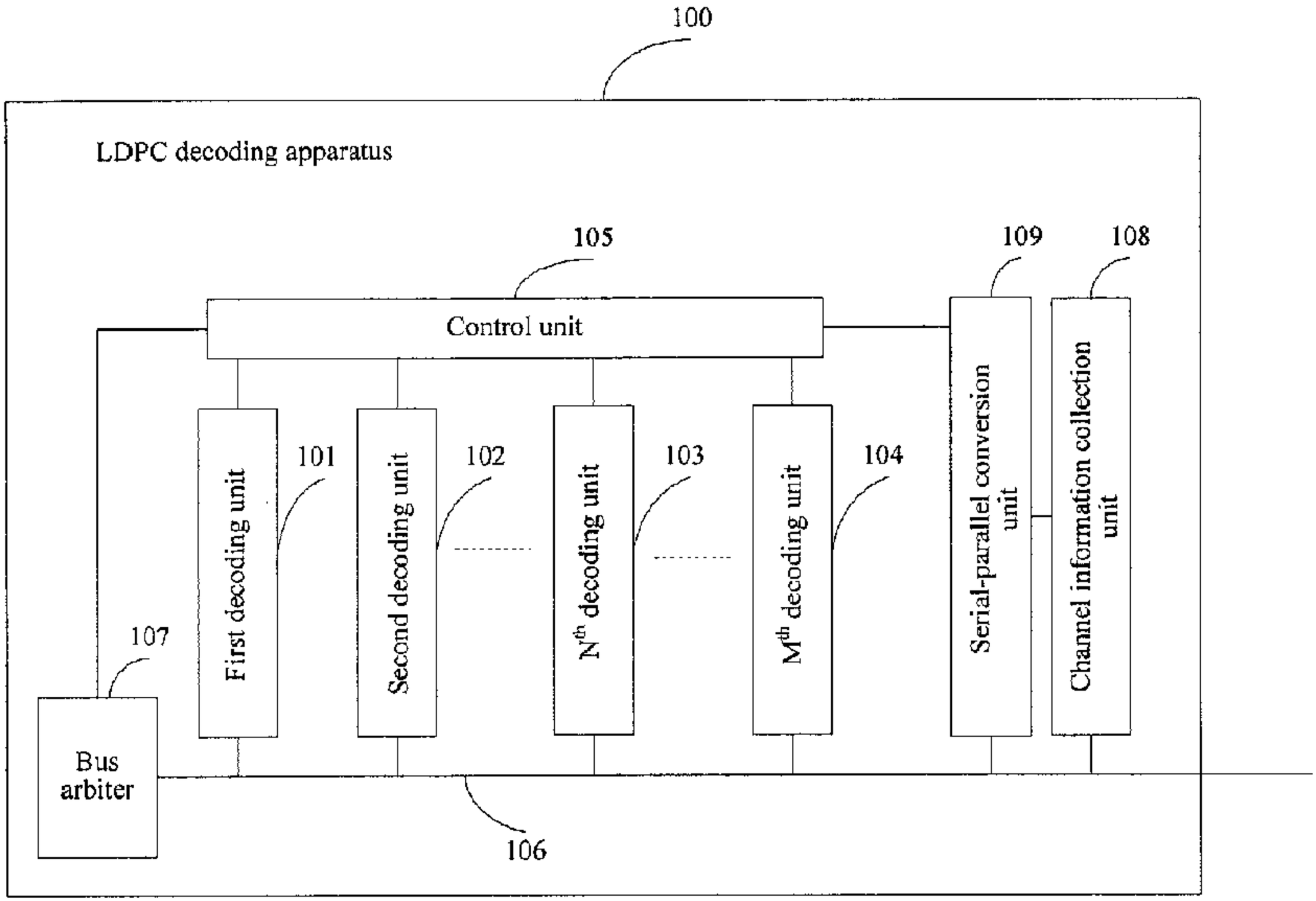

400
LDPC decoding apparatus
405
409
408
First decoding unit
401
Second decoding unit
402
Third decoding unit
403
Fourth decoding unit
404
Control unit
Serial-parallel conversion unit
Channel information collection unit
407
Bus arbiter
406

FIG. 4


100
LDPC decoding apparatus
105
Control unit
109
108
Serial-parallel conversion unit
Channel information collection unit
First decoding unit
101
Second decoding unit
102
N^th decoding unit
103
M^th decoding unit
104
107
Bus arbiter
106