(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 November 2009 (12.11.2009)

PCT

(10) International Publication Number
WO 2009/136317 A1

(51) International Patent Classification:
H03M 7/02 (2006.01) *H05B 33/08* (2006.01)
H03M 7/14 (2006.01) *H03M 1/82* (2006.01)
H03M 7/26 (2006.01)

(21) International Application Number:
PCT/IB2009/051729

(22) International Filing Date:
28 April 2009 (28.04.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/051,458 8 May 2008 (08.05.2008) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,

[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR SPECTRUM SPREADING BY TEMPORAL DITHERING OF PULSED SIGNALS

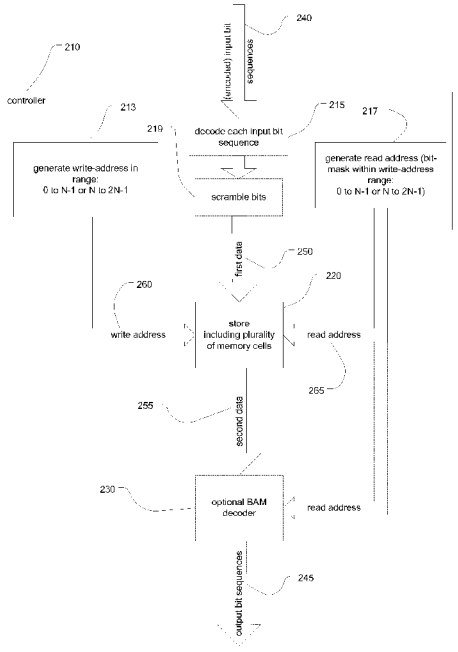

FIGURE 2

(57) Abstract: Disclosed are a method and apparatus for spectrum spreading by temporal dithering of pulsed signals. The apparatus and method are configured for processing an input bit sequence provided at the input into an output bit sequence provided at the output. The apparatus includes a receiver for receiving the input bit sequence, and a multiplexer for reordering bits of the input bit sequence according to a predetermined reordering method, thereby providing bits of the output bit sequence.

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MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

METHOD AND APPARATUS FOR SPECTRUM SPREADING BY TEMPORAL DITHERING OF PULSED SIGNALS

FIELD OF THE INVENTION

[0001] The present invention pertains to the generation of pulsed signals and, more particularly, to the formation of pulsed signals to provide a spread spectrum.

BACKGROUND

[0002] Pulse-width modulation (PWM) is a known method often used for controlling operating conditions of electrical machines or devices such as the rotational speed of electrical motors, the magnetic field strength in electrical power generators, the output voltage in switched-mode power supplies or the brightness in light-emitting diodes (LEDs) or other electrically powered devices, for example.

[0003] A PWM signal comprises rectangular pulses. The beginning of each pulse is typically aligned with the beginning of an interval of fixed predetermined width but can also be aligned to end at the end of the interval or positioned elsewhere within the interval. In its simplest form, PWM utilizes pulses with fixed predetermined finite amplitude separated by zero-amplitude signal portions. The average power provided per interval is determined by the amplitude of the pulse and the duty factor. The duty factor refers to the ratio of the width of the respective pulse per interval. The average power provided by a PWM signal can be adjusted by choosing a corresponding duty factor.

[0004] Pulse-code modulation (PCM) is another known method. PCM is often used for digitally encoding data but can also be used for controlling operating conditions of electronic devices and electrical machines. A PCM signal comprises signal portions of fixed finite amplitude and signal portions of zero amplitude. In its simplest form, each of the finite-amplitude and zero-amplitude portions has the same duration. The duration typically corresponds to a fixed predetermined period or an integer-multiple of a fixed predetermined period. A single PCM pulse typically lasts one predetermined fixed period. A PCM signal can change from a high

to a low state typically no faster than at the frequency corresponding to the inverse of the fixed predetermined period.

[0005] PCM is often used in combination with a clock signal to encode or transmit binary encoded data. The binary data can be represented as an ordered sequence of ones and zeroes that can be encoded as a PCM signal of corresponding high and low pulses. PCM can also be used to control the average power provided to an electrical machine. The average power is accordingly determined by the density of the PCM pulses.

[0006] PWM and PCM and other pulse-modulation methods, including variants of PWM and PCM methods, are known that may modulate width, amplitude or frequency of pulses in various different ways and combinations. Some known pulse-modulation methods can generate pulses in a predetermined order according to certain schemes that may be used in order to equilibrate load or to mitigate mechanical vibration in or emission of electromagnetic radiation of a device or machine or the surrounding system while, for example, maintaining the average power provided or other intended effect provided by the pulsed signal. For example, bit angle modulation (BAM) can generate a sequence of pulses, in which the pulse lengths correspond to the significance and the order of pulses corresponds to the order of bits of a corresponding binary code.

[0007] A number of pulse-modulation methods are known that provide signals with unique characteristics and that are used in a number of different applications. These methods can achieve control of operating conditions of electrical machines with different levels of accuracy and some can equilibrate power loads or achieve certain compositions by providing a pulsed signal that is shaped in a predetermined way or merely shift power to higher frequencies. The known methods, however, provide limited functionality, scale poorly for applications that require independent control of more than one channel, and provide limited improvement of electromagnetic interference (EMI) characteristics.

[0008] A key challenge for pulse-modulation methods is their ability to provide pulsed signals with suitable electromagnetic interference and vibration stimulation properties while providing adequate control of the operating conditions of electrical devices and machines. There is therefore a need for a new pulse-modulation method that addresses at least one of the deficiencies of existing methods.

[0009] This background information is provided to disclose information believed by the applicant to be of possible relevance to the present invention. No admission is necessarily

intended, nor should be construed, that any of the preceding information constitutes prior art against the present invention.

SUMMARY OF THE INVENTION

[0010] An object of the present invention is to provide a method and apparatus for spectrum spreading by temporal dithering of pulsed signals. Generally, in one aspect, the invention relates to an apparatus having an input and an output, the apparatus for processing an input bit sequence provided at the input into an output bit sequence provided at the output, the apparatus comprising: a receiver for receiving the input bit sequence; a multiplexer for reordering bits of the input bit sequence according to a predetermined reordering process, thereby generating a reconfigured bit sequence; and providing the reconfigured bit sequence at the output as the output bit sequence.

[0011] Also, in another aspect, the invention relates to an apparatus for processing K input bit sequences, each one of the K input bit sequences having N bits, the apparatus having an input and an output, the apparatus comprising: a store comprising a plurality of memory cells, each memory cell comprising K bits, the store providing a first address interface, a second address interface, a first data interface and a second data interface; the store configured for storing first data provided at the first data interface in the store in correspondence with a first address provided at the first address interface; the store further configured for providing second data at the second data interface in correspondence with a second address provided at the second address interface, the second data corresponding to the K bits of one of the plurality of memory cells, the one of the plurality of memory cells corresponding to the second address; a controller operatively connected to the store, the controller configured for receiving the input bit sequences and for saving the input bit sequences in the store; the controller further configured for generating read addresses according to a predetermined reordering method and for providing each one of the read addresses to the second address interface for providing corresponding data stored in the store at the each one of the read addresses at the second data interface at a time; wherein K and N are positive integer numbers.

[0012] In accordance with yet another aspect of the present invention, there is provided a method for processing an input bit sequence, the method comprising: receiving and storing the input bit sequence; determining an output bit sequence of bits comprising bits selected from the

input bit sequence which are reconfigured based on a predetermined reordering process; and providing the output bit sequence at an output one or more times.

Definitions

[0013] The term "light-emitting element" (LEE) is used to define a device that emits radiation in a region or combination of regions of the electromagnetic spectrum for example, the visible region, infrared and/or ultraviolet region, when activated by applying a potential difference across it or by passing an electrical current through it, for example. An LEE can have monochromatic, quasi-monochromatic, polychromatic or broadband spectral emission characteristics. Examples of LEEs include semiconductor, organic, or polymer/polymeric light-emitting diodes, optically pumped phosphor coated light-emitting diodes, optically pumped nano-crystal light-emitting diodes or other similar devices as would be readily understood by a worker skilled in the art. Furthermore, the term light-emitting element is used to define the specific device that emits the radiation, for example a LED die, and can equally be used to define a combination of the specific device that emits the radiation together with a housing or package within which the specific device or devices are placed.

[0014] As used herein, the term "about" refers to a +/-10% variation from the nominal value. It is to be understood that such a variation is always included in any given value provided herein, whether or not it is specifically referred to.

[0015] Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs.

BRIEF DESCRIPTION OF THE FIGURES

[0016] Figure 1 illustrates a series of discrete Fourier transform (DFT) coefficients of output bit sequences that may be obtained from an example input bit sequence according to an embodiment of the present invention.

[0017] Figure 2 illustrates a block diagram of the architecture of an apparatus according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0018] The present invention contemplates a method and an apparatus for processing at least one input bit sequence of a predetermined number of input bits. The method for processing the input bit sequence includes receiving the input bit sequence, optionally decoding the input bit sequence into a decoded bit sequence, and providing the bits of the input or decoded bit sequence which are reconfigured according to a predetermined reordering method as an output bit sequence of a predetermined number of output bits such that the output bit sequence has a spectrum different from the spectrum of the input bit sequence.

[0019] It is understood that each input pulse of a suitable pulsed signal such as a PWM signal can be interpreted as comprising multiple component pulses each of adequate duration. For example, a PWM signal may be represented as a corresponding PCM signal wherein each PCM pulse has a duration corresponding to a fraction of the period of the PWM signal, for example, corresponding to the resolution used or intended to control or adjust the duty factor of the PWM signal. The component pulses can then be interpreted as an input bit sequence and processed with methods and apparatus according to the present invention. It is further noted, that decomposing a pulsed signal into component pulses and reordering of the component pulses may have certain effects beyond the ones described and depending on the system or device, for example, an electrical machine, to which the pulses are provided.

[0020] Generally, a pulsed signal that extends over one or more first and one or more second regions and that has a first amplitude within the one or more first regions and a second amplitude within the one or more second regions can be represented as a pulse code. Such a pulsed signal can be decomposed into a plurality of portions of a predetermined width of either the first or the second amplitude. The plurality of portions can then be encoded in a first sequence of bits using one bit per portion so that the order of bits in the first sequence corresponds to the order of the portions in the pulsed signal so that each bit represents either the first or the second amplitude and can be used in the pulse code.

[0021] According to some embodiments of the present invention, the spectrum of a plurality of output bit sequences generated by repeat application of the predetermined reordering method can be spread and high spectral densities can be lowered in comparison to the spectrum of the same number of repetitions of mere repeat copies of the input bit sequence.

[0022] A corresponding apparatus according to various embodiments of the present invention comprises a receiver for receiving the input bit sequence an optional decoder for decoding the input bit sequence into the decoded bit sequence and a multiplexer for reordering the input or decoded bit sequence. The receiver and the multiplexer or both may be implemented with devices and components such as a number of discrete or integrated circuits or in a microcontroller or microprocessor or suitable combination of devices or components. The apparatus is configured to provide the bits of the input or decoded bit sequence according to the predetermined reordering method as an output bit sequence. Input and output bit sequence can be provided at a respective input and output of the apparatus. The multiplexer is configured to provide output bit sequences with spectra in accordance with the corresponding input bit sequence and the reordering method.

[0023] According to embodiments of the present invention, the input bit sequence can be a binary pulse code, a bit angle modulation (BAM) code or pulse with modulation (PWM) code, for example, or another pulse code as would be readily understood by a person skilled in the art. Certain input bit sequences such as a PWM code, for example, may need to be decoded into an intermediate decoded bit sequence before further processing can occur. The input bit sequence or the decoded bit sequence can then be provided at the output in a certain order. The output bit sequence may have the same number of bits included in the input or decoded bit sequence. The order in which bits of the input or decoded bit sequence may be provided in the output bit sequence can be a random or predetermined based on a fixed permutation, for example.

[0024] In one embodiment, random permutations may be generated by reading every bit once but in a random manner. This may be achieved with random or pseudo-random number generating schemes which may optionally utilize a look-up table. Random and pseudo-random number generating schemes are well known in the art and would be readily understood by a worker skilled in the art.

[0025] Each bit of the input or decoded bit sequence may be provided one or more times per output bit sequence. Apparatus or methods according to embodiments of the present invention, in which bits of the input or decoded bit sequence are included multiple times in one output bit sequence may be configured to provide repeat permutations of the input or decoded bit sequence, or a permutation of correspondingly repeated bits of all bits of the input or decoded bit sequence, for example.

Reordering Methods

[0026] **Figure 1** illustrates series of discrete Fourier transform (DFT) coefficients of output bit sequences that can be obtained from an example input bit sequence, according to an embodiment of the present invention. Each series can be obtained by applying a certain reordering method when copying bits from the input bit sequence to the output bit sequence. The exemplary input bit sequence used as a basis for Figure 1 corresponds to {1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 0, 0, 0, 0, 0} which includes ten one bits and five zero bits, or 15 bits in total. This exemplary input bit sequence can be interpreted as a pulse code of ten high pulses followed by five low pulses. Alternatively, this input bit sequence can also be interpreted as a list of a binary sampled PWM cycle with 15 equally spaced samples. It is noted that embodiments of the present invention may not require input bit sequences to be ordered in a particular way. This exemplary PWM cycle has a duty factor of ten out of 15 or about 67%. According to other embodiments of the present invention, this example input bit sequence may represent encoded information corresponding to a pulse code, pulse width modulation code or bit angle modulation code, for example, in which case the meaning of the example sequence depends on the corresponding encoding scheme.

[0027] In this example, the DFT coefficient series **110** and **120** that are illustrated in Figure 1, where obtained by interpreting the example input bit sequence as a pulse code modulation signal with 15 equally wide contiguous pulses. No further decoding was applied. For each PWM cycle, the example input bit sequence was reordered according to a corresponding one of three reordering methods to provide an output bit sequence for the cycle. This method was repeatedly applied to provide output bit sequences for further cycles. The output bit sequences from the cycles, when combined in a sequential order so that the first pulse of one output bit sequence follows the last pulse of a previous output bit sequence in a contiguous way, can be interpreted as a corresponding PCM signal. When combined in this way, a continuous PCM signal may be generated out of repeatedly generated, albeit differently ordered, stitched together output bit sequences.

[0028] The PCM signals, on which the illustrated DFT coefficient series illustrated in Figure 1 are based, each include a predetermined number of cycles and each cycle includes one copy of the bits provided in the example input bit sequence which have been reordered according to a corresponding reordering method. It is noted that according to other embodiments of the present invention, bits from the input bit sequence may be repeated more than once in the output bit

sequence, that is each bit from the input bit sequence can occur in the output bit sequence one or more times in a cycle.

[0029] DFT coefficients of output signals generated by an apparatus according to embodiments of the present invention may be obtained by measuring and adequately processing the output from the apparatus. Alternatively, the corresponding PCM signals may be computed and derived from a simulation or a model of a corresponding apparatus or method in which each output bit sequence is considered time shifted for purposes of computing the DFT. In order to determine the DFT coefficients, the time shift can be accounted for by applying principles of Fourier Transformations that are well known in the art.

[0030] Figure 1 illustrates the results of a computational analysis according to one embodiment of the present invention, in which DFTs were obtained for 100 and 10^4 cycles for three example reordering methods. The DFT coefficient values illustrated in Figure 1 indicate scaled values per cycle to correct for the otherwise increased intensity by the repeat contribution to the spectrum of each output bit sequence per cycle. The illustrated DFT coefficients are the result of dividing the corresponding computed DFT coefficients obtained for the total of 100 or 10^4 cycles by the respective number of cycles. Scaling can allow for the comparison of the values of like DFT coefficients that otherwise correspond to different numbers of cycles.

[0031] According to one embodiment of the present invention, a first reordering method is a PWM reordering method that copies each of the bits of the input bit sequence to the output bit sequence in the exact same order in which the bits appear in the input bit sequence. For ordered input bit sequences in which all one bits are contiguous, the PWM reordering method may be used to provide an output bit sequence that can be interpreted as a typical PWM modulated signal.

[0032] According to one embodiment of the present invention a second reordering method is a PCM reordering method which applies a random permutation to the bits of the input bit sequence and provides the permuted bits in the output bit sequence. The PCM reordering method can be configured so that output bit sequences of different cycles correspond to likely different permutations of the input bit sequence. The PCM reordering method can also be configured to provide permutations that are always different from the input bit sequence. The PCM reordering method employed to provide the data illustrated in Figure 1 preserves the number of bits, that is, each output bit sequence includes the same number of bits as the input bit sequence.

[0033] According to one embodiment of the present invention a third reordering method is a BAM reordering method, for which DFTs are illustrated in Figure 1. The example input bit sequence noted above can be considered to be the result of a reordered decoded corresponding example BAM code. The example BAM code that corresponds to the example input bit sequence can be expressed as the binary number 1010. According to typical BAM, this binary number can be decoded by repeating each bit in the binary number by its significance to provide the following example sequence of bit sequences {{1, 1, 1, 1, 1, 1, 1, 1}, {0, 0, 0, 0}, {1, 1}, {0}}. As can be seen, the example sequence of bit sequences can be reduced to a flat bit sequence and further reordered to provide the example input bit sequence noted above which is used as the basis for Figure 1. Other appropriate reordering methods would be readily understood by a worker skilled in the art.

[0034] In one embodiment, the BAM reordering method used to provide the corresponding DFTs illustrated in Figure 1 randomly permutes the bit sequences of the example sequence of bit sequences above before it reduces the reordered sequence of bit sequences to a flat bit sequence. The flat bit sequence is then interpreted as a pulse code. For example, {{1, 1, 1, 1, 1, 1, 1, 1}, {0, 0, 0, 0}, {1, 1}, {0}} may be reordered into {{0, 0, 0, 0}, {1, 1, 1, 1, 1, 1, 1, 1}, {1, 1}, {0}} thereby providing {0, 0, 0, 0, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 0} as one possible output bit sequence. It is noted that the BAM reordering method of Figure 1 typically cannot randomize bits as effectively as the PCM reordering method as it preserves the order of bits in each of the bit sequences of the sequence of bit sequences itself. It is further noted that there are other ways of interpreting BAM signals or generating bit sequences from BAM codes as would be readily understood by a person skilled in the art.

[0035] It is noted that for comparative purposes 15 samples per cycle are used consistently for the PWM, PCM and BAM reordering methods used to generate Figure 1. It is also noted that, typically, a positive integer power of two minus one (2^n-1 with n being the number of bits required for BAM encoding) samples may be chosen for BAM. Alternatively a positive integer power of two (2^n) samples may be used for BAM when complementing the decoded bit sequence by one filler bit, for example, a zero bit, to provide the one bit that BAM is naturally short of a positive integer power of two bits. Similar considerations can apply when determining the resolution of binary encoded PWM signals or when decoding binary PWM codes into, for example, a positive integer power of two or a positive integer power of two minus one pulses.

[0036] As illustrated in Figure 1, the DFT coefficient series for 100 and 10^4 cycles, as indicated in the legend of the diagram by respective reference numerals **110** and **120**, corresponding to the three reordering methods used are shown in a semi-logarithmic diagram. The abscissa provides a linear scale for the DFT coefficient indices. Each DFT coefficient series includes 15 DFT coefficients of which the absolute values are shown per coefficient index. The DFT coefficient absolute values are shown in arbitrary units and range from about zero to about two. Zero coefficient values occur for certain DFT coefficients provided by the PWM reordering method for the example input bit sequence and are not shown in the illustration because of the logarithmic scale of the ordinate axis. Zero coefficient values occur for the fourth, seventh, tenth and 13^{th} PWM coefficients for both 100 and 10^4 cycles.

[0037] As illustrated in Figure 1, the first DFT coefficients of each reordering method for 100 as well as for 10^4 cycles appear to be the same. This is expected since the first DFT coefficients correspond to the time average of the respective output bit sequences which in turn, because of the scaling of the DFT coefficients, correspond to the time average of the example input bit sequence. As will be further noted, the DFT coefficients generated by the PWM reordering method appear the same for both 100 and 10^4 cycles.

[0038] It is noted, that, alternatively, data acquired by measuring and processing the output signal of a respective apparatus according to the an embodiment of the present invention, will typically include measurement and processing artifacts as well as noise and superimposed signals from other sources and therefore provide spectra that may depend on the number of cycles investigated. In contrast, a simulation generates identical copies of the input bit sequence irrespective of the specific cycle but may still be prone to accumulation of errors, for example, due to possibly finite numerical precision used in computations of the simulation.

[0039] As is also shown in Figure 1, both DFT coefficient series, the one for 100 and the one for 10^4 cycles, for the BAM reordering method, relatively closely mimic the DFT coefficient series for the PWM reordering method in a number of aspects. For example, while some BAM coefficients are about half an order of magnitude smaller than their corresponding PWM coefficients, they remain relatively unaffected by the increase of the number of cycles from 100 to 10^4. The BAM coefficients with the same index as the zero value PWM coefficients, however, drop relatively quickly with the number of cycles by about one to two orders of magnitude with the number of cycles.

[0040] According to one embodiment of the present invention, as is illustrated in Figure 1, the PCM reordering method appears to generate smaller DFT coefficients in comparison to the other illustrated methods for all coefficients except for the ones with the same index as the zero value PWM coefficients. Generally, the PCM reordering method can generate output bit sequences, for the example input bit sequence that provide small, relatively evenly distributed DFT coefficient values across the spectrum. It is noted that the described reordering methods provide similar spectrum spreading effects for other input bit sequences that are different from the example input bit sequence.

[0041] The relatively even distribution of DFT coefficient values for the PCM reordering method indicates that little spectral power is concentrated at one frequency or in one spectral band. This can be particularly useful for certain applications for which an apparatus according to an embodiment of the present invention may be used. For example, when an apparatus is required to provide low electromagnetic emissions across a predetermined spectral range, typically high emissions at other frequencies are not feasible. Spectrum spreading according to the present invention can also be employed for controlling or limiting stimulation of mechanical resonances and vibrations in an apparatus according to an embodiment of the present invention, components or other systems in acoustic or other frequency ranges. Accordingly, and in accordance with one embodiment, the PCM or a similar reordering method may be used to significantly spread the spectral power distribution of corresponding PWM modulated signals by randomly permuting pulse codes when practically equivalent functions may be achieved. While it may be employed in embodiments of the present invention, a BAM reordering method will likely spread the spectrum less effectively for different input bit sequences than a PCM reordering method.

Receiver

[0042] The apparatus according to embodiments of the present invention may be configured to receive input bit sequences in various different ways such as parallel or serial, for example. For this purpose, an apparatus according to embodiments of the present invention can comprise, for example, a receiver. Receivers are configured to adequately receive one or more bits of one or more input bit sequences at a time. A receiver can be implemented with devices and components such as a number of discrete or integrated circuits or in a microcontroller or microprocessor or suitable combination of devices or components.

[0043] According to an embodiment of the present invention, input bit sequences may be provided intermittently, at a predetermined rate or otherwise. An apparatus according to embodiments of the present invention may be configured to process transitions from one input bit sequence to another in different ways. For example, an apparatus and method according to one embodiment of the present invention may be configured to, for example, stop, switch or interrupt decoding or multiplexing of a respective input or decoded bit sequence or providing bits to the output bit sequence immediately upon receipt of one or more bits of a new input bit sequence.

[0044] In one embodiment of the present invention, apparatus and methods are configured so that an adequate number of output bits that are based on the input bit sequence prior to the new input bit sequence are continued to be provided to the output bit sequence until new bits or new decoded bits that are derived from the new input bit sequence become available and can be provided to the output bit sequence so that a transition can be facilitated in a number of predetermined ways. Further, in the apparatus according to various embodiments of the present invention can be configured so that it can adequately communicate indications of status of transitions between components such as the receiver and the multiplexer, for example, when a new input bit sequence is about to be or is being or has been received.

Decoder

[0045] In some embodiments, the apparatus may optionally include a decoder to enable decoding encoded input bit sequences into decoded bit sequences in case it may be intended to receive encoded input bit sequences that are encoded according to a predetermined encoding scheme. The decoder can be implemented with devices and components such as a number of discrete or integrated circuits or in a microcontroller or microprocessor or suitable combination of devices or components.

[0046] Decoding of encoded input bit sequences into decoded input bit sequences may commence upon receipt of the full encoded input bit sequence or while receipt of the encoded input bit sequence is ongoing. Commencing decoding based upon only a part of an encoded input bit sequence may be possible depending on the encoding scheme. Decoding encoded input bit sequences may provide some bits of the decoded bit sequence earlier than other bits or it may practically generate all bits of the decoded bit sequence at once, depending on the encoding scheme.

[0047] In one embodiment, reading and further processing of certain bits from a decoded input bit sequence may be possible depending on the number of bits required for further processing before all bits of the decoded input bit sequence have been determined. An apparatus according to different embodiments of the present invention may be configured to operate accordingly and commence decoding of or reading from a partially received encoded input bit sequence or reading from a partially decoded input bit sequence. Alternatively, an apparatus may be configured to commence reading bits or decoding bits from incomplete bit sequences, even if it may be feasible, only upon receipt of the complete input bit sequence or completion of the decoding process, respectively.

[0048] An apparatus according to embodiments of the present invention may be configured to perform and commence operations such as receiving, decoding as well as multiplexing operations, for example, in various ways depending on whether input bit sequences are intended to be received in a parallel, serial or other manner. In accordance with embodiments of the present invention, these operations may also determine when and how the output of the bits of the output bit sequence is transitioned from output bits that are derived from one input bit sequence to those derived of a new input bit sequence..

[0049] For example, an interrupt may be performed synchronous or asynchronous with receipt of the input bit sequence or receipt of a predetermined number of the bits of the input bit sequence or similarly with the output of the output bit sequence of a predetermined bit of the output bit sequence. Similarly, an apparatus or method according to embodiments of the present invention may be configured to synchronize the transition between consecutive input bit sequences with a certain bit of a decoded bit sequence, for example when decoding of the input bit sequence into a decoded bit sequence is employed.

[0050] In some embodiments of the present invention, the manner in which the input bit sequence may be provided can be different from the manner in which the output bit sequence may be provided. For example, an input bit sequence may be provided in parallel and the output bit sequence may be provided serially.

[0051] Furthermore, a method or apparatus according to an embodiment of the present invention may be configured to provide bits of the output bit sequence on average at the same rate or at a rate that is a multiple of the rate at which bits of the decoded or input bit sequence are provided or generated.

Multiplexer

[0052] According to embodiments of the present invention, the multiplexer performs the function of transferring bits from the input or decoded bit sequence to the output bit sequence according to a predetermined reordering method. The multiplexer can read the input or decoded bit sequence and can provide and apply a predetermined reordering method such as one as described above, for example. The multiplexer generates a permuted bit sequence that can be provided as the output bit sequence. The multiplexer can be configured to read bits from the input or decoded bit sequence in a predetermined order such as arbitrarily or randomly, for example, and provide the read bits for output. The read bits provided for output may be provided at the output as an output bit sequence immediately or assembled in an intermediate binary word for output as an output bit sequence. The output bit sequence may be provided in serial or a parallel fashion. The multiplexer can be implemented with devices and components such as a number of discrete or integrated circuits or in a microcontroller or microprocessor or suitable combination of devices or components.

Controller

[0053] Embodiments according to the present invention can comprise a controller such as a microcontroller or microprocessor or a similar device or system including a controller as would be readily known by a person skilled in the art. A controller may be used in combination with a store or memory of a one or more of a variety of memory formats as would be readily understood by a worker skilled in the art. Embodiments of the present invention may also be implemented in general or special purpose computer systems such as a personal computer, for example, or other computer system as would be readily known by a person skilled in the art.

Store

[0054] Embodiments according to the present invention can comprise a store such as an addressable non-volatile or volatile memory device, for example, a static or magnetic or other random access memory as would be readily known to a person skilled in the art. Depending on the embodiment, the store may be an integral part of a controller or a separate device operatively connected to the controller or the multiplexer.

[0055] The store may provide one or more data interfaces and one or more address interfaces. The store may be configured to receive or provide data at one or more of its interfaces in a serial

or parallel way, for example, as would be readily understood by a person skilled in the art. The store can be a dual-port random access memory or another type of memory as would be readily known by a person skilled in the art that may allow reading and writing to and from the store in a practically simultaneous fashion.

[0056] According to one embodiment of the present invention, the store may include a single-port random access memory or similar memory device for allowing reading and writing from and to the store via one data and one address interface in a time-multiplexed fashion. Respective embodiments may include an output bit sequence extracting device with an input operatively connected to the store and an output operatively connected to the output of the apparatus for providing only output bit sequences at the output of the apparatus that are provided by reading data from the store during a read cycle. The extracting device can be configured to reject data other than output bit sequences from the time-multiplexed data stream that are provided at the data interface of the store. Respective embodiments can be configured, wherein for example, the controller can be configured, to control the extracting device to transfer data only output bit sequences to the output of the apparatus.

[0057] Corresponding methods according to embodiments of the present invention can be generalized and employed at little computational cost for processing multiple independent input bit sequences synchronously on a bit level, for example, in parallel, for the control of a corresponding number of devices via multiple independent control channels. An apparatus according to the present invention that is employed for certain applications may furthermore require that transitions between output bit sequences on the same channel can be effected in ways that provide intended effect(s) but do not interfere with the intended operation of the device that is controlled by the output bit sequence or to which the output bit sequence is supplied.

[0058] Furthermore, changing or transitioning input bit sequences of multiple channels to subsequent input bit sequences may need to be performed in a sufficiently synchronous manner depending on the application. Generally, an apparatus according to embodiments of the present invention can be configured to synchronize transitions from one set of input bit sequences to a subsequent set of input bit sequences across all or at least some channels. Synchronous transitions may be provided by embodiments of the present invention that can then be employed for certain applications. Synchronous transitions may be required, for example, for the control of the intensity of the light emitted by multi-color light-emitting elements in order to avoid

perceptible color or brightness variations in the mixed light emitted by a corresponding luminaire. For example, the multi-color light-emitting elements may be operatively combined by color and each color may be assigned a channel. Each channel may then be controlled independently to, for example, control power provided to the light-emitting elements of like color separately from the power provided to light-emitting elements of another color.

[0059] The invention will now be described with reference to particular examples. It will be understood that the following examples are intended to describe embodiments of the invention and are not intended to limit the invention in any way.

EXAMPLES

EXAMPLE 1:

[0060] In this example and according to one embodiment of the present invention, each PCM cycle is divided into m time slices and their temporal order is randomly permuted, wherein this approach will result in spectral power distribution (SPD) spreading of the signal. In one embodiment, each time slice has a width of $1 / (m * f)$ seconds, where f is the PCM switching frequency. As a refinement of this embodiment, m is an integral power of two, namely $2^k = m$, where k is a positive integer. This configuration can ensure that the leading or trailing edge of a PCM pulse is synchronized with the beginning of a time slice, thereby avoiding the occurrence of arbitrarily narrow pulses within a time slice. This can also apply to a PWM pulse as a PWM signal is a special case of a PCM signal whose pulses have been sequentially ordered.

[0061] Random permutation of time slices has the advantage of being computationally less expensive when compared to randomized bit shifting. For example, randomized bit shifting of n bits has about an $O(2^{n-1})$ time complexity due to the need to sequentially shift the bit string 2^{n-1} times on average. The random permutation of time slices as defined in this embodiment can have about an O(1) time complexity if a lookup table is used to determine the n-bit permutation. In another embodiment an $O(n)$ permutation algorithm can be employed to calculate the random permutation for each cycle.)

[0062] This method may be readily extended to spread the SPDs of a multiplicity of PCM channels. For example, in one embodiment, p PCM channels with n-bit resolution are connected to the data input of a dual-port random-access memory (RAM) which has a capacity of $2 * n$ words with p bits. On a first cycle with duration $1 / f$ seconds (where f is the PCM switching

frequency), the input address line is sequentially incremented n times at $1 / (n * f)$ second intervals. Consequently, the RAM stores the p PCM channels as n sequential p-bit words.

[0063] Subsequently, once these words have been stored in RAM memory locations 0 to $n - 1$, a random permutation of n sequential addresses from 0 to n – 1 is determined by a lookup table operation.

[0064] On a second and subsequent cycle, the input address line is sequentially incremented n times at $1 / (n * f)$ second intervals to store an additional p PCM channels as n sequential p-bit words. Each time the input address line is incremented however over the address range of n to $2 * n - 1$, the output address line is set to the random permutation of the current address less n, namely the output address is a random address in the range 0 to $n - 1$. The addressed p-bit word is then available on the RAM data output.

[0065] Once the data input words have been stored in RAM memory locations n to $2 * n - 1$, a random permutation of n sequential addresses from n to $2 * n - 1$ is determined by a lookup table operation.

[0066] On a third and subsequent cycle, the input address line is sequentially incremented n times at $1 / (n * f)$ second intervals to store an additional p PCM channels as n sequential p-bit words in the RAM memory address range 0 to $n - 1$. Each time the input address line is incremented, the output address line is set to the random permutation of the current address plus n, namely the output address is a random address in the range n to $2 * n - 1$. The addressed p-bit word is then available on the RAM data output.

[0067] The repetition of these operations can effectively stream the multiple PCM channel data with a one-cycle delay while randomly permuting each cycle into n time slices. In other embodiments, the time slice widths may be integer multiples or submultiples of $1 / (n * f)$ seconds without significantly affecting the implementation of this method. An advantage of employing different time slice widths is that they can determine the spreading characteristics of the PCM channels spectral power distributions.

[0068] In one embodiment of the present invention, where multiple color channels are connected to a common power supply, the random permutation chosen for each channel during a given cycle can be different, thereby further spreading the spectral power distribution for the power supply ferromagnetic components.

[0069] In another embodiment of the present invention, the pulse width may be extended *j* times every *m* cycles in a random or deterministic order. An advantage of randomly ordering the extended pulse widths is that it can further spread the data signal spectral power distribution.

EXAMPLE 2:

[0070] Figure 2 illustrates a block diagram of the architecture of an apparatus according to one embodiment of the present invention. The apparatus is configured for processing a positive integer number of K input bit sequences provided under operating conditions as indicated by arrow **240**. Each one of the K input bit sequences comprise a positive integer number of N bits that may be provided to one of a number of corresponding channels. The apparatus has an input and an output and can be configured to perform transitions between input bit sequences synchronously as discusses above.

[0071] It is noted that, alternatively, the apparatus may be configured to receive and process encoded input bit sequences. Further alternatively, it is noted that the apparatus may also be configured to be able to receive and process encoded as well as unencoded input bit sequences. In the latter case the apparatus may optionally be configured to receive a further input signal or provide another input, for example a switch, indicative of whether a corresponding input bit sequence should be considered by the apparatus as an encoded or an unencoded input bit sequence.

[0072] The apparatus comprises a store **220** including a plurality of memory cells. Each memory cell comprises K bits. The store provides a first address interface, a second address interface, a first data interface and a second data interface. The store is configured to store first data that is provided at the first data interface in the store at a first address provided at the first address interface. It is noted that the first data and the first address may be required to be provided in a way, for example at certain times or within certain time frames, that is compatible with the requirements of the store and may also require further control signals to be provided to the store that indicate one or more functions that the store is intended to perform in correspondence with the first data and the first address or similarly with other data or other addresses provided at other interfaces of the store.

[0073] The store is further configured for providing second data as indicated by arrow **255** at the second data interface in correspondence with a second address or read address as indicated

by arrow **265** provided at the second address interface. The second data corresponds to the K bits stored in one of one of the plurality of memory cells corresponding to the second address.

[0074] The apparatus further comprises a controller **210** operatively connected to the store **220**. The controller is configured to receive the input bit sequences and to save the input bit sequences in the store by providing first data as indicated by arrow **250** to the store **220** in correspondence with respective write addresses as indicated by arrow **260** which are generated by the controller as indicated by **213**. The controller is further configured to generate read addresses as indicated by **217** according to a predetermined reordering method, for example, one of the reordering methods described. The controller is also configured to provide each one of the read addresses to the second address interface of the store, so the store can provide second data that is stored in the store at the read address provided at the read address interface. The store provides the second data at the second data interface as is indicated by arrow **265**.

[0075] The controller can be configured for generating read addresses within a first address range including N first addresses or within a second address range including N second addresses. The controller can further be configured for generating write addresses within the first address range or the second address range. Furthermore, the controller can be configured for generating read addresses within the first address range and write addresses within the second address range or read addresses within the second address range and write addresses within the first address range. Moreover, the controller can be configured for generating read addresses in alternating address ranges by periodically alternating between the first address range and the second address range.

[0076] In order to enable the apparatus to receive input bit sequences while also providing the apparatus with the ability to continue processing previously received and stored input bit sequences for a complete set of K channels, the apparatus may be configured in a number of ways. The apparatus can be configured to generate N first addresses and N second addresses providing a first address range that is disjunct from the second address range so that no single address included in the first address range is included in the second address range and vice versa. For example, the apparatus can be configured so that the N first addresses range from 0 to N-1 and the N second addresses range from N to 2N-1.

[0077] A reordering method as, for example, discussed earlier for a single channel, can be implemented in the apparatus intended for the control of K channels by configuring the

controller to generate read corresponding addresses. For example, by interpreting the reordering of single bits of a single bit sequence, instead, as a reordering of N binary words of K bits each.

[0078] The apparatus can be configured for receiving the N input bit sequences at a first rate and for providing the N output bit sequences as indicated by arrow **245** in Figure 2 at a second rate that can be supported by the components of the apparatus, for example, at a suitably chosen frequency so that the store can reliably provide stored data when reading from its memory cells at that frequency, as would be readily understood by a person skilled in the art. Providing output bit sequences at a second rate can be facilitated by synchronously, while possibly requiring correction of time delays that may be characteristic to a specific embodiment, providing read addresses at the same second rate. The store may be configured to provide data at the second data interface in parallel. Alternatively, the second data interface may be a serial data interface for providing second data at the second data interface in serial, in which case the apparatus may be combined with a suitable serial-to-parallel converter in order to be able to provide output bit sequences for multiple channels synchronously.

[0079] The apparatus can be configured for receiving each bit of one of the K input bit sequences in parallel or, alternatively, for receiving each bit of one of the K input bit sequences in serial. The apparatus, for example, the controller, may further be configured for receiving a plurality of the K input bit sequences periodically or intermittently, for example, or in another way, as would be readily understood by a person skilled in the art.

[0080] It is noted that in general apparatus according to the present invention may be configured for providing each bit of the output bit sequence as one bit of a pulse code signal for use in control of power provided to one or more light-emitting elements.

[0081] Optionally, apparatus according to an embodiment of the present invention may be configured, to receive and process input bit sequences that are BAM encoded, in which the bits of BAM encoded input bit sequences are reordered in the BAM encoded format. Such an apparatus may additionally comprise or be combined with an operatively connected BAM decoder **230** as illustrated in Figure 2 for converting second data read from the store into corresponding decoded output bit sequences **245**.

EXAMPLE 3:

[0082] In another embodiment of the present invention, an example apparatus can be generally configured like the apparatus whose architecture is illustrated in Figure 2. However, in this

embodiment the apparatus is configured to save bits of like significance for the K channels in parallel. For example, the apparatus may receive N binary words serially and each one of the N binary words comprises K corresponding bits. For this purpose the store of the apparatus is further configured for storing first data comprising K bits provided at the first data interface at one of the plurality of memory cells corresponding to an address provided at the first address interface. The controller of the apparatus is further configured to generate a corresponding write address for each one of N binary words. Each one of the N binary words corresponds to K bits of like-significance of the K input bit sequences. The controller is further configured to provide each one of the N binary words at the first data interface in correspondence with providing the corresponding write address at the first address interface for saving the N binary words in the store. The controller is configured to save each one of the N binary words to the store one at a time. The apparatus can be configured for receiving one of the N binary words at a time.

[0083] The apparatus, for example, the controller, can be further configured for providing a specific read address for reading from the store only when all bits of the corresponding data stored in the store have previously been initialized accordingly, for example, so that the bits correspond to a previously saved one of N binary words.

[0084] The apparatus can optionally be configured to operate with a properly configured store of only N memory cells, while still allowing the apparatus to read from the store and write to it in order to overwrite previously saved input bit sequences with new input bit sequences as the new input bit sequences are being received. If a transition from one set of input bit sequences to a subsequent input bit sequence across all channels is intended to be only performed, not only synchronously across all channels, but also synchronously only after the full length or every N bits of a full input bit sequence, the controller can be configured to generate read and write addresses during those transitional periods in a further specific way by temporarily limiting or temporarily deviating from the predetermined reordering method. For example, as new binary words are being received and are still being saved to the store at corresponding write addresses, the controller can be configured to read from only those memory cells that have not yet been overwritten with new binary words, and only once all memory cells have been overwritten with the complete set of N binary words, that is, all K new input bit sequences, does the controller resume generating read addresses according to the predetermined reordering method.

[0085] It is noted, however, that for certain applications, temporarily deviating from generating read addresses according to the predetermined reordering method may not be required for as long as read-write address collisions can be avoided that may otherwise lead to erratic output bit sequences when it is attempted to read from and to write to the very same memory cell simultaneously. This relaxed method of generating read addresses may be applied, whenever blending, for example, by sequentially overwriting memory cells, while randomly reading from the memory cells, does not generate undesired practically relevant side effects. In fact blending transitions of output bit sequences that can be derived from adjacent input bit sequences may be desired for certain applications of apparatus according to certain embodiments of the present invention.

EXAMPLE 4:

[0086] In another embodiment of the present invention an apparatus can be generally configured like the apparatus whose architecture is illustrated in Figure 2. However the apparatus is configured to save N bits of each one of the K input bit sequences to the store at a time while the store can be used to read binary words of K bits per memory cell. For illustrative purposes only, this may be envisioned as using a store that is configured as a matrix of bits to which data is written to columns of the matrix while data is read from rows of the matrix.

[0087] For this purpose the store is further configured for storing first data comprising N bits provided at the first data interface in N bits of N of the plurality of memory cells of a first significance, and the first significance is determined by an address provided at the first address interface. That is the first address can correspond to a bit address within a certain number, for example N, memory cells. Furthermore, the controller is further configured for generating one corresponding write address for each one of the input bit sequences, and for providing each one of the input bit sequences to the first data interface in correspondence with the corresponding write address that is provided at the first address interface so that one of the input bit sequences can be saved in the store at a time. The apparatus can be configured for receiving one of the K input bit sequences at a time.

[0088] Optionally, the example apparatus may be configured to scramble each input bit sequence as indicated by **219** before saving it to the store. Scrambling of input bit sequences before saving may be employed in order to decorrelate possible otherwise occurring artifacts that may arise from correlations of bits across multiple channels, for example, when input bit

sequences are ordered corresponding to a PWM order in which all one bits are bunched up together. Scrambling input bit sequences and saving the scrambled input bit sequence can help provide better randomized output bit sequences in embodiments that randomly read from the store. For example, scrambling may be performed by saving a random permutation of the input bit sequence.

[0089] Further optionally, the example apparatus may be configured for decoding encoded bit sequences as indicated by **215** in applications in which input bit sequences are provided in an encoded format.

[0090] While several inventive embodiments have been described and illustrated herein, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the function and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or modifications is deemed to be within the scope of the inventive embodiments described herein. More generally, those skilled in the art will readily appreciate that all parameters, dimensions, materials, and configurations described herein are meant to be exemplary and that the actual parameters, dimensions, materials, and/or configurations will depend upon the specific application or applications for which the inventive teachings is/are used. Those skilled in the art will recognize, or be able to ascertain using no more than routine experimentation, many equivalents to the specific inventive embodiments described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described and claimed. Inventive embodiments of the present disclosure are directed to each individual feature, system, article, material, kit, and/or method described herein. In addition, any combination of two or more such features, systems, articles, materials, kits, and/or methods, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the inventive scope of the present disclosure.

[0091] Accordingly, as indicated above, the foregoing embodiments of the invention are examples and can be varied in many ways. Such present or future variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be apparent to one skilled in the art are intended to be included within the scope of the following claims.

[0092] All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

[0093] The indefinite articles "a" and "an," as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean "at least one."

[0094] The phrase "and/or," as used herein in the specification and in the claims, should be understood to mean "either or both" of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases. Multiple elements listed with "and/or" should be construed in the same fashion, i.e., "one or more" of the elements so conjoined. Other elements may optionally be present other than the elements specifically identified by the "and/or" clause, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, a reference to "A and/or B", when used in conjunction with open-ended language such as "comprising" can refer, in one embodiment, to A only (optionally including elements other than B); in another embodiment, to B only (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

[0095] As used herein in the specification and in the claims, "or" should be understood to have the same meaning as "and/or" as defined above. For example, when separating items in a list, "or" or "and/or" shall be interpreted as being inclusive, i.e., the inclusion of at least one, but also including more than one, of a number or list of elements, and, optionally, additional unlisted items. Only terms clearly indicated to the contrary, such as "only one of" or "exactly one of," or, when used in the claims, "consisting of," will refer to the inclusion of exactly one element of a number or list of elements. In general, the term "or" as used herein shall only be interpreted as indicating exclusive alternatives (i.e. "one or the other but not both") when preceded by terms of exclusivity, such as "either," "one of," "only one of," or "exactly one of." "Consisting essentially of," when used in the claims, shall have its ordinary meaning as used in the field of patent law.

[0096] As used herein in the specification and in the claims, the phrase "at least one," in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and

not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase "at least one" refers, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, "at least one of A and B" (or, equivalently, "at least one of A or B," or, equivalently "at least one of A and/or B") can refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

[0097] It should also be understood that, unless clearly indicated to the contrary, in any methods claimed herein that include more than one step or act, the order of the steps or acts of the method is not necessarily limited to the order in which the steps or acts of the method are recited. In the claims, as well as in the specification above, all transitional phrases such as "comprising," "including," "carrying," "having," "containing," "involving," "holding," "composed of," and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases "consisting of" and "consisting essentially of" shall be closed or semi-closed transitional phrases, respectively.

I CLAIM:

1. An apparatus having an input and an output, the apparatus for processing an input bit sequence provided at the input into an output bit sequence provided at the output, the apparatus comprising:
   (a) a receiver for receiving the input bit sequence;
   (b) a multiplexer for reordering bits of the input bit sequence according to a predetermined reordering process, thereby generating a reconfigured bit sequence and providing the reconfigured bit sequence at the output as the output bit sequence.

2. The apparatus according to claim 1, further comprising a decoder configured to decode an encoded input bit sequence into the input bit sequence.

3. The apparatus according to claim 1, wherein the input bit sequence comprises a same number of bits as the output bit sequence.

4. The apparatus according to claim 1, wherein the predetermined reordering process is a random permutation.

5. The apparatus according to claim 1, wherein the predetermined reordering process is a predetermined permutation.

6. An apparatus for processing K input bit sequences, each one of the K input bit sequences having N bits, the apparatus having an input and an output, the apparatus comprising:
   (a) a store comprising a plurality of memory cells, each memory cell comprising K bits, the store providing a first address interface, a second address interface, a first data interface and a second data interface; the store configured for storing first data provided at the first data interface in the store in correspondence with a first address provided at the first address interface; the store further configured for providing second data at the second data interface in correspondence with a second address provided at the second address interface, the second data corresponding to the K bits of one of the plurality of memory cells, the one of the plurality of memory cells corresponding to the second address;

(b) a controller operatively connected to the store, the controller configured for receiving the input bit sequences and for saving the input bit sequences in the store; the controller further configured for generating read addresses according to a predetermined reordering method and for providing each one of the read addresses to the second address interface for providing corresponding data stored in the store at the each one of the read addresses at the second data interface at a time;

wherein K and N are positive integer numbers.

7. The apparatus according to claim 6, further comprising a decoder configured to decode an encoded input bit sequence into one or more of the K input bit sequences.

8. A method for processing an input bit sequence, the method comprising:
(a) receiving and storing the input bit sequence;
(b) determining an output bit sequence of bits comprising bits selected from the input bit sequence which are reconfigured based on a predetermined reordering process; and
(c) providing the output bit sequence at an output one or more times.

9. The method according to claim 8, prior to step (a) performed the step of decoding an encoded input bit sequence into the input bit sequence.

10. The method according to claim 8, wherein the input bit sequence comprises a same number of bits as the output bit sequence.

11. The method according to claim 8, wherein the predetermined reordering process is a random permutation.

12. The method according to claim 8, wherein the predetermined reordering process is a predetermined permutation.

13. The method according to claim 8, wherein each bit of the input bit sequence is provided in the output bit sequence one or more times.

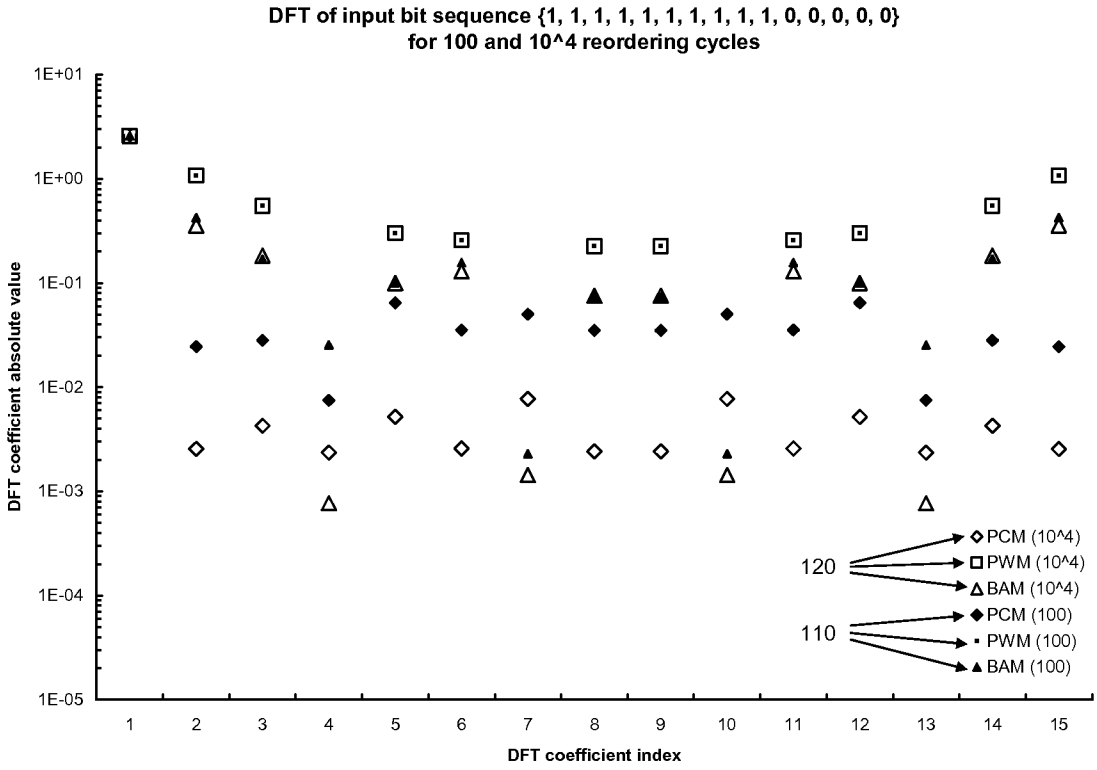
DFT of input bit sequence {1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 0, 0, 0, 0, 0}
for 100 and 10^4 reordering cycles
DFT coefficient absolute value
1E+01
1E+00
1E-01
1E-02
1E-03
1E-04
1E-05
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
DFT coefficient index
120
110
PCM (10^4)
PWM (10^4)
BAM (10^4)
PCM (100)
PWM (100)
BAM (100)

FIGURE 1

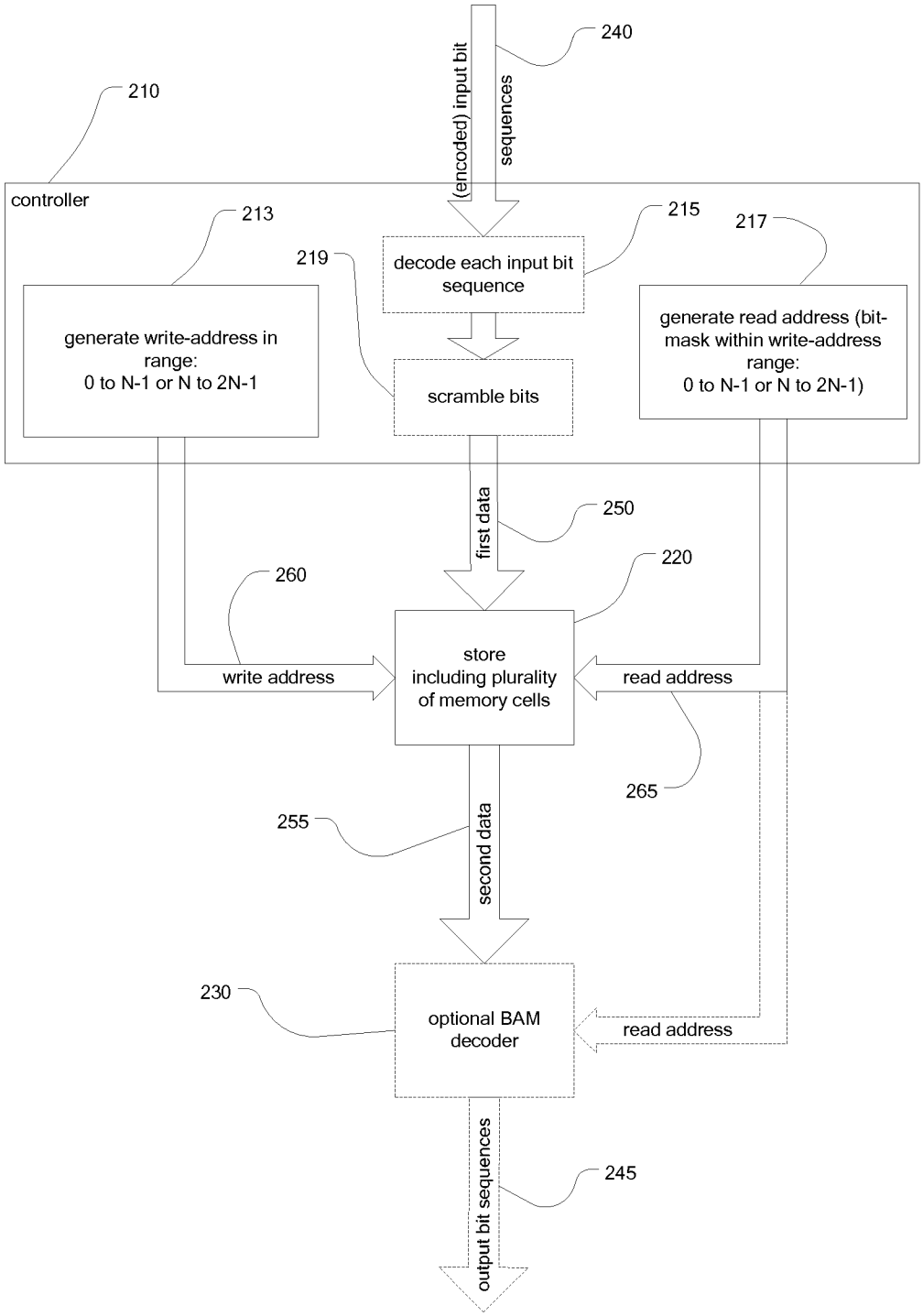
240
(encoded) input bit sequences
210
controller
213
215
217
219
decode each input bit sequence
generate write-address in range:
0 to N-1 or N to 2N-1
scramble bits
generate read address (bit-mask within write-address range:
0 to N-1 or N to 2N-1)
first data
250
260
220
store including plurality of memory cells
write address
read address
265
255
second data
230
optional BAM decoder
read address
output bit sequences
245

FIGURE 2

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/051729

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M7/02 H03M7/14 H03M7/26 H05B33/08 H03M1/82

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	RAMSEY J L: "REALIZATION OF OPTIMUM INTERLEAVERS" IEEE TRANSACTIONS ON INFORMATION THEORY, IEEE, US, vol. 16, no. 3, 1 May 1970 (1970-05-01), pages 338-345, XP002010849 ISSN: 0018-9448 figure 1 page 340, left-hand column, line 15 - line 16 page 338, right-hand column, line 12	1-5,8-13
X	US 6 362 766 B1 (ROWAN BRYAN SCOTT [US] ET AL) 26 March 2002 (2002-03-26) figure 1 column 4, line 14 - line 18	1-2,4-5, 8-9, 11-13

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 August 2009	24/08/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Winkler, Gregor

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/051729

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2004/062111 A1 (ICOMM TECHNOLOGIES INC [US]) 22 July 2004 (2004-07-22) figures 4,21 paragraph [0137]	6-7
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