



- (51) **International Patent Classification:**
H01L 21/8238 (2006.01) *H01L 29/78* (2006.01)
H01L 21/336 (2006.01)
- (21) **International Application Number:**
PCT/US2010/059395
- (22) **International Filing Date:**
8 December 2010 (08.12.2010)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
12/655,463 30 December 2009 (30.12.2009) US
- (71) **Applicant (for all designated States except US):** INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, MS: RNB-4-150, Santa Clara, CA 95052 (US).
- (72) **Inventors; and**
- (75) **Inventors/Applicants (for US only):** PILLARISETTY, Ravi [US/US]; 1330 SW, 3rd Avenue, Apt. 1103, Port-

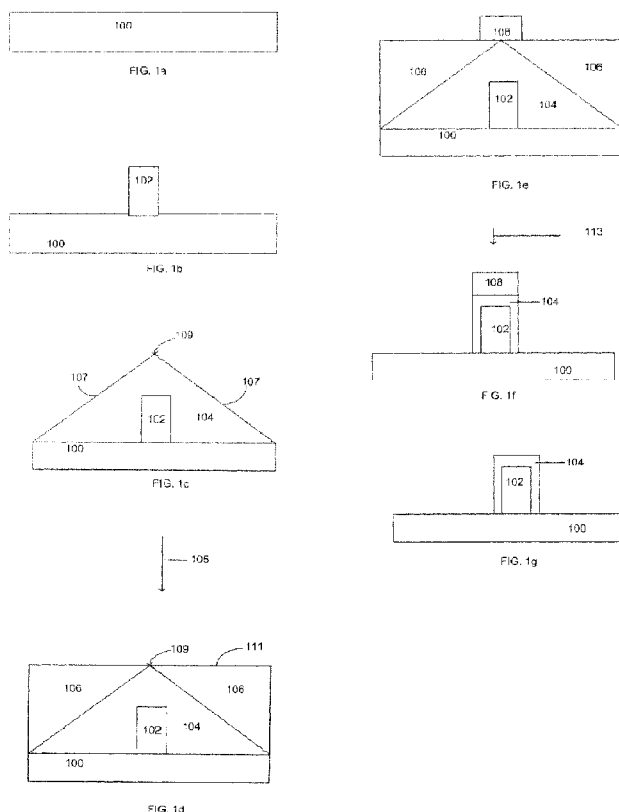
land, OR 97209 (US). KAVAILEROS, Jack [US/US]; 14260 NW Belle Court, Portland, OR 97229 (US). MUKHERJEE, Niloy [IN/US]; 7732 SW Carrollon Drive, Beaverton, OR 97007 (US). RADOSAVLJEVIC, Marko [US/US]; 4129 NW Chaparral Ter., Beaverton, OR 97006 (US). CHAU, Robert S. [US/US]; 8875 SW 171st Avenue, Beaverton, OR 97006 (US). SHAH, Uday [NP/US]; 13409 NW Keeton Park Lane, Portland, OR 97229 (US). DEWEY, Gilbert [US/US]; 920 SE 58th Ave, Hillsboro, OR 97123 (US). RAKSHIT, Titash [IN/US]; 319 NW Wildwood St, Hillsboro, OR 97124 (US). METZ, Mathew V. [US/US]; 18860 NW Aurora Pl., Portland, OR 97229 (US).

(74) **Agents:** VINCENT, Lester J. et al.; Blakely Sokoloff Taylor & Zafman, 1279 Oakmead Parkway, Sunnyvale, CA 94085 (US).

(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,

[Continued on next page]

(54) **Title:** MULTI-GATE III-V QUANTUM WELL STRUCTURES



(57) **Abstract:** Methods of forming microelectronic structures are described. Embodiments of those methods include forming a III-V tri-gate fin on a substrate, forming a cladding material around the III-V tri-gate fin, and forming a hi k gate dielectric around the cladding material.



HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ,

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

MULTI-GATE III-V QUANTUM WELL STRUCTURES

5 BACK GROUND

A variety of electronic and optoelectronic devices use thin film relaxed lattice constant III-V semiconductors on semiconductive substrates such as elemental silicon (Si) substrates. Surface layers capable of using the properties of III-V materials may host a variety of high performance electronic devices such as complementary metal oxide semiconductor (CMOS) and quantum well (QW) transistors.

10 BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming certain embodiments, the advantages of the various embodiments can be more readily ascertained from the following description of the embodiments when read in conjunction with the accompanying drawings in which:

FIGS. 1a-1g represent methods of forming structures according to an embodiment.

FIGS. 2a-2c represent methods of forming structures according to an embodiment.

FIGS. 3a-3c represent methods of forming structures according to an embodiment.

FIGS. 4a-4d represent methods of forming structures according to an embodiment.

20 FIGS. 5a-5d represent methods of forming structures according to an embodiment.

FIGS. 6a-6g represent methods of forming structures according to an embodiment.

FIG. 7 represents a system according to an embodiment.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, the specific embodiments which may be practiced. These
25 embodiments are described in sufficient detail to enable those skilled in the art to practice the embodiments. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented
30 within other embodiments without departing from their spirit and scope. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from their spirit and scope. The following detailed description is, therefore, not to be taken in a limiting sense, and the

scope of the embodiments is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the claims are entitled. In the drawings, like numerals refer to the same or similar functionality throughout the several views.

5

Methods and associated structures of forming and utilizing microelectronic structures, such as quantum well structures, are described. Those methods and structures may include forming a III-V tri-gate fin on a substrate, forming a cladding layer around the III-V tri-gate fin, and forming a hi k gate dielectric around the cladding layer. Various
10 embodiments included herein enable growth of a cladding layer around III-V fins to enable III-V tri-gate devices with high k dielectrics.

FIGS. 1a-1g illustrate embodiments of forming microelectronic structures, such as forming quantum well structures, for example. FIG. 1a illustrates a substrate 100. In one embodiment, the substrate 100 may comprise a silicon on insulator substrate (SOI) 100,
15 but may also include any type of suitable substrate material. A fin 102 may be formed on the substrate 100. The fin may comprise III-V materials, such as but not limited to InGaAs, InAs, and InSb (FIG. 1b). The fin 102 may comprise a portion of a trigate transistor, and may comprise a tri-gate fin 102.

A cladding material 104, which may comprise such materials as InP, AlInAs, AlInSb, for example, may be formed around the fin 102 (FIG. 1c). The cladding material 104 may comprise any suitable III-V material in some embodiments. The cladding material 104 may be formed by using an epitaxial technique, such as molecular beam epitaxy (MBE) or molecular orbital vapor phase epitaxy (MOVPE), or other conformal techniques such as atomic layer deposition (ALD), chemical vapor deposition (CVD),
25 sputtering, etc. In an embodiment, the cladding material 104 may form along specific crystalline planes, which may result in a triangular shape of the cladding material 104. The triangular cladding material 104 may comprise side portions 107 and a tip 109. In an embodiment, the cladding material 104 may undergo a dielectric formation process 105 (FIG. 1d), wherein a dielectric material 106, such as but not limited to an oxide, may be
30 formed/grown on the cladding material 104, such as by an oxidation, chemical vapor deposition process 105, for example. The dielectric material 106 may form on the sides 107 of the triangular shaped cladding material 104, such that a top surface 111 of the dielectric material 106 may be coplanar with the tip 109 of the triangular cladding material

104.

In an embodiment, a resist material 108 may be formed on/over the tip 109 of the cladding material 104, as well as over the fin 102 (FIG. 1e). In an embodiment, a removal process 113, such as a dielectric etching process and/or a chemical mechanical processing for example, may be performed in which the dielectric material 106 and a portion of the cladding material not covered by the resist material 108 may be removed (FIG. 1f). A rectangular portion of the cladding material 104 surrounds the fin 102 after the removal process 113. The resist material 108 may then be removed, wherein the rectangular portion of the cladding material 104 is exposed (FIG. 1g).

Thus the triangular cladding material 104 may undergo a series of dielectric formation and removal processes to form a more useful structure for the fin 102 of a quantum well tri-gate (non-planar) transistor structure, for example. In an embodiment, due to tri-gate architecture, the cladding material 104 physical thickness (and whole T_{oxe}) can be relaxed as compared to that in a planar device, while maintaining the same electrostatic integrity due to the three-dimensional nature of the tri-gate device. A high dielectric may be subsequently grown on the cladding material, in some embodiments.

In another embodiment, a trigate fin 202 may be disposed on a substrate 200 (similar to the fin 100 and substrate 100 of FIG. 1b, for example) (FIG. 2a). The trigate fin 202 may comprise a tri-gate channel of a trigate device, (wherein the tri-gate fin 202 comprises a top gate 203 and two side gates 205, 209) in an embodiment. A cladding material 204 may be formed on a top surface and on the sides of the fin/channel 202 (FIG. 2b). In an embodiment, the cladding material 204 may be formed according to a process similar to the processes depicted in FIGS (1a-1g) disclosed previously herein. The cladding material 204 may comprise any suitable III-V cladding material, in some embodiments. In an embodiment, the cladding material comprises a conformal cladding material layer around the tri-gate fin 202. A high k dielectric 207 (comprising a dielectric constant greater than about 4.0) may be formed on the cladding material 204 to form a trigate structure 215, and may comprise a high k gate dielectric 207 disposed on the tri-gate fin 202 (FIG. 2c). In an embodiment, the tri-gate structure 215 may further comprise a gate material and source/drain regions, similar to the trigate structure 315 of FIG. 3c, for example.

In an embodiment, the trigate structure 215 may comprise a portion of a III-V trigate quantum well device suitable for ultimate scalability of gate length and off-state

leakage while simultaneously preserving high mobility and high speed of the III-V quantum well device.. The high k dielectric 207 formed on the cladding material 204 may preserve high mobility of the tri-gate channel and may enable high speed of the tri-gate quantum well device. The III-V trigate quantum well architecture enables scaling (both
5 Ioff control and pitch/density scaling) and further enables high performance (high mobility) devices. The tri-gate structure 215 may be further optimized by combining re-growth for Rext (important in narrow fins), modulation halo (opposite sign dopants to further control Ioff) and multiple fin channels.

In another embodiment, a trigate fin 302 may be disposed on a substrate 300
10 (similar to the fin 202 and substrate 200 of FIG. 2a, for example) (FIG. 3a). The tri-gate fin 302 may comprise three sides. The tri-gate fin 302 may comprise a channel of a tri-gate device, in an embodiment. A high k dielectric 307 may be formed directly on the three sides of the tri-gate fin 302, to form a tri-gate structure 315, and may comprise a high k gate dielectric 307 disposed on the tri-gate channel 302 (FIG. 3b). In an embodiment, the
15 trigate structure 315 may comprise a portion of a III-V tri-gate quantum well device. FIG. 3c depicts an embodiment wherein a gate material 309 is formed on the three gate dielectric layers 307 around the three sides of the trigate fin 302, and source/drain regions 310 are disposed adjacent the gate material 309. In an embodiment, the high-k dielectric 307 formed directly on the channel 302 may improve for effective oxide thickness (EOT)
20 scaling. The EOT may be reduced, and the short channel effect improved resulting in ability to further reduce gate length of the device and increase the density of the transistors packed on the chip and the microprocessor complexity and functionality. The high k dielectric 307 may be formed by an atomic level deposition (ALD) process in some cases.

In another embodiment, a trigate fin 402 may be disposed on a substrate 400
25 (similar to the fin 202 and substrate 200 of FIG. 2a, for example) (FIG. 4a). The trigate fin 402 may comprise a tri-gate channel of a trigate quantum well device, in an embodiment, and may comprise a top surface 403. A top barrier material 408 may be formed on the top surface 403 of the tri-gate fin 402 (FIG. 4b). The top barrier material 408 may comprise AlInAs, AlInSb, AlGaAs and InP. A portion 410 of the top barrier material 408 may be
30 delta doped, wherein a monolayer of dopant atoms such as Si, S or Te in the case of an n-channel device and Be or C in the case of a p-channel device are incorporated into the barrier material 408. These dopants are physically separate (remote) from the quantum well but due to band bending in this structure provide free carriers to the quantum well

channel 402 (FIG. 4c).

A high k dielectric 407 may be formed on the top barrier material 408 and on the sides of the fin 402 (FIG. 4d) to form the tri-gate structure 415, that may comprise a portion of a III-V tri-gate quantum well device. The delta doping of the tri-gate structure
5 415 improves the mobility of the device, and enables better contact resistance to quantum well 402 due to band bending thru the layer 408 as enabled by the delta doping layer 410. The quantum well tri-gate structure 415 with delta doping above the channel 402 may comprise a quantum well planar growth and ALD high-K formation without a need for technically difficult epitaxial growth on the sides of the III-V trigate quantum well channel
10 402. In an embodiment, the tri-gate structure 415 may further comprise a gate material and source/drain regions, similar to the tri-gate structure 315 of FIG. 3c, for example.

In another embodiment, a trigate fin 502 may be disposed on a substrate 500 (similar to the fin 202 and substrate 200 of FIG. 2a, for example) (FIG. 5a). The trigate fin 502 may comprise a channel of a tri-gate device, in an embodiment. A cladding material
15 504 may be formed on a top surface and on the sides of the fin/channel 502 (FIG. 5b). In an embodiment, the cladding material 504 may be formed according to a process similar to the processes depicted in FIGS (1a-1g) disclosed previously herein. The cladding material 504 may comprise a material similar to the cladding material 104 of FIG. 1c, for example. In an embodiment, the cladding material 504 comprises a conformal cladding material
20 layer around the tri-gate fin 502.

A portion 510 of the cladding material 504 may be delta doped, wherein monolayer of dopant atoms such as Si, S or Te in the case of n-channel devices and Be or C in the case of p-channel devices are incorporated in the cladding material 504. These dopants are physically separate (remote) from the quantum well but due to band bending
25 in this structure, they provide free carriers to the quantum well device (FIG. 5c).

The portion 510 may comprise a top barrier/interfacial layer with delta doping 510 in some cases. A high k dielectric 507 may be formed on the delta doped cladding material 504 to form a tri-gate structure 515, and may comprise a high k gate dielectric 507 disposed on the tri-gate fin/channel(s) 502 (FIG. 5d). The tri-gate structure 515 may
30 comprise a portion of a quantum well tri-gate device 515 with delta doping 510 surrounding the tri-gate channel 502. The tri-gate device 515 may comprise conformal re-growth of top barrier 510 and ALD high-K in some cases. The tri-gate structure 515 may increase to the mobility and performance and reduce the Rc of the to max speed and

performance of the tri-gate device. In an embodiment, the tri-gate structure 515 may further comprise a gate material and source/drain regions, similar to the trigate structure 315 of FIG. 3c, for example.

FIG. 6a depicts a first substrate 600. The first substrate may comprise any type of substrate that may support a nanowire structure. In an embodiment, the second substrate 600 may comprise an InP material, but may comprise other materials such as but not limited to AlInAs, AlInSb, AlGaAs. A first nanowire layer 610 may be formed/placed on the first substrate 600 (FIG. 6b). The first nanowire layer 610 may comprise a gate/all around tri-gate channel. In an embodiment, the first nanowire layer may comprise a III-V material, such as but not limited to InGaAs, InSb, InAs, GaAs, for example. In an embodiment, the first substrate 600 may be lattice matched with the first nanowire 610, yet may be chemically different than the first nanowire layer 610.

A second substrate 600' may be formed/placed on the first nanowire layer 610 (FIG. 6c). In an embodiment, the second substrate 600 may comprise an InP material, but may comprise other materials AlInAs, AlInSb, AlGaAs. A second nanowire layer 610' may be placed/formed on the second substrate 600' (FIG. 6d). In an embodiment, the second substrate 600' may be lattice matched with the second nanowire 610' yet may be chemically different than the second nanowire layer 610. In an embodiment, the second nanowire layer may comprise a III-V material, such as but not limited to InGaAs, InSb, InAs, GaAs, for example. The stacked substrates/channels 600, 610, 600', 610' may comprise side portions 611. In some embodiments, more than two sets of stacked substrates/channels may be stacked upon each other to form a stacked structure 612 comprising any number of channels, according to the particular design requirements.

Source/drain regions 640 may be formed on the side portions 611 of the stacked channels/substrates 600, 610, 600', 610' (FIG. 6e). The substrates 600, 600' may be removed from the stacked substrate channels 600, 610, 600', 610' through a selective etching process 620 (FIG. 6f) to form a stacked channel tri-gate structure 615. In an embodiment, the stacked channel tri-gate structure may comprise a portion of a quantum well device. In an embodiment, a gap 616 separates the first nanowire channel 610 and the second nanowire channel 610', and the source/drain regions 640 are disposed on side portions 618, 617 of the first nanowire channel 610 and the second nanowire channel 610'. Chemistries may be chosen that may undercut and generate the stacked tri-gate structure 615. The channel fins 610, 610' may be anchored to the source/drain regions 640, while

the substrates 600, 600' may be selectively etched out from the sides of the suspended structure.

The channel structures 610, 610' possess improved scalability, and stacking several channels in a vertical structure increases the current per unit design footprint.

5 Because of III-V high mobility/lower Rext, the stacked tri-gate structure 615 increases access to more channels than in prior art tri-gate structures, such as silicon based structures. In another embodiment, a first cladding layer 620 and a second cladding layer 620' may be formed on the first and second channels 610, 610' respectively, and a first high k dielectric gate material 621 and a second high k dielectric material 621' may be
10 formed on the first and second cladding layers 620, 620' respectively, of the stacked tri-gate structure 615 (FIG. 6g).

The cladding layers and high k dielectric layers may be formed around the channels 610, 610' (depicted as disposed on top and bottom surfaces of the channels 610, 610' in FIG. 6g).

15 FIG. 7 shows a computer system according to an embodiment. System 700 includes a processor 710, a memory device 720, a memory controller 730, a graphics controller 740, an input and output (I/O) controller 750, a display 752, a keyboard 754, a pointing device 756, and a peripheral device 758, all of which may be communicatively coupled to each other through a bus 760, in some embodiments. Processor 710 may be a
20 general purpose processor or an application specific integrated circuit (ASIC). I/O controller 750 may include a communication module for wired or wireless communication. Memory device 720 may be a dynamic random access memory (DRAM) device, a static random access memory (SRAM) device, a flash memory device, or a combination of these memory devices. Thus, in some embodiments, memory device 720
25 in system 700 does not have to include a DRAM device.

One or more of the components shown in system 700 may include one or more tri-gate devices of the various embodiments included herein. For example, processor 710, or memory device 720, or at least a portion of I/O controller 750, or a combination of these components may include in an integrated circuit package that includes at least one
30 embodiment of the structures herein.

These elements perform their conventional functions well known in the art. In particular, memory device 720 may be used in some cases to provide long-term storage for the executable instructions for a method for forming structures in accordance with some

embodiments, and in other embodiments may be used to store on a shorter term basis the executable instructions of a method for forming structures in accordance with embodiments during execution by processor 710. In addition, the instructions may be stored, or otherwise associated with, machine accessible mediums communicatively
5 coupled with the system, such as compact disk read only memories (CD-ROMs), digital versatile disks (DVDs), and floppy disks, carrier waves, and/or other propagated signals, for example. In one embodiment, memory device 720 may supply the processor 710 with the executable instructions for execution.

System 700 may include computers (e.g., desktops, laptops, hand-helds, servers,
10 Web appliances, routers, etc.), wireless communication devices (e.g., cellular phones, cordless phones, pagers, personal digital assistants, etc.), computer-related peripherals (e.g., printers, scanners, monitors, etc.), entertainment devices (e.g., televisions, radios, stereos, tape and compact disc players, video cassette recorders, camcorders, digital cameras, MP3 (Motion Picture Experts Group, Audio Layer 3) players, video games,
15 watches, etc.), and the like.

Benefits of the embodiments included herein include the enablement of quantum well III-V tri-gate technology. The embodiments enable high mobility, EOT scaling, Rext reduction, improved scalability for both Ioff control and pitch/density scaling and enabling of high performance, high mobility devices.

20 Although the foregoing description has specified certain steps and materials that may be used in the embodiments, those skilled in the art will appreciate that many modifications and substitutions may be made. Accordingly, it is intended that all such modifications, alterations, substitutions and additions be considered to fall within the spirit and scope of the embodiments as defined by the appended claims. In addition, it is
25 appreciated that various microelectronic structures, such as transistor devices, are well known in the art. Therefore, the Figures provided herein illustrate only portions of an exemplary microelectronic structure that pertains to the practice of the embodiments. Thus the embodiments are not limited to the structures described herein.

IN THE CLAIMS

What is claimed is:

5

1. A method comprising:

forming a III-V material fin on a substrate;

forming a triangular cladding material on the III-V material fin;

forming an oxide on the triangular cladding material; and

10

forming a rectangular cladding material around the III-V material
fin.

2. The method of claim 1 further comprising wherein the rectangular cladding
material comprises a III-V cladding material disposed on a top surface and the
sides of the III-V material fin.

15

3. The method of claim 1 wherein forming the rectangular cladding material
comprises:

forming a resist material on the oxide over the III-V material fin;

20

etching the cladding material; and

removing the resist.

4. The method of claim 1 further comprising wherein the III-V material fin
comprises a III-V tri-gate channel of a quantum well device.

25

5. The method of claim 4 further comprising forming a high k dielectric on
the rectangular cladding material, wherein the high k dielectric comprises a hi k
gate dielectric.

30

6. The method of claim 4 further comprising forming a delta doped barrier on
the cladding material surrounding the III-V tri-gate channel.

7. A method comprising:

forming a III-V tri-gate fin on a substrate; and
forming a hi k dielectric directly on the III-V tri-gate fin.

- 5 8. The method of claim 1 wherein forming the III-V tri-gate fin further
comprises forming a top barrier with delta doping on a top surface of the III-V tri-
gate fin.
- 10 9. A method comprising:
forming a III-V tri-gate fin on a substrate;
forming a cladding layer around the III-V tri-gate fin; and
forming a hi k gate dielectric around the cladding layer.
- 15 10. A method comprising:
forming a first nanowire channel on a first substrate;
forming a second substrate on the first nanowire channel;
forming a second nanowire channel on the second substrate to form
a stacked structure;
forming source/drain regions on side portions of the stacked
20 structure; and
removing the first and second substrates to form a stacked channel
tri-gate structure.
- 25 11. The method of claim 10 further comprising:
forming a cladding layer on the first and second nanowire channels; and
forming a high k dielectric on the cladding layer.
- 30 12. The method of claim 10 further comprising:
forming a cladding layer on the first and second nanowire channels; and
forming a high k dielectric on the cladding layer.
13. The method of claim 10 wherein removing the first and second substrates
comprises selectively etching the first and second substrates from the stacked

structure.

14. The method of claim 10 further comprising wherein the first substrate and the first channel are latticed matched, and wherein the second substrate and the second nanowire are lattice matched.

15. The method of claim 10 further comprising wherein the first and second nanowire channels comprise III-V tri-gate channels, and wherein the first and second substrates comprise InP.

16. The method of claim 10 further comprising wherein the stacked channel tri-gate structure comprises a portion of a quantum well device.

17. A structure comprising:
a III-V tri-gate fin disposed on a substrate; and
a cladding layer disposed on a top surface and on side portions of the III-V tri-gate fin.

18. The structure of claim 17 wherein the III-V tri-gate fin comprises at least one of InGaAs, InAs, InSb, and GaAs.

19. The structure of claim 17 further comprising a hi k gate dielectric layer disposed around the cladding layer, wherein the structure comprises a quantum well device.

20. A structure comprising:
a III-V trigate fin disposed on a SOI substrate;
a cladding layer disposed on and around the III-V tri-gate fin;
a barrier interfacial layer disposed on the cladding layer around the III-V tri-gate fin; and
a hi k gate dielectric disposed on the barrier interfacial layer.

21. The structure of claim 20 wherein the III-V tri-gate fin comprises a tri-gate

channel.

22. The structure of claim 20 wherein the barrier interfacial layer comprises delta doping.

5

23. The structure of claim 20 wherein the III-V tri-gate fin comprises InGaAs, and wherein the structure comprises a quantum well structure.

24. A structure comprising:

10

a III-V trigate fin disposed on a SOI substrate; and
a hi k dielectric disposed directly on the III-V tri-gate fin.

25. The structure of claim 24 further comprising a system, wherein the system comprises:

15

a bus communicatively coupled to the structure; and
a DRAM communicatively coupled to the bus.

26. The structure of claim 24 wherein the structure comprises a portion of a quantum well device.

20

27. A structure comprising:

a III-V tri-gate fin disposed on a substrate;
a top barrier disposed on a top surface of the III-V trigate fin; and
a hi k gate dielectric disposed directly on the top barrier and directly on the
sides of the III-V tri-gate fin.

25

28. The structure of claim 27 wherein the structure comprises a portion of a quantum well device.

30

29. The structure of claim 27 wherein the top barrier comprises delta doping.

30. A structure comprising:

a first nanowire channel disposed above a

a second nanowire channel;
a gap separating the first nanowire channel and the second nanowire
channel; and
source/drain regions disposed on side portions of the first nanowire
channel and the second nanowire channel.

5

31. The structure of claim 30 further comprising a first cladding
disposed on the first nanowire channel and a second cladding disposed on the
second nanowire channel.

10

32. The structure of claim 31 further comprising a first high k dielectric
disposed on the first cladding and a second high k dielectric disposed on
the second cladding.

15

33. The structure of claim 30 further comprising wherein the first and second
nanowire channels comprise III-V tri-gate channels.

34. The structure of claim 30 further comprising wherein the structure
comprises a quantum well device.

20

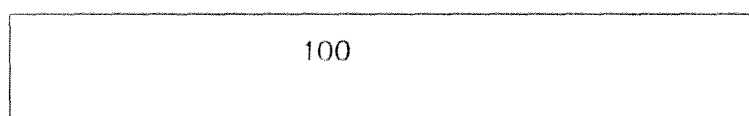


FIG. 1a

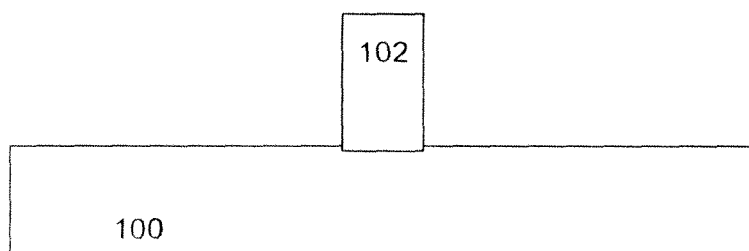


FIG. 1b

2/12

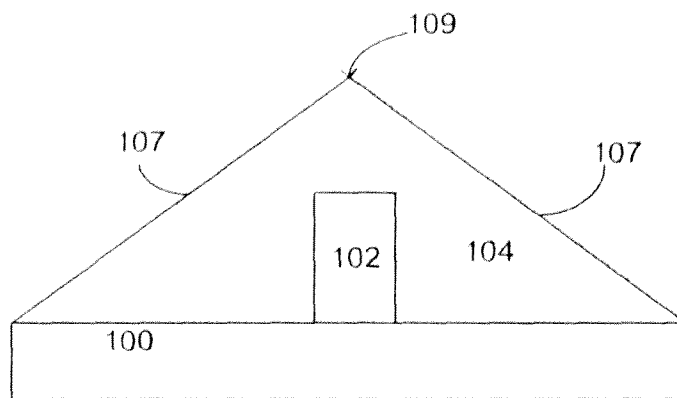


FIG. 1c

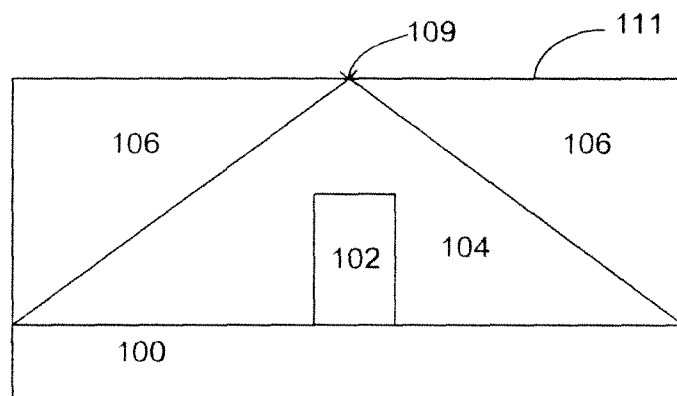
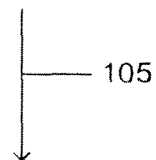


FIG. 1d

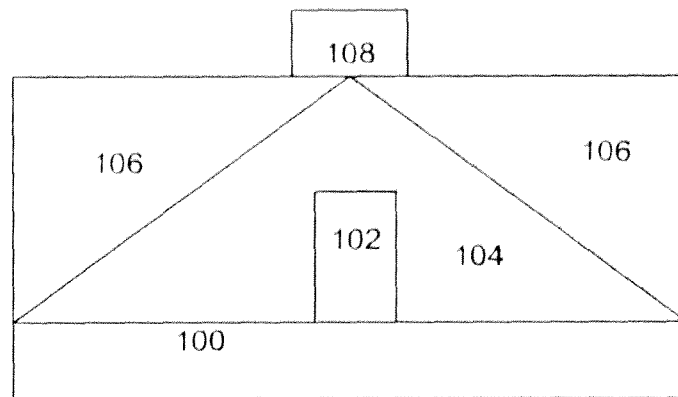


FIG. 1e

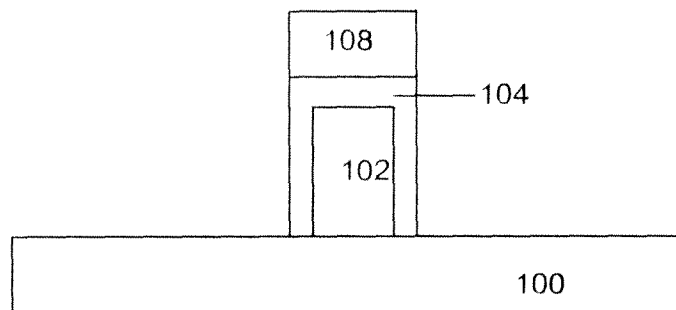


FIG. 1f

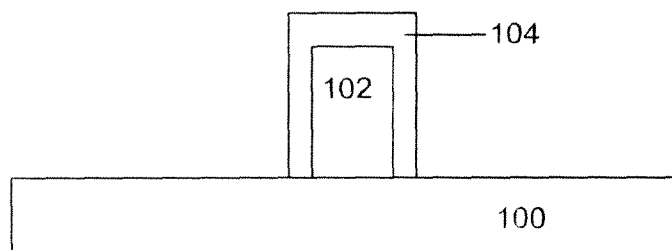


FIG. 1g

4/12

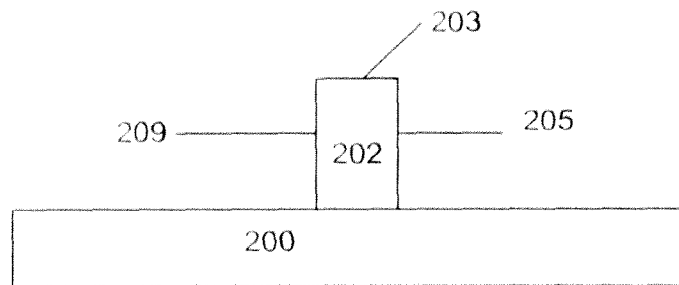


FIG. 2a

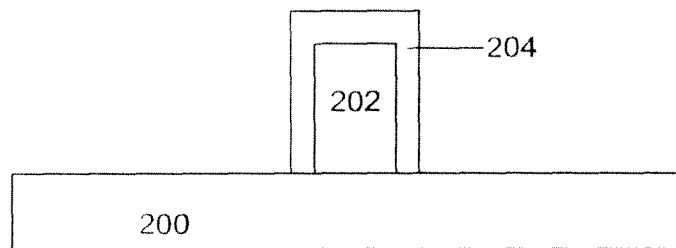


FIG. 2b

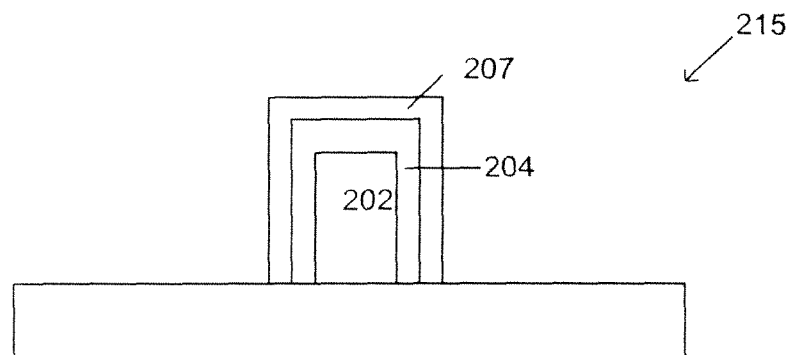


FIG. 2c

5/12

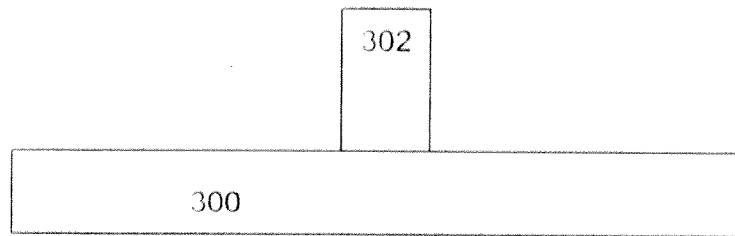


FIG. 3a

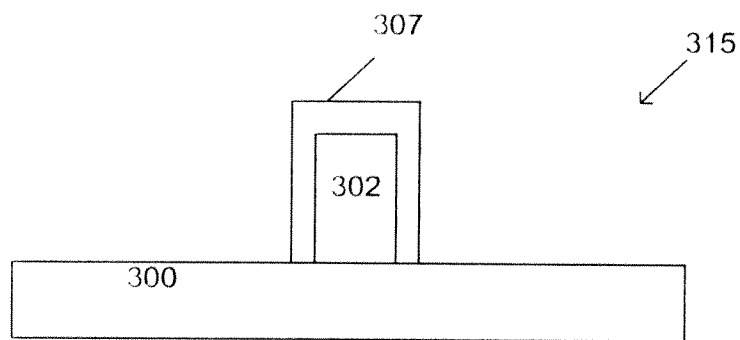


FIG. 3b

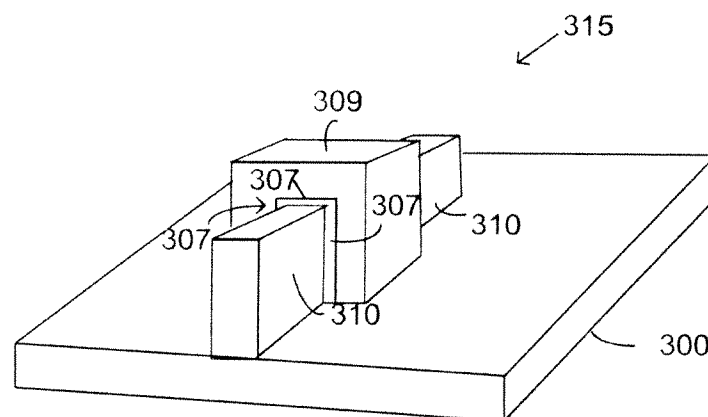


FIG. 3c

6/12

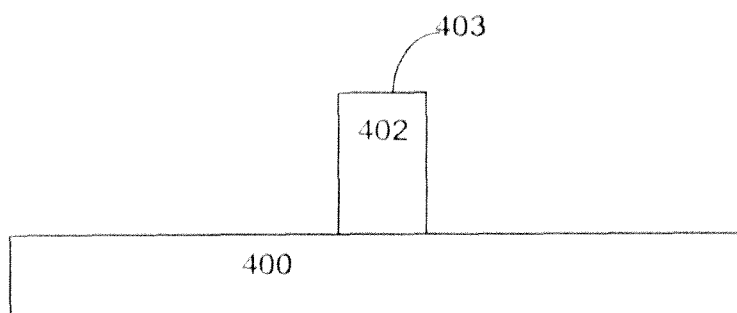


FIG. 4a

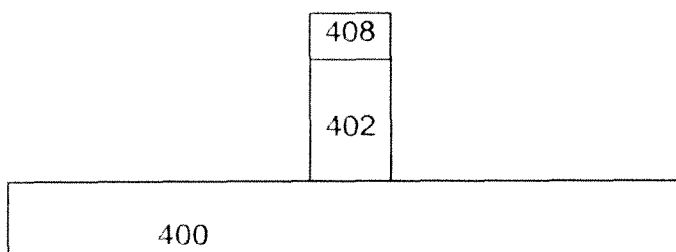


FIG. 4b

7/12

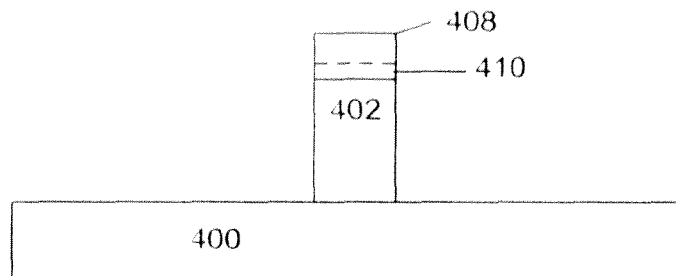


FIG. 4c

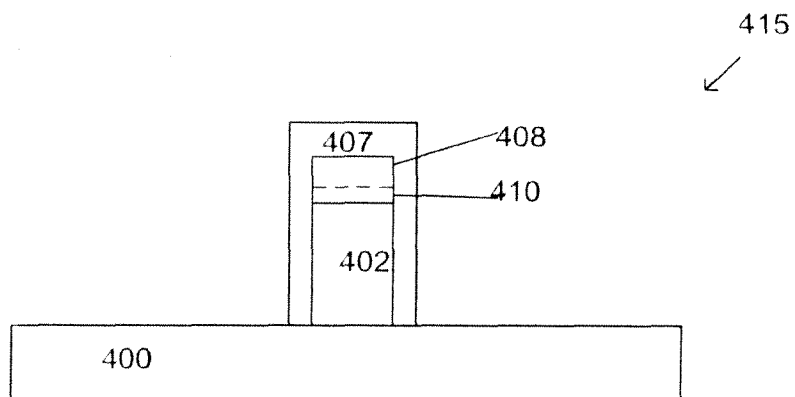


FIG. 4d

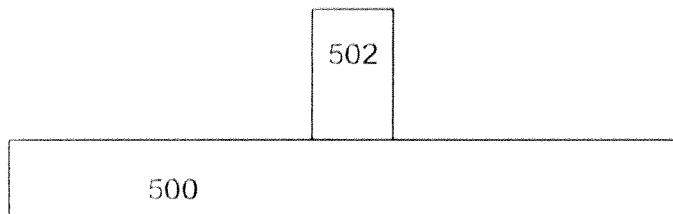


FIG. 5a

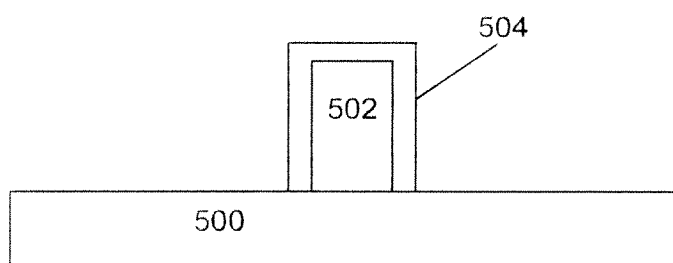


FIG. 5b

9/12

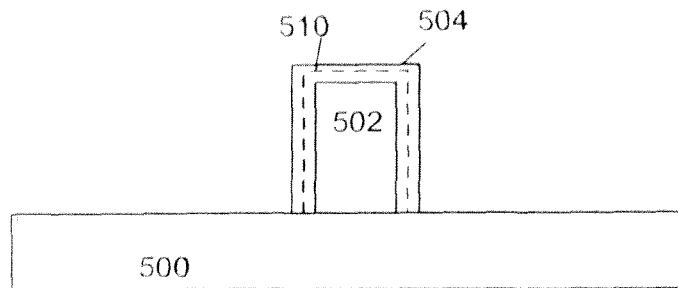


FIG. 5c

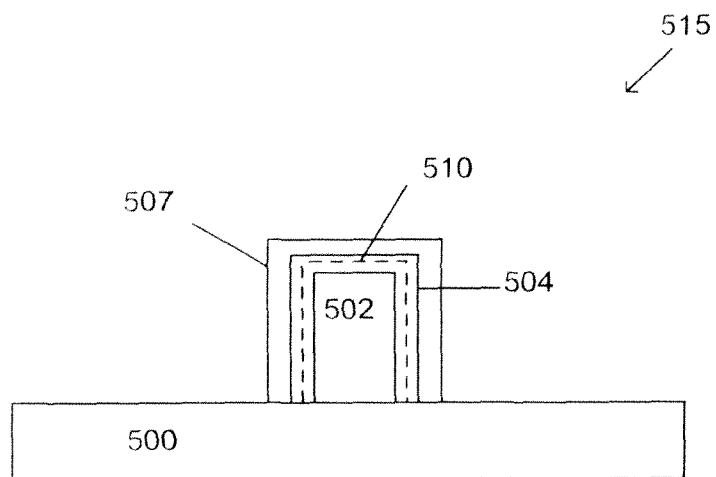


FIG. 5d



Fig. 6a

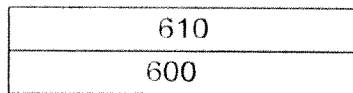


FIG. 6b

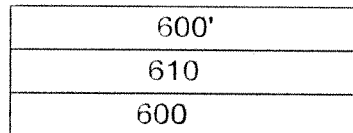


FIG. 6c

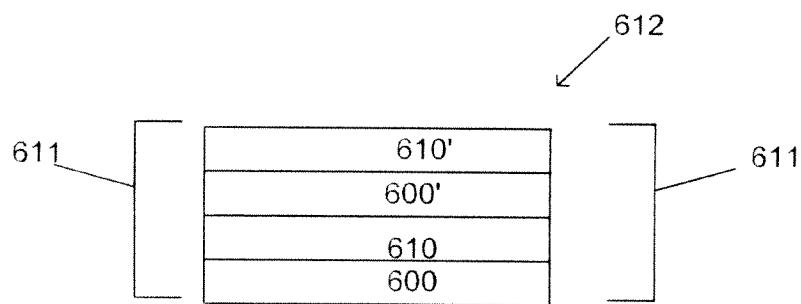
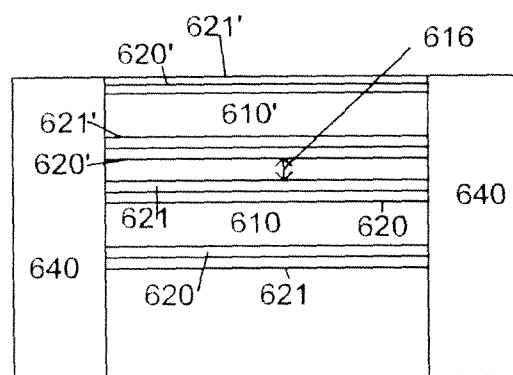
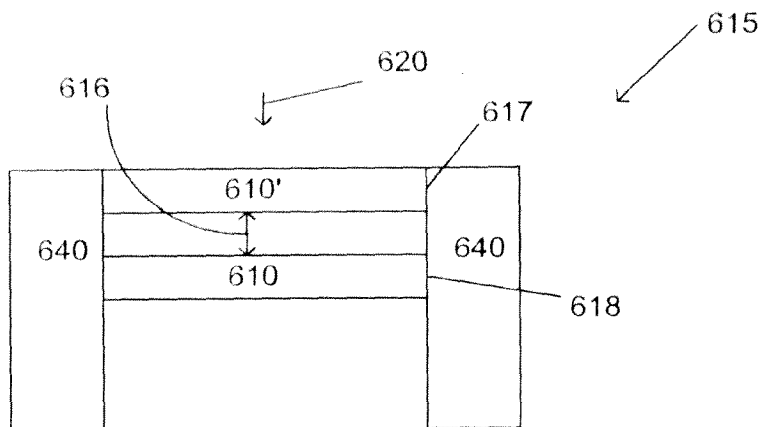
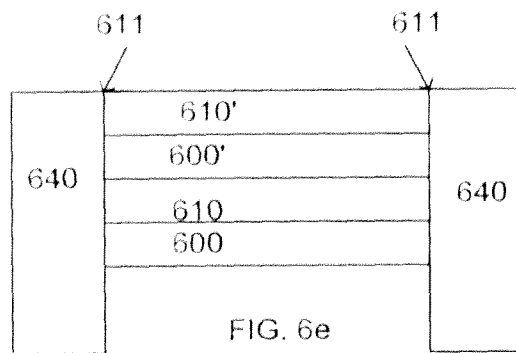


FIG. 6d

11/12



12/12

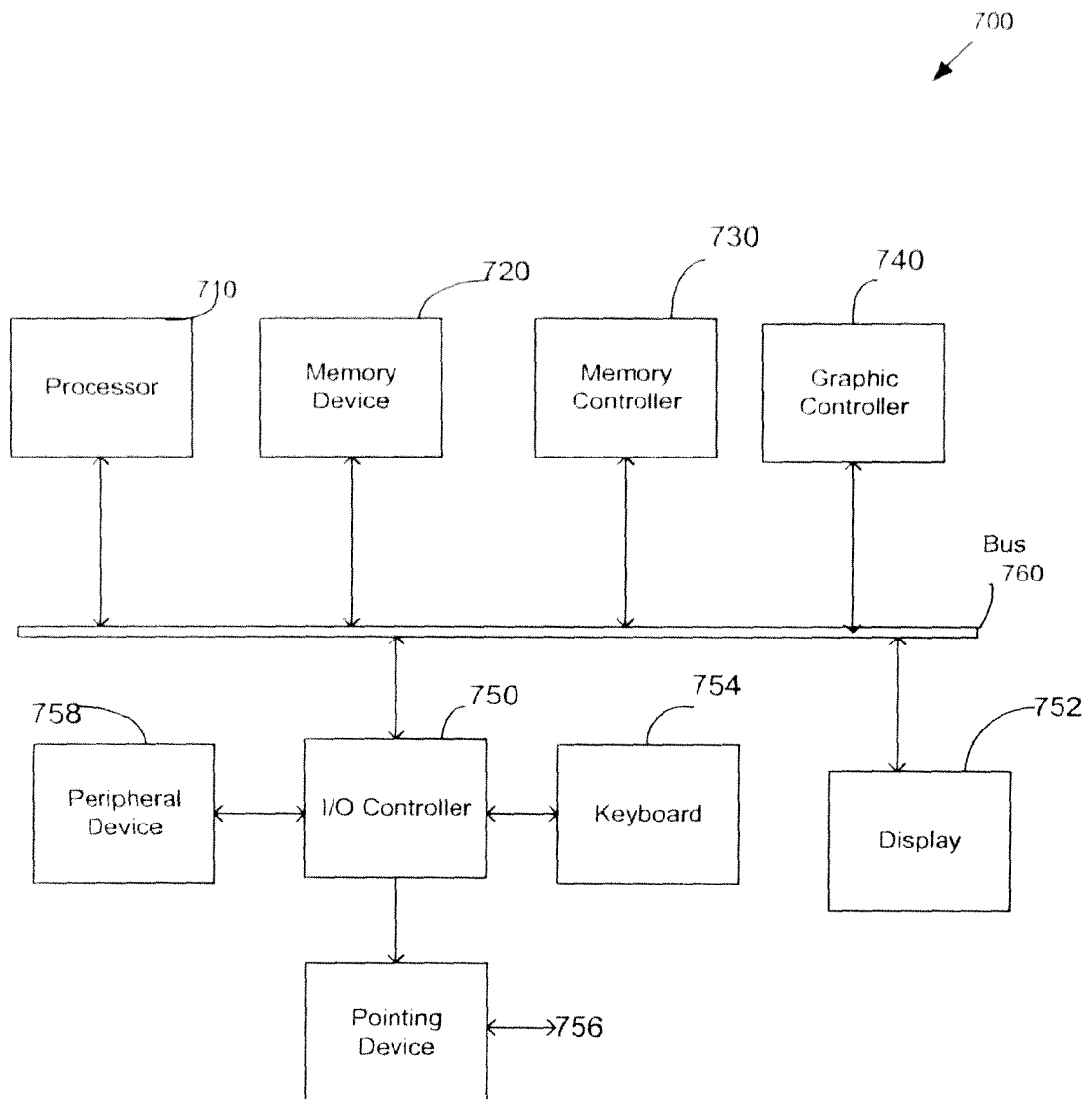


FIG. 7