

- [54] **PATROL TOUR SYSTEM**
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[51] Int. Cl.**G08b 25/00**
[58] Field of Search**340/147 P, 223, 286, 340/305, 306, 309.1, 311, 312, 313, 213.1, 409, 287**

[56] **References Cited**

UNITED STATES PATENTS			
3,577,079	5/1971	Horstmann	340/306 X
3,579,221	5/1971	Ashley et al.	340/306 X
3,631,536	12/1971	Mosman	340/286 X

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[57] **ABSTRACT**
A patrol tour system for insuring that the tour station switches are operated in the proper sequence and within a predetermined amount of time by the guard making the tour which system comprises a common logic circuit for providing an indication of a delinquency in the time between the operation of the tour stations, an indication when the tour stations are operated out of a prescribed sequence, a tour in process indication, and a tour end indication, a status circuit having latching circuits connected to each of the tour station switches for prohibiting the repetitive reset of a common logic timing means by repetitive operation of only one of the tour station switches, and optionally a program circuit for establishing a predetermined sequence of operations of the tour stations.

20 Claims, 7 Drawing Figures

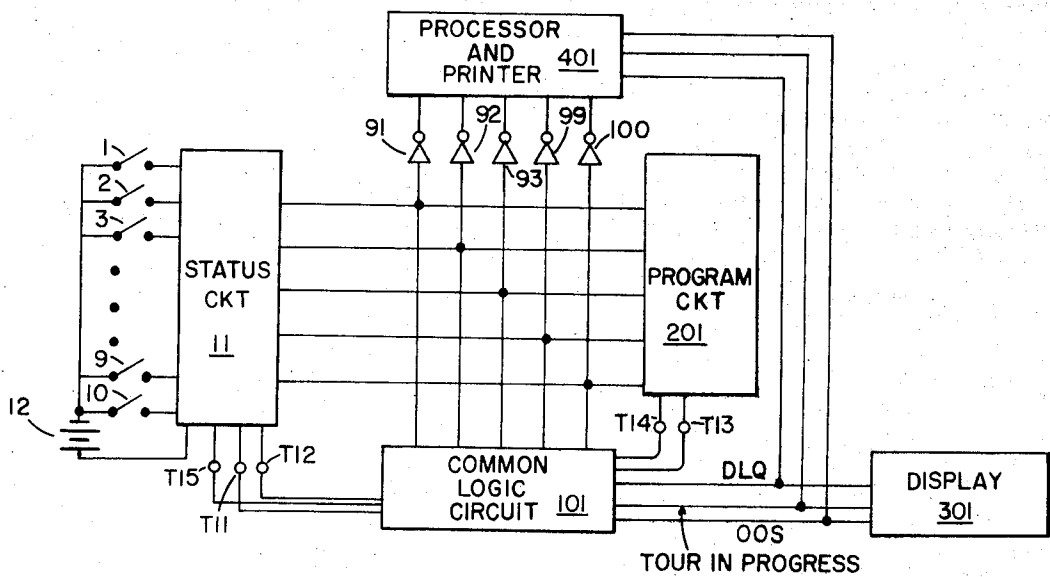


FIG. 1.

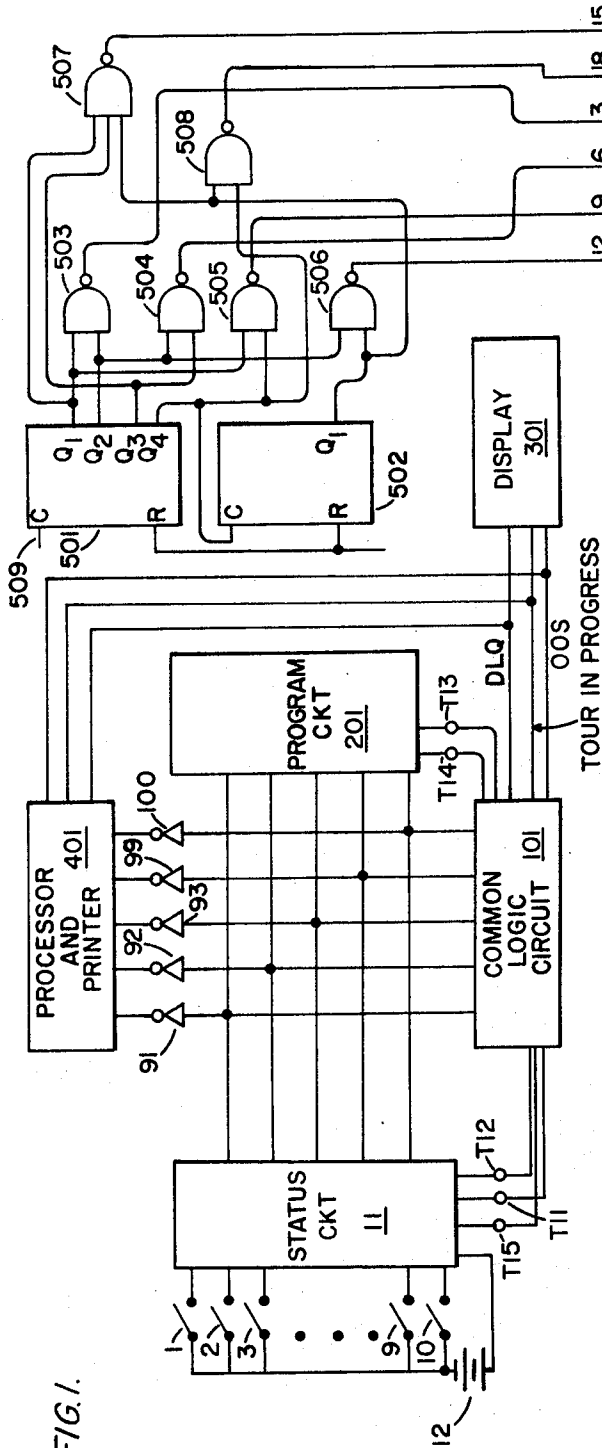


FIG. 7

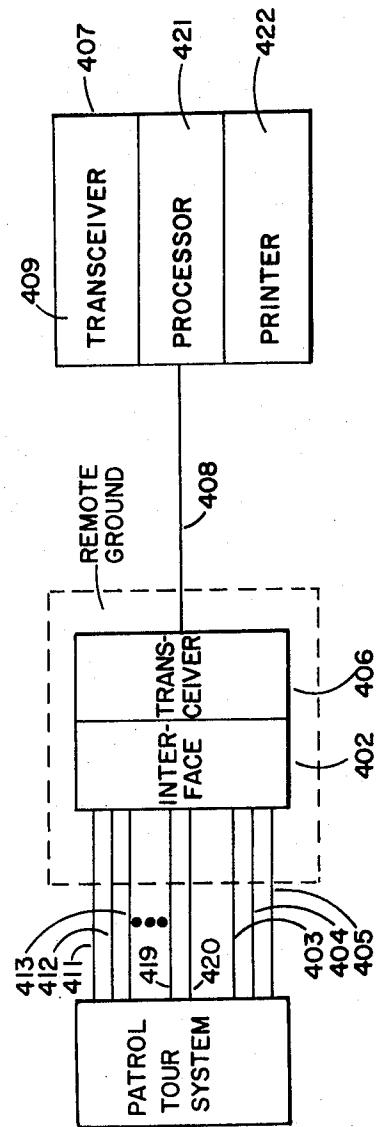
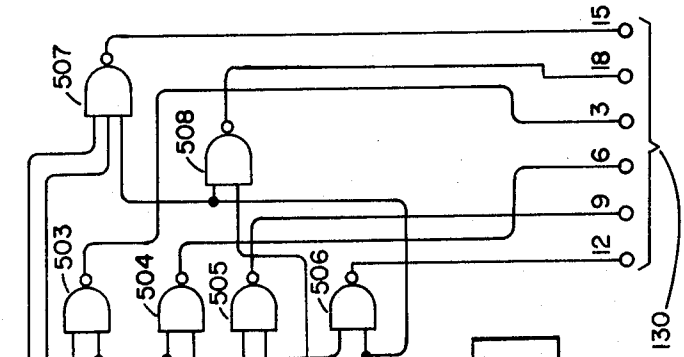
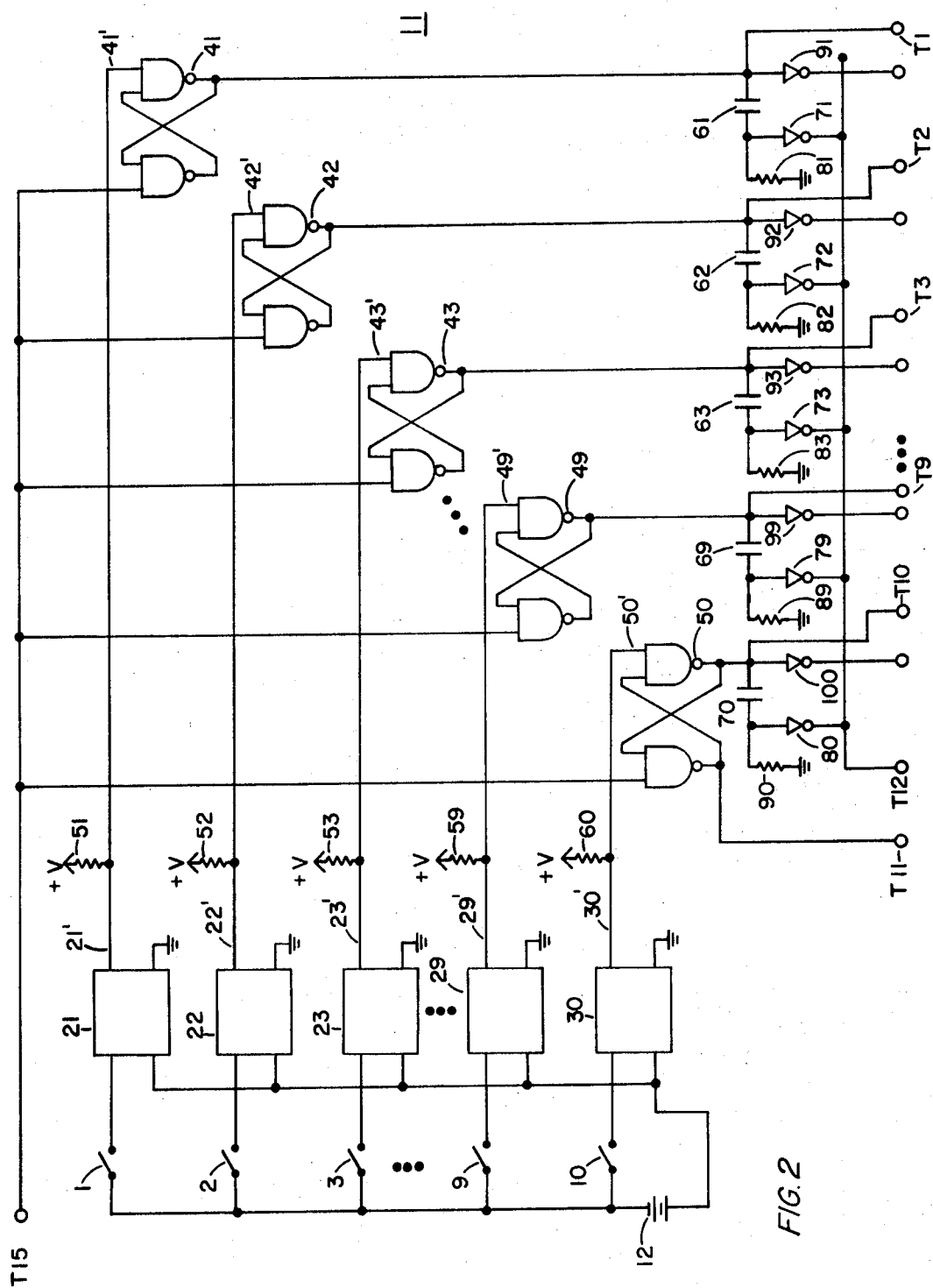
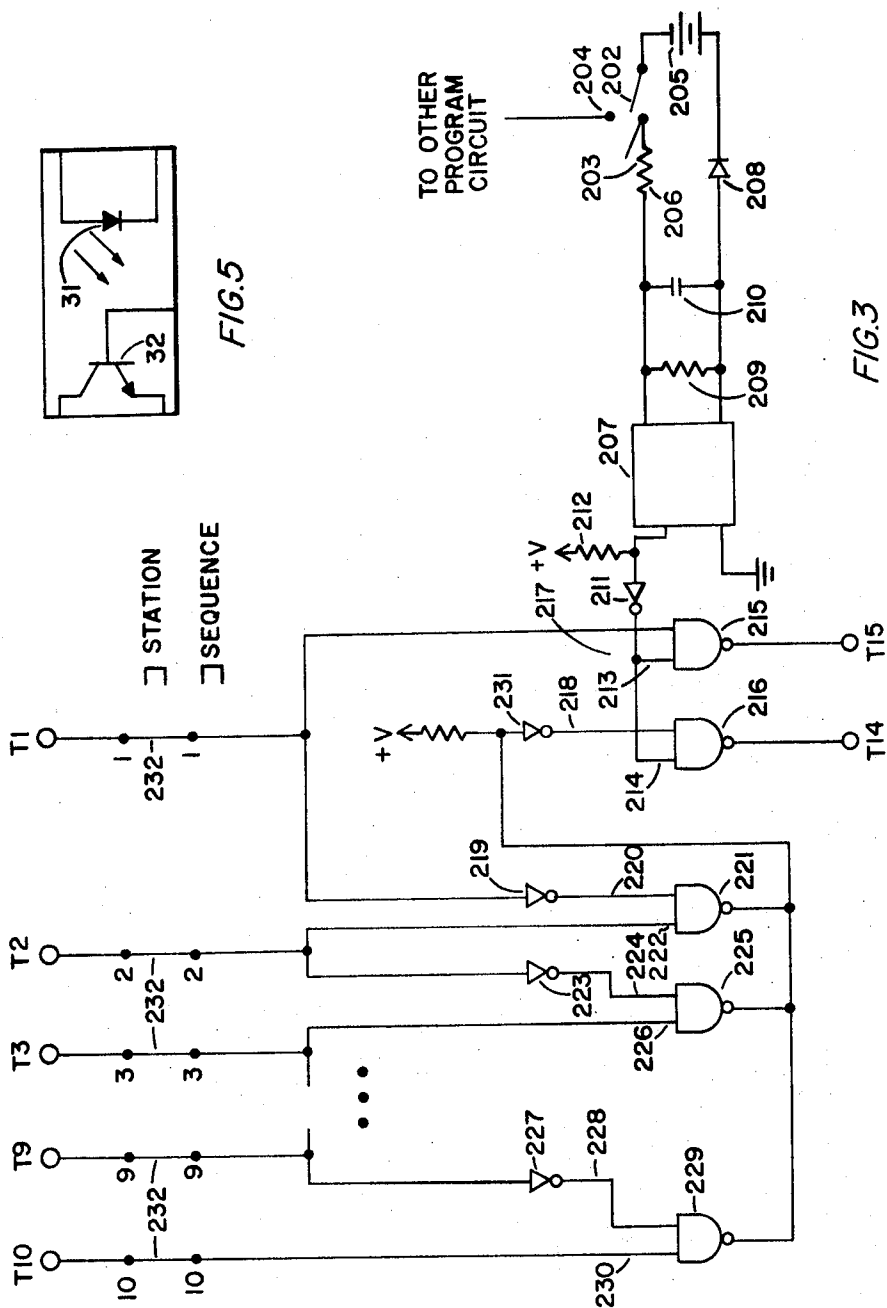


FIG. 6







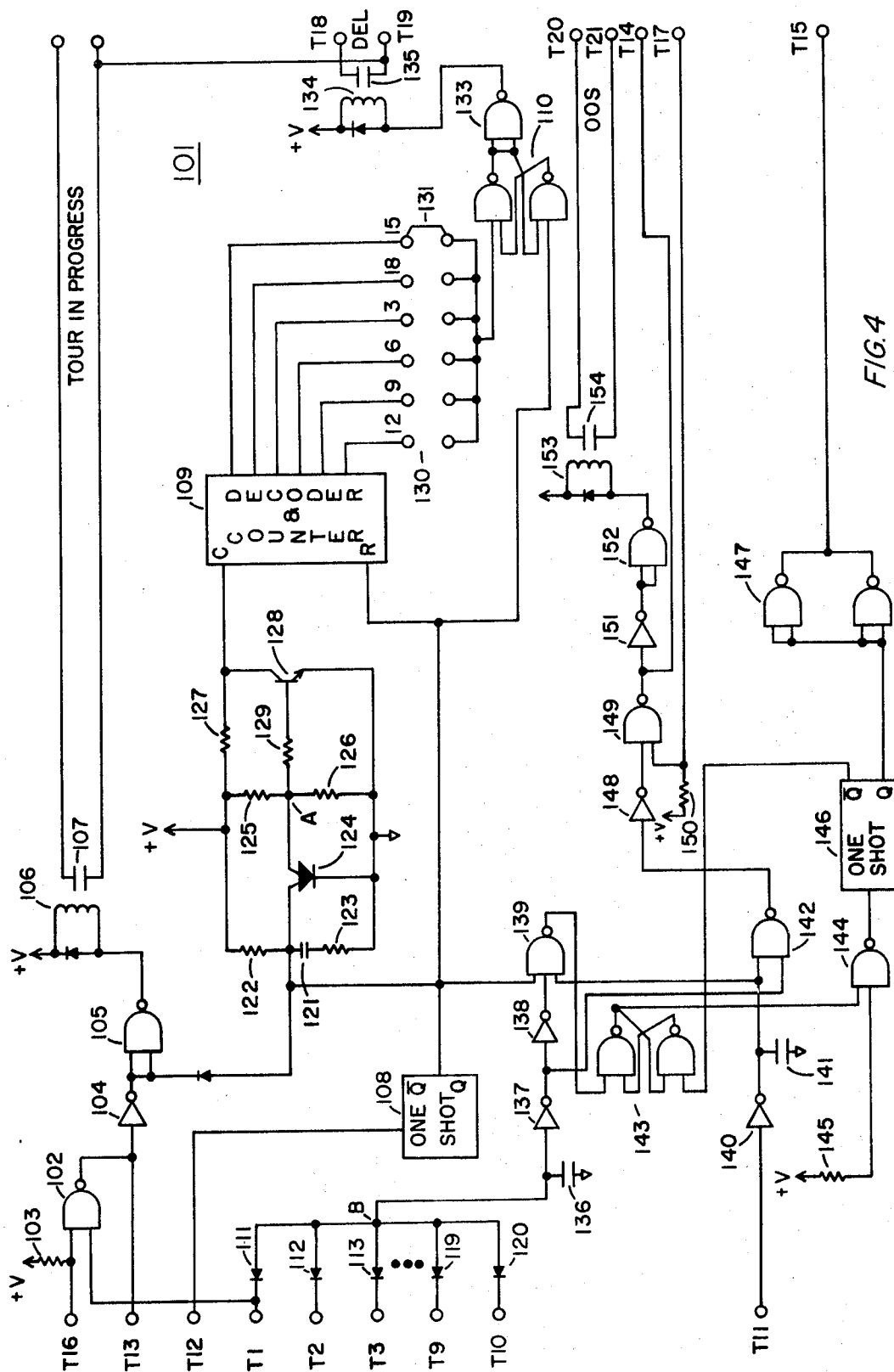


FIG. 4

PATROL TOUR SYSTEM

This invention involves a fire and/or security patrol system. The philosophy behind such a system is to insure that a guard, who is assigned the task of investigating predetermined locations, i.e., stations, within a building to insure that such locations are free from fire and in a secured status, properly conducts his tour (investigation).

To acknowledge that the guard has investigated the stations, a key switch is positioned at each tour station which the guard is to investigate. As the guard actuates the key switch, a latching circuit is operated such that further actuation of the switch will not affect the rest of the tour system. When the latching circuit is operated, a timer is reset. If the timer were not reset, i.e., were allowed to time out, a delinquency signal is provided on appropriate display apparatus. The timer would not be reset if the guard failed to operate a tour station switch within the prescribed amount of time.

The system is designed to operate with or without a program according to a prescribed sequence. If the system is to be operated without a program, the prescribed sequence is such that the guard must operate the first station first and the last station last. The intermediary stations can be operated in any sequence whatsoever. Upon the operation of the first station first, a tour in progress signal is provided on the display apparatus. If the first station is not operated first, this tour in progress signal is not provided. If the last station is not operated last, an out of sequence signal is provided.

With the use of a program, however, the prescribed sequence in which the stations are to be operated can be established according to a program and in any predetermined manner and, should any station be operated out of the prescribed sequence, an out of sequence signal is provided.

Furthermore, the outputs from the latching circuits are optionally connected to a processor and printer. The processor and printer can, for instance, provide a print out as each station is operated or a printout of a log of all stations which have been operated whenever an out of sequence or a delinquency has occurred.

The patrol tour system collects all of the information without use of a memory at the central station. In this manner, the printer or display apparatus need only indicate the occurrence of a delinquency or an out of sequence operation.

These and other features will be seen more clearly in the following detailed description of the drawings in which:

FIG. 1 is a block diagram of the patrol tour system.

FIG. 2 is a detailed schematic of the status circuit.

FIG. 3 is a detailed schematic of the program circuit.

FIG. 4 is a detailed schematic diagram of the common logic circuit.

FIG. 5 is a circuit diagram of the optical isolator used in the circuits of FIGS. 2 and 3.

FIG. 6 is a detailed representation of the counter and decoder used in the circuit of FIG. 4.

FIG. 7 is a block diagram showing how the patrol tour system can be mated with a data gathering system.

In FIG. 1, switches 1-10 represent the key switches located at the tour stations to be investigated by the patrolling guard. These switches are connected to the status card such that as each one of the switches is operated a signal is provided at terminal T12 which is con-

nected to the common logic circuit 101 to reset a timing apparatus within the logic circuit.

Reference numerals T1-T15 are used throughout the schematics to show the common connections between the circuits of FIGS. 2-4.

If a program circuit is used, the status switches 1-10 are connected through the status circuit to the program circuit. The program circuit 201 establishes the sequence in which stations 1-10 must be operated by the guard. When the first station which is programmed number 1 by the program circuit is operated, an output signal appears at terminal T13 which is connected to the common logic circuit to provide a tour in progress signal to the display apparatus 301. If any of the stations 1-10 are operated out of the sequence established by the program circuit, an output signal is produced at terminal T14 which is connected to the common logic circuit for providing an out of sequence signal (OOS) to the display apparatus 301.

The timing circuit located within the common logic circuit establishes a predetermined amount of time within which each tour station must be operated. If the time between operation of any two stations 1-10 exceeds the time preset by the timing circuit of the common logic circuit 101, a delinquency signal (DLQ) is provided by the common logic circuit to the display apparatus 301.

The operation and manner of use of the circuit shown in FIG. 1 is as follows:

The key switches 1-10 are positioned at those locations, e.g., rooms or areas, of a building to be investigated by a guard to insure that such locations are secured and free from fire. The remainder of the circuit shown in FIG. 1 is located at a central location within the building. Assuming that the proper sequence of operation of the key switches 1-10 is in the numerical order 1-10, the guard will proceed to conduct his tour at the proper time. Upon arrival at the first location, the guard will operate key switch 1 which causes a circuit in the status circuit 11 to latch. The latching of this circuit provides two functions. The first is to reset the delinquency timer apparatus of the common logic circuit 101. The second function is to use this latching output to determine if the stations are in the proper sequence. If a program card is used, this second function is provided by an output signal from the status circuit to the program circuit 201.

Upon operation of station number 1, the status circuit latching means will provide an output to the program circuit 201. This output is used to provide an output from program circuit 201 to terminal T13. This signal is then supplied to the common logic circuit 101 to provide the tour in progress signal to the display apparatus 301.

After the timer in the common logic 101 has been reset, it begins a new timing operation. The guard then proceeds to location number 2. If the timer apparatus in the common logic circuit 101 times out before the guard reaches station number 2, a delinquency signal is provided to the display apparatus 301. However, if the guard reaches station number 2 and operated its associated key switch within the time allotted him by the timing circuit in the common logic circuit 101, the corresponding latching circuit in the status circuit 11 is operated to reset the timer of the common logic circuit 101 and to provide an output to the program circuit 201.

If the guard omits station number 3 in his tour and instead proceeds to station number 4 and operates the key switch there, the latching circuit, associated with station 4, in the status circuit 11 will be operated to reset the timer apparatus in the common logic circuit 101. However, the latching of this circuit will also provide an output to the program circuit 201 which will sense the failure to operate station 3 in its prescribed sequence. As a result, the program circuit 201 will provide an output on terminal T14 to the common logic circuit 101 to provide a delinquency output to display apparatus 301.

Upon proper operation of stations 1-10 by the guard making his tour, the operation of the last station 10 will cause status circuit 11 to provide an output on terminal T11 which is supplied to the common logic circuit 101 to provide a reset circuit signal. This reset circuit signal is supplied from the common logic circuit 101 to terminal T15 and then to the status circuit 11 to reset all of the latching circuits contained therein. At this point, the circuit is ready for the guard to begin a new tour.

When discussing the details of the status circuit 11, the common logic circuit 101 and the program circuit 201, reference numerals T1-T15 are redundantly used throughout these three circuits to show the common connections between the circuits of FIGS. 2-4.

STATUS CIRCUIT

FIG. 2 shows in more detail the status circuit 11 shown in block form in FIG. 1. A positive terminal of battery 12 is connected to the movable contacts of tour station switches 1-10 the stationary contacts of which are connected to one of the input lines of their respective optical isolators 21-30. The other input line to optical isolators 21-30 are all connected together and to the negative terminal of battery 12.

FIG. 5 shows the optical isolator which comprises a light emitting diode 31 and a light responsive transistor 32. When the diode 31 is supplied with current, it gives off light which causes the transistor 32 to conduct. When placed in one of the boxes 21-30 of FIG. 2, the light emitting diode is connected between the input lines from the switches 1-10 and battery 12 and the collector emitter circuit of the transistor is connected between the output line and the ground terminal which is shown in FIG. 2. The output lines 21'-30' from optical isolators 21-30 are connected to respective latching circuits 41-50.

Each latching circuit comprises two interconnected Nand gates whose output is normally low and which goes high upon the application of a low signal to their respective input terminals 41'-50'. Each output line 21'-30' is connected to a +V source through a respective resistor 51-60. Thus, when the transistor and the optical isolator is de-energized, the inputs 41'-50' to latches 41-50 are normally in a high condition such that the outputs from these latches are normally in a low condition.

The outputs from latches 41-50 are directly connected to terminals T1-T10 which are connected to input terminals T1-T10 of FIG. 3 and terminals T1-T10 of FIG. 4.

Additionally, the outputs from latches 41-50 are connected through capacitors 61-70 and inverters 71-80, respectively, to an output terminal T12. Resistors 81-90 are connected from the junctions of their respective capacitors 61-70 and inverters 71-80 to

ground. The capacitors function to give a short pulse on terminal T12 whenever one of the outputs from latching circuits 41-50 go high. As will be seen hereinafter, a pulse on terminal T12 resets the timing apparatus of the common logic circuits 101.

As can be seen from FIGS. 1 and 2, the output from latches 41-50 are also connected through inverters 91-100 to the processor and printer apparatus 401.

PROGRAM CIRCUIT

FIG. 3 shows the program circuit which can be used with the disclosed patrol tour system. If it is desired to operate the system without a program, then the prescribed sequence becomes such that the first station must be operated first, the last station must be operated last, and the intermediary stations can be operated in any sequence whatsoever. However, when using a program circuit, either of two program circuits can be used depending upon the position of switch 202. Thus, two different sequences can be established for the patrol tour system. If the switch 202 is closed on stationary contact 203, the program circuit shown in FIG. 3 is selected. However, if the switch 202 is in an upper position against stationary contact 204, the other program circuit, not shown, is selected. The other program circuit is merely connected in parallel to the one shown in FIG. 3. If it is desired to have the guard operate the stations according to the program established by the circuit of FIG. 3, switch 202 is closed upon stationary contact 203. The battery 205, thereby, supplies current through resistor 206 to the optical isolator 207 and back to the negative terminal of battery 205 through diode 208. Connected between the inputs lines to optical isolator 207 is a resistor 209 and a capacitor 210.

With no current being supplied to the optical isolator, the isolator, as shown in FIG. 5, emits no light from the diode 31 and, therefore, the transistor 32 is non-conducting such that the inverter 211, because its input is connected through a resistor 212 to a +V source, presents a low signal to input lines 213 and 214 of Nand gates 215 and 216 respectively. With a low signal on the inputs 213 and 214, the Nand gates 215 and 216 are inhibited from providing a low signal on terminals T13 and T14. Regardless of the signal applied to terminal T1, the terminals T13 and T14 will have a high output.

Terminal T1 is connected from station contact 1 by a jumper 232 to sequence contact 1 which in turn is connected to the other input 217 of Nand circuit 215. Also, terminal T1 is connected through inverter 219 to input 220 of Nand gate 221. Terminal T2 is shown connected to input terminal 222 of Nand gate 221 and also through inverter 223 to input terminal 224 of Nand circuit 225.

Terminal T3 is shown connected to input terminal 226 of Nand gate 225 and will be connected through an inverter to the next Nand circuit (not shown) and so on for each of the input terminals. Terminal T9 is connected to the input of the preceding Nand gate (not shown) and is also connected through an inverter 227 to the input 228 of Nand gate 229. Terminal T10 is connected directly to input 230 of Nand circuit 229.

Although FIG. 3 is shown such that the station contacts 1-10 are directly jumpered to their respective sequence contacts 1-10, it can readily be seen that the jumpers can be arranged in any desired manner. The manner in which the station contacts are jumpered to

the sequence contacts will determine the tour sequence that the guard is to follow. Thus, the station contact 1 can be connected to sequence contact 10 if it is desired to operate station number 1 as the last station in the sequence. If it is desired to operate station 10 as the first station in the sequence, station contact 10 will be jumpered to sequence contact 1.

COMMON LOGIC CIRCUIT

FIG. 4 shows the common logic circuit shown in block diagram form of FIG. 1. The same terminal numbers have been used to indicate the manner in which the common logic circuit is to be connected to the status circuit of FIG. 2 and the program circuit shown in FIG. 3.

When the guard begins his tour and assuming that a program circuit is not used (when a program circuit is used, terminals T16 and T17 shown in FIG. 4 are grounded) the operation of key switch 1, representing the key switch of the first station, causes input 41' (FIG. 2) to go low which drives the output from latch 41 (FIG. 2) high. This high is connected to terminal T1 of FIG. 2 and, as shown in FIG. 4, back biases diode 111 which presents a high to the input of Nand gate 102. Since the other terminal of the Nand gate is connected through a resistor 103 to a +V source, the output of the Nand gate goes low which drives the output of inverter 104 high which drives the output of Nand gate 105 (acting as an inverter) low energizing relay coil 106 to pull in relay contacts 107 to provide a tour in progress signal. The tour in progress signal may be used to energize a tour in progress light, or it may be used to provide a signal to the processor and printer to print out a patrol tour start signal.

Also, when the output from latch 41 of the status circuit goes high, a momentary signal is applied by capacitor 61 and inverted by inverter 71 and applied to terminal T12. This signal is a momentary low which is connected through the terminal T12 of FIG. 4 (the common logic circuit) to a one shot circuit 108. The inverted terminal of the one shot is utilized to reset the counter and decoder 109, the reset latch 110 and to discharge capacitor 121.

When the inverted terminal of the one shot 108 again goes high, the capacitor 121 is allowed to charge from the +V source through resistor 122, resistor 123 and to ground. The capacitor is connected to one input terminal of PUT 124, the other input terminal of which is connected to a voltage divider 125 and 126 connected between the +V source and ground. The +V source is also connected through a resistor 127 to the emitter of transistor 128 the collector which is connected to ground. The junction of resistors 125 and 126 is connected through a resistor 129 to the base of transistor 128. When the charge on capacitor 121 reaches 0.6 volt above the voltage established by the junction of resistors 125 and 126, the capacitor discharges through the PUT 124 which momentarily pulls down the voltage at junction A which applies a pulse to transistor 129 momentarily turning it off. The output from the transistor is used to step the counter and decoder 109.

The outputs from the counter and decoder are connected to terminals 130 which provide for 3 minute, 6 minute, 9 minute, 12 minute, 15 minute or 18 minute time intervals. A jumper 131 is used to select the time during which a guard is required to operate the stations in his tour. As shown, a 15 minute interval is chosen.

Should the guard fail to energize the proper station in the sequence within 15 minutes, the capacitor 121 will have charged and discharged a sufficient number of times to step the counter around to a position where it provides an output through jumper 131 to latch circuit 132 which presents a high to the input of Nand gate 133 which causes relay 134 to be energized closing contacts 135 to present a delinquency signal on the output of terminals T18 and T19. These terminals T18 and T19 may be directly connected to a light to provide a delinquency signal or may be connected to the processor and printer apparatus for providing a print out of a delinquency.

However, if the guard operates station 2, for instance, within the 15 minute time interval, latching circuit 42 (FIG. 2) presents a high on its output which is connected through capacitor 62 and inverter 72 to present a momentary low signal on terminal T12. As shown in FIG. 4, a momentary low on T12 will energize the one shot 108 to discharge capacitor 121, to reset the counter and decoder 109 to a 0 count. As the guard operates each station within the predetermined amount of time (i.e., 15 minutes) the one shot 108 will repeatedly reset the timer and the counter and decoder circuit 109 such that relay coil 134 remains de-energized.

It is to be noted that the output terminals T1 and T10 of the status circuit of FIG. 2 are connected to the diodes 111-120 of FIG. 4. Since terminals T1-T10 of the status circuit (FIG. 2) are normally low, the output from all the diodes will be low until all diodes 111-120 are back biased. When all stations have been operated, terminal B of FIG. 4 will go high which presents, through a time delay capacitor 136, a high to the input of inverter 137 which drives the input to inverter 138 low which presents a high to one of the inputs of Nand circuit 139.

Upon closure of station switch 10, the last station, latch 50 of the status circuit will provide a low signal on terminal T11 which, as shown in FIG. 4 (common logic circuit), will present a high on the output of inverter 140 which is connected through a time delay capacitor 141 to one of the inputs to Nand circuit 142. In addition, inverter 140 presents a high to a second input of Nand circuit 139. Furthermore, when latch 50 shown in FIG. 2 is tripped, terminal T12 is presented with a momentary low which energizes one shot 108 to provide a momentary low to the third input of Nand circuit 139. It is noted that the output from one shot 108 is normally high and will, after a predetermined time from a low signal applied to terminal T12 go back to a high status. The signal coming from diodes 111-120 and from terminal T11, by virtue of capacitors 136 and 141, are time delayed so that a high is applied to the inputs of Nand gate 139 when the output of one shot 108 goes back high. A high on all inputs of Nand 139, which results from all tour stations having been operated and from the operation of the last station, presents a low to the input of latching circuit 143 which presents a high to one of the inputs of Nand gate 144 the other input of which is always high due to its connection through a resistor 145 to the +V source. The output of Nand 144 therefore goes low which energizes a one shot circuit 146. The non-inverting input of one shot 146 operates parallel Nand circuit 147 to present a signal on terminal T15 which, as shown in the status circuit (FIG. 2), will reset all latches 41-50. This

unlatching of latches 41-50 occurs when the proper sequence has been carried out.

However, assume that station 10, the last station, is operated before one of the previous stations, e.g., station 9, is operated. Output terminal B from diodes 111-120 will be low which causes the output from inverter 137 to be high which is applied to one of the input terminals of Nand 142. Also, the closure of switch 10 results in a low being applied to terminal T11 (status circuit to the common logic circuit) which drives the output of inverter 140 high which is connected to the other input of Nand circuit 142. With both inputs being high, a low is presented at the output of Nand 142 which causes the output of inverter 148 to go high. When the output of inverter 148 goes high, a high is presented to one input terminal of Nand gate 149 the other input terminal of which is high because it is connected through resistor 150 to the +V source. When both input terminals of Nand gate 149 are high, the output goes low which drives the output of inverter 151 high which drives the output of Nand gate 152 low. The relay 153 is thus energized to close contacts 154 to provide an out of sequence signal on terminals T20 and T21 which may be connected to a light on the display apparatus or may be connected to the processor and printing apparatus to provide an out of sequence print out.

It is noted that stations 2-9 may be operated in any sequence whatsoever as long as the first station is operated first and the last station is operated last. When all stations 1-10 are operated and the last station is operated last, the terminal B is presented with a high signal which causes a low signal on the output of 137 which is connected to one of the inputs of Nand 142 which inhibits the out of sequence signalling circuit.

When a program circuit is used, terminals T17 and T16 of FIG. 4 are grounded. The grounding of terminal T16 prohibits energization of Nand gate 102 and the grounding of terminal T17 inhibits the output from inverter 148 such that the out of sequence signal must now come from terminal T14 originating at the program circuit. When using the program circuit as shown in FIG. 3 and with the jumpers as shown, the closure of switch 202 to stationary contact 203 results in a high signal being placed on inputs 213 and 214 of Nand gates 215 and 216 respectively. When the station 1 switch is closed, latching circuit 41 presents a high on its output which is connected through terminal T1 and applies a high to the other input terminal of Nand gate 215 (FIG. 3) which causes the output of that Nand gate to go low. A low on T13 results in a high on the output of inverter 104 (FIG. 4) which results in a low from the output of Nand gate 105 which energizes relay 106 closing contacts 107 to provide the tour in progress signal. Also, a high on terminal T1 (FIG. 3) results in a low from the output of inverter 219 which inhibits the operation of Nand gate 221. Normally, the output from the inverters 219, 223, and 227 are high such that if, for instance, station T10 were operated before station 9, a 1 would appear on both inputs 228 and 230 of Nand gate 229 which will result in a low on the output bus connected to the outputs of Nand gates 221, 225 and 229. A low on any one of the outputs of these Nand gates result in the whole bus going low which results in the output from inverter 231 going high which causes terminal T14 to go low. This low on terminal T14, as shown in FIG. 4, is applied to the input of inverter 151

causing its output to go high which causes the output of Nand gate 152 to go low energizing relay 153 to close contacts 154 to provide the out of sequence signal on terminals T20 and T21.

However, if all stations are operated in the proper sequence, each time a station is energized, the inverted input to the corresponding Nand gate 221, 225 or 229 will go low inhibiting the change in the output from that Nand gate as the subsequent station is operated. Since the input to inverter 231 is normally high and the output from the inverter is normally low, the output of Nand gate 216 is prohibited from changing its state.

In FIG. 6, the counter and decoder 109 comprises two counters 501 and 502 and Nand circuits 503, 504, 505, 506, 507 and 508. The outputs from the Nand gates are connected to the terminals 130 for providing time durations from 3 minutes to 18 minutes in increments of 3 minutes each. Once the two counters have been reset, a 0 appears on all outputs. When the first pulse arrives from the timing circuit in the common logic circuit of FIG. 4, a 1 appears on the Q1 output of counter 501. However, it can be seen from FIG. 6 that this 1 will not change the states of any of the Nand circuits. Upon the next pulse being received by counter 501, Q1 goes to 0 and Q2 has a 1 on its output. Again, this arrangement is insufficient to provide an output from any of the Nand circuits. However, when the next pulse is received to counter 501, output Q1 goes high which presents two 1's on the input of Nand circuit 503 driving its output low which, if the 3 minute terminals are jumpered, drives the output of latch 110 high which pulls the output of Nand circuit 133 low to energize the relay. If the jumper is not across the 3 minute terminals, the counter continues counting until either it reaches the proper jumper terminals or it is reset.

FIG. 7 shows how the patrol tour system may be used in a data gathering system such as the Honeywell DELTA 2000. Instead of using the display apparatus 301 as shown in FIG. 1, the outputs from the patrol tour system are fed into an interface apparatus 402 which is designed to convert the information supplied from the patrol tour system by way of lines 411-420 from the inverters 91-100 shown in FIG. 1 into binary coded form. In addition lines 403-405, corresponding to the delinquency signal, tour in progress signal and out of sequence signal shown in FIG. 1 are fed from the patrol tour system to the interface apparatus.

The interface apparatus is connected to a transceiver apparatus 406 for transmitting binary coded messages to the central station 407 by way of a coax transmission line 408. The central station comprises a transceiver 409 adapted to receive the messages coming in over line 408 and supplying the messages to a processor apparatus 421 for display on a printer 422.

The manner in which generally the messages are constructed and the operation of the data gathering system are shown in copending application Ser. No. 178,095 filed Sept. 7, 1971. The manner in which the printer apparatus receives the messages and provides a print out display is shown in U.S. Pat. No. 3,618,026.

The central station 407 may be programmed to provide a print out as each tour station is operated or may give a print out of only the start of the tour, the end of the tour, a delinquency and an out of sequence indication. Alternatively, the printer may print out a log of all stations operated whenever a delinquency has occurred as well as the start of the tour and the end of the tour.

The embodiments of the invention in which an exclusive property or right is claimed are defined as follows:

1. A patrol tour system having a plurality of stations to be operated in a prescribed sequence, the system comprising:

status circuit means having a latching means for each of said stations whereby the latching means is latched upon operation of its associated station;

delinquency reset means connected to said latching means for providing a delinquency reset signal each time one of said latching means is latched;

logic circuit means having timing means for providing a delinquency signal upon the lapse of a predetermined time, said logic circuit means being responsive to each of said delinquency reset signals for resetting said timing means upon the receipt of said delinquency reset signals, said logic circuit further having out of sequence sensing means for providing an out of sequence signal whenever said stations are operated out of said prescribed sequence; and

display apparatus responsive to said delinquency signal and said out of sequence signal for providing a delinquency alarm and an out of sequence alarm respectively.

2. The system of claim 1 wherein said system further comprises a program means connected to said latching means and to said logic circuit means for establishing a predetermined sequence in which said station must be operated.

3. The system of claim 2 wherein said program means comprises at least two programs and means to select the particular sequence in which the stations must be operated.

4. The system of claim 3 wherein said program means includes means for providing a program out of sequence signal when said stations have been operated out of the program sequence, and said logic circuit means including means responsive to said program out of sequence signal for providing said out of sequence signal.

5. The system of claim 1 wherein said timing means comprises a timer apparatus for providing periodic pulses, a counter means connected to said timer apparatus for receiving said pulses and a decoder connected to said counter for decoding the output of said counter into a plurality of time durations.

6. The system of claim 5 wherein said logic means further comprises latch reset means responsive to the operation of all of said stations and to said last station for resetting the latching means.

7. The system of claim 6 wherein said status means includes means for providing a last station signal, said logic circuit means includes means responsive to the latching means for providing a signal when all stations have been operated, and said logic circuit means further includes means responsive to said last station signal and to said signal provided when all stations have been operated for providing said out of sequence signal.

8. The system of claim 6 further comprising a program means connected to said latching means and to said logic circuit means for establishing a predetermined sequence in which the stations must be operated.

9. The system of claim 8 wherein said program means comprises at least two programs and selection means to

select the particular sequence in which the stations must be operated.

10. The system of claim 1 wherein said status circuit means, said delinquency reset means and said logic circuit means are located at a remote area and transmit their information in binary coded form over a channel to a central station for display.

11. A patrol tour system having a plurality of stations to be operated in a prescribed sequence, the system comprising:

status circuit means having a latching means for each of said stations whereby the latching means is latched upon operation of its associated station;

delinquency reset means connected to said latching means for providing a delinquency reset signal each time one of said latching means is latched;

logic circuit means having timing means for providing a delinquency signal upon the lapse of a predetermined time between operation of said stations, said timing means being reset upon the receipt of said delinquency reset signal, said logic circuit further having out of sequence sensing means for providing an out of sequence signal whenever said stations are operated out of said prescribed sequence; and

display apparatus consisting of a first means responsive to the operation of the first station for providing a patrol tour start signal, a second means responsive to the operation of said last station for providing a tour end signal, a third means responsive to said delinquency signal for providing a delinquency indication, and a fourth means responsive to said out of sequence signal for providing an out of sequence indication, whereby only indications of the patrol tour start, tour end, delinquency and out of sequence are given.

12. The system of claim 11 wherein said system further comprises a program means connected to said latching means and to said logic circuit means for establishing a predetermined sequence in which said stations must be operated.

13. The system of claim 12 wherein said program means comprises at least two programs and means to select the particular sequence in which the stations must be operated.

14. The system of claim 13 wherein said program means includes means for providing a program out of sequence signal when said stations have been operated out of sequence, and said logic circuit means including means responsive to said program out of sequence signal for providing said out of sequence signal.

15. The system of claim 11 wherein said timing means comprises a timer apparatus for providing periodic pulses, a counter means connected to said timer apparatus for receiving said pulses and a decoder connected to said counter for decoding the output of said counter into a plurality of time durations.

16. The system of claim 15 wherein said logic means further comprises latch reset means responsive to the operation of all of said stations and to said last station for resetting the latching circuit means.

17. The system of claim 16 wherein said status means includes means for providing a last station signal, said logic circuit means includes means responsive to the latching circuit means for providing a signal when all stations have been operated, and said logic circuit means further includes means responsive to said last

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station signal and to said signal provided when all stations have been operated for providing said out of sequence signal.

18. The system of claim 16 further comprising a program means connected to said latching means and to said logic circuit means for establishing a predetermined sequence in which the stations must be operated.

19. The system of claim 18 wherein said program

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means comprises at least two programs and selection means to select the particular sequence in which the stations must be operated.

20. The system of claim 11 wherein said status circuit means, said delinquency reset means and said logic circuit means are located at a remote area and transmit their information in binary coded form over a channel to a central station for display.

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