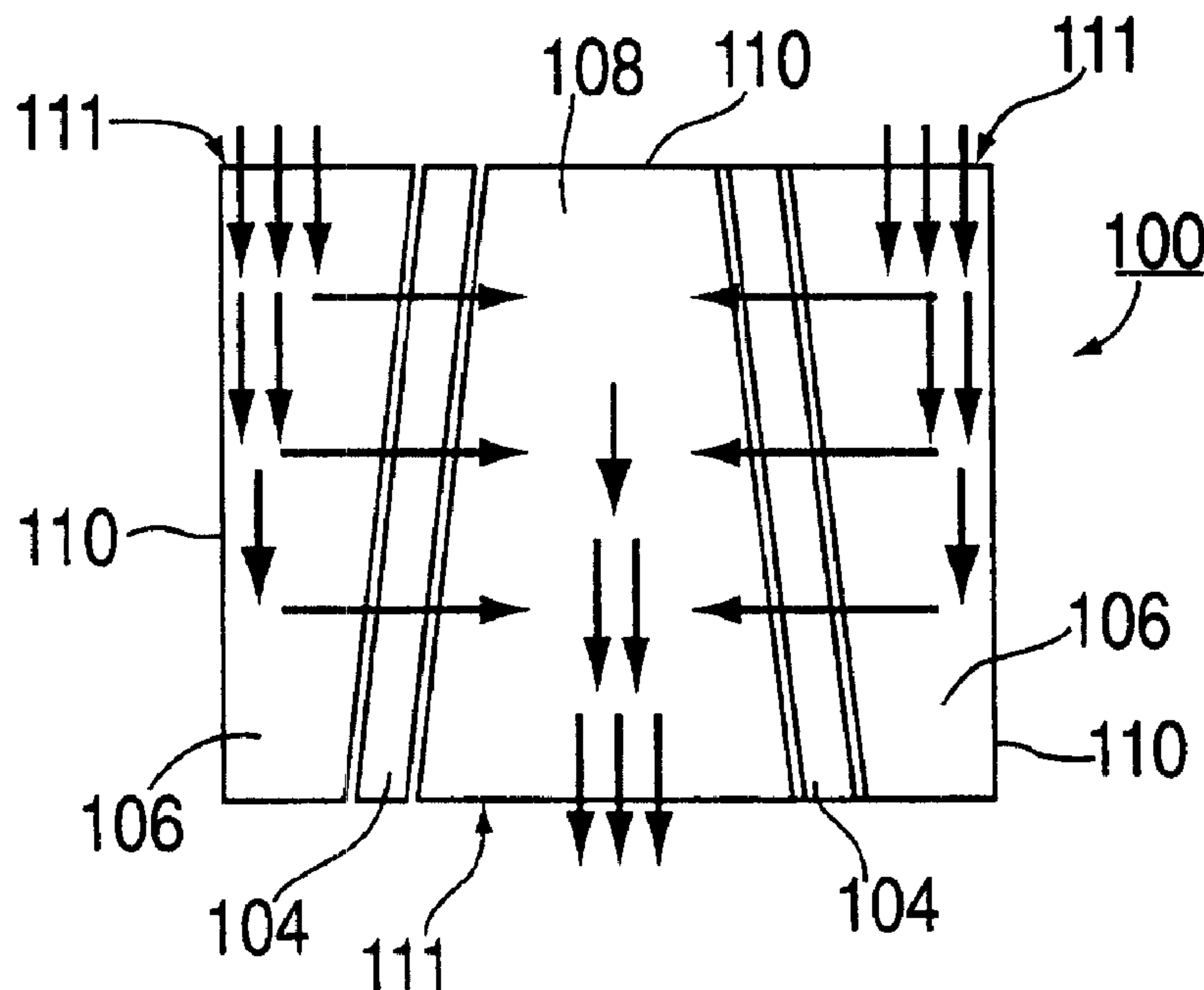




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(71) Demandeur/Applicant:
ALLIEDSIGNAL INC., US
(72) Inventeurs/Inventors:
MCKITTERICK, JOHN BURT, US;
TSANG, JOSEPH CHEUNG-SANG, US
(74) Agent: GOWLING LAFLEUR HENDERSON LLP

(54) Titre : TRANSISTOR A HAUTE TEMPERATURE PRESENTANT UN RISQUE REDUIT D'ELECTROMIGRATION
(54) Title: HIGH TEMPERATURE TRANSISTOR WITH REDUCED RISK OF ELECTROMIGRATION



(57) **Abrégé/Abstract:**

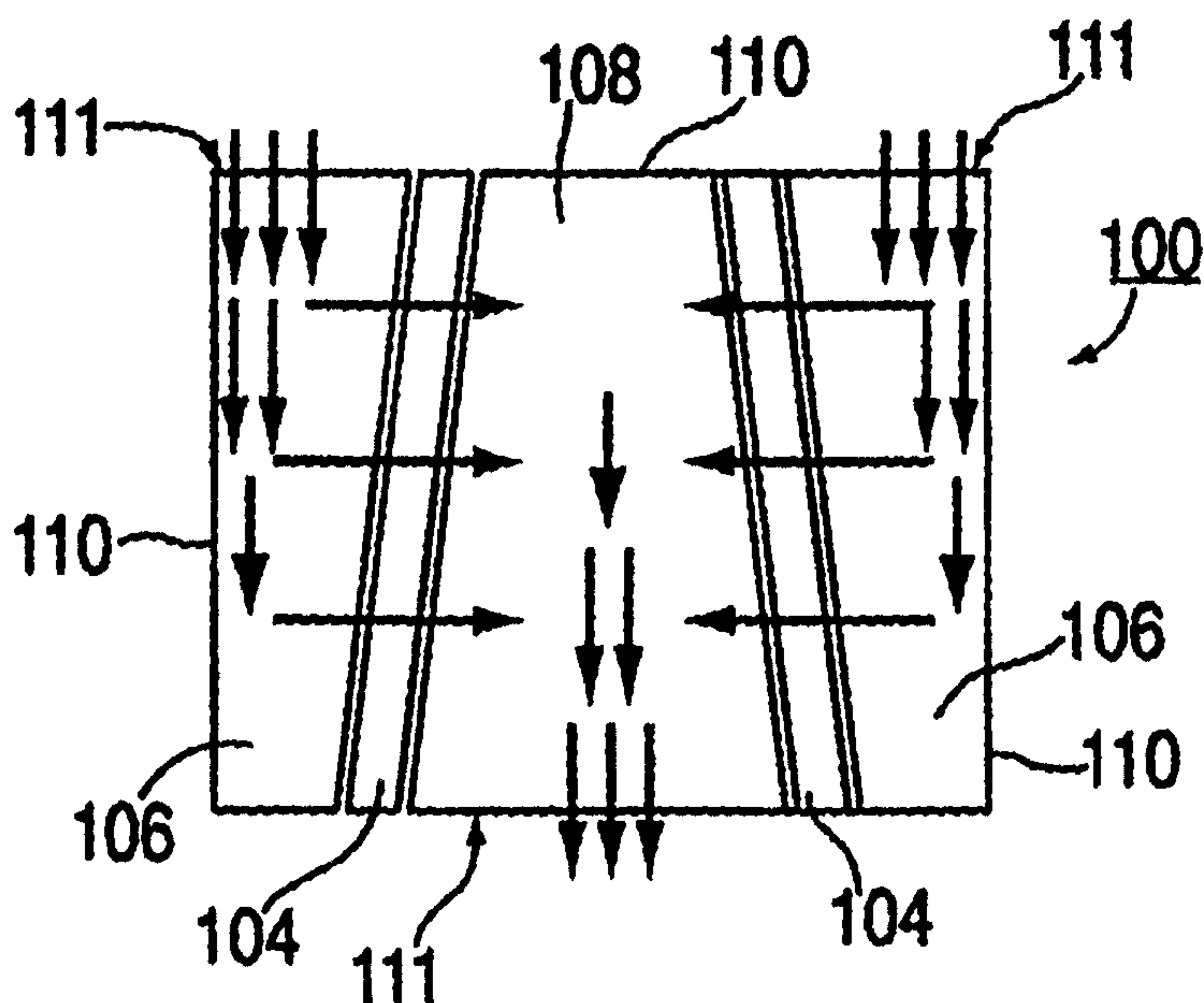
A semiconductor device, in accordance with the present invention, includes a source region and a drain region disposed on opposite sides of a gate structure. A first conductive region is disposed over and is electrically connected to the source region and a second conductive region disposed over and electrically connecting to the drain region, the first and second conductive regions disposed on opposite sides of the gate structure. The first conductive region has a narrow end portion on a first side and gradually widens to a wide end portion on a second side. Also, the second conductive region has a narrow end portion on the second side and gradually widens to a wide end portion on the first side, the gradual widening for increasing cross sectional areas of the conductive regions in accordance with an increase in a magnitude of current flow. The current flow is generated by activation of the gate structure.



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(54) Title: HIGH TEMPERATURE TRANSISTOR WITH REDUCED RISK OF ELECTROMIGRATION (57) Abstract A semiconductor device, in accordance with the present invention, includes a source region and a drain region disposed on opposite sides of a gate structure. A first conductive region is disposed over and is electrically connected to the source region and a second conductive region disposed over and electrically connecting to the drain region, the first and second conductive regions disposed on opposite sides of the gate structure. The first conductive region has a narrow end portion on a first side and gradually widens to a wide end portion on a second side. Also, the second conductive region has a narrow end portion on the second side and gradually widens to a wide end portion on the first side, the gradual widening for increasing cross sectional areas of the conductive regions in accordance with an increase in a magnitude of current flow. The current flow is generated by activation of the gate structure.		



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PCT PATENT APPLICATION FOR:

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**HIGH TEMPERATURE TRANSISTOR WITH REDUCED
RISK OF ELECTROMIGRATION****GOVERNMENTAL INFORMATION**

This invention was made with Government support under contract
15 F33615-96-Z-2618 awarded by the United States Air Force, Air Force Command.
The Government has certain rights in this invention.

BACKGROUND OF THE INVENTION20 **1. Field of the Invention**

The present invention relates to semiconductor structures and, more particularly, to a high temperature semiconductor device and a method of manufacturing the device.

25 **2. Description of the Related Art**

Semiconductor devices are versatile and are used in many application in many different industries. However, many applications that could more fully benefit from the use of semiconductor devices have been precluded from their use due to harsh operating environments. For example, industrial environments where
30 high temperatures are experienced.

A demand exists in aerospace, automotive and other industries for high temperature control and power electronics which can be mounted very close in proximity to a heat source, such as, a combustion chamber for an internal combustion engine. By providing a high temperature integrated circuit or semiconductor device many discrete components may be replaced by a single chip. In this way, a more compact and lightweight device may be implemented with less fasteners and electrical wires. Further, integrated semiconductor devices provide more intelligent functions and programming capability. The smaller size and less maintenance required for integrated semiconductor devices aid in reducing costs as well.

Bulk silicon semiconductor devices are impractical for high temperature applications, i.e., greater than 175 °C. This is due to device leakage current for the bulk silicon device which doubles for every 8 °C increase in temperature. In contrast silicon-on-insulator (SOI) technology devices have been demonstrated to produce functional devices up to about 400 °C. However, despite operational benefits of SOI technology, high temperature devices suffer from increased likelihood of electromigration failures.

Referring to FIG. 1, a conventional layout of a semiconductor device 10 is shown having arrows representing currents. The arrow size indicated in FIG. 1 is proportional to the magnitude of the current at the various locations on device 10. Device 10 includes gate structures 12 and metal lines 14. Below metal structures are diffusion regions (not shown) common to semiconductor transistor devices. During operation, currents are generated in device 10 as indicated. In a high temperature application electromigration failures occur in places where the current density is highest. Therefore, a highest probability of electromigration failure will occur in regions 16, 18 and 20 at the ends of device 10.

Therefore, a need exists for a semiconductor device that may be used under high temperature conditions. A further need exists for a semiconductor device that reduces the risk of electromigration failures despite high temperature operation. This invention satisfies those needs.

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SUMMARY OF THE INVENTION

A semiconductor device, in accordance with the present invention, includes a source region and a drain region disposed on opposite sides of a gate structure. A first conductive region is disposed over and is electrically connected to the source region, and a second conductive region is disposed over and is electrically connected to the drain region. The first and second conductive regions are disposed on opposite sides of the gate structure. The first conductive region has a narrow end portion on a first side and gradually widens to a wide end portion on a second side. Also, the second conductive region has a narrow end portion on the second side and gradually widens to a wide end portion on the first side, the gradual widening for increasing cross sectional areas of the conductive regions in accordance with an increase in a magnitude of current flow. The current flow is generated by activation of the gate structure.

Another semiconductor device includes a plurality of alternating source and drain regions. Each of the plurality of regions is disposed on opposite sides of a gate structure. A plurality of conductive regions are included, each conductive region being electrically connected to one of a corresponding source region and a corresponding drain region. The conductive regions includes a same gradually widening shape as the corresponding source regions and the corresponding drain regions, the gradually widening shape for drain regions widening in a first direction and the gradually widening shape for source regions widening in a second direction opposite the first direction. The gradually widening shape increases cross

sectional areas of the conductive regions in accordance with an increase in a magnitude of current flow. The current flow is generated by activation of the gate structure.

A silicon-on-insulator semiconductor device includes a plurality of
5 alternating source and drain regions, each of the plurality of regions disposed on opposite sides of a gate structure. A plurality of conductive regions is also included, each conductive region being electrically connected to one of a corresponding source region and a corresponding drain region by a contact. Each conductive region is separated by the gate structures. The conductive regions
10 having a substantially constant thickness and having a same gradually widening shape as the corresponding source regions and the corresponding drain regions, the gradually widening shape for drain regions widening in a first direction and the gradually widening shape for source regions widening in a second direction opposite the first direction. The gradually widening shape increases cross sectional areas of
15 the conductive regions in accordance with an increase in a magnitude of current flow. The current flow is generated by activation of the gate structure.

In alternate embodiments, the conductive regions are preferably substantially trapezoidal in shape. The gate structures may have a length sufficient to generate currents in the first and second conductive regions of between about
20 300mA to about 5 A. The device is preferably a silicon-on insulator structure. The device is preferably operable at temperatures above about 175 degrees Celsius. The conductive regions may include aluminum. The wide end portions may correspond to one of current flow entrance regions and current flow exit regions. The gate structures have a length which is preferably skewed by between 60 to less than 90
25 degrees from edges of a device region. The devices are preferably field effect transistors (FETs) and preferably DMOS (double diffused metal oxide semiconductor) FETs.

These and other objects, features and advantages of the present invention will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in detail in the following description of preferred embodiments with reference to the following figures wherein:

FIG. 1 is a top plan view of a conventional layout of a semiconductor device showing current magnitudes through metal lines;

FIG. 2 is a top plan view of a layout of a semiconductor device in accordance with the present invention showing alternating source and drain conductors having a trapezoidal shape;

FIG. 3 is a top plan view of a layout of a semiconductor device in accordance with the present invention showing current magnitudes through conductive regions;

FIG. 4 is a cross-sectional view taken along section line 4-4 of the semiconductor device of FIG. 2 in accordance with the present invention; and

FIG. 5 is a cross-sectional view taken along section line 5-5 of the semiconductor device of FIG. 2 in accordance with the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention relates to semiconductor structures and, more particularly, to a high temperature semiconductor device and a method of manufacturing the device. The present invention employs the high temperature capability offered by silicon-on-insulator (SOI) technology and provides the same or better reliability as commercially available devices suitable for lower temperature.

Metal and diffusion regions for the device in accordance with the invention are advantageously trapezoidal in shape. Areas of current flow are thereby adjusted to reduce current density to reduce the risk of electromigration failures. The present invention is preferably implemented using SOI technology but may be applied to
5 bulk silicon technology as well. The present invention will be described in terms applicable to a SOI DMOS (double diffused metal oxide semiconductor) transistor for illustrative purposes only and the device is not intended to limit the applicability of the invention.

Referring now in specific detail to the drawings where like numerals
10 represent the same or similar elements and initially to FIG. 2, a top view of a semiconductor device 100 is shown in accordance with the present invention. Device 100 includes transistors 102 which may include bulk silicon or silicon-on-insulator (SOI) technology. Transistors 102, preferably include SOI technology for use with high temperature applications, i.e. for temperatures above 175 °C and
15 more preferably above 300 °C. Transistors 102 adapted for use for high voltage applications may include double diffused metal oxide (DMOS) semiconductor transistors, however, normal complementary metal oxide semiconductor (CMOS) transistors are also contemplated. Transistors 102 include a gate 104, a source conductor 106 and a drain conductor 108. Source conductor 106 and drain
20 conductor 108 correspond to source and drain diffusion regions therebelow. Source conductors 106 and drain conductors 108 may be collectively referred to hereinafter as conductive regions 110. Gates 104 connect to bond pads (not shown) on device 100 to enable conduction between sources and drains. Conductive regions 110 connect to bond pads (not shown) to provide appropriate connections to device 100
25 for operation.

As mentioned, below conductive regions 110 are diffusion regions associated with source conductors 106 and drain conductors 108. These diffusion

regions are shown in FIGS. 4 and 5. FIG. 2 shows alternating source conductor 106 and drain conductor 108 regions to conserve layout area. Alternating sources and drains are shared between adjacent transistors 102 as indicated. Other configurations are contemplated as well for the present invention.

5 According to the present invention, conductive regions 110 and their corresponding diffusion regions therebelow, are preferably substantially trapezoidal in shape. Advantageously, the trapezoidal shape provides for increased cross sectional area for current flow, thereby reducing current density therethrough. Since the allowable current density in conductive regions 110 is directly
10 proportional to the cross-sectional area of conductive regions 110, where currents are increased, the cross-sectional area is increased as shown in FIG. 3. For device 100 in FIG. 3 arrows representing currents are shown. The arrow size indicated in FIG. 3 is proportional to the magnitude of the current at the various locations in conductive regions 110. Risk of electromigration of conductive regions 110 is
15 thereby greatly reduced according to the present invention. FIGS. 2 and 3 show wider conductive regions 110 where currents exit and enter conductive regions 110. These entrance and exit regions 111 represent higher magnitude currents and therefore are wider to provide a constant or decreased current density along conductive regions 110. Further, since a minimum cross sectional area is to be met
20 for operating currents through conductive regions 110 to provide adequate protection from electromigration, the trapezoidal shape of conductive regions 110 reduces layout area of device 100 by as much as about 22 %, although higher reductions may be achieved. In preferred embodiments, gates 104 are oriented as indicated by an angle to obtain the trapezoidal shape for conductive regions 110.
25 Angle is preferably between about 60 degrees to about 90 degrees depending on the allowable current density and design criteria.

In one preferred embodiment of the present invention, device 100 is used in a high temperature environment and is a power field effect transistor. For this application, to supply a load with sufficient power, high currents may be developed on device 100. The need for high currents translates to longer gates 104.

5 The length of gates is indicated by an "x" in FIG. 2. The length of gates 104 is proportional to the delay of the gate which may be represented by x^2rc , where x is the length, r is the resistance of the gate per unit length and c is the parasitic capacitance of the gate per unit length. The present invention permits longer gates by reducing risk of electromigration failures. In this way, higher currents can be

10 developed and power field effect transistors may be realized for powering discrete devices such as a motor or an actuator. Device 100 preferably generates currents between from about 300mA to about 5 A depending on gate length.

Referring to FIGS. 4 and 5, cross-sectional views at section lines 4-4 and 5-5 of FIG. 2 are shown. FIGS. 4 and 5 show a SOI DMOS transistor structure

15 for device 100, however other structures may also be implemented in accordance with the invention. Device 100 includes a substrate 200, preferably a monocrystalline silicon substrate. In one embodiment, substrate 200 is preferably a portion of a silicon-on-insulator (SOI) structure. A buried dielectric layer 202 is provided on substrate 200, buried dielectric layer 202 preferably includes an

20 insulator such as a silicon oxide. A silicon layer 204 is provided on dielectric layer 202. Silicon layer 204 is doped to provide a source diffusion region 206, drain diffusion region 208, a drift region 210 and a channel diffusion region 212. As illustrated in FIGS. 4 and 5, source diffusion region 206 and drain diffusion region 208 have varied widths as indicated. Source conductor 106 and drain conductor 108

25 respectively correspond to source diffusion region 206 and drain diffusion region 208 and are likewise increased and decreased in width in accordance with the diffusion regions. Source conductor 106 and drain conductor 108 are electrically

connected to source diffusion region 206 and drain diffusion region 208 by contacts 210, which preferably extend the length (i.e., into and out of the page) of source conductor 106 and drain conductor 108. Contacts 210 and conductive regions 110 (FIG. 2) are preferably formed of a metal such as aluminum and for high
5 temperature applications aluminum may be alloyed with titanium and/or tungsten, further alloys including chromium and molybdenum may be used.

Source conductor 106 and drain conductor 108 and diffusion regions 206 and 208 have a dielectric layer 222 therebetween. Dielectric layer 222 also provides a gate cap layer 224 for electrically isolating gate structure 104. Gate
10 structure 104 includes a conductive material 226, preferably polysilicon or doped polysilicon. Conductive material 226 is isolated from drift region 210 and channel diffusion region 212 by a gate oxide 230. A second conductive material 228, preferably a block oxide is included electrically connecting to conductive material 226. Conductive material 226 and second conductive material 228 are separated
15 from drift region 210 by a field oxide layer 232.

During operation, gate structure 104 is activated through bond pads (not shown). Voltage is applied to conductive material 226 and second conductive material 228. The voltage creates a field which forms a channel in channel diffusion and in drift region 210. Drift region 210 provides a voltage standoff function when,
20 for example, device 100 is used in a power circuit including a motor (not shown). When the device and therefore the motor are switched off a relatively large potential may still be applied to drain diffusion 208. Drift region 210 protects device 100 from possible damage during this condition.

The thickness of buried dielectric layer 202, the length (between
25 source and drain) of drift region 210, doping profiles and gate oxide 230 thickness are determined by the particular application of device 100. For example, a higher source-drain breakdown voltage, such as 28 volts, necessitates a longer drift region

210 and thicker buried dielectric layer 202. Likewise, a heavier doped channel diffusion region 212 creates a higher MOS threshold voltage for high temperature applications in accordance with the present invention.

Additional metal layers and dielectric layers may be introduced onto
5 the structures of FIGS. 4 and 5. It is desirable to provide additional metal layers in the same trapezoidal shapes as conductive regions 110. This advantageously avoids overlap of conductive regions in different layers which may introduce parasitic capacitances.

In other embodiments of the present invention, other shapes may be
10 provided for conductive regions and corresponding source and drain diffusion regions. Other shapes are contemplated and are only limited by the fabrication process capabilities. It is to be understood that additional electromigration reduction may be provided by increasing the thickness of the conductive regions to further increase the area thereof. However, substantially constant thickness
15 conductive regions are preferred.

Having described preferred embodiments of high temperature transistor with reduced risk of electromigration (which are intended to be illustrative and not limiting), it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be
20 understood that changes may be made in the particular embodiments of the invention disclosed which are within the scope and spirit of the invention as outlined by the appended claims. Having thus described the invention with the details and particularity required by the patent laws, what is claimed and desired protected by Letters Patent is set forth in the appended claims.

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WHAT IS CLAIMED IS:

1. A semiconductor device (100) comprising:
a source region (206) and a drain region (208) disposed on opposite sides of a
5 gate structure (104);
a first conductive region (106) disposed over and electrically connecting to the
source region (206) and a second conductive region (108) disposed over and
electrically connecting to the drain region (208), the first and second conductive
regions (106, 108) disposed on opposite sides of the gate structure (104); and
10 the first conductive region having a narrow end portion on a first side and
gradually widening to a wide end portion (111) on a second side, the second
conductive region having a narrow end portion on the second side and gradually
widening to a wide end portion (111) on the first side, the gradual widening for
increasing cross sectional areas of the conductive regions in accordance with an
15 increase in a magnitude of current flow, the current flow being generated by
activation of the gate structure (104).
2. The device (100) as recited in claim 1, wherein the first and second conductive
regions (106, 108) are substantially trapezoidal in shape, and wherein the gate
structure (104) is located substantially between the first and second conductive
5 regions (106, 108).
3. The device (100) as recited in claim 1, wherein the gate structure (104) has a
length (x) sufficient to generate currents in the first and second conductive regions
(106, 108) of between about 300 mA to about 5 A.
4. The device (100) as recited in claim 1, wherein device (100) includes a
silicon-on-insulator structure (200, 202).
5. The device (100) as recited in claim 4, wherein the device is operable at
temperatures above about 175 degrees Celsius.
6. The device (100) as recited in claim 1, wherein the first and second conductive
regions (106, 108) include aluminum.

7. The device (100) as recited in claim 1, wherein the wide end portions (111) correspond to one of current flow entrance regions and current flow exit regions.
8. A semiconductor device (100) comprising:
 - a plurality of source regions (206);
 - a plurality of drain regions (208);
 - a plurality of gate structures (104), wherein each gate structure (104) is located
 - 5 substantially between a corresponding one of the plurality of source regions (206) and a corresponding one of the plurality of drain regions (208);
 - a plurality of first conductive regions (106) each disposed over and electrically connecting to a corresponding one of the plurality of source regions (206), wherein each of the plurality of source regions (206) and each of the plurality of first
 - 10 conductive regions (106) has a first side and a second side (111), wherein the first side is narrower than the second side (111), wherein the first side gradually widens to the second side (111), and wherein each of the plurality of first conductive regions (106) is shaped substantially similarly to the corresponding one of the plurality of source regions (206); and
 - 15 a plurality of second conductive regions (108) each disposed over and electrically connecting to a corresponding one of the plurality of drain regions (208), wherein each of the plurality of drain regions (208) and each of the plurality of second conductive regions (108) has a first side (111) and a second side, wherein the first side (111) is wider than the second side, wherein the first side (111) gradually narrows to
 - 20 the second side, wherein each of the plurality of second conductive regions (108) is shaped substantially similarly to the corresponding one of the plurality of drain regions (208), and wherein adjacent gate structures (104) are disposed on opposite sides of either of a first conductive region (106) or a second conductive region (108).
9. The device (100) as recited in claim 8, wherein each of the pluralities of first and second conductive regions (106, 108) includes a substantially trapezoidal shape, and wherein, for each of the plurality of gate structures (104), the first side of one of
- 5 the plurality of first conductive regions (106) is opposite the gate structure (104) from the first side (111) of one of the plurality of second conductive regions (108).

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10. The device (100) as recited in claim 8, wherein each of the plurality of gate structures (104) has a length (x) sufficient to generate currents in the first and second conductive regions (106, 108) of between about 300 mA to about 5 A.

11. The device (100) as recited in claim 8, wherein the device (100) includes a silicon-on-insulator structure (200, 202).

12. The device (100) as recited in claim 11, wherein the device (100) is operable at temperatures above about 175 degrees Celsius.

13. The device (100) as recited in claim 8, wherein each of the pluralities of first and second conductive regions (106, 108) includes aluminum.

14. The device (100) as recited in claim 8 wherein the second side (111) of each of the plurality of first conductors and the first side (111) of each of the plurality of second conductors correspond to one of current flow entrance regions and current
5 flow exit regions.

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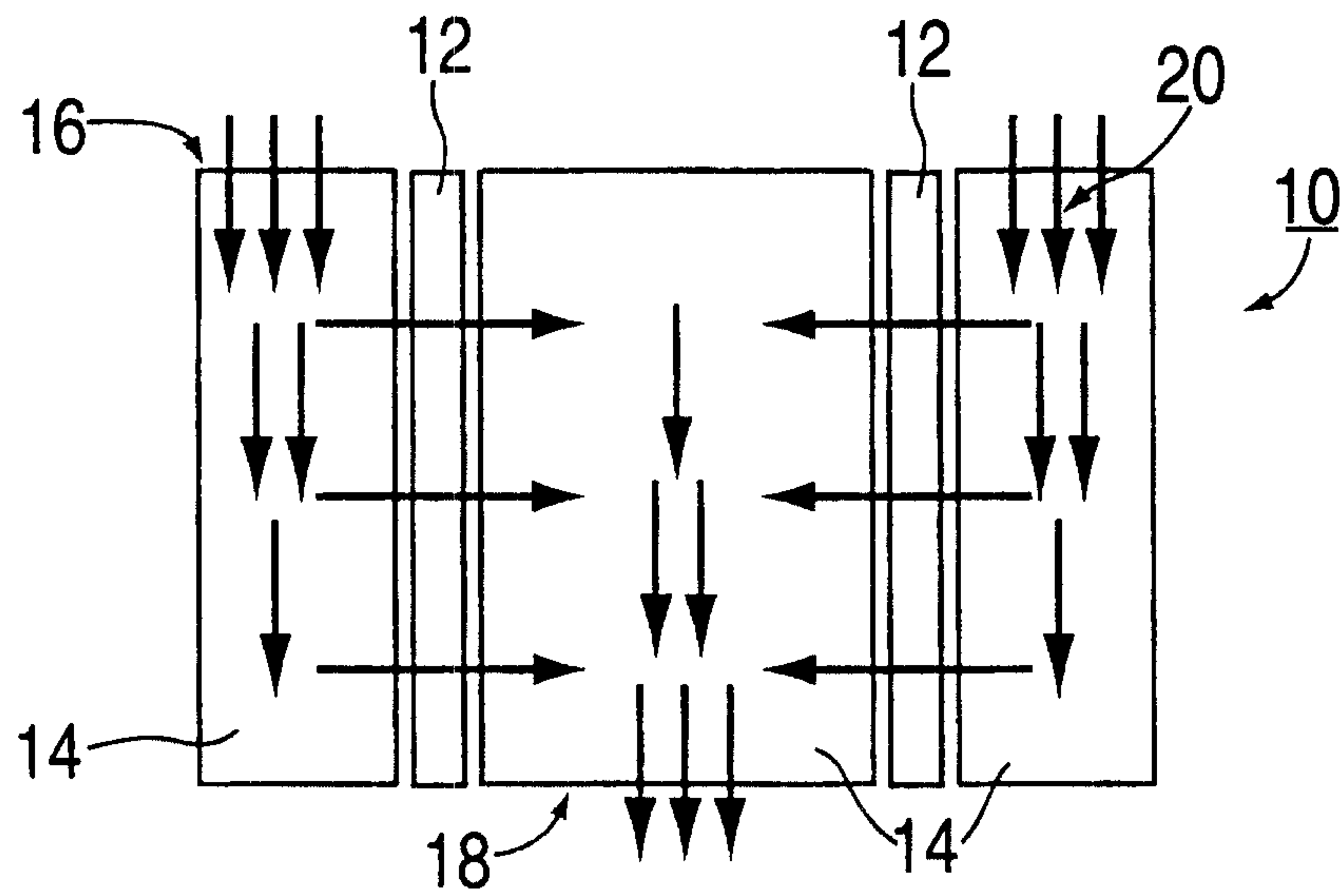


FIG. 1
(Prior Art)

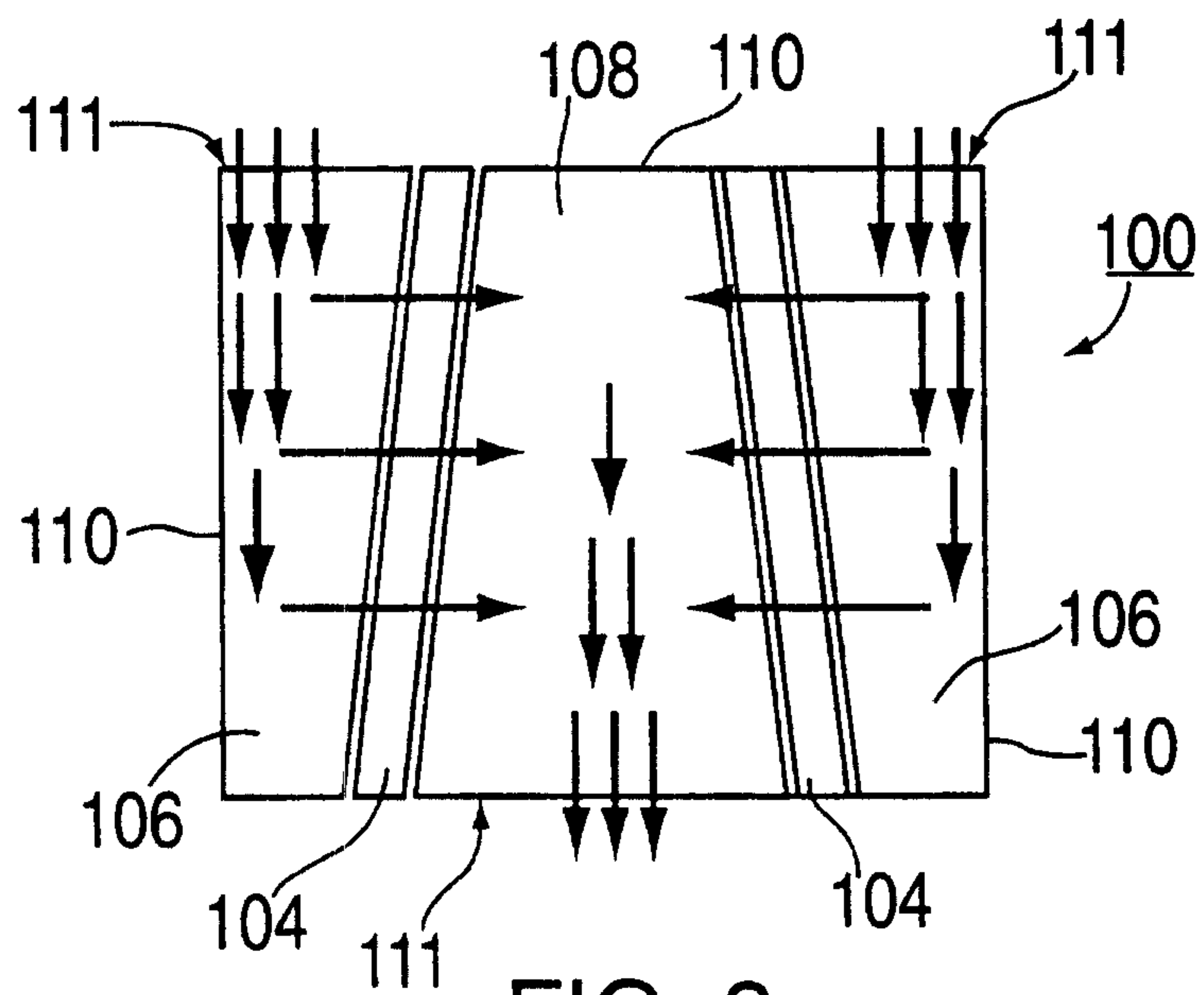
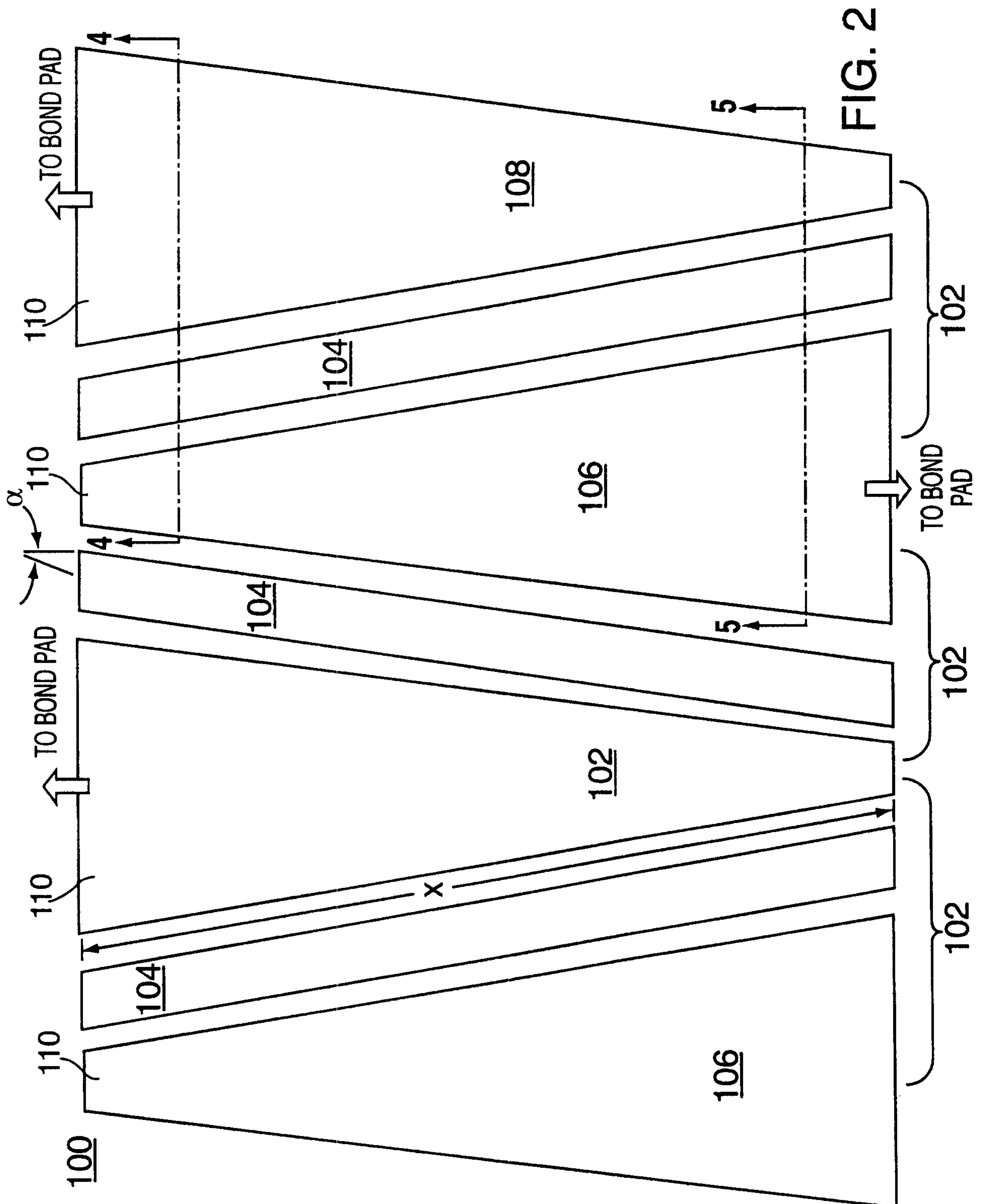


FIG. 3

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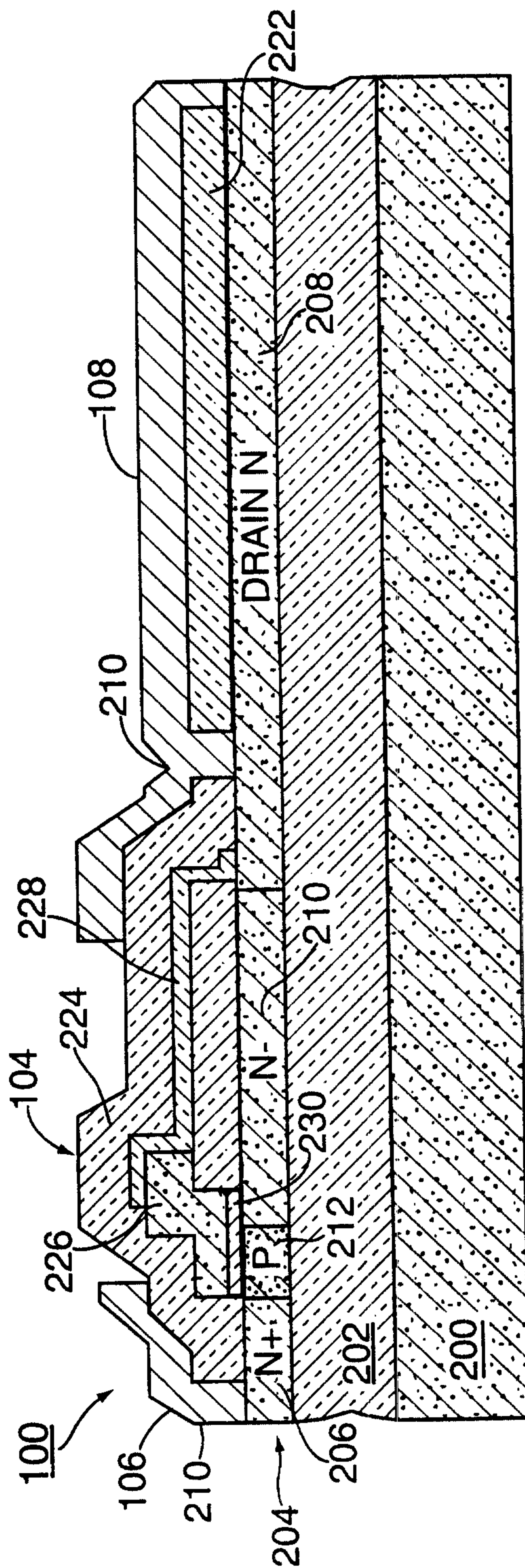


Fig. 4

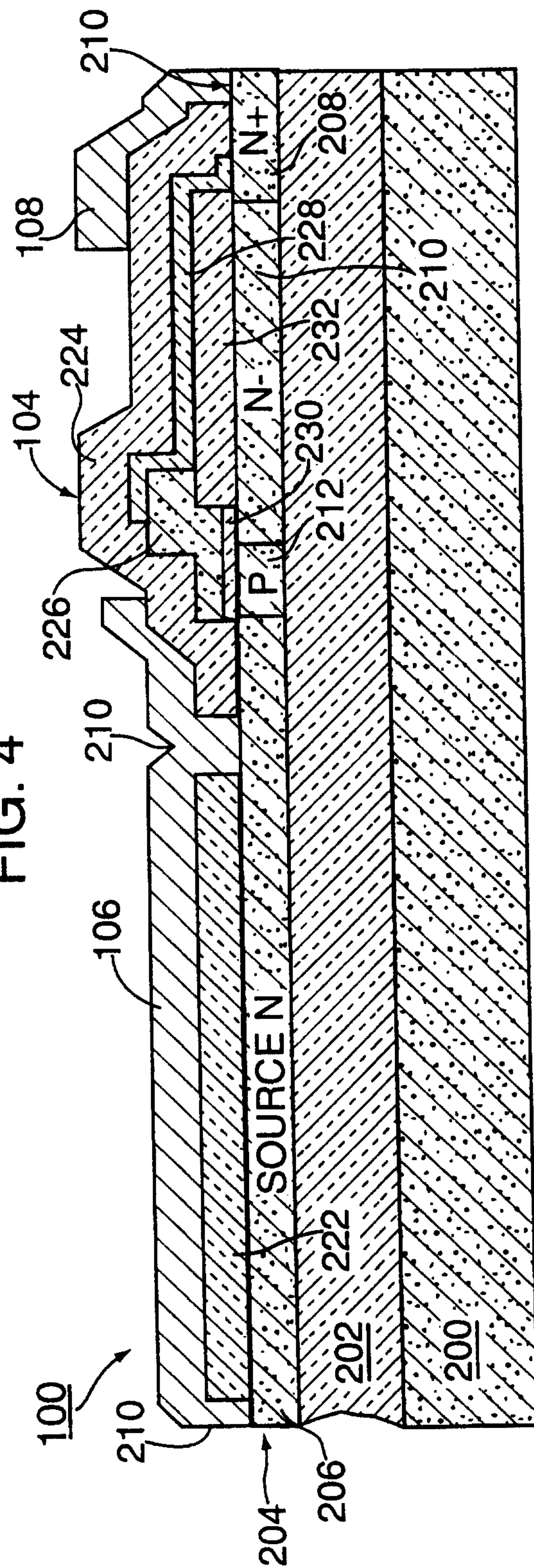


FIG. 5

