

SPIN AND CHARGE INTERCONNECTS WITH RASHBA EFFECTS

BACKGROUND

[0001] Conversion of a magnetic state to a charge variable is used by magnetic spin logic and interconnects. For example, a charge variable such as current can flow through long interconnects to other magnetic spin logic. Long range spin interconnects are also a critical part of spin based logic for computing. Spin based logic can enable, for example, scalable logic devices for low energy delay, improved device density via three dimensional (3D) integration, improved circuit density via majority logic, and non-volatility.

[0002] However existing spin based interconnects suffer from limited spin diffusion length in copper, silver, and aluminum (e.g., less than 1000 nm). Existing spin based interconnects also suffer from reduction in spin diffusion length as the wire width is scaled. The need for repeaters for enabling spin interconnects also make existing spin interconnects less favorable for low power devices. Further, vulnerability to spin scattering at the vias where a liner/barrier may be used during the fabrication process also makes existing spin based interconnects unfavorable. These constraints result in limited interconnect scalability for spin based logic devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The embodiments of the disclosure will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the disclosure, which, however, should not be taken to limit the disclosure to the specific embodiments, but are for explanation and understanding only.

[0004] **Fig. 1A** illustrates a Magnetic Tunneling Junction (MTJ) with typical Tunnel Magneto Resistance (TMR) based readout of the MTJ.

[0005] **Fig. 1B** illustrates a stack of layers having a MTJ coupled to an electrode formed of Spin Hall Effect (SHE) material, where the SHE material converts charge current to spin current.

[0006] **Fig. 1C** illustrates a top view of the stack of **Fig. 1C**.

[0007] **Fig. 2A** illustrates a portion of an interconnect or via formed of a super-lattice stack and corresponding side view (or perpendicular view) of its atomic structure, according to some embodiments.

[0008] **Fig. 2B** illustrates a portion of an interconnect or via formed of a super-lattice stack and corresponding top view of its atomic structure, according to some embodiments.

[0009] **Fig. 3A** illustrates a hybrid interconnect comprising a first interconnect with a super-lattice stack, a second interconnect formed of metal, and third interconnect with a super-lattice stack, in accordance with some embodiments.

[0010] **Fig. 3B** illustrates a cross-section of the first interconnect, in accordance with some embodiments.

[0011] **Fig. 3C** illustrates a hybrid interconnect comprising a first interconnect with a super-lattice stack, a second interconnect formed of metal, and third interconnect with a super-lattice stack, in accordance with some embodiments.

[0012] **Fig. 3D** illustrates a cross-section of the first interconnect, in accordance with some embodiments.

[0013] **Figs. 4A-B** illustrate two interconnects with super-lattice stacks coupled together by a metallic via, in accordance with some embodiments.

[0014] **Fig. 5** illustrate two interconnects with super-lattice stacks coupled together by a via formed of a super-lattice stack, in accordance with some embodiments.

[0015] **Fig. 6** illustrates spin-to-charge conversion over layers of the super-lattice stack when used as a via, according to some embodiments of the disclosure.

[0016] **Figs. 7A-B** illustrate plots showing spin-to-charge conversion efficiency for different Silver (Ag) diffusion lengths, according to some embodiments of the disclosure.

[0017] **Figs. 8A-B** illustrate cross-sections of a die showing fabrication of templated super-lattice interconnects and vias, in accordance with some embodiments of the disclosure.

[0018] **Fig. 9** illustrates a cross-section of a die showing one of the fabrication steps where templated super-lattice interconnects and templated super-lattice vias are formed, in accordance with some embodiments.

[0019] **Fig. 10** illustrates a smart device or a computer system or a SoC (System-on-Chip) with super-lattice stack based interconnect, according to some embodiments.

DETAILED DESCRIPTION

[0020] Tunnel Magneto Resistance (TMR) based spin-to-charge variable conversion has limited conversion efficiency. **Fig. 1A** illustrates a typical TMR based readout of a Magnetic Tunneling Junction (MTJ) 100. In one example, MTJ 101/102 comprises stacking a ferromagnetic layer (e.g., Free Magnet) with a tunneling dielectric (e.g., MgO) and another ferromagnetic layer (Fixed Magnet). The plot in the center illustrates the dependence of resistance (R_{MTJ}) on voltage across MTJ 101/102 for the two magnetization directions of the Free Magnet relative to the Fixed Magnet, where resistance is in Ohms and voltage in Volts.

Here, MTJ 101 illustrates the low resistance state where the magnetization of the Free Magnet is in the same direction as the magnetization of the Fixed Magnet (e.g., the directions of magnetizations are parallel (P) to each other). MTJ 102 illustrates the high resistance state where the direction of magnetization of the Free Magnet is in the opposite direction as the direction of magnetization of the Fixed Magnet (e.g., the directions of magnetizations are anti-parallel (AP) to each other).

[0021] Here, the read out of the magnetization is obtained via sensing of a resistance change across MTJ 101/102 on the order of 4 kOhms (which translates to a voltage of 40 mV to 80 mV at 10 μ A read current). In this example, 10 μ A of read current limits the total read time to 5 ns to 10 ns, which is slow. As such, the TMR based read out of MTJs 101/102 is highly limited in the signal strength and speed it can generate.

[0022] **Fig. 1B** illustrates stack of layers 120 having a MTJ coupled to an electrode formed of Spin Hall Effect (SHE) material, where the SHE material converts charge current I_w (or write current) to spin current I_s . Stack 120 forms a three terminal memory cell with SHE induced write mechanism and MTJ based read-out. Stack 120 comprises MTJ 121, SHE Interconnect or electrode 122, and non-magnetic metal(s) 123a/b. In one example, MTJ 121 comprises stacked ferromagnetic layer with a tunneling dielectric and another ferromagnetic layer. One or both ends along the horizontal direction of SHE Interconnect 122 is formed of non-magnetic metals 123a/b.

[0023] A wide combination of materials can be used for material stacking of MTJ 121. For example, the stack of materials include: $\text{Co}_x\text{Fe}_y\text{B}_z$, MgO, $\text{Co}_x\text{Fe}_y\text{B}_z$, Ru, $\text{Co}_x\text{Fe}_y\text{B}_z$, IrMn, Ru, Ta, and Ru, where 'x,' 'y,' and 'z' are fractions of elements in the alloys. Other materials may also be used to form MTJ 121. MTJ 121 stack comprises free magnetic layer, MgO tunneling oxide, a fixed magnetic layer which is a combination of CoFe, Ru, and CoFe layers referred to as Synthetic Anti-Ferromagnet (SAF), and an Anti-Ferromagnet (AFM) layer. The SAF layer has the property, that the magnetizations in the two CoFe layers are opposite, and allows for cancelling the dipole fields around the free magnetic layer such that a stray dipole field will not control the free magnetic layer.

[0024] SHE Interconnect 122 (or the write electrode) is made of one or more of β -Tantalum (β -Ta), Ta, β -Tungsten (β -W), W, Pt, Copper (Cu) doped with elements such as Iridium, Bismuth and any of the elements of 3d, 4d, 5d and 4f, 5f periodic groups in the Periodic Table which may exhibit high spin orbit coupling. SHE Interconnect 122 transitions into high conductivity non-magnetic metal(s) 123a/b to reduce the resistance of SHE

Interconnect 122. The non-magnetic metal(s) 123a/b are formed from one or more of: Cu, Co, α -Ta, Al, CuSi, or NiSi.

[0025] In one case, the magnetization direction of the fixed magnetic layer is perpendicular relative to the magnetization direction of the free magnetic layer (e.g., magnetization directions of the free and fixed magnetic layers are not parallel, rather they are orthogonal). For example, magnetization direction of the free magnetic layer is in-plane while the magnetization direction of the fixed magnetic layer is perpendicular to the in-plane. In another case, magnetization direction of the fixed magnetic layer is in-plane while the magnetization direction of the free magnetic layer is perpendicular to the in-plane.

[0026] The thickness of a ferromagnetic layer (i.e., fixed or free magnetic layer) may determine its magnetization direction. For example, when the thickness of the ferromagnetic layer is above a certain threshold (depending on the material of the magnet, e.g. approximately 1.5 nm for CoFe), then the ferromagnetic layer exhibits magnetization direction which is in-plane. Likewise, when the thickness of the ferromagnetic layer is below a certain threshold (depending on the material of the magnet), then the ferromagnetic layer exhibits magnetization direction which is perpendicular to the plane of the magnetic layer.

[0027] Other factors may also determine the direction of magnetization. For example, factors such as surface anisotropy (depending on the adjacent layers or a multi-layer composition of the ferromagnetic layer) and/or crystalline anisotropy (depending on stress and the crystal lattice structure modification such as FCC (face centered cubic lattice), BCC (body centered cubic lattice), or L10-type of crystals, where L10 is a type of crystal class which exhibits perpendicular magnetizations), can also determine the direction of magnetization.

[0028] In this example, the applied current I_w is converted into spin current I_s by SHE Interconnect 122. This spin current switches the direction of magnetization of the free layer and thus changes the resistance of MTJ 121. However, to read out the state of MTJ 121, a sensing mechanism is needed to sense the resistance change. In the case of **Fig. 1A**, this resistance change can be significantly higher than 4 kOhms and therefore is easier to sense. The conversion of charge current to spin current is described with reference to **Fig. 1C**.

[0029] **Fig. 1C** illustrates top view 130 of the stack of **Fig. 1C**. It is pointed out that those elements of **Fig. 1C** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. Top view 130 shows that the magnet is oriented along the width of SHE Interconnect 122 for appropriate spin injection.

[0030] The magnetic cell is written by applying a charge current via SHE Interconnect 122. The direction of the magnetic writing (in the free magnet layer) is decided by the direction of the applied charge current. Positive currents (e.g., currents flowing in the +y direction) produce a spin injection current with transport direction (along the +z direction) and spins pointing to the +x direction. The injected spin current in-turn produces spin torque to align the free magnet (coupled to the SHE material) in the +x or -x direction. The injected spin current $\vec{I}_s$ generated by a charge current $\vec{I}_c$ in the write electrode is given by:

$$\vec{I}_s = P_{SHE}(w, t, \lambda_{sf}, \theta_{SHE})(\hat{z} \times \vec{I}_c) \dots (1)$$

where, the vector of spin current $\vec{I}_s = \vec{I}_{\uparrow} - \vec{I}_{\downarrow}$ is the difference of currents with spin along and opposite to the spin direction, $\hat{z}$ is the unit vector perpendicular to the interface, P_{SHE} is the spin Hall injection efficiency which is the ratio of magnitude of transverse spin current to lateral charge current, w is the width of the magnet, t is the thickness of the SHE Interconnect 122, λ_{sf} is the spin flip length in SHE Interconnect 122, θ_{SHE} is the spin Hall angle for SHE Interconnect 122 to free ferromagnetic layer interface. The injected spin angular momentum responsible for the spin torque given by:

$$\vec{S} = h \vec{I}_s / 2e \dots (2)$$

[0031] The spin to charge conversion described with reference to **Figs. 1A-C** is based on TMR which is highly limited in the signal strength generated. As such, the TMR based spin to charge conversion has low efficiency (e.g., less than one).

[0032] Some embodiments describe a highly efficient transduction method and associated apparatus for converting spin currents to charge currents. In some embodiments, spin-to-charge conversion is achieved via spin orbit interaction in metallic interfaces (e.g., using Inverse Rashba-Edelstein Effect and/or SHE) where a spin current injected from an input magnet produces a charge current. **Table 1** summarizes transduction mechanisms for converting spin current to charge current and charge current to spin current for bulk materials and interfaces.

Table 1: Transduction mechanisms for Spin to Charge and Charge to Spin Conversion

	Charge $\rightarrow$ Spin	Spin $\rightarrow$ Charge
Bulk	Spin Hall Effect	Inverse Spin Hall Effect
Interface	Rashba-Edelstein Effect	Inverse Rashba-Edelstein

[0033] Some embodiments describe a spin interconnect where the spin polarization of the interconnect current is maintained via spin orbit interaction. This is enabled by the use of

two dimensional (2D) electron gas in a high spin orbit coupling (e.g., Rashba effect) system where the electric current is continuously polarized via the Rashba effect.

[0034] Some embodiments describe a high spin orbit coupling (SOC) spin/electrical interconnect where the conducting layers exhibit spin to linear momentum relationship. In some embodiments, the interconnect can be a single layer Rashba gas or a super lattice of multiple layers of metal interfaces with high SOC. In some embodiments, a traditional via technology (e.g., employing barriers) is employed where the spin polarization of the interconnect is lost but recovered in a subsequent high SOC interconnect. In some embodiments, a hybrid interconnect is described (e.g., a spin interconnect) which is combined (e.g., in series) with a charge interconnect, where the spin polarization is lost in the charge section of the hybrid interconnect. In some embodiments, the charge section of the interconnect can employ metals such as Ru or Co which have low spin diffusion length. In some embodiments, spin polarization is recovered when the current enters the high SOC region. In some embodiments, a magnetic stack is provided at the input of the interconnect which structurally matches to the super-lattice at the atomistic scale.

[0035] There are many technical effects of the various embodiments. For example, high efficient long range transport of spin current (e.g., greater than 100 nm) is achieved with close to no loss of spin polarization. The use of low spin diffusion materials or vias enable processing of such interconnects. In some embodiments, a metallic super lattice is described which enhances the spin-to-charge conversion (e.g., improves the conversion efficiency). The super-lattice stack of materials for conversion of spin to charge variable in vias is highly efficient (e.g., conversion efficiency of 1). In some cases, a net gain in spin to charge conversion is achieved for some stacks. In some embodiments, a metallic stack is described which structurally matches to the super-lattice at the atomistic scale for high quality spin injection. Other technical effects will be evident by various embodiments.

[0036] In the following description, numerous details are discussed to provide a more thorough explanation of embodiments of the present disclosure. It will be apparent, however, to one skilled in the art, that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring embodiments of the present disclosure.

[0037] Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate more constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. Such

indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme.

[0038] Throughout the specification, and in the claims, the term "connected" means a direct physical, electrical, or wireless connection between the things that are connected, without any intermediary devices. The term "coupled" means either a direct electrical or wireless connection between the things that are connected or an indirect electrical or wireless connection through one or more passive or active intermediary devices. The term "circuit" means one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function. The term "signal" means at least one current signal, voltage signal, magnetic signal, electromagnetic signal, or data/clock signal. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0039] The terms "substantially," "close," "approximately," "near," and "about," generally refer to being within +/- 10% of a target value (unless specifically specified). Unless otherwise specified the use of the ordinal adjectives "first," "second," and "third," etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0040] For the purposes of the present disclosure, phrases "A and/or B" and "A or B" mean (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C). The terms "left," "right," "front," "back," "top," "bottom," "over," "under," and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions.

[0041] **Fig. 2A** illustrates a portion 201 of an interconnect or via formed of super-lattice stack and corresponding side view (or perpendicular view) of its atomic structure 202, according to some embodiments. Super-lattice stack 201 is functionally equivalent to spin Hall interconnect 122 in **Fig. 1B** when super-lattice stack 201 is used as a via, in accordance with some embodiments. In some embodiments, super-lattice stack 201 comprises layers of metals, such as Copper (Cu), Silver (Ag), Gold (Au), and layers of a surface alloy, e.g. Bismuth (Bi) on Ag. In some embodiments, 'N' number of layers of surface alloy and metal are stacked in alternating fashion, where 'N' is an integer. In one example, N=10 which is

sufficient to convert input spin current to corresponding charge current with efficiency of one or higher. In other examples, other number of layers may be used to trade off conversion efficiency versus area of the stack.

[0042] In some embodiments, the surface alloy is one of: Bi-Ag, Antimony-Bismuth (Sb-Bi), Sb-Ag, or Lead-Nickel (Pb-Ni), etc. In some embodiments, the metal is a noble metal (e.g., Ag, Cu, and Au) doped with other elements for group 4d and/or 5d of the Periodic Table. In some embodiments, one of the metals of the surface alloy is an alloy of heavy metal or of materials with high Spin Orbit Coupling (SOC) strength, where the SOC strength is directly proportional to the fourth power of the atomic number of the metal.

[0043] In some embodiments, all metal layers in the stack are of the same type of metal. For example, all metal layers of stack 201 are formed of Ag which is sandwiched between layers of Bi or Sb. In other embodiments, different metal layers may be used in the same stack for the metal portion of the layers. For example, some metal layers of stack 201 are formed of Ag and others are formed of Cu such that the metal is adjacent to layers of Bi or Sb.

[0044] In some embodiments, the atomic structure in side view 202 shows non-uniform patterns of Ag and Bi atoms of the surface alloy sandwiched between layers of Cu or other metals. Here, the crystals of Ag and Bi have lattice mismatch (i.e. the distance between neighboring atoms of Ag and Bi is different). In some embodiments, the surface alloy is formed with surface corrugation resulting from the lattice mismatch (i.e. the positions of Bi atoms are offset by varying distance from a plane parallel to a crystal plane of the underlying metal). The surface alloy is a structure not symmetric relative to the mirror inversion defined by a crystal plane. This inversion asymmetry leads to spin-orbit coupling in electrons near the surface (also referred to as the Rashba effect). **Fig. 2B** illustrates the portion 201 of the interconnect or via formed of a super-lattice stack and corresponding top view of its atomic structure 220, according to some embodiments.

[0045] In some embodiments, the interface surface alloy of BiAg₂ or PbAg₂ comprises of a high density two dimensional (2D) electron gas with high Rashba SOC. The spin orbit mechanism responsible for spin-to-charge conversion is described by Rashba effect in 2D electron gases. In some embodiments, 2D electron gases are formed between Bi and Ag, and when current flows through the 2D electron gases, it becomes a 2D spin gas because as charge flows, electrons get polarized.

[0046] The Hamiltonian energy H_R of the SOC electrons in the 2D electron gas corresponding to the Rashba effect is expressed as:

$$H_R = \alpha_R (k \times \hat{z}) \cdot \hat{\sigma} \dots (3)$$

where α_R is the Rashba coefficient, ' k ' is the operator of momentum of electrons, $\hat{z}$ is a unit vector perpendicular to the 2D electron gas, and $\hat{\sigma}$ is the operator of spin of electrons.

[0047] The following equations are described with reference to a nanomagnets (e.g., ferromagnet) coupled to the super-lattice stack of layers. The spin polarized electrons with direction of polarization in-plane (e.g., in the xy-plane) experience an effective magnetic field dependent on the spin direction which is given as:

$$B(\hat{k}) = \frac{\alpha_R}{\mu_B} (\hat{k} \times \hat{z}) \dots (4)$$

where μ_B is the Bohr magneton.

[0048] This results in the generation of a charge current in the interconnect which is proportional to the spin current I_s . The spin orbit interaction at the Ag and Bi interface (i.e., the Inverse Rashba-Edelstein Effect (IREE)) produces a charge current I_c in the horizontal direction which is expressed as:

$$I_c = \frac{\lambda_{IREE} I_s}{w_m} \dots (5)$$

where w_m is width of the ferromagnet coupled to the stack of layers, and λ_{IREE} is the IREE constant (with units of length) proportional to α_R .

[0049] The IREE effect produces spin-to-charge current conversion around 0.1 with existing materials at 10 nm magnet width. For scaled nanomagnets (e.g., 5 nm width) and exploratory SHE materials such as Bi_2Se_3 , the spin-to-charge conversion efficiency can be between 1 and 2.5, in accordance with some embodiments. The net conversion of the drive charge current I_d to magnetization dependent charge current is:

$$I_c = \pm \frac{\lambda_{IREE} P I_d}{w_m} \dots (6)$$

where P is the spin polarization.

[0050] **Fig. 3A** illustrates hybrid interconnect 300 comprising a first interconnect with a super-lattice stack, a second interconnect formed of metal, and third interconnect with a super-lattice stack, in accordance with some embodiments. It is pointed out that those elements of **Fig. 3A** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0051] In some embodiments, hybrid interconnect 300 comprises first interconnect 301 (a portion of which is illustrated in **Figs. 2A-B**) coupled in series with second interconnect 302 (e.g., metal interconnect) which is coupled in series with third interconnect

303. In some embodiments, first interconnect 301 includes a stack of metal layers having a non-alloy metal and a templating layer adjacent to the non-alloy metal. In some embodiments, the non-alloy metal is formed of a material which is selected from a group consisting of: Ag, Cu, Al, and Au. In some embodiments, the templating layer is formed of MgO. In some embodiments, the non-alloy metal is adjacent to a metal formed of a material selected from group consisting of: Bi, Pb, and chalcogenide material. In some embodiments, the chalcogenide material is selected from a group consisting of: TiSe_2 , MoSe_2 , WSe_2 , SiS_2 , B_2S_3 , Sb_2S_3 , Ta_2S_5 , Re_2S_7 , and semiconductors of the type MX_2 , with 'M' being a transition metal atom (e.g., Mo, W, etc.) and 'X' being an achalcogen atom (e.g., S, Se, or Te.).

[0052] In some embodiments, first interconnect 301 is configured to carry spin current I_s and charge current I_c together over long distances along the length of first interconnect 301. Here, the direction of spin and charge are locked. For example, when charge I_c is to flow from left to right along the length of first interconnect 301, then the spin direction is positive. In another example, when charge I_c is to flow from right to left along the length of first interconnect 301, then the spin direction is negative. As such, the materials of first interconnect 301 (which is formed of a super-lattice e.g., of Ag, Bi, and Cu repeated as a pattern in a stack) allow propagation of spin in concert with charge along the length of first interconnect 301.

[0053] Spin current is known to diminish and completely lost as it propagates through a normal interconnect (e.g., a traditional metal interconnect made of Cu). The super-lattice interconnect of various embodiments, however, allows the spin current to propagate without being diminished because the spin is locked with a corresponding charge, and charge current does not diminish like spin current when it flows through a metal interconnect. This allows for transmission of spin current I_s over long distances through an interconnect without the need of repeaters.

[0054] In this example, the spin I_s and charge I_c are flowing from left to right along the length of first interconnect 301. When the spin and charge enter second interconnect 302, then spin begins to dissipate and eventually lost, leaving only charge current I_c . In some embodiments, second interconnect 302 is formed of materials that are zero Rashba materials. For example, second interconnect 302 is formed of a material selected from a group consisting of: Ru, Cu, Ta, W, Co, Ni, NiSi, and semiconductors of the type MX_2 , with 'M' being a transition metal atom (e.g., Mo, W, etc.) and 'X' being an achalcogen atom (e.g., S, Se, or Te.).

[0055] In some embodiments, third interconnect 303 is adjacent (e.g., coupled in series) to the second interconnect 302. In some embodiments, third interconnect 303 comprises a stack of metal layers having a non-alloy metal and a templating layer adjacent to the non-alloy metal. In some embodiments, the stack of materials for third interconnect 303 can be the same as the stack of materials for first interconnect 301. In some embodiments, the stack of materials for third interconnect 303 can be different than the stack of materials for first interconnect 301, but still capable to carry spin current I_s and charge current I_c over long distances.

[0056] In some embodiments, when charge current I_c travels through second interconnect 302 and reaches third interconnect, the spin current I_s is again formed and has the same direction as the spin direction in first interconnect 301. One reason for the adaption of the same spin current I_s in third interconnect 303 is that when the stack of third interconnect 303 receives I_c , it develops spin current I_s which is locked with the charge current I_c .

[0057] For example, when charge I_c is to flow from left to right along the length of second interconnect 302, then the direction of spin I_s in third interconnect 303 is positive. As such, the materials of third interconnect 303 (which is formed of a super-lattice e.g., of Ag, Bi, and Cu repeated as a pattern in a stack) allow propagation of spin in concert with charge along the length of third interconnect 303. This allows for transmission of spin current I_s over long distances through hybrid interconnect 300 without the need of repeaters.

[0058] In some embodiments, templating layer 304 is formed around the first, second, third interconnects. In some embodiments, templating layer 304 is formed of MgO. In other embodiments, other materials may be used for templating layer 304. In some embodiments, templating layer 304 is a crystallinity templating layer which is coupled to a metal (e.g., Ag or Bi). In some embodiments, the crystallinity templating layer 304 is one of: MgO (Magnesium Oxide), STO (Strontium Titanate), MgAlO (Magnesium Aluminum Oxide, Ag (Silver), DyScO₃, GdScO₃, BTO (e.g., BaTiO₃), SrRuO₃ (SRO) or Molybdenum. In some embodiments, the crystallinity templating layer and the metal layer together form a pair of layers which is one of: MgO and Ag, MgO and Au; MgO and Cu; or MgO and Al.

[0059] While the embodiment of **Fig. 3A** illustrates the same templating layer for first, second, and third interconnects 301, 302, and 303, respectively, different interconnects can have same or different templating layers. For example, in some embodiments, when second interconnect 302 is formed of Ru then the crystallinity templating layer associated with second interconnect 302 is Molybdenum. In this case, a metal templates another metal.

In some embodiments, a crystalline axis of the metal layer is set by crystallinity templating layer 304. In some embodiments, the metal layer and crystallinity templating layer 304 together form at least one of: via; interconnect; contact, or transistor gate.

[0060] In some embodiments, the crystallinity templating layer 304 is coupled to three sides of the metal layer. In some embodiments, crystallinity templating layer 304 is coupled to four sides of the metal layer (e.g., Ru, Cu, Ta, W, Co, Ni, NiSi). **Fig. 3B** illustrates cross-section 320 along dotted line YY through first interconnect 301 where templating layer 304 surrounds the stack of materials of first interconnect 301 on four sides, in accordance with some embodiments. In some embodiments, crystallinity templating layer 304 is coupled to two sides of the metal layer. In some embodiments, crystallinity templating layer 304 is coupled to one side of the metal layer. In some embodiments, crystallinity templating layer 304 has an unordered structure. The process of templating metal improves crystallinity of the metal coupled to the templating metal which in turn reduces the resistivity and electro-migration of the metal. The templating of metal as described with reference to the various embodiments also improves fabrication using subtracting processing.

[0061] **Fig. 3C** illustrates another hybrid interconnect 330 comprising first interconnect 331 with a super-lattice stack, second interconnect 302 formed of metal, and third interconnect 303 with a super-lattice stack, in accordance with some embodiments. It is pointed out that those elements of **Fig. 3C** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. So as not to obscure the embodiment of **Fig. 3C**, differences between **Fig. 3C** and **Fig. 3A** are described. Here, first interconnect 331 is different than first interconnect 301.

[0062] In some embodiments, first interconnect 331 comprises a first interface layer (e.g., Ag, Cu, Al, or Au) coupled to a bulk layer. In some embodiments, the bulk layer formed of a material selected from a group consisting of: Ta, Hf, W, Pt, Bi; Ag doped with Ta, Hf, W, Pt, Bi, or Ir; Al doped with Ta, Hf, W, Pt, Bi, or Ir; Cu doped with Ta, Hf, W, Pt, Bi, or Ir; and Au doped with Ta, Hf, W, Pt, Bi, or Ir. In some embodiments, the bulk layer is coupled to a second interface layer (e.g., Ag, Cu, Al, or Au) which in turn is coupled Bi followed by layers of Cu, Ag, and Bi in that pattern. In some embodiments, charge current and spin together flow in concert along the first interface. In some embodiments, the bulk layer provides the bulk spin orbit coupling effect in parallel with the interface effect of the first interface layer.

[0063] For example, the bulk layer may provide 80% of the charge and spin current transfer along the length of first interconnect 331 while the first interface layer may provide 20% of the charge and spin current transfer along the length of first interconnect 331. In another example, the bulk layer may provide 20% of the charge and spin current transfer along the length of first interconnect 331 while the first interface layer may provide 80% of the charge and spin current transfer along the length of first interconnect 331. In some embodiments, the second interface layer behaves the same way as the first interface layer. **Fig. 3D** illustrates a cross-section 340 of first interconnect 331 along the dotted line YY, in accordance with some embodiments.

[0064] In some embodiments, templating layer 304 surrounds the stack of materials of first interconnect 331 on four sides, in accordance with some embodiments. In some embodiments, crystallinity templating layer 304 is coupled to two sides of the metal layer. In some embodiments, crystallinity templating layer 304 is coupled to one side of the metal layer. In some embodiments, crystallinity templating layer 304 has an unordered structure. The process of templating metal improves crystallinity of the metal coupled to the templating metal which in turn reduces the resistivity and electro-migration of the metal. The templating of metal as described with reference to the various embodiments also improves fabrication using subtracting processing.

[0065] **Figs. 4A-B** illustrate apparatuses 400 and 420, respectively, having two interconnects with super-lattice stacks coupled together by a metallic via, in accordance with some embodiments. It is pointed out that those elements of **Figs. 4A-B** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. **Fig. 4A** is described with reference to **Fig. 3A**. **Fig. 4A** is described with reference to **Fig. 4B**.

[0066] In some embodiments, apparatus 400 comprises first interconnect 301 (a portion of which is illustrated in **Figs. 2A-B** and **Fig. 3A**) coupled in series with a metal via which is coupled in series which is coupled in series with second interconnect 403. The embodiments are also applicable to first interconnect 331, but for the sake of explaining the various embodiments, first interconnect 301 is used as an example. In this configuration, first interconnect 301 is on a different conducting layer than second interconnect 403.

[0067] As discussed with reference to **Fig. 3A**, first interconnect 301 is configured to carry spin current I_s and charge current I_c over long distances along the length of first interconnect 301. Here, the direction of spin and charge are locked. For example, when charge I_c is to flow from left to right along the length of first interconnect 301, then the spin

direction is positive. As such, the materials of first interconnect 301 (which is formed of a super-lattice e.g., of Ag, Bi, and Cu repeated as a pattern in a stack) allow propagation of spin in concert with charge along the length of first interconnect 301.

[0068] Spin current is known to diminish and completely lost as it propagates through a normal interconnect (e.g., a traditional metal interconnect made of Cu). The super-lattice interconnect of various embodiments allows the spin current to propagate without being diminished because the spin is locked with a corresponding charge current, and charge current does not diminish like spin current when it flows through a metal interconnect. This allows for transmission of spin current I_s over long distances through an interconnect without the need to repeaters.

[0069] In this example, the spin I_s and charge I_c are flowing from left to right along the length of first interconnect 301. When the spin and charge enter via 402, then spin begins to dissipate and eventually lost, leaving only charge current I_c . The direction of the charge current depends on the potential difference between second interconnect 403 and first interconnect 301. In some embodiments, via 402 is formed of materials that are zero Rashba materials. For example, via 402 is formed of a material selected from a group consisting of: Ru, Cu, Ta, W, Co, Ni, Al, Ag, NiSi, and semiconductors of the type MX_2 , with 'M' being a transition metal atom (Mo, W, etc.) and 'X' being a chalcogen atom (S, Se, or Te).

[0070] In some embodiments, second interconnect 403 is adjacent to (e.g., coupled to) via 402. In some embodiments, second interconnect 403 comprises a stack of metal layers having a non-alloy metal and a templating layer adjacent to the non-alloy metal. In some embodiments, the stack of materials for second interconnect 403 can be the same as the stack of materials for first interconnect 301. In some embodiments, the stack of materials for second interconnect 403 can be different than the stack of materials for first interconnect 301, but still capable to carry spin current I_s and charge current I_c over long distances.

[0071] In some embodiments, when charge current I_c travels through via 402 and reaches second interconnect 403, the spin current I_s is again formed and has the same direction as the direction in first interconnect 301. One reason for the adaption of the same spin current I_s in second interconnect 403 is that when the stack of second interconnect 403 receives I_c , it develops spin current I_s which is locked with the charge current I_c . As such, the materials of second interconnect 403 (which is formed of a super-lattice e.g., of Ag, Bi, and Cu repeated as a pattern in a stack) allow propagation of spin in concert with charge along the length of second interconnect 403. This allows for transmission of spin current I_s over long distances without the need to repeaters.

[0072] In some embodiments, templating layer 404 is formed around via 402 and second interconnect 403. In some embodiments, templating layer 404 is a crystallinity templating layer which is coupled to a metal (e.g., Ag or Bi) and formed of the same material as templating layer 304. While the embodiment of **Fig. 4A** illustrates the templating layer of second interconnect 403 to be the same as templating layer for via 402, in some embodiments, the templating layer coupled to via 402 is different than the templating layer for first and second interconnects.

[0073] Apparatus 420 of **Fig. 4B** is similar to apparatus 400 of **Fig. 4A** except that via 422 has a barrier layer 423 (e.g., via 402 is similar to via 423 but for the barrier layer 423). In some embodiments, 423 is an interlayer barrier layer used in backend metal stacks. Interlayer barrier layer is a low electro-migration layer typically formed of high impedance (Z) materials with large melting points.

[0074] **Fig. 5** illustrates apparatus 500 showing two interconnects with super-lattice stacks coupled together by a via formed of a super-lattice stack, in accordance with some embodiments. It is pointed out that those elements of **Fig. 5** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. So as not to obscure the embodiments of **Fig. 5**, difference between **Fig. 4A** and **Fig. 5** are described. Here, via 402 is replaced with via 502. In some embodiments, via 502 is formed of the same stack of materials as first interconnect 301 and second interconnect 403.

[0075] In some embodiments, when spin and charge current from first interconnect 301 enter via 502, the stack of materials of 502 convert the spin current into charge current. When this charge current I_c reaches second interconnect 403, it becomes spin polarized. As such, the spin current I_s is again formed that has the same direction as the direction of spin in first interconnect 301. One reason for the adaption of the same spin current I_s in second interconnect 403 is that when the stack of second interconnect 403 receives I_c , it develops spin current I_s which is locked with the charge current I_c .

[0076] **Fig. 6** illustrates plots 600 showing a spin-to-charge conversion over layers of super-lattice stack 502 which is used as via in **Fig. 5**, according to some embodiments of the disclosure. It is pointed out that those elements of **Fig. 6** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0077] Plots 602 and 603 illustrate conversion efficiency as a function of the thickness of the super-lattice stack 502. Here, for plot 602, the x-axis is the injected spin

current I_s (in the z-direction) while the y-axis is the thickness of super-lattice stack 601 (in nanometer (nm)), while for plot 603, the x-axis is charge current I_c (in the x-direction) while the y-axis is the thickness of super-lattice stack 601. The horizontal dashed-lines indicate the interfaces of the layers of super-lattice stack 502 for plots 602 and 603.

[0078] Plot 602 indicates an exponential decay of the injected spin current I_s in super-lattice stack 601 due to the spin de-coherence in Ag. The decay occurs down the thickness of super-lattice stack 601, according to some embodiments. The spin current I_s drops in steps at the interface of surface alloy and the metal of stack 601, and is a gradient between the surface, according to some embodiments. Plot 603 indicates the conversion of the injected spin current I_s to charge current I_c at every interface of metal and surface alloy. For example, spin-to-charge conversion occurs at every interface of Bi and Ag leading to the production of an in-plane charge current, according to some embodiments. In some embodiments, after ten layers of surface alloy and metal layers of super-lattice stack 502, most of the injected spin current I_s decays (i.e., the spin current is converted to charge current).

[0079] **Figs. 7A-B** illustrate plots 700 and 720, respectively, showing spin-to-charge conversion efficiency for different Silver (Ag) diffusion lengths, according to some embodiments of the disclosure. It is pointed out that those elements of **Figs. 7A-B** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. For both plots 700 and 720, the x-axis is the Electrode Thickness in nm (i.e., thickness of super-lattice stack 502), the y-axis to the left is Spin Polarization (i.e., ratio of Spin Current I_c to Charge Current I_s), and the y-axis to the right is the ratio of spin to charge conversion (i.e., I_c/I_s).

[0080] Plot 700 illustrates two waveforms—solid and dashed. In this example, the spin diffusion length of Ag is 15 nm (i.e., $\lambda_{Ag} = 15$ nm). The solid waveform shows how charge current increases as spin current passes through the layers of super-lattice stack 502. The rise in the steps of the charge current are at the interface of Bi/Ag. At the end of super-lattice stack 502 (in this example, near the stack thickness of 20nm), 85% of spin current I_s converts into charge current I_c (e.g., the efficiency is 0.85). The dashed waveform shows the spin polarization as a function of electrode thickness. As spin current flows down through the layers of super-lattice stack 502, it loses polarization because it converts to charge current. At the end of super-lattice stack 502 (in this example, at a stack thickness of 20nm), most spin current is gone (e.g., converted to charge current). This charge current then enters third interconnect 403 and spin polarizes third interconnect 403. As such, spin and charge current begin to flow in concert in third interconnect 403

[0081] Plot 720 is similar to plot 700, but the spin diffusion length of Ag is increased to 200 nm from 15 nm. Plot 720 shows a gain in the charge current (e.g., greater than one spin-to-charge current conversion efficiency). Here, a net conversion efficiency of four can be achieved with a spin diffusion length of 200 nm.

[0082] **Figs. 8A-B** illustrate cross-sections 800, 820, 830, 840, 850, 860, and 870 of a die showing fabrication of templated super-lattice interconnects and vias, in accordance with some embodiments of the disclosure. Although the fabrication processes with reference to **Figs. 8A-B** are shown in a particular order, the order of the actions can be modified. Thus, the illustrated embodiments can be performed in a different order, and some actions/fabrication processes may be performed in parallel. Some of the fabrication processes listed in **Figs. 8A-B** are optional in accordance with certain embodiments. The numbering of the fabrication processes presented is for the sake of clarity and is not intended to prescribe an order of operations in which the various blocks must occur. Additionally, operations from the various flows may be utilized in a variety of combinations.

[0083] **Fig. 8A** illustrates one example of a starting point. Here, the die cross-section 800 shows deposition of a layer of dielectric 801. In some embodiments, the dielectric is an oxide (e.g., SiO₂). In some embodiments, the process of fabricating the templated super-lattice stacked interconnect and vias can start at various points in the fabrication process as described with reference to various embodiments. **Fig. 8B** illustrates cross-section 820 of the die after deposition of a metal layer 802a on layer 801. For example, a layer of Cu, Fe, Ni, Co, Al, Ag, NiFe, NiCo, or Heusler Alloy is deposited as metal layer 802a over layer of oxide 801. This layer of metal 802a may have an unordered crystalline structure.

[0084] Here, the term “unordered” crystalline structure generally refers to a crystalline structure in which the electron wave diffraction is not defined by Bragg’s law. Unordered materials may exhibit high directional and angular isotropy without long range spatial/directional periodicity. Unordered materials are characterized by a signature on a TEM (Transmission Electron Microscopy), STEM (Scanning Transmission Electron Microscopy) or RHEED (Reflection High-Energy Electron Diffraction), XRD (X-ray Powder Diffraction) metrology.

[0085] **Fig. 8C** illustrates cross-section 830 of the die after deposition of a templating material 803 over metal layer 802a. In some embodiments, after increasing temperature, e.g., to 298 K, templating material 803 causes metal layer 802a to transform to metal layer 802b, where metal layer 802b has an ordered crystalline structure while metal layer 802a has an unordered crystalline structure. In some embodiments, metal layer 802a is Metal 0 (M0)

layer. In other embodiments, metal layer 802a can be any metal layer of a process technology node.

[0086] **Fig. 8D** illustrates cross-section 840 of the die after templating material 803 is removed and dielectric layer 804 (e.g., layer of oxide) is deposited over ordered metal layer 802b. Here, the term “ordered” generally refers to material condition that shows electron wave diffraction as defined by Bragg’s law. Ordered material may be characterized by one of the space groups combined with a unit cell. Ordered material exhibit long range periodicity both in direction and displacement. In Metrology tools such as XRD and RHEED, an interferometric signature is evident for ordered materials.

[0087] In some embodiments, templating material 803 is a sacrificial layer which is removed after the crystalline structure of metal layer 802b is ordered to be metal layer 802a. In some embodiments, templating material 803 remains as is and further processing steps are performed above templating material 803. In some embodiments, metal layer 802a/b is one of: Fe, Co, Ni, Ru, Cu, alloys of Fe and Co; alloys of Ni and Co; Ag, and Heusler alloy metals. In some embodiments, the Heusler alloy metals is at least one of: Cu_2MnAl , Cu_2MnIn , Cu_2MnSn , Ni_2MnAl , Ni_2MnIn , Ni_2MnSn , Ni_2MnSb , Ni_2MnGa , Co_2MnAl , Co_2MnSi , Co_2MnGa , Co_2MnGe , Pd_2MnAl , Pd_2MnIn , Pd_2MnSn , Pd_2MnSb , Co_2FeSi , Co_2FeAl , Fe_2VAl , Mn_2VGa , or Co_2FeGe .

[0088] In some embodiments, templating material 803 is a crystallinity templating layer which is one of: MgO, STO, MgAlO, Ag, DyScO_3 , GdScO_3 , BTO (e.g., BaTiO_3), SrRuO_3 (SRO) or Molybdenum. In some embodiments, metal layer 802a/b is Ru and templating material 803 is Molybdenum. This is a case of metal templating another metal. In some embodiments, a crystalline axis of metal layer 802a/b is set by templating material 803.

[0089] **Fig. 8E** illustrates cross-section 850 of the die after trenches 805 are etched through dielectric layer 804. Any known suitable process of forming trenches 805 may be used. In this example, two trenches are etched (e.g., the left and right trenches) and each trench is a future location of a via to couple to metal layer 802b and a future location of another super-lattice stacked interconnect layer. In some embodiments, the super-lattice stacked interconnect extends orthogonal to metal layer 802b. For example, metal layer 802b is metal layer 1 (M1) and the via (later shown as 807) is metal layer 2 (M2).

[0090] **Fig. 8F** illustrates cross-section 860 of the die after templating material 806 (e.g., 304 or 404) is deposited along the outer walls of trenches 805. In some embodiments, templating material 806 is any of the materials discussed with reference to templating material 803, 304, and/or 404. Any known method for depositing templating material 806

along the outer walls may be used. In this example, templating material 806 behaves as a liner which separates the via and super-lattice stacked interconnect from dielectric 804.

[0091] **Fig. 8G** illustrates cross-section 870 of the die after metal 807 is deposited in trench 805. Metal 807 forms the via. In some embodiments, via 807 is formed of materials that are zero Rashba materials. For example, via 807 is formed of a material selected from a group consisting of: Ru, Cu, Ta, W, Co, Ni, Al, Ag, and NiSi. In some embodiments, after metal for via 807 is deposited, metal layers forming super-lattice interconnect 808 are deposited one at a time. The materials for the metal layers forming super-lattice 808 can be the materials discussed with reference to first interconnect 301. In some embodiments, after increasing temperature (e.g., to 298 K), templating material 806 causes metal 807 and metal layers forming super-lattice 808 to transform from unordered crystalline structure to ordered crystalline structure.

[0092] In some embodiments, damascene based processing method are used for creating templated interconnect 802b, via 807, and super-lattice interconnect 808. In some embodiments, subtractive processing methods are used for creating templated interconnect 802b, via 807, and super-lattice interconnect 808. In some embodiments, recess processing method are used to take advantage of the templated interconnect 802b, via 807, and super-lattice interconnect 808. In some embodiments, super-lattice stacks comprising of repeated patterns of template enhancing material are used for metal 802b and metal 806.

[0093] **Fig. 9** illustrates cross-section 900 of a die showing one of the fabrication steps where templated super-lattice interconnects and templated super-lattice vias are formed, in accordance with some embodiments. It is pointed out that those elements of **Fig. 9** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. **Fig. 9** illustrates alternative fabrication processes after process described with reference to **Fig. 8F**. Here, instead of depositing metal 807 to form vias, super-lattice stack of materials (e.g., 502) are deposited to form super-lattice stack vias 907 for efficient spin-to-charge conversion. After via 907 is formed, super-lattice interconnect 908 is formed just as super-lattice interconnect 808 is formed, in accordance with some embodiments.

[0094] **Fig. 10** illustrates a smart device or a computer system or a SoC (System-on-Chip) 1600 with super-lattice stack based interconnect, according to some embodiments. It is pointed out that those elements of **Fig. 10** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0095] **Fig. 10** illustrates a block diagram of an embodiment of a mobile device in which flat surface interface connectors could be used. In some embodiments, computing device 1600 represents a mobile computing device, such as a computing tablet, a mobile phone or smart-phone, a wireless-enabled e-reader, or other wireless mobile device. It will be understood that certain components are shown generally, and not all components of such a device are shown in computing device 1600.

[0096] For purposes of the embodiments, the transistors in various circuits and logic blocks described here are metal oxide semiconductor (MOS) transistors, which include drain, source, gate, and bulk terminals. The transistors also include Tri-Gate and FinFET transistors, Gate All Around Cylindrical Transistors, Tunneling FET (TFET), Square Wire, or Rectangular Ribbon Transistors or other devices implementing transistor functionality like carbon nanotubes or spintronic devices. MOSFET symmetrical source and drain terminals i.e., are identical terminals and are interchangeably used here. A TFET device, on the other hand, has asymmetric Source and Drain terminals. Those skilled in the art will appreciate that other transistors, for example, Bi-polar junction transistors—BJT PNP/NPN, BiCMOS, CMOS, eFET, etc., may be used without departing from the scope of the disclosure. The term “MN” indicates an n-type transistor (e.g., NMOS, NPN BJT, etc.) and the term “MP” indicates a p-type transistor (e.g., PMOS, PNP BJT, etc.).

[0097] In some embodiments, computing device 1600 includes first processor 1610 with super-lattice stack based interconnect, according to some embodiments discussed. Other blocks of the computing device 1600 may also include super-lattice stack based interconnect, according to some embodiments. The various embodiments of the present disclosure may also comprise a network interface within 1670 such as a wireless interface so that a system embodiment may be incorporated into a wireless device, for example, cell phone or personal digital assistant.

[0098] In some embodiments, processor 1610 can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 1610 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, and/or operations related to connecting the computing device 1600 to another device. The processing operations may also include operations related to audio I/O and/or display I/O.

[0099] In some embodiments, computing device 1600 includes audio subsystem 1620, which represents hardware (e.g., audio hardware and audio circuits) and software (e.g., drivers, codecs) components associated with providing audio functions to the computing device. Audio functions can include speaker and/or headphone output, as well as microphone input. Devices for such functions can be integrated into computing device 1600, or connected to the computing device 1600. In one embodiment, a user interacts with the computing device 1600 by providing audio commands that are received and processed by processor 1610.

[00100] In some embodiments, computing device 1600 comprises display subsystem 1630. Display subsystem 1630 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display for a user to interact with the computing device 1600. Display subsystem 1630 includes display interface 1632, which includes the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 1632 includes logic separate from processor 1610 to perform at least some processing related to the display. In one embodiment, display subsystem 1630 includes a touch screen (or touch pad) device that provides both output and input to a user.

[00101] In some embodiments, computing device 1600 comprises I/O controller 1640. I/O controller 1640 represents hardware devices and software components related to interaction with a user. I/O controller 1640 is operable to manage hardware that is part of audio subsystem 1620 and/or display subsystem 1630. Additionally, I/O controller 1640 illustrates a connection point for additional devices that connect to computing device 1600 through which a user might interact with the system. For example, devices that can be attached to the computing device 1600 might include microphone devices, speaker or stereo systems, video systems or other display devices, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

[00102] As mentioned above, I/O controller 1640 can interact with audio subsystem 1620 and/or display subsystem 1630. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of the computing device 1600. Additionally, audio output can be provided instead of, or in addition to display output. In another example, if display subsystem 1630 includes a touch screen, the display device also acts as an input device, which can be at least partially managed by I/O controller 1640. There can also be additional buttons or switches on the computing device 1600 to provide I/O functions managed by I/O controller 1640.

[00103] In some embodiments, I/O controller 1640 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other hardware that can be included in the computing device 1600. The input can be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

[00104] In some embodiments, computing device 1600 includes power management 1650 that manages battery power usage, charging of the battery, and features related to power saving operation. Memory subsystem 1660 includes memory devices for storing information in computing device 1600. Memory can include nonvolatile (state does not change if power to the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory subsystem 1660 can store application data, user data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of the computing device 1600.

[00105] Elements of embodiments are also provided as a machine-readable medium (e.g., memory 1660) for storing the computer-executable instructions (e.g., instructions to implement any other processes discussed herein). The machine-readable medium (e.g., memory 1660) may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, phase change memory (PCM), or other types of machine-readable media suitable for storing electronic or computer-executable instructions. For example, embodiments of the disclosure may be downloaded as a computer program (e.g., BIOS) which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

[00106] In some embodiments, computing device 1600 comprises connectivity 1670. Connectivity 1670 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers, protocol stacks) to enable the computing device 1600 to communicate with external devices. The computing device 1600 could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

[00107] Connectivity 1670 can include multiple different types of connectivity. To generalize, the computing device 1600 is illustrated with cellular connectivity 1672 and wireless connectivity 1674. Cellular connectivity 1672 refers generally to cellular network

connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, or other cellular service standards. Wireless connectivity (or wireless interface) 1674 refers to wireless connectivity that is not cellular, and can include personal area networks (such as Bluetooth, Near Field, etc.), local area networks (such as Wi-Fi), and/or wide area networks (such as WiMax), or other wireless communication.

[00108] In some embodiments, computing device 1600 comprises peripheral connections 1680. Peripheral connections 1680 include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that the computing device 1600 could both be a peripheral device ("to" 1682) to other computing devices, as well as have peripheral devices ("from" 1684) connected to it. The computing device 1600 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on computing device 1600. Additionally, a docking connector can allow computing device 1600 to connect to certain peripherals that allow the computing device 1600 to control content output, for example, to audiovisual or other systems.

[00109] In addition to a proprietary docking connector or other proprietary connection hardware, the computing device 1600 can make peripheral connections 1680 via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other types.

[00110] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the

specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

[00111] Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

[00112] While the disclosure has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description. The embodiments of the disclosure are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

[00113] In addition, well known power/ground connections to integrated circuit (IC) chips and other components may or may not be shown within the presented figures, for simplicity of illustration and discussion, and so as not to obscure the disclosure. Further, arrangements may be shown in block diagram form in order to avoid obscuring the disclosure, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the present disclosure is to be implemented (i.e., such specifics should be well within purview of one skilled in the art). Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the disclosure, it should be apparent to one skilled in the art that the disclosure can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

[00114] The following examples pertain to further embodiments. Specifics in the examples may be used anywhere in one or more embodiments. All optional features of the apparatus described herein may also be implemented with respect to a method or process.

[00115] For example, an apparatus is provided which comprises: a first super-lattice possessing spin-orbit coupling for electrons; a metal interconnect adjacent to the first super-lattice; and a second super-lattice possessing spin-orbit coupling for electrons, the second super-lattice being adjacent to the metal interconnect. In some embodiments, the first or second super-lattices comprise: a first interface layer formed of a material selected from a group consisting of: Ag, Cu, Au, and Al; a bulk layer adjacent to the first interface layer, wherein the bulk layer is formed of a material selected from a group consisting of: Ta, Hf, W, Pt, Bi; Ag doped with Ta, Hf, W, Pt, Bi, or Ir; Al doped with Ta, Hf, W, Pt, Bi, or Ir; Cu

doped with Ta, Hf, W, Pt, Bi, or Ir; and Au doped with Ta, Hf, W, Pt, Bi, or Ir; a second interface layer adjacent to the bulk layer, wherein the second interface layer is formed of a different material than the first interface layer, wherein the different material for the second interface layer is selected from a group consisting of: Ag, Cu, Al, and Au; and a metal layer adjacent to the second interface layer, wherein the metal layer is formed of a material selected from group consisting of: Bi, Pb, and chalcogenide material.

[00116] In some embodiments, the chalcogenide material is selected from a group consisting of: TiSe_2 , MoSe_2 , WSe_2 , SiS_2 , B_2S_3 , Sb_2S_3 , Ta_2S_5 , Re_2S_7 , and semiconductors of the type MX_2 , with 'M' being a transition metal and 'X' being an achalcogen. In some embodiments, 'M' is selected from a group consisting of: Mo and W, and wherein 'X' is selected from a group consisting of: S, Se, and Te. In some embodiments, the metal interconnect is formed of a material which is selected from a group consisting of: Ru, Cu, Ta, W, Co, Al, Ag, Ni, and NiSi.

[00117] In another example, a system is provided which comprises: a memory; a processor coupled to the memory, the processor including an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to couple to another device.

[00118] In another example, an apparatus is provided which comprises: a first interconnect including: a first interface layer formed of a material selected from a group consisting of: Ag, Cu, Al, and Au; and a bulk layer adjacent to the first interface layer, wherein the bulk layer is formed of a material selected from a group consisting of: Ta, Hf, W, Pt, Bi; Ag doped with Ta, Hf, W, Pt, Bi, or Ir; Al doped with Ta, Hf, W, Pt, Bi, or Ir; Cu doped with Ta, Hf, W, Pt, Bi, or Ir; and Au doped with Ta, Hf, W, Pt, Bi, or Ir; a second interface layer adjacent to the bulk layer, wherein the second interface layer is formed of a material selected from a group consisting of: Ag, Cu, Al, and Au; a metal layer adjacent to the second interface layer, wherein the metal layer is formed of a material selected from a group consisting of: Bi, Pb, and chalcogenide material; and a second interconnect adjacent to the first interconnect, the second interconnect formed of a material selected from a group consisting of: Ru, Cu, Ta, W, Co, Ni, NiSi and semiconductors of the type MX_2 , with 'M' being a transition metal and 'X' being an achalcogen.

[00119] In some embodiments, 'M' is selected from a group consisting of: Mo and W, and wherein 'X' is selected from a group consisting of: S, Se, and Te. In some embodiments, the apparatus comprises a third interconnect adjacent to the second interconnect, the third interconnect including a stack of metal layers having a third non-alloy metal and a third

templating layer adjacent to the third non-alloy metal. In some embodiments, the third non-alloy metal is formed of a material which is selected from a group consisting of: Ag, Cu, Al, and Au. In some embodiments, the third templating layer is formed of a material which is selected from a group consisting of: MgO, STO, MgAlO, Ag, DyScO₃, GdScO₃, BTO, SrRuO₃ (SRO) and Molybdenum.

[00120] In some embodiments, the third non-alloy metal is adjacent to a metal formed of a material selected from a group consisting of: Bi, Pb, chalcogenide material. In some embodiments, the chalcogenide material is selected from a group consisting of: TiSe₂, MoSe₂, WSe₂, SiS₂, B₂S₃, Sb₂S₃, Ta₂S, Re₂S₇, and semiconductors of the type MX₂, with 'M' being a transition metal and 'X' being an achalcogen. In some embodiments, the apparatus comprises: a via adjacent to the first interconnect, wherein the via is formed from a metal having material which is selected from a group consisting of: Ru, Cu, Ta, W, Co, Ni, Al, Ag, and NiSi; and a fourth interconnect adjacent to the via, wherein the fourth interconnect comprises a stack of metal layers having a fourth non-alloy metal and a fourth templating layer adjacent to the fourth non-alloy metal.

[00121] In some embodiments, the fourth non-alloy metal is formed of a material which is selected from a group consisting of: Ag, Cu, Al, and Au, and wherein the fourth templating layer is formed of a material which is formed from a group consisting of: MgO, STO, MgAlO, Ag, DyScO₃, GdScO₃, BTO, SrRuO₃ (SRO) and Molybdenum. In some embodiments, the apparatus comprises a via adjacent to the first interconnect, wherein the via is formed from a stack of metal layers including a non-alloy metal and a templating layer; and a fifth interconnect adjacent to the via, wherein the fifth interconnect comprises a stack of metal layers having a fifth non-alloy metal and a fifth templating layer adjacent to the fifth non-alloy metal. In some embodiments, the fifth non-alloy metal is formed of a material which is selected from a group consisting of: Ag, Cu, Al, and Au, and wherein the fifth templating layer is formed of a material which is formed from a group consisting of: MgO, STO, MgAlO, Ag, DyScO₃, GdScO₃, BTO, SrRuO₃ (SRO) and Molybdenum.

[00122] In another example, a system is provided which comprises: a memory; a processor coupled to the memory, the processor including an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to couple to another device.

[00123] In another example, an apparatus is provided which comprises a first interconnect including a stack of metal layers having a first non-alloy metal adjacent to a metal and a first templating layer. In some embodiments, the first non-alloy metal is formed

of a material which is selected from a group consisting of: Ag, Cu, Al, and Au. In some embodiments, the first templating layer is formed of a material which is selected from a group consisting of: MgO, STO, MgAlO, Ag, DyScO₃, GdScO₃, BTO, SrRuO₃ (SRO), and Molybdenum. In some embodiments, the metal is formed of a material selected from a group consisting of: Bi, Pb, and chalcogenide materials. In some embodiments, the chalcogenide material is selected from a group consisting of: TiSe₂, MoSe₂, WSe₂, SiS₂, B₂S₃, Sb₂S₃, Ta₂S₅, Re₂S₇, and semiconductors of the type MX₂, with 'M' being a transition metal and 'X' being an achalcogen

[00124] In some embodiments, the apparatus comprises a second interconnect adjacent to the first interconnect. In some embodiments, the second interconnect is formed of a metal having material selected from a group consisting of: Ru, Cu, Ta, W, Co, Al, Ag, Ni, NiSi, and semiconductors of the type MX₂, with 'M' being a transition metal and 'X' being an achalcogen. In some embodiments, the apparatus comprises a third interconnect adjacent to the second interconnect, wherein the third interconnect comprises a stack of metal layers having a third non-alloy metal and a third templating layer adjacent to the third non-alloy metal.

[00125] In some embodiments, the third non-alloy metal is formed of a material which is formed from a group consisting of: Ag, Cu, Al, and Au, and wherein the third templating layer is formed of a material which is formed from a group consisting of: MgO, STO, MgAlO, Ag, DyScO₃, GdScO₃, BTO, SrRuO₃ (SRO), and Molybdenum. In some embodiments, the apparatus comprises: a via adjacent to the first interconnect, wherein the via is formed from a stack of metal layers including a non-alloy metal and a templating layer; and a second interconnect adjacent to the via, wherein the second interconnect comprises a stack of metal layers having a second non-alloy metal and a second templating layer adjacent to the second non-alloy metal.

[00126] In some embodiments, the non-alloy metal of the via is formed of a material which is selected from a group consisting of: Ag, Cu, Al, and Au, and wherein the templating layer of the via is formed of a material which is formed from a group consisting of: MgO, Strontium Titanate (STO), Magnesium Aluminum Oxide (MgAlO), Ag, DyScO₃, GdScO₃, BaTiO₃ (BTO), SrRuO₃ (SRO) and Molybdenum. In some embodiments, the apparatus comprises: a via adjacent to the first interconnect, wherein the via is formed from a metal having a material which is selected from a group consisting of: Ru, Cu, Ta, W, Co, Al, Ag, Ni, and NiSi; and a second interconnect adjacent to the via, wherein the second interconnect comprises a stack of metal layers having a second non-alloy metal and a second templating

layer adjacent to the second non-alloy metal, wherein the second non-alloy metal is formed of a material which is selected from a group consisting of: Ag, Cu, Al, and Au, and wherein the second templating layer is formed of a material which is formed from a group consisting of: MgO, STO, MgAlO, Ag, DyScO₃, GdScO₃, BTO, SrRuO₃ (SRO), and Molybdenum.

[00127] In another example, a system is provided which comprises: a memory; a processor coupled to the memory, the processor including an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to couple to another device.

[00128] In another example, an apparatus comprises: a first layer formed of a material possessing spin-orbit coupling for electrons, the material selected from a group consisting of: W, Pt, Ta, and Bi₂Se₃; a metal interconnect adjacent to the first layer; and a second layer made of a material possessing spin-orbit coupling for electrons, wherein the material is selected from a group consisting of: W, Pt, Ta, and Bi₂Se₃, wherein the second layer is adjacent to the metal interconnect. In some embodiments, the metal interconnect is formed of a material which is selected from a group consisting of: Ru, Cu, Ta, W, Co, Al, Ag, Ni, and NiSi.

[00129] In another example, a system is provided which comprises: a memory; a processor coupled to the memory, the processor including an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to couple to another device.

[00130] In another example, a method is provided which comprises: forming a first super-lattice possessing spin-orbit coupling for electrons; depositing a metal interconnect adjacent to the first super-lattice; and forming a second super-lattice possessing spin-orbit coupling for electrons, the second super-lattice being adjacent to the metal interconnect. In some embodiments, forming the first or second super-lattices comprises: forming a first interface layer formed of a material selected from a group consisting of: Ag, Cu, Au, and Al; forming a bulk layer adjacent to the first interface layer, wherein the bulk layer is formed of a material selected from a group consisting of: Ta, Hf, W, Pt, Bi; Ag doped with Ta, Hf, W, Pt, Bi, or Ir; Al doped with Ta, Hf, W, Pt, Bi, or Ir; Cu doped with Ta, Hf, W, Pt, Bi, or Ir; and Au doped with Ta, Hf, W, Pt, Bi, or Ir; forming a second interface layer adjacent to the bulk layer, wherein the second interface layer is formed of a different material than the first interface layer, wherein the different material for the second interface layer is selected from a group consisting of: Ag, Cu, Al, and Au; and forming a metal layer adjacent to the second

interface layer, wherein the metal layer is formed of a material selected from group consisting of: Bi, Pb, and chalcogenide material.

[00131] In some embodiments, the chalcogenide material is selected from a group consisting of: TiSe_2 , MoSe_2 , WSe_2 , SiS_2 , B_2S_3 , Sb_2S_3 , Ta_2S_5 , Re_2S_7 , and semiconductors of the type MX_2 , with 'M' being a transition metal and 'X' being an achalcogen. In some embodiments, 'M' is selected from a group consisting of: Mo and W, and wherein 'X' is selected from a group consisting of: S, Se, and Te. In some embodiments, the metal interconnect is formed of a material which is selected from a group consisting of: Ru, Cu, Ta, W, Co, Al, Ag, Ni, and NiSi.

[00132] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the claims. The following claims are hereby incorporated into the detailed description, with each claim standing on its own as a separate embodiment.

CLAIMS

We claim:

1. An apparatus comprising:
 - a first super-lattice possessing spin-orbit coupling for electrons;
 - a metal interconnect adjacent to the first super-lattice; and
 - a second super-lattice possessing spin-orbit coupling for electrons, the second super-lattice being adjacent to the metal interconnect.
2. The apparatus of claim 1, wherein the first or second super-lattices comprise:
 - a first interface layer formed of a material selected from a group consisting of: Ag, Cu, Au, and Al;
 - a bulk layer adjacent to the first interface layer, wherein the bulk layer is formed of a material selected from a group consisting of: Ta, Hf, W, Pt, Bi; Ag doped with Ta, Hf, W, Pt, Bi, or Ir; Al doped with Ta, Hf, W, Pt, Bi, or Ir; Cu doped with Ta, Hf, W, Pt, Bi, or Ir; and Au doped with Ta, Hf, W, Pt, Bi, or Ir;
 - a second interface layer adjacent to the bulk layer, wherein the second interface layer is formed of a different material than the first interface layer, wherein the different material for the second interface layer is selected from a group consisting of: Ag, Cu, Al, and Au; and
 - a metal layer adjacent to the second interface layer, wherein the metal layer is formed of a material selected from group consisting of: Bi, Pb, and chalcogenide material.
3. The apparatus of claim 2, wherein the chalcogenide material is selected from a group consisting of: TiSe_2 , MoSe_2 , WSe_2 , SiS_2 , B_2S_3 , Sb_2S_3 , Ta_2S_5 , Re_2S_7 , and semiconductors of the type MX_2 , with 'M' being a transition metal and 'X' being an achalcogen.
4. The apparatus of claim 3, wherein 'M' is selected from a group consisting of: Mo and W, and wherein 'X' is selected from a group consisting of: S, Se, and Te.
5. The apparatus of claim 1, wherein the metal interconnect is formed of a material which is selected from a group consisting of: Ru, Cu, Ta, W, Co, Al, Ag, Ni, and NiSi.
6. An apparatus comprising:
 - a first interconnect including:

a first interface layer formed of a material selected from a group consisting of: Ag, Cu, Al, and Au; and

a bulk layer adjacent to the first interface layer, wherein the bulk layer is formed of a material selected from a group consisting of: Ta, Hf, W, Pt, Bi; Ag doped with Ta, Hf, W, Pt, Bi, or Ir; Al doped with Ta, Hf, W, Pt, Bi, or Ir; Cu doped with Ta, Hf, W, Pt, Bi, or Ir; and Au doped with Ta, Hf, W, Pt, Bi, or Ir;

a second interface layer adjacent to the bulk layer, wherein the second interface layer is formed of a material selected from a group consisting of: Ag, Cu, Al, and Au;

a metal layer adjacent to the second interface layer, wherein the metal layer is formed of a material selected from a group consisting of: Bi, Pb, and chalcogenide material; and

a second interconnect adjacent to the first interconnect, the second interconnect formed of a material selected from a group consisting of: Ru, Cu, Ta, W, Co, Ni, NiSi and semiconductors of the type MX_2 , with 'M' being a transition metal and 'X' being an achalcogen.

7. The apparatus of claim 6, wherein 'M' is selected from a group consisting of: Mo and W, and wherein 'X' is selected from a group consisting of: S, Se, and Te.
8. The apparatus of claim 6 comprises a third interconnect adjacent to the second interconnect, the third interconnect including a stack of metal layers having a third non-alloy metal and a third templating layer adjacent to the third non-alloy metal.
9. The apparatus of claim 8, wherein the third non-alloy metal is formed of a material which is selected from a group consisting of: Ag, Cu, Al, and Au.
10. The apparatus of claim 8, wherein the third templating layer is formed of a material which is selected from a group consisting of: MgO, STO, MgAlO, Ag, DyScO₃, GdScO₃, BTO, SrRuO₃ (SRO) and Molybdenum.
11. The apparatus of claim 8, wherein the third non-alloy metal is adjacent to a metal formed of a material selected from a group consisting of: Bi, Pb, chalcogenide material.

12. The apparatus of claim 11, wherein the chalcogenide material is selected from a group consisting of: TiSe_2 , MoSe_2 , WSe_2 , SiS_2 , B_2S_3 , Sb_2S_3 , Ta_2S_5 , Re_2S_7 , and semiconductors of the type MX_2 , with 'M' being a transition metal and 'X' being an achalcogen.
13. The apparatus of claim 6 comprises:
 - a via adjacent to the first interconnect, wherein the via is formed from a metal having material which is selected from a group consisting of: Ru, Cu, Ta, W, Co, Ni, Al, Ag, and NiSi; and
 - a fourth interconnect adjacent to the via, wherein the fourth interconnect comprises a stack of metal layers having a fourth non-alloy metal and a fourth templating layer adjacent to the fourth non-alloy metal.
14. The apparatus of claim 13, wherein the fourth non-alloy metal is formed of a material which is selected from a group consisting of: Ag, Cu, Al, and Au, and wherein the fourth templating layer is formed of a material which is formed from a group consisting of: MgO, STO, MgAlO, Ag, DyScO_3 , GdScO_3 , BTO, SrRuO_3 (SRO) and Molybdenum.
15. The apparatus of claim 6 comprises:
 - a via adjacent to the first interconnect, wherein the via is formed from a stack of metal layers including a non-alloy metal and a templating layer; and
 - a fifth interconnect adjacent to the via, wherein the fifth interconnect comprises a stack of metal layers having a fifth non-alloy metal and a fifth templating layer adjacent to the fifth non-alloy metal.
16. The apparatus of claim 15, wherein the fifth non-alloy metal is formed of a material which is selected from a group consisting of: Ag, Cu, Al, and Au, and wherein the fifth templating layer is formed of a material which is formed from a group consisting of: MgO, STO, MgAlO, Ag, DyScO_3 , GdScO_3 , BTO, SrRuO_3 (SRO) and Molybdenum.
17. A system comprising:
 - a memory;
 - a processor coupled to the memory, the processor including an apparatus according to any one of apparatus claims 1 to 5; and
 - a wireless interface for allowing the processor to couple to another device.

18. A system comprising:

- a memory;
- a processor coupled to the memory, the processor including an apparatus according to any one of apparatus claims 6 to 16; and
- a wireless interface for allowing the processor to couple to another device.

19. An apparatus comprising:

- a first layer formed of a material possessing spin-orbit coupling for electrons, the material selected from a group consisting of: W, Pt, Ta, and Bi₂Se₃;
- a metal interconnect adjacent to the first layer; and
- a second layer made of a material possessing spin-orbit coupling for electrons, wherein the material is selected from a group consisting of: W, Pt, Ta, and Bi₂Se₃, wherein the second layer is adjacent to the metal interconnect.

20. The apparatus of claim 19, wherein the metal interconnect is formed of a material which is selected from a group consisting of: Ru, Cu, Ta, W, Co, Al, Ag, Ni, and NiSi.

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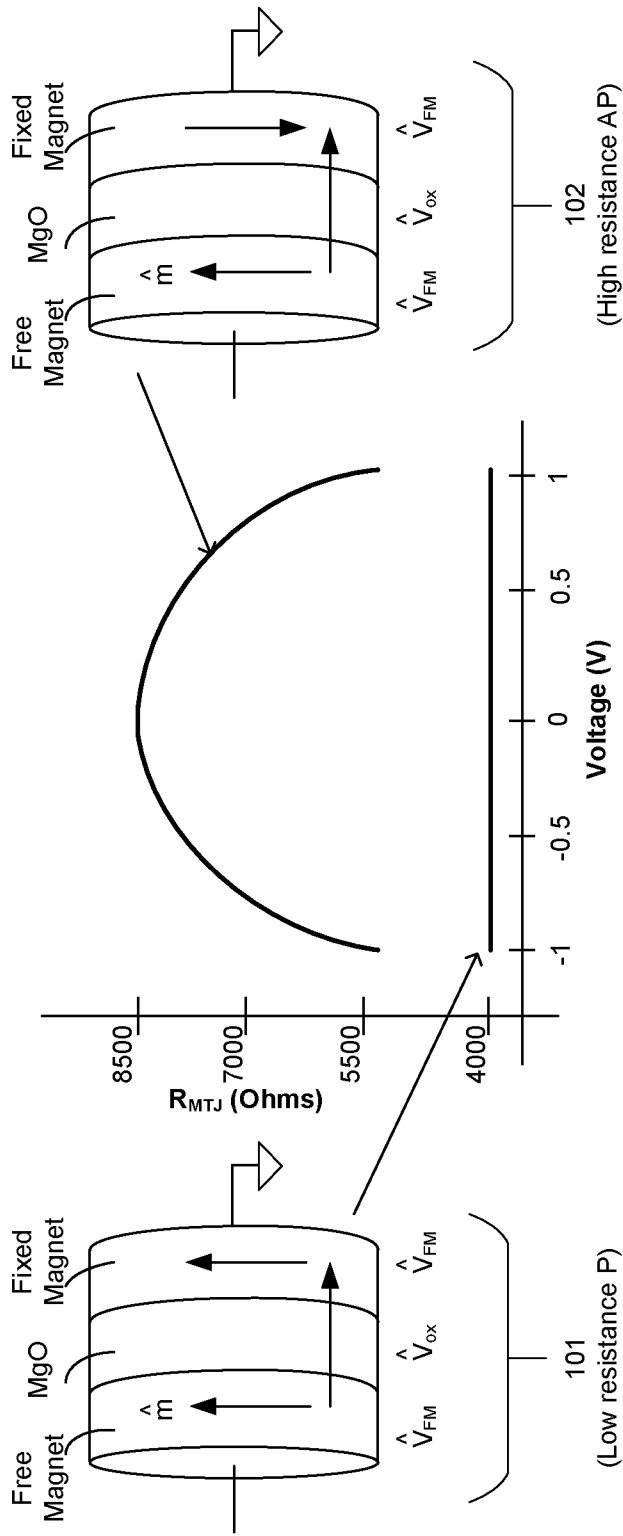
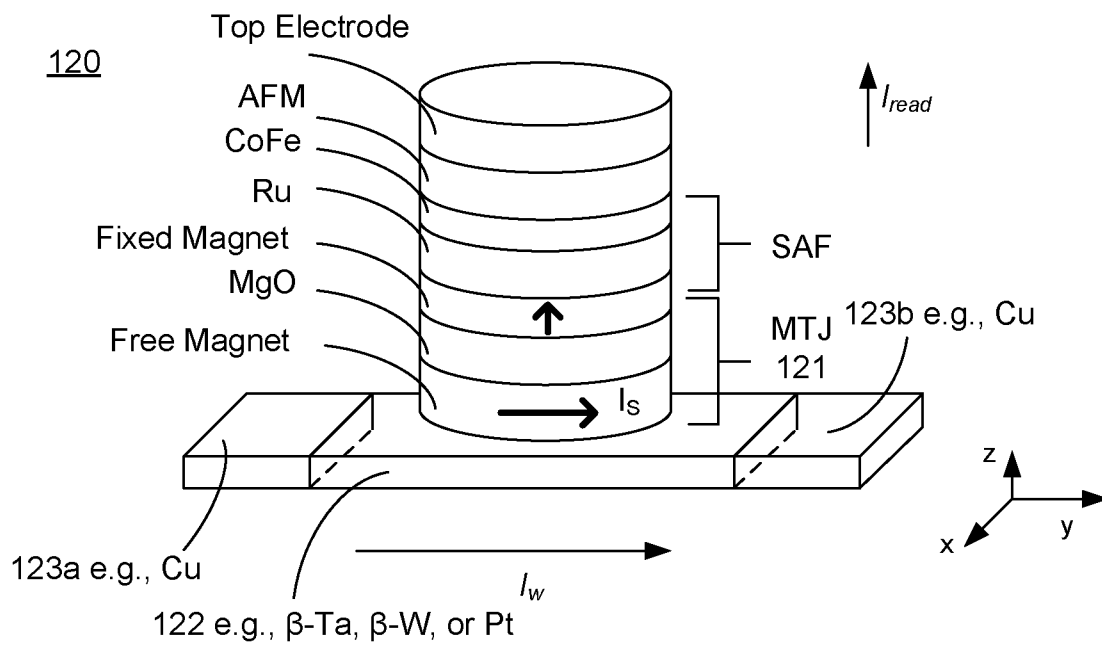
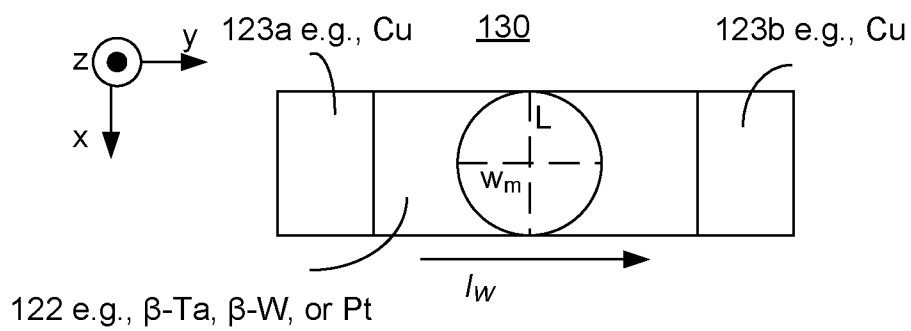


Fig. 1A
(prior art)

**Fig. 1B****Fig. 1C**

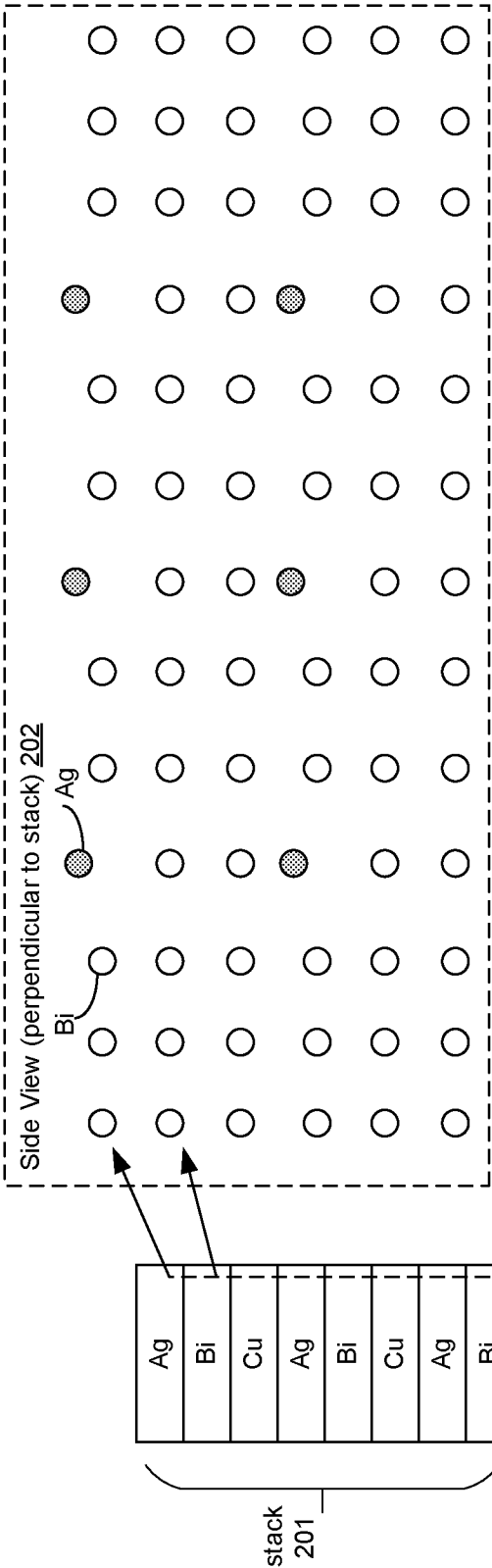


Fig. 2A

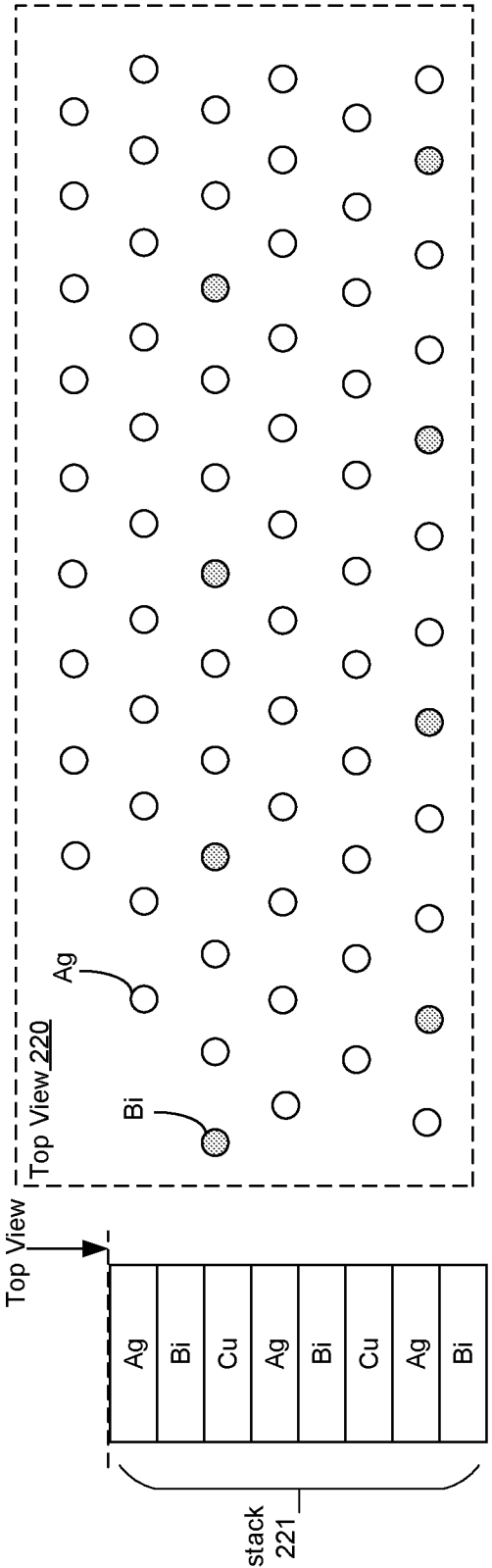
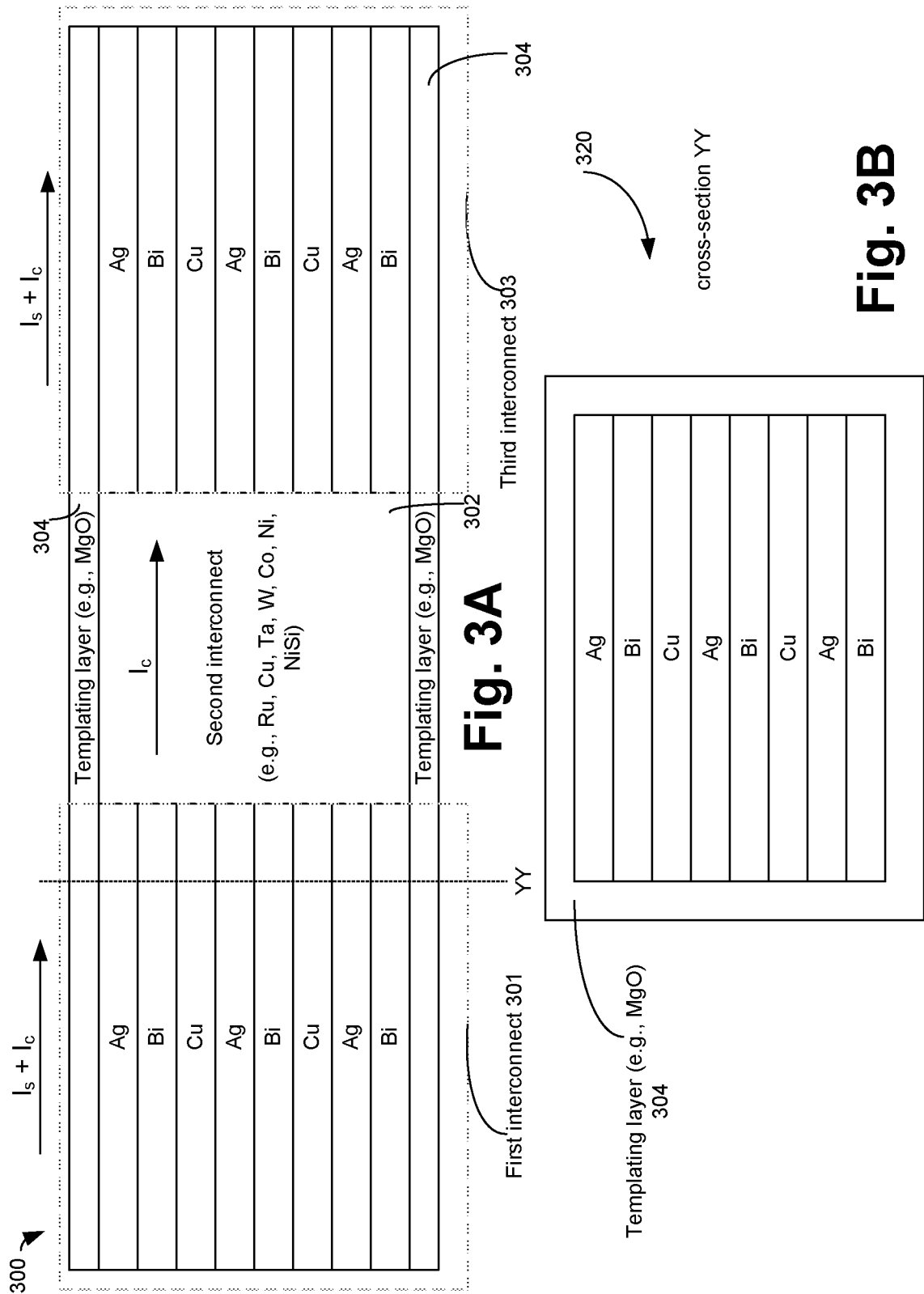
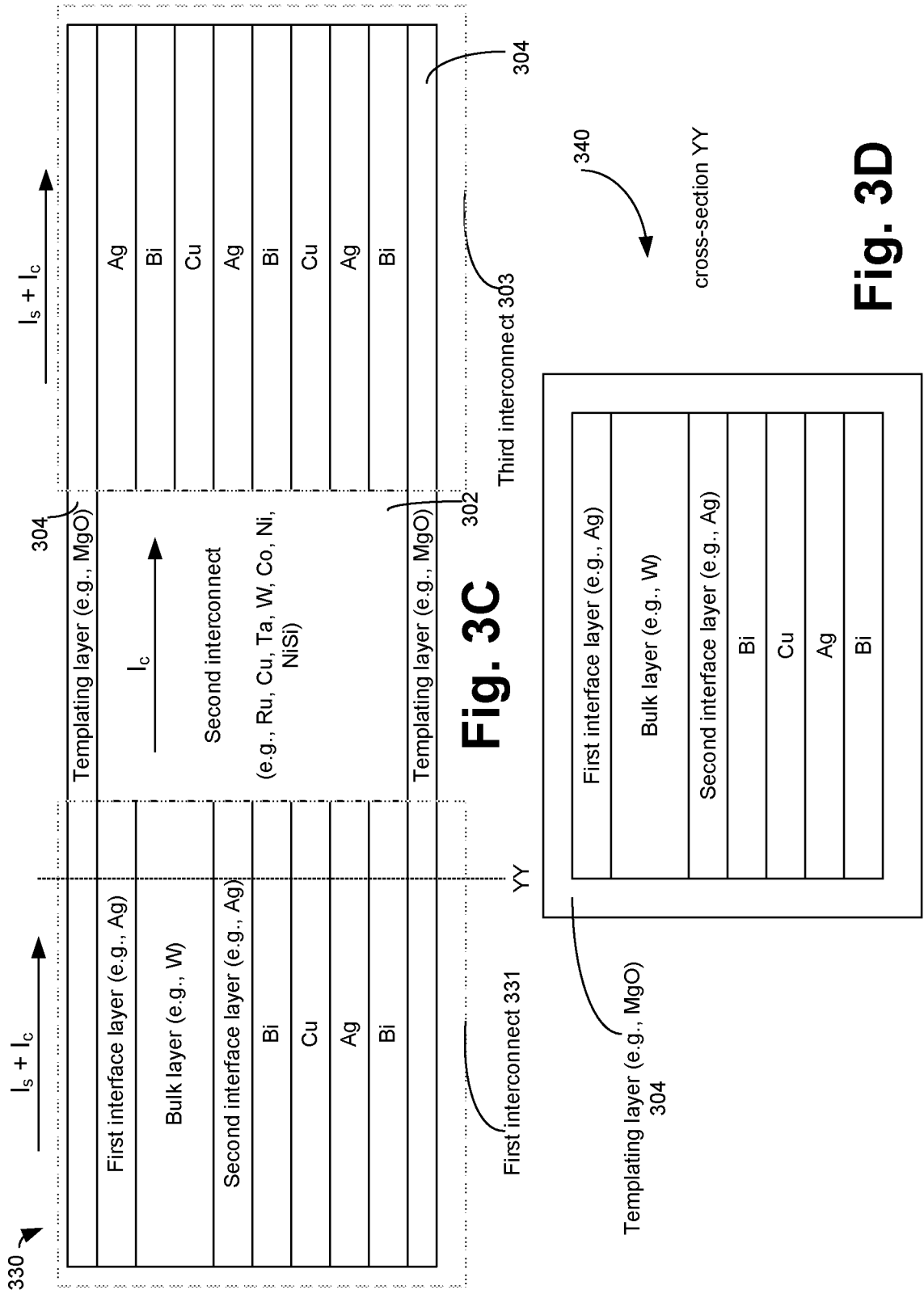


Fig. 2B





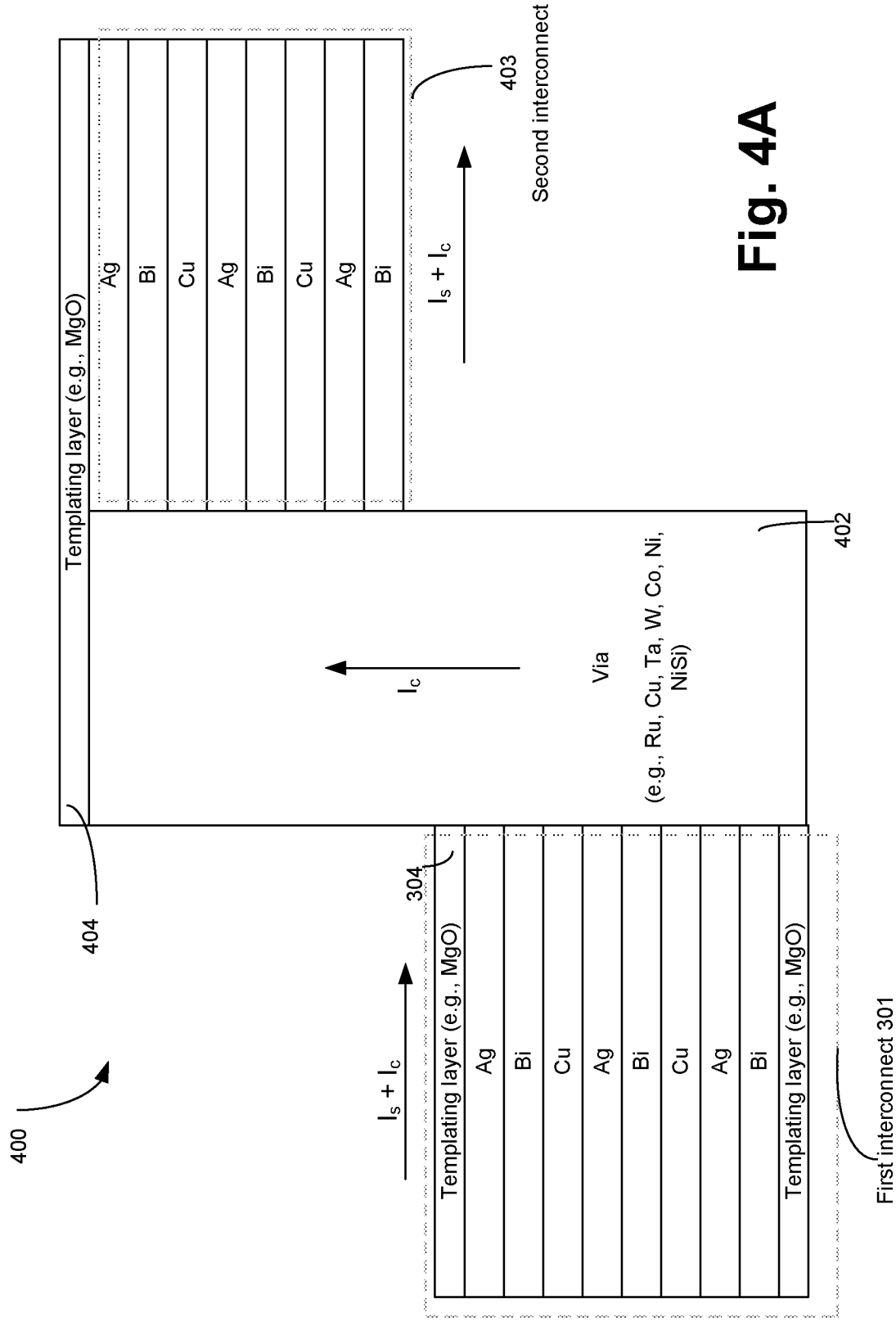


Fig. 4A

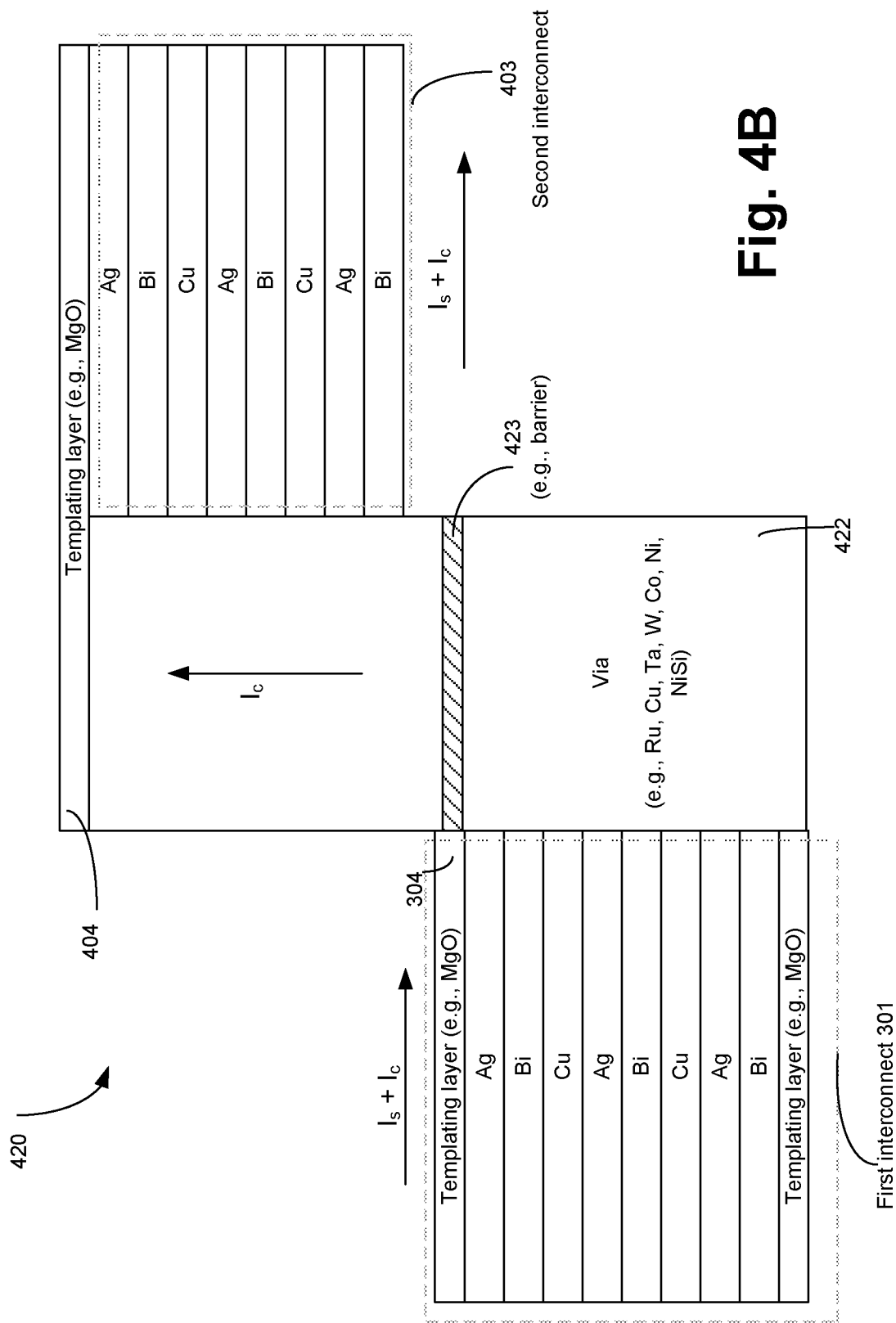


Fig. 4B

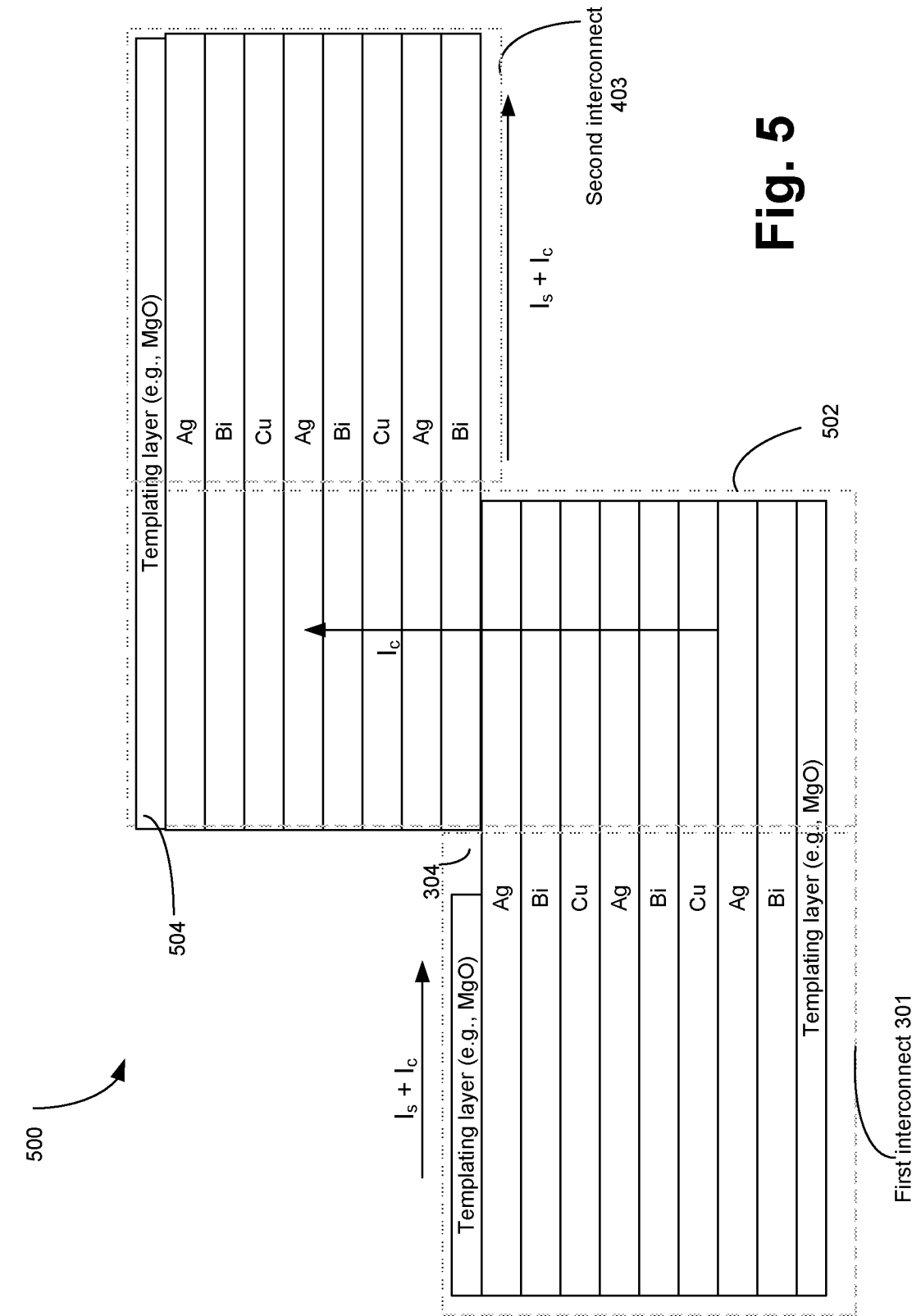


Fig. 5

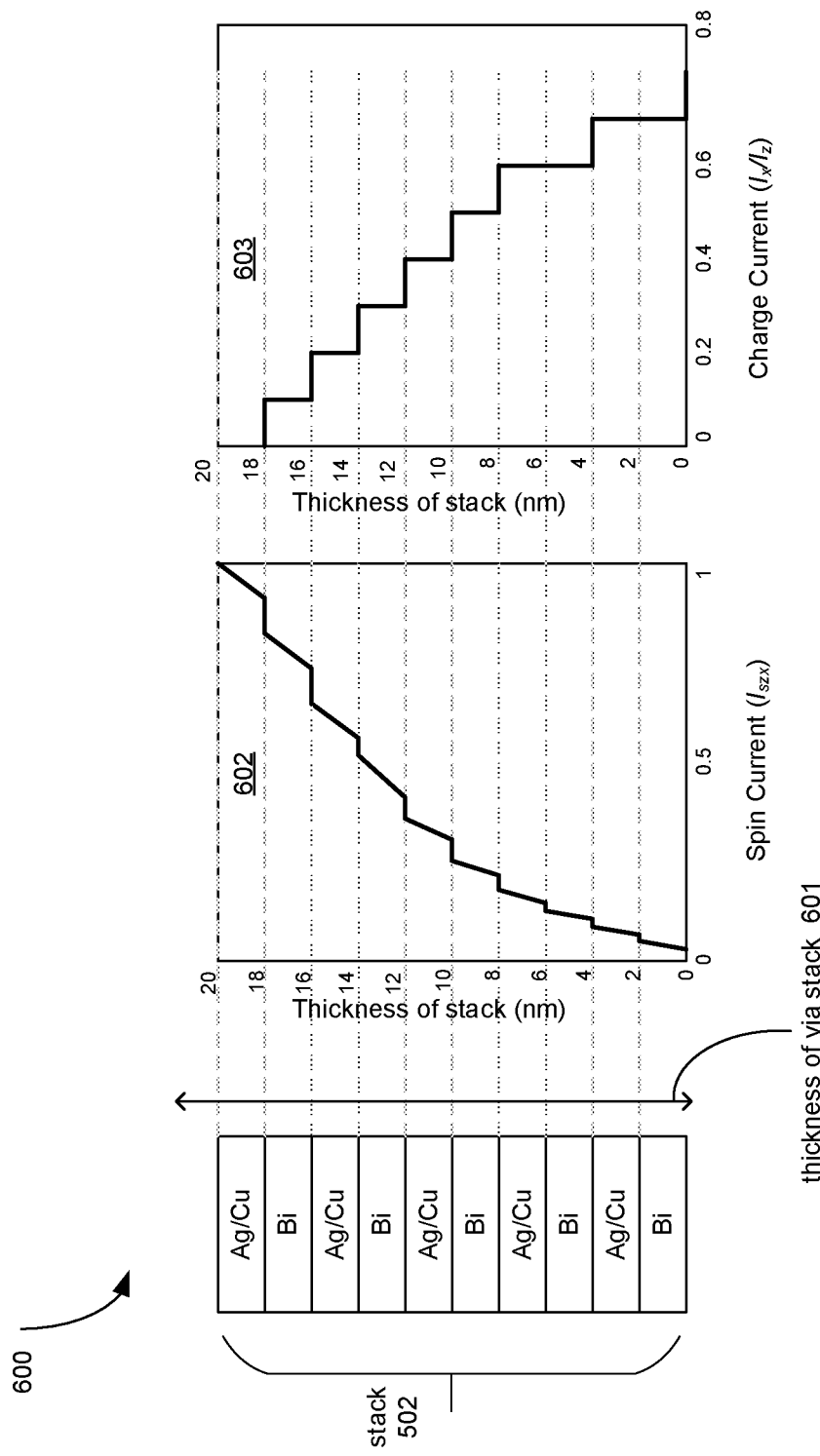


Fig. 6

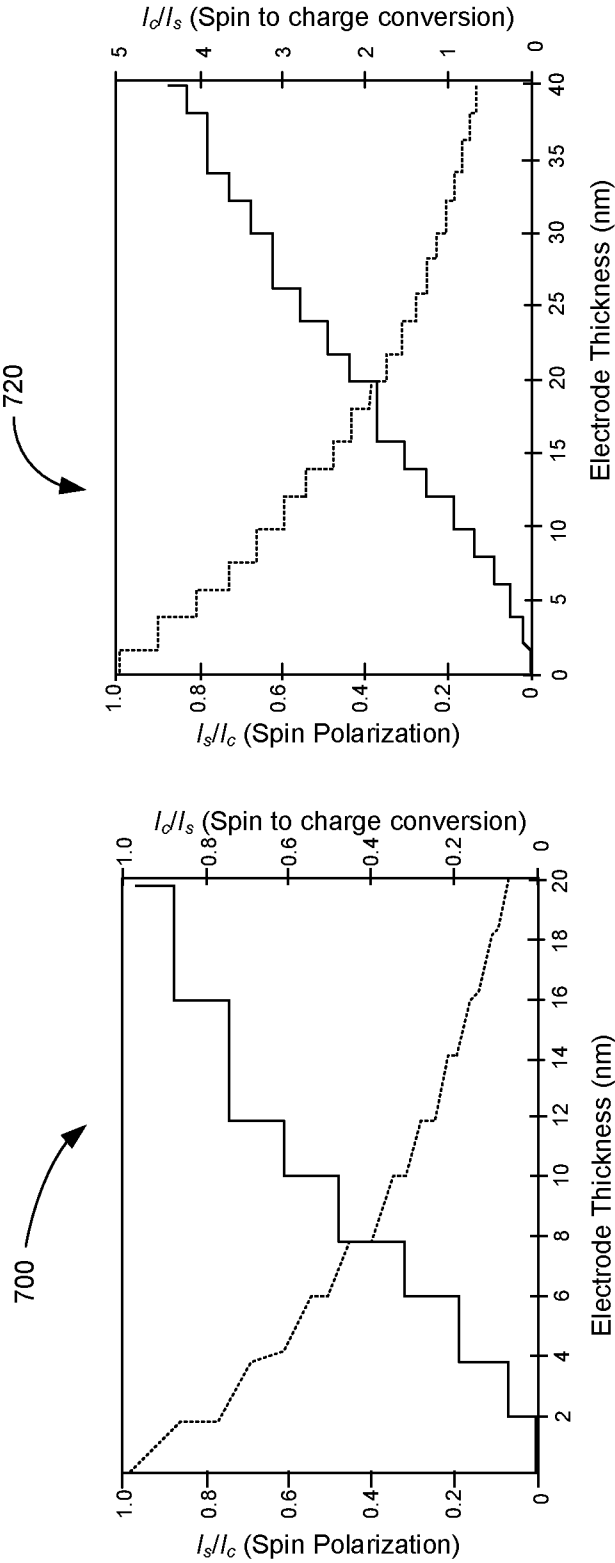
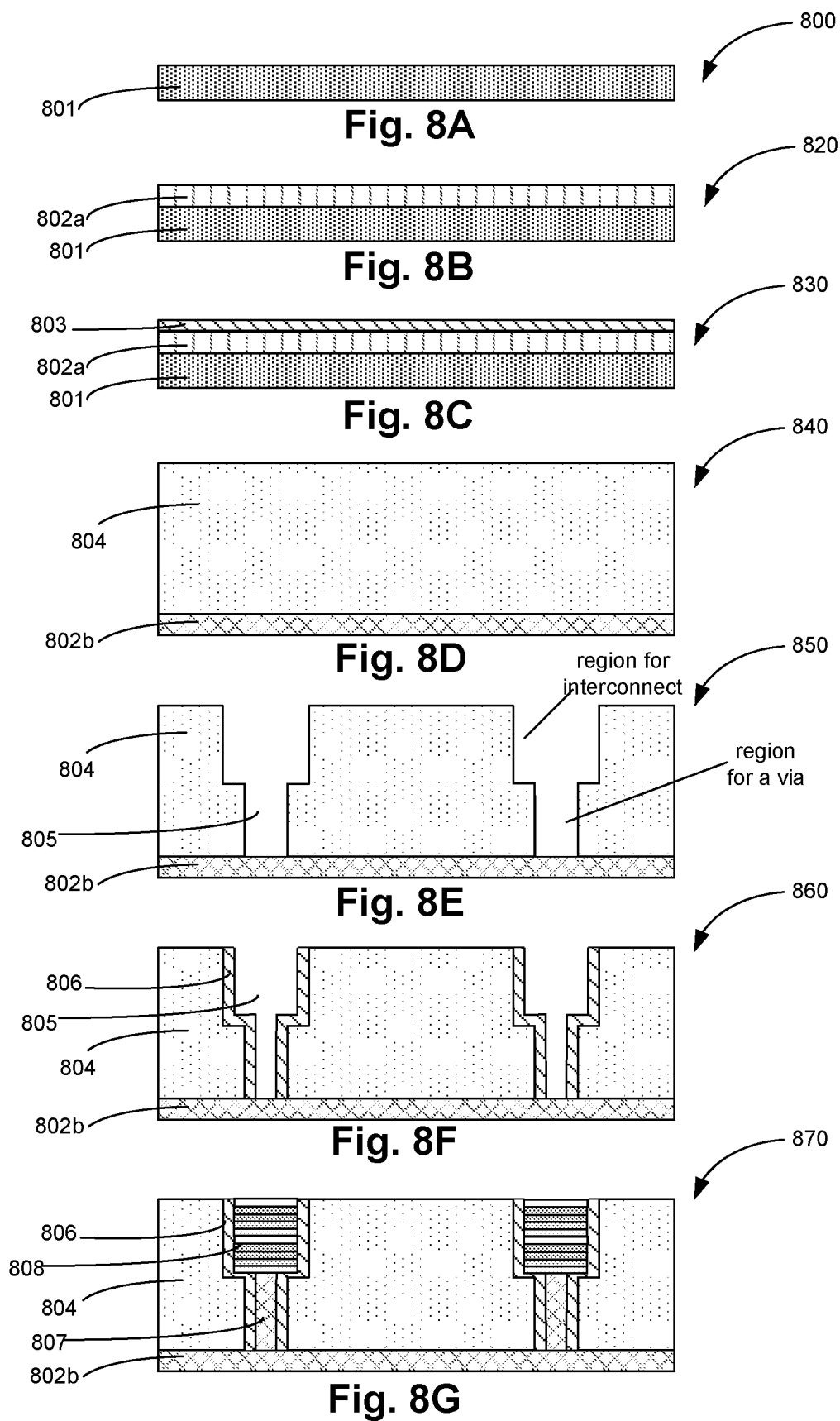


Fig. 7A

Fig. 7B



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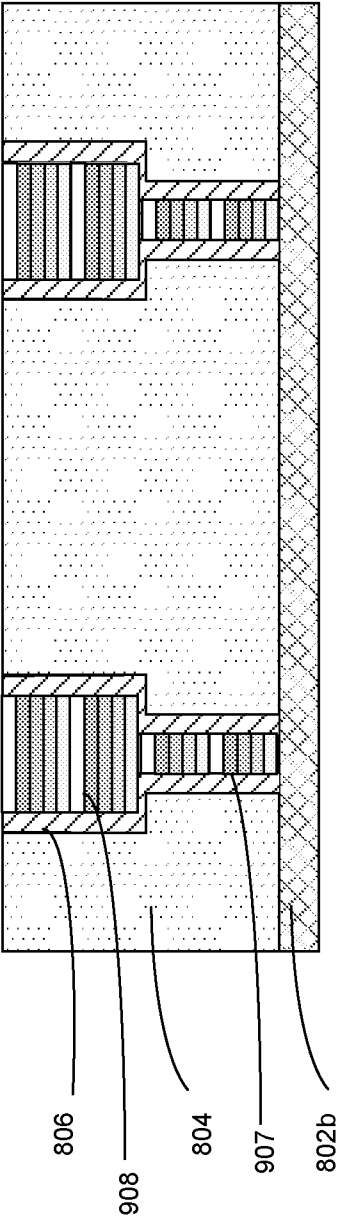


Fig. 9

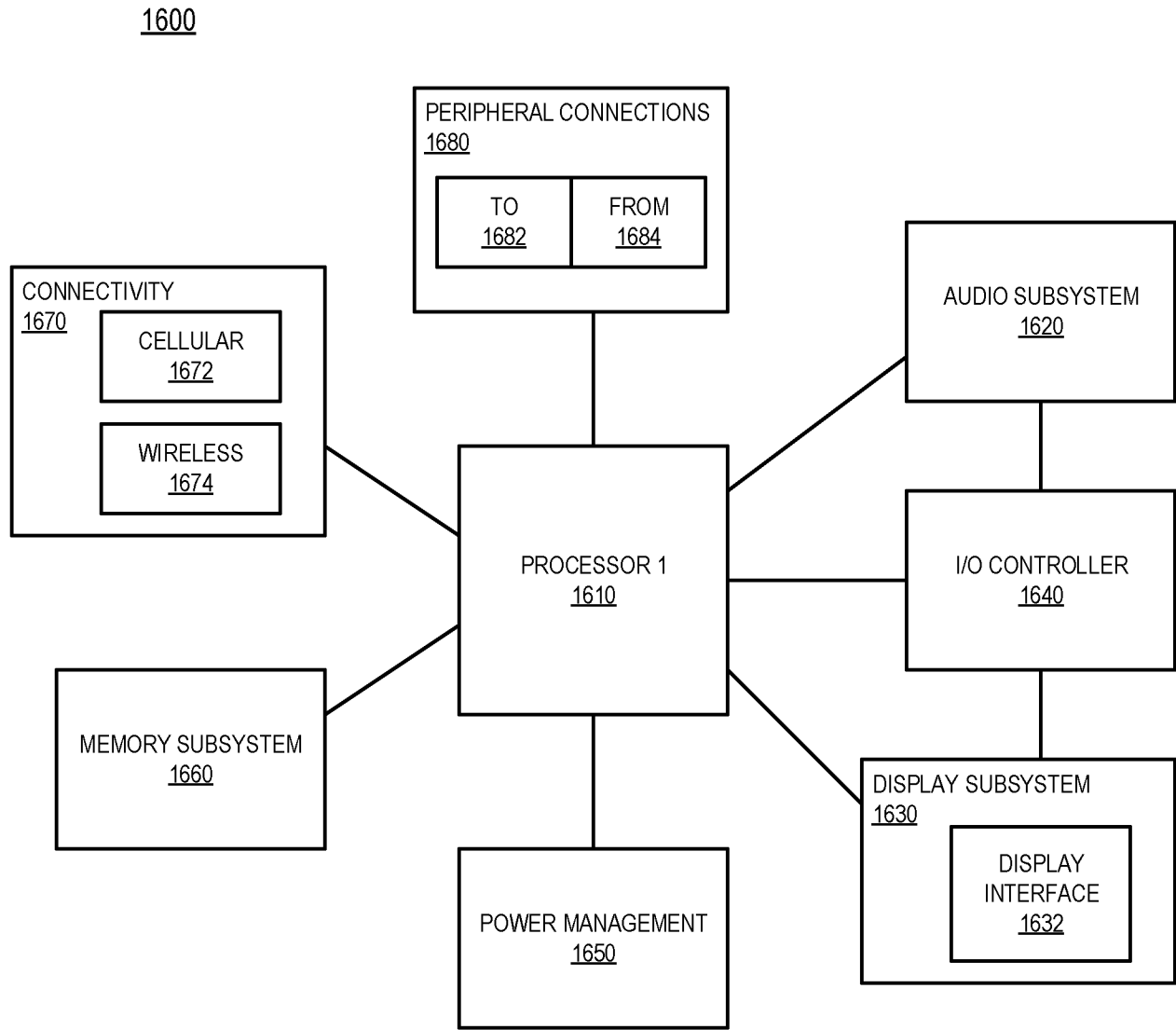


Fig. 10

A. CLASSIFICATION OF SUBJECT MATTER**H01L 43/02(2006.01)i, H01L 43/10(2006.01)i, G11C 11/16(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 43/02; H01F 10/32; H01L 21/8246; G11C 11/16; H01L 29/82; H01L 27/22; H01L 21/8238; H01L 43/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:super-lattice, spin-orbit coupling, electrons, metal interconnect, Rashba effect

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007-0059877 A1 (HYUN CHEOL KOO et al.) 15 March 2007 See paragraphs [0005], [0032]-[0044], claim 1 and figures 1-3E.	1-20
A	WO 2015-047194 A1 (NATIONAL UNIVERSITY OF SINGAPORE) 02 April 2015 See page 2, lines 9-11, page 5, lines 5-10, claims 1-3 and figure 1.	1-20
A	US 2014-0091411 A1 (SASIKANTH MANIPATRUNI et al.) 03 April 2014 See paragraphs [0013]-[0029], claim 1 and figure 1a.	1-20
A	US 2014-0001524 A1 (SASIKANTH MANIPATRUNI et al.) 02 January 2014 See paragraphs [0038]-[0040], claims 1, 2 and figure 10.	1-20
A	JP 2009-158554 A (HITACHI LTD.) 16 July 2009 See paragraphs [0008], [0020], [0021], claim 1 and figure 1.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

25 November 2016 (25.11.2016)

Date of mailing of the international search report

25 November 2016 (25.11.2016)

Name and mailing address of the ISA/KR

International Application Division

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/021260

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