United States Patent

Schmersal

[15] **3,684,918**

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[54] **GAS DISCHARGE DISPLAY/MEMORY PANELS AND SELECTION AND ADDRESSING CIRCUITS THEREFOR**

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[73] Assignee: **Owens-Illinois, Inc.**

[22] Filed: **Aug. 7, 1970**

[21] Appl. No.: **62,015**

[52] **U.S. Cl.**.....**315/169 R,** 315/169 TV

[51] **Int. Cl.**.....**H05b 37/00**

[58] **Field of Search**.....315/169, 169 TV

[56] **References Cited**

UNITED STATES PATENTS

3,499,167	3/1970	Baker et al.	315/169 R
2,995,682	8/1961	Livingston	315/169 R
3,043,988	7/1962	Hurvitz	315/169 TV

Primary Examiner—Roy Lake
Assistant Examiner—James B. Mullins
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[57] **ABSTRACT**

There is disclosed a gas discharge display and memory panel having parallel row and parallel column conductor arrays carried on support plates in which both ends of the conductors in the arrays are connected to selection and addressing circuitry so that, in effect, the conductors are made a part of the selection and addressing circuitry. In one embodiment, a dielectric coating on the conductors in the active area of the panel is extended a distance beyond the spacer sealant for the gas chamber and holes are formed in a pattern in the dielectric, which holes contain circuit components as, for example, resistance elements and/or diodes. In another embodiment, various integrated circuit packages, such as LIDS, MSI, and LSI packages, are secured to the conductor ends, respectively.

8 Claims, 7 Drawing Figures

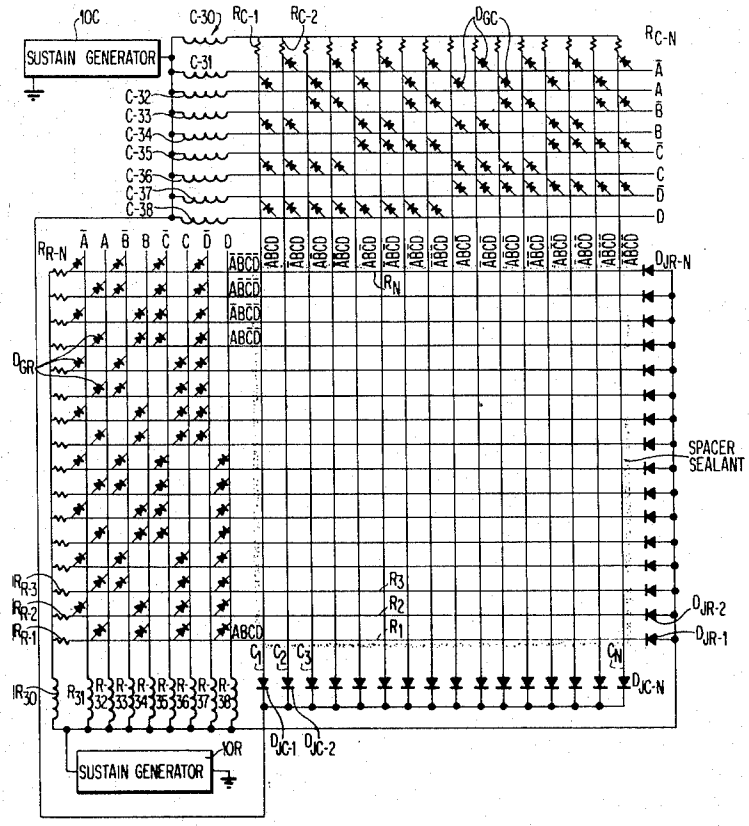

FIG. 1

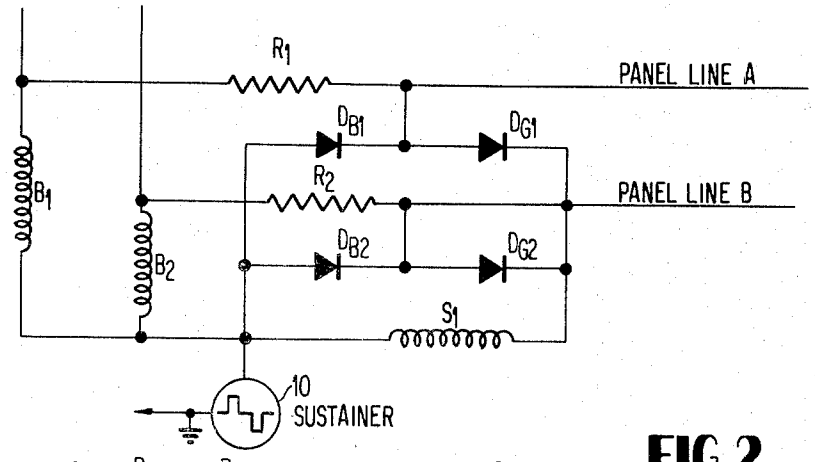

FIG. 2

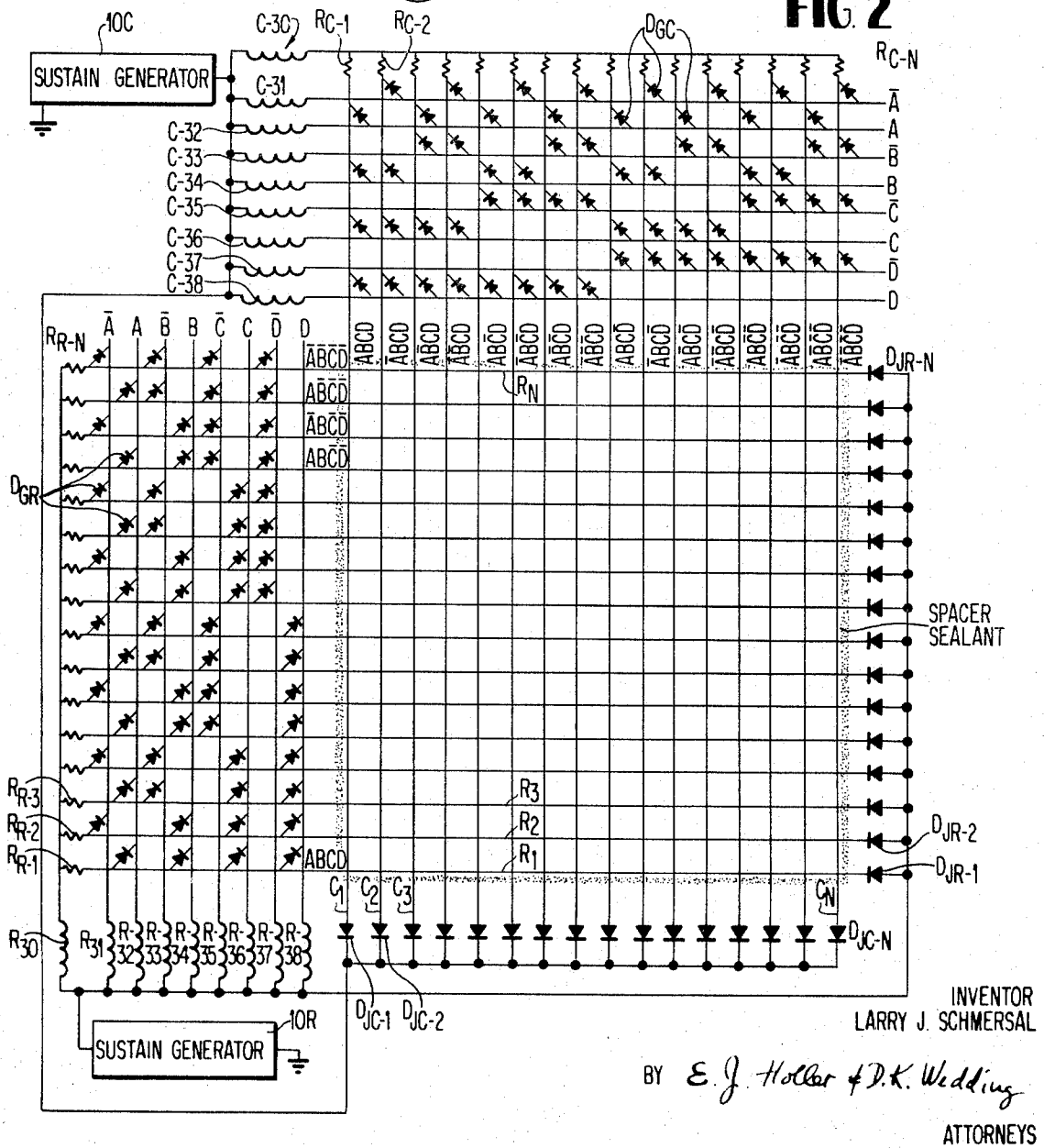

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FIG. 3

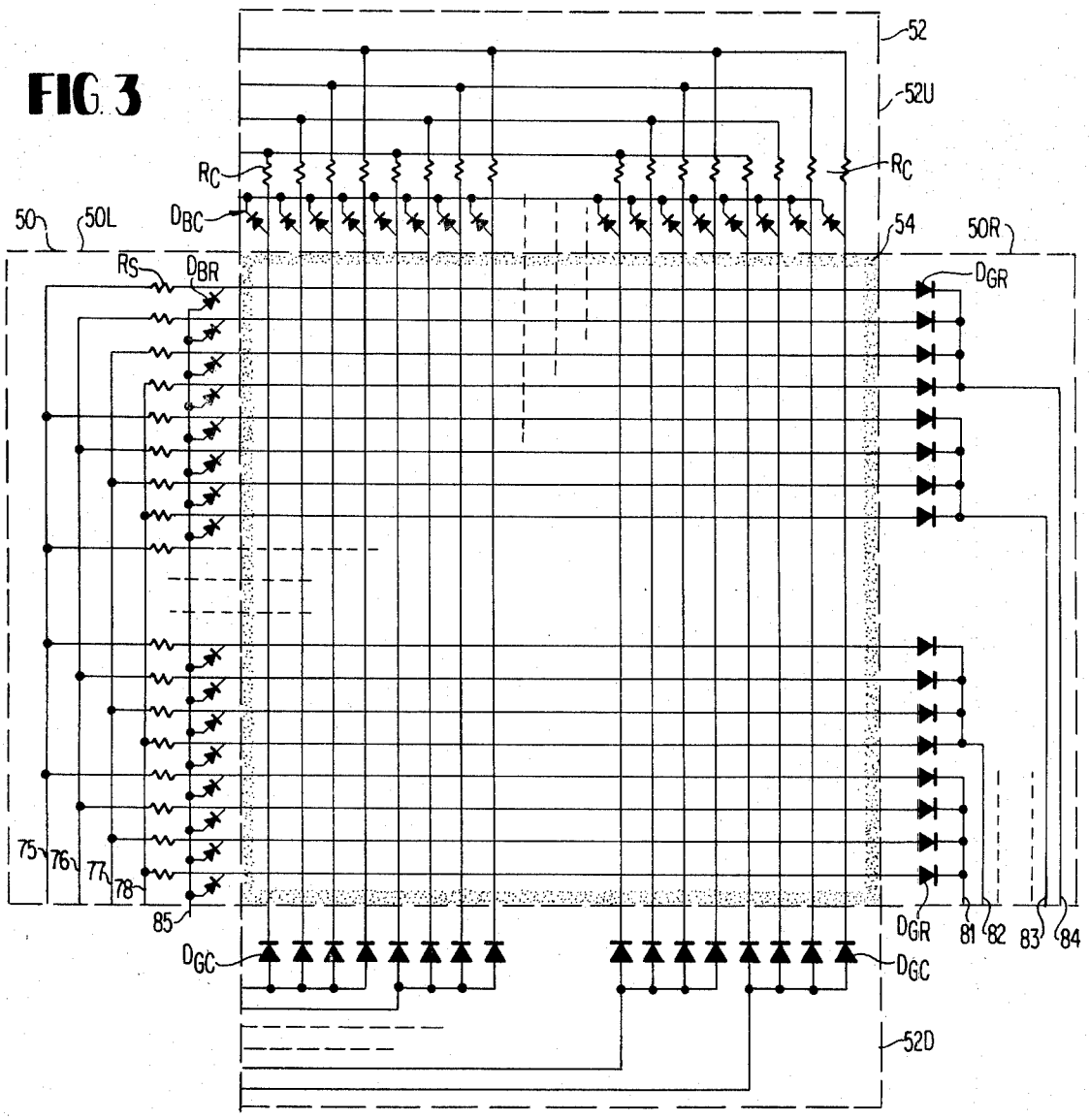
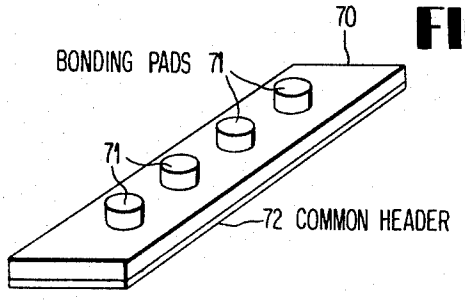


FIG. 7



"N" COMPONENTS LONG
("N"=4 ILLUSTRATED)

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FIG. 4

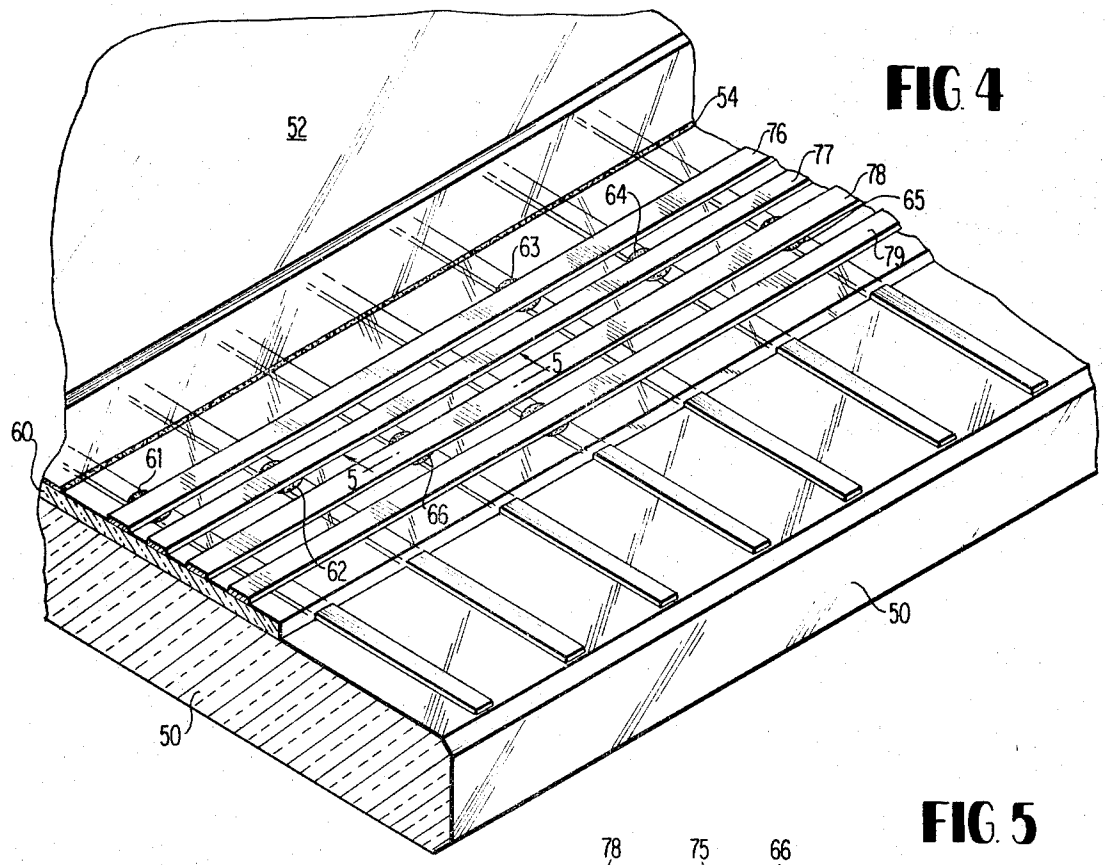


FIG. 5

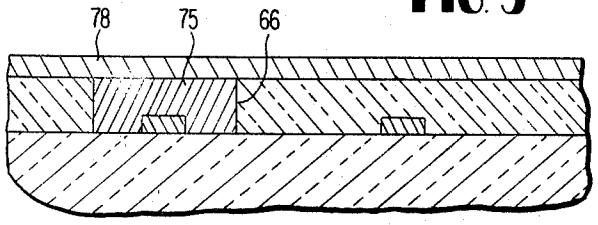
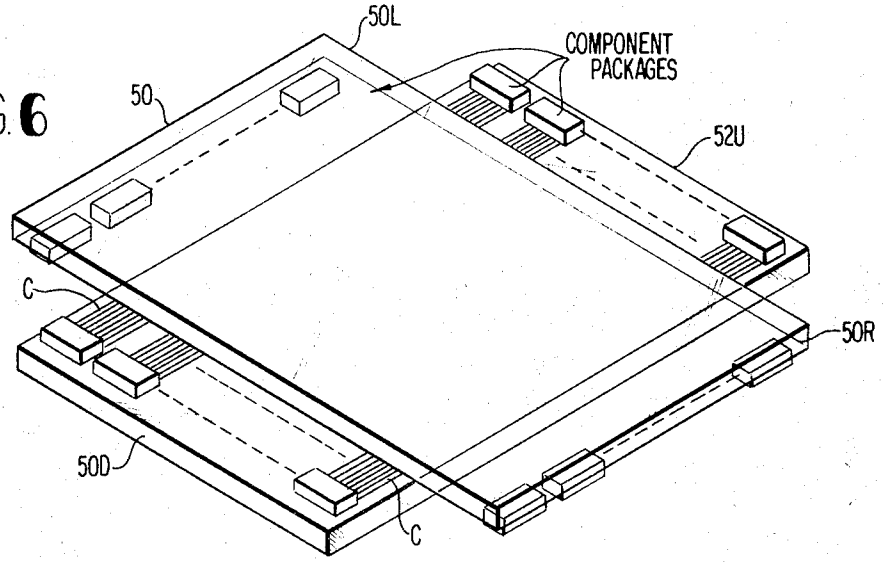


FIG. 6



GAS DISCHARGE DISPLAY/MEMORY PANELS AND SELECTION AND ADDRESSING CIRCUITS THEREFOR

BACKGROUND OF THE INVENTION

The present invention relates to gas discharge display and memory panels of the type disclosed in Baker et al. U.S. Pat. No. 3,499,167, issued Mar. 3, 1970. In this Baker et al. patent, there is disclosed a gas discharge display/memory device in which a pair of rectangular glass plate members are joined in spaced apart relation, the gas plate members carrying dielectrically coated multiple conductor arrays, with the row and column conductor arrays in the active panel area being comprised of linear conductors extending parallel to the long direction to the plates, respectively. The plates are joined by a spacer sealant with their long axes transverse to each other and with the conductor ends extending beyond the point where the plates are spacedly joined towards both edges of the plates, respectively.

The present invention is directed towards the utilization of the natural geometry of the panel as described above and a unique packaging method for containing and mounting diode-resistors, or other electrical components used in a diode resistor addressing matrix as disclosed in the application of William E. Johnson filed Aug. 3, 1970, Ser. No. 60,402, now abandoned and entitled "Selection and Addressing Circuitry for Matrix Type Gas Display Panel." Thus, the present invention is based on the fact that the conductors in the row and column arrays have two ends and one end may be utilized for the group select diodes and the other end is utilized by making electrical contact to the sustainer by-pass diodes as well as the bit select resistors. Alternatively, the group select diode and the bit select resistor may be at the same conductor end and the sustainer bypass diode connected at the opposite conductor end. Where discreet components are utilized, there are six electrical circuit connections per conductor line which comprises the two diodes referred to above and the one resistor per line. In order to reduce costs of packaging, techniques which permit mass processing of electrical components, such as pellet diodes or chip diodes, or monolithic diodes in a strip with either a common anode or a common cathode, as well as header type monolithic resistors can be used. In this fashion, a multiplicity of electrical connections may be made, in which operation, using standard bonding techniques, either solder reflow or gold ultrasonic bonding, etc. may be utilized.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages, and features of the invention will become more apparent from the following specification and drawings, wherein:

FIG. 1 illustrates basic diode-resistor address/selection circuitry for a pair of conductors in either a row or column conductor array;

FIG. 2 illustrates a configuration utilizing an electrical component layout on a physical panel wherein the group select diodes and bit select resistors are positioned on the left hand edge extension of a panel plate member for the row conductors and the sustainer bypass diodes are positioned on the right hand edge extension of the panel, and the column select diodes and the column select resistors are mounted on the upper

plate edge extension along with the pulsing circuits, whereas the sustainer bypass diodes for the column conductors are on the lower plate extension;

FIG. 3 is somewhat similar to FIG. 2 in the location of the components except in this case it will be noted that the group select diodes are positioned at one end of the panel line, whereas the bit select resistor, as well as the bypass diodes for the sustainer voltages, are positioned on the other or opposite end of the panel plate edge extensions for the row and column conductor, respectively;

FIG. 4 is an enlarged view of a plate edge extension showing the manner in which the dielectric coatings on the conductors have been opened up or have a hole formed therein;

FIG. 5 is a cross sectional view taken on lines 5—5 of FIG. 4;

FIG. 6 illustrates the invention as applied to discreet packaged components, as for example, LIDS, MSI, and LSI packages; and

FIG. 7 discloses a header assembly and package for a group of diodes having common anodes or cathodes or resistors.

Referring now to FIG. 1, the basic circuit is the same circuit as is disclosed in Johnson application Ser. No. 60,402 filed Aug. 3, 1970 now abandoned and entitled "Selection and Addressing Circuitry for Matrix Type Gas Display Panel," and as shown, the entire selection and address system floats on top of the sustainer voltage wave form from sustainer voltage generator **10** which may be square wave, sinusoidal, trapozoidal, or any other periodic wave form of an alternating character. As described in the aforementioned Johnson application, the voltage from sustainer **10** constitutes one-half of the sustaining voltage necessary to operate the panel, the remaining one-half at 180° phase is supplied to the other conductors in the opposite array. Thus, one-half the sustainer potential is applied to the row conductors and one-half the sustainer potential, at 180° phase relationship, is applied to the column conductors for the panel. While in FIG. 1 the pulse sources **B1**, **B2** and **G1** are shown as being constituted by the secondaries of pulse transformers, which may be low impedance pulse voltage sources disclosed in Johnson U.S. Pat. No. 3,513,327 entitled "Low Impedance Pulse Generator," the pulse sources may be constituted by solid state pulsing circuits, as is disclosed in Johnson application Ser. No. 821,306 filed May 2, 1969, as well as other solid state or hybrid pulser circuits.

As illustrated, panel line A has its selection resistor **R1** in circuit with pulse source **B1** and selection resistor **R2** for panel line B is in circuit with its pulse source **B2**. Diodes **DG1** and **DG2** are pulsed or reverse biased by pulses from pulse source **G1**. Diode D_{B1} serves as the sustainer bypass or feed through diode for panel line B to sustainer source **10**, as is described in the above mentioned Johnson patent application, Ser. No. **60,402** entitled "Selection and Addressing Circuitry for Matrix Type Discharge Panel."

The action of this circuit is as follows: when transformer secondary or pulse source **B1** is pulsed and none of the other sources are pulsed, then the resulting voltage will be communicated to diode **DG1** through resistor **R1** and all of that voltage will be dropped across resistor **R1**. However, in the event that pulse

sources B1 and G1 are simultaneously pulsed, then the pulse from source G1 will act in such a way as to reverse bias diode DG1, and the result will be that on panel line A the voltage will be elevated above that which the sustainer voltage is at at that particular instant by an amount equal to the lower of the two pulsers B1 and G1, and it will be as wide as the coincident overlap of the pulsers B1 and G1 respectively. In the basic circuit illustrated in FIG. 1, the diode types are a group of common anode diodes on a header and a group of common cathode diodes on a header. In addition, each conductor line on the panel has associated with it, one resistor and two diodes. The DB1 and DB2 diodes are the sustainer bypass diodes referred to above and return directly to the sustainer source **10**. This diode strip in FIG. 1 may be as long as desired and does not necessarily have to be a binary chain. On the other hand, the resistor inputs have the characteristic that each are driven by a pulser, B1 and B2. There are as many resistor pulsers as there are diodes in each group driven by a group selector. Note that in any case, the number of bit pulsers times the number of group selectors must equal the total number of lines on the panel in the row and the column conductor array respectively. With further reference to FIG. 1, it should be noted that to produce opposite polarity pulses, both diodes are poled in a reverse direction and the pulses generated are of reverse polarity.

Referring now to FIG. 2, there is disclosed for the row conductors R1, R2, R3 ...RN, a diode-resistor address and selector matrix which is composed of resistors R_{r-1}, R_{r-2}. . . R_{r-n} for each conductor on the row conductor plate. In this embodiment, all of the row resistors are pulsed from a single pulse source **R30**, corresponding to pulse source B1 or B2 in FIG. 1. By reference to FIG. 3, it will be clear that the row resistors as well as the column resistors may be driven in groups or in any sequence or binary pattern as desired. Pulse sources **R31, R32, R33, R34, R35, R36, R37** and **R38** corresponding to diode pulser D1 in FIG. 1, are connected to the row conductors R1, R2, R3 . . . RN by means of bit diodes DB which, as illustrated, are connected in a digital logical sequence and pattern. Thus, the row pulser bus A is driven by pulse generator **32**, and the complement pulser bus $\overline{A}$ is driven by pulse generator **R31**. (In the notation utilized, when A is energized, $\overline{A}$ is not, and when $\overline{A}$ is energized, A is not.) And, similarly, in connection with the remaining row pulsers **R33–34, R35–36**, and **R37–38**. Thus, when pulse generator **R30** supplies a pulse to all of the row select resistors R_{r1}, R_{r2} . . . R_{r-n}, and the particular combinations of pulse generators **31–38** shown in the grid are energized, a particular row conductor is likewise energized. It will be noted that the sustaining generator **10R** applies its potential to the panel conductors at all times. A corresponding arrangement is followed in connection with the column conductors C1, C2, . . . CN. Thus, any particular cross point in the panel may be selected by proper pulsing of the pulse generators illustrated.

As mentioned above, the sustaining generators **10R** and **10C** are bypassed by means of bypass diodes D_{JR-1}, D_{JR-2}, . . . D_{JR-N} and the column conductors are likewise provided with sustaining bypass diodes D_{JC-1}, D_{JC-2}, . . . D_{JC-N}, the purpose and functioning of said bypass diodes being as more fully described in the aforementioned Johnson application Ser. No. 60,402 now abandoned entitled "Selection and Addressing Circuitry for Matrix Type Gas Discharge Panel." It will be noted that in the circuitry illustrated in FIG. 2, the panel conductor line between the anodes of the bypass diodes and the connections of the terminal ends of the row conductors on the left hand side edge extension is, in effect, an integral part of the addressing and selection circuitry. In this way, maximum and economical utilization of the space on the panel is effected. A similar scheme is applied to the column conductors, column sustainer bypass diodes D_c being at the lower edge of the panel extension and connected to the panel conductors and the upper edge extension of the column conductors being connected to the diode-resistor matrix in the pattern shown. As also illustrated in FIG. 2, the sustaining generators **10C** for the column conductors and **10R** for the row conductors as well as the pulse sources **R30** and **R31, R32 . . . R38** and **C31 . . . C38** may be directly mounted on the panel, the connections to the primary winding for the pulse transformers not being shown, it being understood that the transformer secondaries illustrated are merely indicative of pulse sources, the invention not being limited to transformer type sources but including solid state and hybrid (transformer and solid state) pulse sources, as well.

Referring now to FIG. 3, there is disclosed a further embodiment of the invention wherein the row conductor plate **50** having edge extensions **50L** and **50R** is disposed at a 90° angle relative to column conductor plate **52** which has edge extensions **52U** and **52D**, the plates being joined by a spacer sealant means **54**. In this case, the group selection diodes D_{GR} are located on edge extensions **50R**, whereas the row sustainer return diodes D_{BR} are located on edge extensions **50L**. The row select resistors R_S are also located on edge extension **50L**. The components may be contained in a header type assembly (FIG. 7) which holds all three type components, namely, resistors, diodes with common anodes and diodes with common cathodes. The length of each such header strip **70** (FIG. 7) may be determined by the number of component parts ("N" component long) where an electrical contact would be a common header **72** on one side of the component strip and by means of bonding pads **71** on the other side. The bonding pads **71** may be either solder beads, gold balls, where the solder beads could be reflow soldered to make electrical contact to the panel after proper positioning. In a similar fashion, the gold balls could also be bonded to the conductors of the panel by ultrasonic means. It should be noted that the bonding pads could be staggered so as to permit a favorable spacing and more tolerance in mechanical positioning. In addition, the component strip **70** may serve as a carrier for both the bit select resistors as well as the bypass diodes. In either case, electrical contact of the component strip **70** is made by the inversion of same to the panel, and by bonding by any one of the above techniques.

The component strip **70**, shown in FIG. 7, may be made by a number of different manufacturing technologies comprising either thick film, thin film or monolithic technology, or a combination of these. They may, if fact, be assembled in arrays which are quite

large, such as circuitry for 32 panel lines, 64 panel lines, 128, and even 512 panel lines. In these instances, where the strip becomes excessively large, the monolithic technique would most likely be replaced by the alumina substrates, with the above mentioned bonding pads with the monolithic thick or thin film chips dispersed throughout the other side of the alumina substrate.

As shown in FIG. **4**, the resistors may be formed through a hybrid technique by opening a hole in the dielectric layer **60** which extends beyond the spacer-sealant **34** for the panel proper. In this case, a pattern of holes, such as holes **61**, **62**, **63** et seq., are opened in the dielectric layer during processing and these holes are filled with a resistive paste **75** (FIG. **5**) to form the bit select resistor. (It will be appreciated that the bonding pads **71** may likewise pass through these holes, if desired.) A similar series of holes may be provided to receive pellet diodes (not shown) or the like diodes. Then, cross conductors **76**, **77**, **78** and **79** are applied and extend to the side edges of the support plates. Similar cross conductors **80**, **81** . . . (FIG. **3**) are applied for the row select diodes. In a similar fashion, conductors **85** are applied to the sustainer bypass diodes (or are formed on a common header for same).

Since a gas discharge panel as disclosed in the aforementioned Baker et al. U.S. Pat. No. 3,499,167 requires both plus and minus pulses, and since the circuit, as indicated in FIG. **1**, requires only that the diodes be reversed as well as the generation of opposite polarity pulses, then this would realize an additional cost savings in that only two types of diode components strips would have to be stocked.

In addition to the above, it would be quite simple to implement the same technique by means of a LID type solid state chip carrier or conventional DIP on flat pack standard chip packages to hold a monolithic diode network with thin film resistors for accomplishing the same purpose. This could be mounted as well directly to the panel by the techniques mentioned above.

The basic feature of this invention is in the utilization of the conductors on a gas discharge panel as part of the selection and addressing circuitry, with the use of both ends of such conductors. However, while several forms of the invention have been disclosed, many changes and modifications, some of which have been suggested herein, may be made without departing from the invention as defined in the claims appended hereto.

What is claimed is:

1. In a gas discharge panel device of the type having a pair of identical plates, each having a length which is greater than its width, spacer sealant means joining said plates in spaced relation and at transverse angles to each other to form a thin gas chamber, and linear row-column conductor arrays on said plates, respectively, and parallel to the long axis of said plates, each of said conductors in each said array being extended beyond said spacer sealant means and at both ends of said plates, respectively, and a source of electrical operating potential for said row and said column conductors, respectively, including a continuously applied periodic sustaining voltage and discharge condition manipulating pulse potentials, and a selection and addressing circuitry, having a plurality of functionally discrete electrical components, for selecting individual ones of said linear conductors for application thereto of said pulse potentials, the improvement comprising some of said functionally discrete electrical components in said selection and addressing circuitry being physically on and electrically connected to one end of each conductor in an array, respectively and the remaining of said functionally discrete components being connected to the opposite end of each conductor in an array, respectively.

2. The invention defined in claim **1** wherein said conductors have a dielectric coating thereon, which dielectric extends beyond said spacer sealant and said gas chamber, and wherein said connections to said conductors at at least one end are made through holes in said dielectric over said conductors, respectively.

3. The invention defined in claim **1** wherein said selection and addressing circuitry includes a resistor-diode circuit for each conductor, and a diode for bypassing said sustainer potential from said resistor-diode circuitry, the further improvements comprising at least all of the diodes in said selection and addressing circuit being on one edge extension of said plates and constituting said same functionally discrete components and the said bypassing diodes being on the opposite edge extension thereof and constituting said remaining functionally discrete.

4. The invention defined in claim **2** wherein said selection and addressing circuit includes a resistor-diode circuit for each linear conductor and wherein the resistor for each said circuit, respectively, is formed in situ in a hole through said dielectric, respectively.

5. The invention defined in claim **2** wherein said holes are in a selected geometrical pattern so that an external conductor device may supply operating potentials to a selected group of selection and addressing circuits.

6. The invention defined in claim **1** wherein said selection and addressing circuit includes a selected number of resistor-diode circuits as groups, a common package for said selected number of resistor-diode circuits having bonding pads projecting therefrom, and the further improvement wherein electrical connections to said panel conductors are made by said bonding pads, respectively.

7. The invention defined in claim **1** wherein said selection and addressing circuit includes a selected number of groups of resistor-diode circuits, and a common carrier for at least the diodes of each selected group.

8. The invention defined in claim **3** wherein said selection and addressing circuit includes a selected number of groups of resistor-diode circuits and a common carrier for at least the diodes of each selected group, the said diodes for bypassing said sustainer potential having their common electrodes connected to a common external conductor.

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