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(71) Applicant (for all designated States except US): SEMI-CONDUCTOR ENERGY LABORATORY CO., LTD.
[JP/JP]; 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP).

(72) Inventor; and

(75) Inventor/Applicant (for US only): TOYOTAKA, Kouhei [JP/JP]; c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD., 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP).

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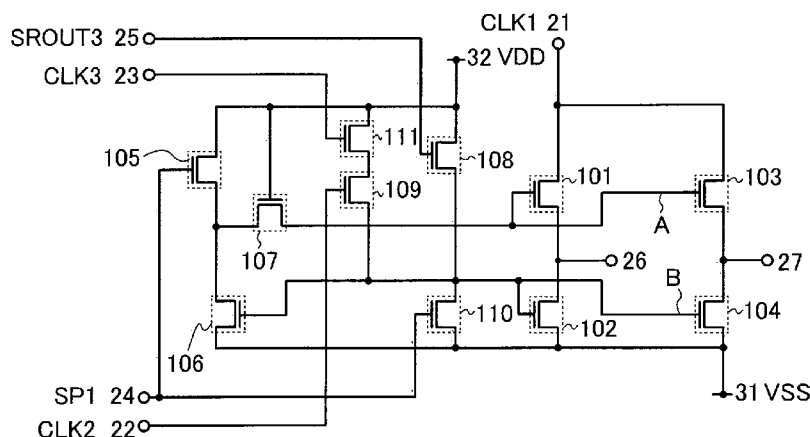
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(54) Title: PULSE SIGNAL OUTPUT CIRCUIT AND SHIFT REGISTER

FIG. 1C



(57) Abstract: An object of the present invention is to provide a pulse signal output circuit capable of operating stably and a shift register including the pulse signal output circuit. In an embodiment of the pulse signal output circuit, a transistor has a source terminal or a drain terminal connected to a gate electrode of another transistor having a source terminal or a drain terminal forming an output terminal of the pulse signal output circuit, the channel length of the transistor being longer than the channel length of the other transistor. Thereby, the amount of a leakage current modifying the gate potential of the other transistor can be reduced, and a malfunction of the pulse signal output circuit can be prevented.

DESCRIPTION

PULSE SIGNAL OUTPUT CIRCUIT AND SHIFT REGISTER

5 TECHNICAL FIELD

[0001]

The disclosed invention relates to pulse signal output circuits and shift registers.

10 BACKGROUND ART

[0002]

Transistors formed over flat plates such as glass substrates and typically used in liquid crystal display devices generally include semiconductor materials such as amorphous silicon or polycrystalline silicon. Although transistors including amorphous silicon have low field effect mobility, they can be formed over large glass substrates. In contrast, although transistors including polycrystalline silicon have high field effect mobility, they need a crystallization process such as laser annealing and are not always suitable for large glass substrates.

[0003]

20 On the other hand, transistors including oxide semiconductors as semiconductor materials have attracted attention. For example, Patent Documents 1 and 2 disclose techniques by which a transistor is formed using zinc oxide or an In-Ga-Zn-O-based oxide semiconductor as a semiconductor material and is used as a switching element of an image display device.

25 [0004]

Transistors including oxide semiconductors in channel regions have higher field effect mobility than transistors including amorphous silicon. Further, oxide semiconductor films can be formed at a temperature of 300 °C or lower by a sputtering method or the like; thus, a manufacturing process of transistors including an oxide semiconductor is simpler than that of transistors including polycrystalline silicon.

[0005]

Such transistors including oxide semiconductors are expected to be used as

switching elements included in pixel portions and driver circuits of display devices such as liquid crystal displays, electroluminescent displays, and electronic paper. For example, Non-Patent Document 1 discloses a technique by which a pixel portion and a driver circuit of a display device include transistors including oxide semiconductors.

5 [0006]

Note that transistors including oxide semiconductors are all n-channel transistors. Therefore, in the case where a driver circuit includes transistors including oxide semiconductors, the driver circuit includes only n-channel transistors.

[Patent Document]

10 [0007]

[Patent Document 1] Japanese Published Patent Application No. 2007-123861

[Patent Document 2] Japanese Published Patent Application No. 2007-096055

[Non-Patent Document]

[0008]

15 [Non-Patent Document 1] T. Osada *et al.*, "Development of Driver-Integrated Panel using Amorphous In-Ga-Zn-Oxide TFT", *Proc. SID 09 Digest*, 2009, pp. 184-187.

DISCLOSURE OF INVENTION

[0009]

20 A driver circuit includes, for example, a shift register having a pulse signal output circuit. In the case where the shift register includes transistors having the same conductivity type, the shift register might have a problem of unstable operation, for example.

[0010]

25 In view of the problem, an object of one embodiment of the present invention is to provide a pulse signal output circuit capable of operating stably and a shift register including the pulse signal output circuit.

[0011]

30 One of objects of the present invention is to provide a pulse signal output circuit capable of operating stably and a shift register including the pulse signal output circuit. In an embodiment of the pulse signal output circuit, a transistor has a source terminal or a drain terminal connected to a gate electrode of another transistor having a

source terminal or a drain terminal forming an output terminal of the pulse signal output circuit, the channel length of the transistor being longer than the channel length of the other transistor. Thereby, the amount of a leakage current modifying the gate potential of the other transistor can be reduced, and a malfunction of the pulse signal output circuit can be prevented.

[0012]

A concrete example of a configuration that can be employed is described below.

[0013]

An embodiment of the present invention is a pulse signal output circuit including first to ninth transistors, a first input signal generation circuit, and a second input signal generation circuit. A first terminal of the first transistor and a first terminal of the second transistor are electrically connected to a first output terminal, and a first terminal of the third transistor and a first terminal of the fourth transistor are electrically connected to a second output terminal. The first input signal generation circuit includes the fifth transistor and the sixth transistor. A first terminal of the fifth transistor and a first terminal of the sixth transistor are electrically connected to each other and collectively function as an output terminal of the first input signal generation circuit. The second input signal generation circuit includes the seventh to ninth transistors. A second terminal of the seventh transistor, a second terminal of the eighth transistor, and a first terminal of the ninth transistor are electrically connected to each other and collectively function as an output terminal of the second input signal generation circuit. A gate terminal of the first transistor, a gate terminal of the third transistor, and the output terminal of the first input signal generation circuit are electrically connected to each other. A gate terminal of the second transistor, a gate terminal of the fourth transistor, and the output terminal of the second input signal generation circuit are electrically connected to each other. A channel length of the sixth transistor is longer than a channel length of the third transistor and longer than a channel length of the fourth transistor. A channel length of the ninth transistor is longer than the channel length of the third transistor and longer than the channel length of the fourth transistor.

[0014]

In the pulse signal output circuit, it is preferable that a first clock signal be input to a second terminal of the first transistor and a second terminal of the third transistor; a first potential be supplied to a second terminal of the second transistor, a second terminal of the fourth transistor, a second terminal of the sixth transistor, and a second terminal of the ninth transistor; a second potential which is higher than the first potential be supplied to a second terminal of the fifth transistor, a first terminal of the seventh transistor, and a first terminal of the eighth transistor; a first pulse signal be input to a gate terminal of the fifth transistor and a gate terminal of the ninth transistor; an output signal of the second input signal generation circuit be input to a gate terminal of the sixth transistor; a third pulse signal be input to a gate terminal of the seventh transistor; a second clock signal be input to a gate terminal of the eighth transistor; and a second pulse signal be output from the first output terminal or the second output terminal.

[0015]

In the pulse signal output circuit, at least one of the sixth transistor and the ninth transistor may be a transistor having a multi-gate structure where at least two gates are arranged in series.

[0016]

Another embodiment of the present invention is a pulse signal output circuit including first to eleventh transistors, a first input signal generation circuit, and a second input signal generation circuit. A first terminal of the first transistor and a first terminal of the second transistor are electrically connected to a first output terminal, and a first terminal of the third transistor and a first terminal of the fourth transistor are electrically connected to a second output terminal. The first input signal generation circuit includes the fifth to seventh transistors. A first terminal of the fifth transistor, a first terminal of the sixth transistor, and a first terminal of the seventh transistor are electrically connected to each other, and a second terminal of the seventh transistor functions as an output terminal of the first input signal generation circuit. The second input signal generation circuit includes the eighth to eleventh transistors. A second terminal of the eleventh transistor and a first terminal of the ninth transistor are electrically connected to each other, and a second terminal of the ninth transistor, a second terminal of the eighth transistor, and a first terminal of the tenth transistor are

electrically connected to each other and collectively function as an output terminal of the second input signal generation circuit. A gate terminal of the first transistor, a gate terminal of the third transistor, and the output terminal of the first input signal generation circuit are electrically connected to each other. A gate terminal of the second transistor, a gate terminal of the fourth transistor, and the output terminal of the second input signal generation circuit are electrically connected to each other. A channel length of the sixth transistor is longer than a channel length of the third transistor and longer than a channel length of the fourth transistor. A channel length of the tenth transistor is longer than the channel length of the third transistor and longer than the channel length of the fourth transistor.

[0017]

In the pulse signal output circuit, it is preferable that a first clock signal be input to a second terminal of the first transistor and a second terminal of the third transistor; a first potential be supplied to a second terminal of the second transistor, a second terminal of the fourth transistor, a second terminal of the sixth transistor, and a second terminal of the tenth transistor; a second potential which is higher than the first potential be supplied to a second terminal of the fifth transistor, a gate terminal of the seventh transistor, a first terminal of the eighth transistor, and a first terminal of the eleventh transistor; a first pulse signal be input to a gate terminal of the fifth transistor and a gate terminal of the tenth transistor; an output signal of the second input signal generation circuit be input to a gate terminal of the sixth transistor; a third pulse signal be input to a gate terminal of the eighth transistor; a second clock signal be input to a gate terminal of the ninth transistor; a third clock signal be input to a gate terminal of the eleventh transistor; and a second pulse signal be output from the first output terminal or the second output terminal.

[0018]

In the pulse signal output circuit, at least one of the sixth transistor and the tenth transistor may be a transistor having a multi-gate structure where at least two gates are arranged in series.

[0019]

In the pulse signal output circuit which is the embodiment of the present invention, a capacitor having a terminal electrically connected to a node where the gate

terminal of the second transistor, the gate terminal of the fourth transistor, and the output terminal of the second input signal generation circuit are electrically connected to each other may be included.

[0020]

5 In the pulse signal output circuit, at least one of the transistors preferably includes an oxide semiconductor. Further, a shift register can include a plurality of pulse signal output circuits.

[0021]

Note that in the pulse signal output circuit, the transistor includes an oxide
10 semiconductor in some cases; however, the disclosed invention is not limited to this.

[0022]

Note that in this specification and the like, a term such as "over" or "below" does not necessarily mean that a component is placed "directly on" or "directly under" another component. For example, the expression "a gate electrode over a gate
15 insulating layer" does not exclude the case where another component is placed between the gate insulating layer and the gate electrode.

[0023]

In addition, in this specification and the like, terms such as "electrode" and "wiring" do not limit the functions of components. For example, an "electrode" can be
20 used as part of a "wiring", and the "wiring" can be used as part of the "electrode". The terms such as "electrode" and "wiring" can also mean a combination of a plurality of "electrodes" and "wirings", for example.

[0024]

Functions of a "source" and a "drain" might be interchanged when, for example,
25 a transistor of opposite polarity is used or the direction of current flow is changed in circuit operation. Therefore, in this specification, the terms "source" and "drain" can be interchanged.

[0025]

Note that in this specification and the like, the term "electrically connected"
30 includes the case where components are connected to each other through an object having any electric function. Here, there is no particular limitation on an object having any electric function as long as electric signals can be transmitted and received between

components that are connected to each other through the object.

[0026]

Examples of an "object having any electric function" are a switching element such as a transistor, a resistor, an inductor, a capacitor, and an element with a variety of functions in addition to an electrode and a wiring.

[0027]

A pulse signal output circuit capable of operating stably and a shift register including the pulse signal output circuit can be provided.

10 BRIEF DESCRIPTION OF DRAWINGS

[0028]

FIGS. 1A to 1C illustrate configuration examples of a pulse signal output circuit and a shift register.

FIG. 2 is a timing chart of a shift register.

15 FIGS. 3A to 3C illustrate operation of a pulse signal output circuit.

FIGS. 4A to 4C illustrate operation of a pulse signal output circuit.

FIGS. 5A and 5B illustrate configuration examples of a pulse signal output circuit.

20 FIGS. 6A to 6C illustrate configuration examples of a pulse signal output circuit and a shift register.

FIG. 7 is a timing chart of a shift register.

FIGS. 8A to 8C illustrate operation of a pulse signal output circuit.

FIGS. 9A and 9B illustrate operation of a pulse signal output circuit.

25 FIGS. 10A and 10B illustrate configuration examples of a pulse signal output circuit.

FIGS. 11A to 11D illustrate structure examples of transistors.

FIGS. 12A to 12E illustrate an example of a method for manufacturing a transistor.

FIGS. 13A to 13C illustrate examples of semiconductor devices.

30 FIGS. 14A to 14F illustrate electronic devices.

BEST MODE FOR CARRYING OUT THE INVENTION

[0029]

Examples of embodiments of the present invention will be described below with reference to the drawings. Note that the present invention is not limited to the following description. It will be readily appreciated by those skilled in the art that modes and details of the present invention can be changed in various ways without departing from the spirit and scope of the present invention. Therefore, the present invention should not be construed as being limited to the following description of the embodiments.

[0030]

10 Note that the position, size, range, or the like of each component illustrated in drawings and the like is not accurately represented in some cases for easy understanding. Therefore, the disclosed invention is not necessarily limited to the position, size, range, or the like disclosed in the drawings and the like.

[0031]

15 Note that in this specification and the like, ordinal numbers such as "first", "second", and "third" are used in order to avoid confusion among components and do not limit the number.

[0032]

(Embodiment 1)

20 In this embodiment, configuration examples of a pulse signal output circuit and a shift register including the pulse signal output circuit will be described with reference to FIGS. 1A to 1C, FIG. 2, FIGS. 3A to 3C, and FIGS. 4A to 4C.

<Circuit Configuration>

[0033]

25 First, examples of circuit configurations of a pulse signal output circuit and a shift register including the pulse signal output circuit will be described with reference to FIGS. 1A to 1C.

[0034]

30 A shift register described in this embodiment includes first to n -th pulse signal output circuits 10₋₁ to 10_{- n} ($n \geq 2$) and first to fourth signal lines 11 to 14 which transmit clock signals (see FIG. 1A). A first clock signal (CLK1) is supplied to the

first signal line 11. A second clock signal (CLK2) is supplied to the second signal line 12. A third clock signal (CLK3) is supplied to the third signal line 13. A fourth clock signal (CLK4) is supplied to the fourth signal line 14.

[0035]

5 The clock signal is a signal which alternates between an H-level signal (high potential) and an L-level signal (low potential) at regular intervals. Here, the first to fourth clock signals (CLK1 to CLK4) are delayed by 1/4 period sequentially. In this embodiment, by using the clock signals, control or the like of the pulse signal output circuit is performed.

10 [0036]

Each of the first to n -th pulse signal output circuits 10_{_1} to 10_{_n} includes a first input terminal 21, a second input terminal 22, a third input terminal 23, a fourth input terminal 24, a fifth input terminal 25, a first output terminal 26, and a second output terminal 27 (see FIG. 1B).

15 [0037]

The first input terminal 21, the second input terminal 22, and the third input terminal 23 are electrically connected to any of the first to fourth signal lines 11 to 14. For example, the first input terminal 21 in the first pulse signal output circuit 10_{_1} is electrically connected to the first signal line 11, the second input terminal 22 in the first pulse signal output circuit 10_{_1} is electrically connected to the second signal line 12, and the third input terminal 23 in the first pulse signal output circuit 10_{_1} is electrically connected to the third signal line 13. In addition, the first input terminal 21 in the second pulse signal output circuit 10_{_2} is electrically connected to the second signal line 12, the second input terminal 22 in the second pulse signal output circuit 10_{_2} is electrically connected to the third signal line 13, and the third input terminal 23 in the second pulse signal output circuit 10_{_2} is electrically connected to the fourth signal line 14. Note that here, the case where the second to fourth signal lines 12 to 14 are connected to the n -th pulse signal output circuit 10_{_n} is described. However, which signal lines are connected to the n -th pulse signal output circuit 10_{_n} depends on the value of n . Thus, it is to be noted that the configuration described herein is just an example.

20

25

30

[0038]

In an m -th pulse signal output circuit ($m \geq 2$) of the shift register described in this embodiment, the fourth input terminal 24 is electrically connected to the first output terminal 26 of an $(m-1)$ -th pulse signal output circuit. In an m -th pulse signal output circuit ($m \leq n-2$); the fifth input terminal 25 is electrically connected to the first output terminal 26 of an $(m+2)$ -th pulse signal output circuit; the first input terminal 26 is electrically connected to the fourth input terminal 24 of an $(m+1)$ -th pulse signal output circuit; and the second output terminal 27 outputs a signal to an OUT(m).

[0039]

For example, the fourth input terminal 24 in the third pulse signal output circuit 10_{_3} is electrically connected to the first output terminal 26 in the second pulse signal output circuit 10_{_2}. The fifth input terminal 25 in the third pulse signal output circuit 10_{_3} is electrically connected to the first output terminal 26 in the fifth pulse signal output circuit 10_{_5}. The first input terminal 26 in the third pulse signal output circuit 10_{_3} is electrically connected to the fourth input terminal 24 in the fourth pulse signal output circuit 10_{_4} and the fifth input terminal 25 in the first pulse signal output circuit 10_{_1}.

[0040]

In addition, a first start pulse (SP1) is input from a fifth wiring 15 to the fourth input terminal 24 in the first pulse signal output circuit 10_{_1}. A pulse output from the previous stage is input to the fourth input terminal 24 in a k -th pulse signal output circuit 10_{_k} (k is a natural number greater than or equal to 2 and less than or equal to n). A second start pulse (SP2) is input to the fifth input terminal 25 in a $(n-1)$ -th pulse signal output circuit 10_{_ $n-1$} . A third start pulse (SP3) is input to the fifth input terminal 25 in the n -th pulse signal output circuit 10_{_n}. The second start pulse (SP2) and the third start pulse (SP3) may be input from the outside or generated inside the circuit.

[0041]

Next, specific configurations of the first to n -th pulse signal output circuits 10_{_1} to 10_{_n} will be described.

[0042]

Each of the first to n -th pulse signal output circuits 10_{_1} to 10_{_n} includes a pulse signal generation circuit including first to fourth transistors 101 to 104, a first input signal generation circuit including fifth to seventh transistors 105 to 107, and a second input signal generation circuit including eighth to eleventh transistors 108 to 111 (see FIG. 1C). Further, signals are supplied to the first to eleventh transistors 101 to 111 from first and second power supply lines 31 and 32, in addition to the first to fifth input terminals 21 to 25.

[0043]

A specific example of a configuration of the pulse signal generation circuit is as follows.

[0044]

A first terminal (hereinafter, "first terminal" means one of a source terminal and a drain terminal) of the first transistor 101 and a first terminal of the second transistor 102 are electrically connected to the first output terminal 26. Similarly, a first terminal of the third transistor 103 and a first terminal of the fourth transistor 104 are electrically connected to the second output terminal 27. A gate terminal of the first transistor 101, a gate terminal of the third transistor 103, and an output terminal of the first input signal generation circuit are electrically connected to each other. A gate terminal of the second transistor 102, a gate terminal of the fourth transistor 104, and an output terminal of the second input signal generation circuit are electrically connected to each other.

[0045]

The first clock signal is input to a second terminal (hereinafter, "second terminal" means the other of the source terminal and the drain terminal) of the first transistor 101. The second terminal of the first transistor 101 also functions as the first input terminal 21 in the pulse signal output circuit. A first potential (for example, a low potential V_{SS}) is supplied to a second terminal of the second transistor 102 through the first power supply line 31. The first clock signal is input to a second terminal of the third transistor 103. The second terminal of the third transistor 103 also functions as the first input terminal 21 in the pulse signal output circuit. The first potential is supplied to a second terminal of the fourth transistor 104 through the first power supply line 31.

[0046]

A specific example of a configuration of the first input signal generation circuit is as follows.

[0047]

5 A first terminal of the fifth transistor 105, a first terminal of the sixth transistor 106, and a first terminal of the seventh transistor 107 are electrically connected to each other. Further, a second terminal of the seventh transistor 107 functions as the output terminal of the first input signal generation circuit.

[0048]

10 A second potential is supplied to a second terminal of the fifth transistor 105 through the second power supply line 32. The first potential is supplied to a second terminal of the sixth transistor 106 through the first power supply line 31. A pulse signal from the previous stage (in the first pulse signal output circuit, the pulse signal includes a start pulse signal) is input to a gate terminal of the fifth transistor 105. The
15 gate terminal of the fifth transistor 105 functions as a first input terminal of the first input signal generation circuit and functions as the fourth input terminal 24 of the pulse signal output circuit. An output signal of the second input signal generation circuit is input to a gate terminal of the sixth transistor 106. The gate terminal of the sixth transistor 106 functions as a second input terminal of the first input signal generation
20 circuit. The second potential is supplied to a gate terminal of the seventh transistor 107 through the second power supply line 32.

[0049]

 Although the seventh transistor 107 is provided in this embodiment, a configuration without the seventh transistor 107 may be employed. With the seventh
25 transistor 107, rise in the potential of the first terminal of the fifth transistor 105, which might be caused by bootstrap operation, can be suppressed. That is to say, application of high bias voltage to a region between a gate and a source (or between the gate and a drain) of the fifth transistor 105 can be prevented; thus, deterioration of the fifth transistor 105 can be suppressed.

30 [0050]

A specific example of a configuration of the second input signal generation circuit is as follows.

[0051]

A second terminal of the eleventh transistor 111 and a first terminal of the ninth transistor 109 are electrically connected to each other. A second terminal of the ninth transistor, a second terminal of the eighth transistor, and a first terminal of the tenth transistor are electrically connected to each other and function as the output terminal of the second input signal generation circuit.

[0052]

The second potential is supplied to a first terminal of the eighth transistor 108 and a first terminal of the eleventh transistor 111 through the second power supply line 32. The first potential is supplied to a second terminal of the tenth transistor 110 through the first power supply line 31. A pulse signal from a second subsequent stage is input to a gate terminal of the eighth transistor 108, as illustrated in FIG. 1A and FIG. 1B. The gate terminal of the eighth transistor 108 functions as a first input terminal of the second input signal generation circuit and as the fifth input terminal 25 in the pulse signal output circuit. The second clock signal is input to a gate terminal of the ninth transistor 109. The gate terminal of the ninth transistor 109 functions as a second input terminal of the second input signal generation circuit and the second input terminal 22 in the pulse signal output circuit. A pulse signal from the previous stage (in the first pulse signal output circuit, the pulse signal is a start pulse signal) is input to a gate terminal of the tenth transistor 110. The gate terminal of the tenth transistor 110 functions as a third input terminal of the second input signal generation circuit and the fourth input terminal 24 in the pulse signal output circuit. The third clock signal is input to a gate terminal of the eleventh transistor 111. The gate terminal of the eleventh transistor 111 functions as a fourth input terminal of the second input signal generation circuit and the third input terminal 23 in the pulse signal output circuit.

[0053]

Note that in the pulse signal output circuit described in this embodiment, a channel length of the sixth transistor 106 is longer than a channel length of the third transistor 103 and longer than a channel length of the fourth transistor 104. Further, a channel length of the tenth transistor 110 is longer than the channel length of the third transistor 103 and longer than the channel length of the fourth transistor 104. Thus, the amount of shifts in the threshold voltage of the sixth transistor 106 and the tenth

transistor 110 can be reduced, so that the deterioration can be suppressed.

[0054]

Note that components of the pulse signal output circuit (e.g., configuration examples of the pulse signal generation circuit, the first input signal generation circuit, and the second input signal generation circuit) are just examples, and the disclosed invention is not limited thereto.

[0055]

In the following description of this embodiment, a node where the gate terminal of the first transistor 101, the gate terminal of the third transistor 103, and the output terminal of the first input signal generation circuit are connected to each other in the pulse signal output circuit illustrated in FIG. 1C is referred to as a node A. In addition, a node where the gate terminal of the second transistor 102, the gate terminal of the fourth transistor 104, and the output terminal of the second input signal generation circuit are connected to each other is referred to as a node B.

[0056]

A capacitor for favorably performing bootstrap operation may be provided between the node A and the first output terminal 26. Furthermore, a capacitor electrically connected to the node B may be provided in order to hold a potential of the node B.

[0057]

Note that each of the first to eleventh transistors 101 to 111 preferably includes an oxide semiconductor. When an oxide semiconductor is included in the transistor, the off-state current of the transistor can be reduced. Further, the on-state current and field-effect mobility of the transistor including an oxide semiconductor can be increased as compared to a transistor including amorphous silicon or the like. Furthermore, the deterioration of the transistor can be suppressed. Thus, an electronic circuit which consumes low power, can operate at high speed, and operates with higher accuracy is realized. Note that the description of the transistor including an oxide semiconductor is omitted here because it is described in detail in an embodiment below.

[0058]

<Operation>

Next, operation of the shift register shown in FIGS. 1A to 1C is described with

reference to FIG. 2, FIGS. 3A to 3C, and FIGS. 4A to 4C. Specifically, operation in each of first to sixth periods 51 to 56 in a timing chart illustrated in FIG. 2 is described with reference to FIGS. 3A to 3C and FIGS. 4A to 4C. In the timing chart, CLK1 to CLK4 denote clock signals; SP1 denotes a first start pulse; OUT1 to OUT4 denote
5 outputs from the second output terminals of the first to fourth pulse signal output circuits 10_{_1} to 10_{_4}; nodes A and B denote potentials at the nodes A and B; and SROUT1 to SROUT4 denote outputs from the first output terminals of the first to fourth pulse signal output circuits 10_{_1} to 10_{_4}.

[0059]

10 Note that in the description below, the first to eleventh transistors 101 to 111 are all n-channel transistors. Further, in FIGS. 3A to 3C and FIGS. 4A to 4C, transistors indicated by solid lines mean that the transistors are in a conduction state (on), and transistors indicated by dashed lines mean that the transistors are in a non-conduction state (off).

15 [0060]

Typical operation of the first pulse signal output circuit 10_{_1} is described. The configuration of the first pulse signal output circuit 10_{_1} is as described above. Further, relation between signals input and potentials supplied is as described above. Note that in the description below, V_{DD} is used for all the high potentials (also referred to as H
20 levels, H-level signals, or the like) to be supplied to input terminals and power supply lines, and V_{SS} is used for all the low potentials (also referred to as L levels, L-level signals, or the like) to be supplied to input terminals and power supply lines.

[0061]

In the first period 51, SP1 is at H level, so that a high potential is supplied to
25 the gate terminal of the fifth transistor 105 and the gate terminal of the tenth transistor 110 which function as the fourth input terminal 24 in the first pulse signal output circuit 10_{_1}. Thus, the fifth transistor 105 and the tenth transistor 110 are turned on. In the first period 51, CLK3 is also at H level, so that the eleventh transistor 111 is also turned on. In addition, since a high potential is supplied to the gate terminal of the seventh
30 transistor 107, the seventh transistor 107 is also turned on (see FIG. 3A).

[0062]

When the fifth transistor 105 and the seventh transistor 107 are turned on, the potential of the node A rises. When the tenth transistor 110 is turned on, the potential of the node B falls. The potential of the second terminal of the fifth transistor 105 is V_{DD} . Therefore, the potential of the first terminal of the fifth transistor 105 becomes $V_{DD} - V_{th105}$, which is a potential obtained by subtracting the threshold voltage of the fifth transistor 105 from the potential of the second terminal. The potential of the gate terminal of the seventh transistor 107 is V_{DD} . Therefore, in the case where V_{th107} , which is the threshold voltage of the seventh transistor 107, is higher than or equal to V_{th105} , the potential of the node A becomes $V_{DD} - V_{th107}$, whereby the seventh transistor 107 is turned off. On the other hand, in the case where V_{th107} is lower than V_{th105} , the potential of the node A rises to $V_{DD} - V_{th105}$ while the seventh transistor 107 is kept on. Hereinafter, the potential of the node A attained in the first period 51 is denoted by V_{AH} . Here, V_{th105} and V_{th107} are the threshold voltage of the fifth transistor 105 and the threshold voltage of the seventh transistor 107, respectively. The same can be said for the other transistors. When the potential of the node A reaches V_{AH} , the fifth transistor 105 and the seventh transistor 107 are turned off; thus, the node A is made to be in a floating state while the potential thereof is kept at V_{AH} .

[0063]

When the potential of the node A becomes V_{AH} , the first transistor 101 and the third transistor 103 are turned on. Here, since CLK1 is at L level, an L-level signal is output from the first output terminal 26 and the second output terminal 27.

[0064]

In the second period 52, the potential of CLK1 is changed from L level to H level. Since the first transistor 101 and the third transistor 103 are on, a potential of the first output terminal 26 and a potential of the second output terminal 27 rise. Further, a capacitance is generated between the gate terminal and the source terminal (or the drain terminal) of the first transistor 101; with the capacitance, the gate terminal and the source terminal (or the drain terminal) thereof are capacitively coupled. Similarly, a capacitance is generated between the gate terminal and the source terminal (or the drain terminal) of the third transistor 103; with the capacitance, the gate terminal and the source terminal (or the drain terminal) thereof are capacitively coupled. Thus, the

potential of the node A in a floating state rises as the potential of the first output terminal 26 and the potential of the second output terminal 27 rise (bootstrap operation). The potential of the node A finally becomes higher than $V_{DD} + V_{th101}$, and each of the potential of the first output terminal 26 and the potential of the second output terminal 27 becomes V_{DD} (H level) (see FIG. 2 and FIG. 3B).

[0065]

In the second period 52, the tenth transistor 110 is on; therefore, the node B is kept at L level. Thus, variation in the potential of the node B due to capacitive coupling, which occurs when the potential of the first output terminal 26 is changed from L level to H level, can be suppressed, so that a malfunction due to the variation in the potential can be prevented.

[0066]

In the third period 53, SP1 becomes L level, so that the fifth transistor 105 and the tenth transistor 110 are turned off. Further, CLK1 is kept at H level and the potential of the node A is not changed; thus, V_{DD} (a H-level signal) is output from the first output terminal 26 and the second output terminal 27 (see FIG. 3C). Note that in the third period 53, although the node B is in a floating state, the potential of the first output terminal 26 is not changed; therefore, a malfunction due to the capacitive coupling is negligible.

[0067]

In the fourth period 54, since both CLK2 and CLK3 are at H level, the potential of the node B rises in a short period of time. Further, CLK1 becomes L level. Consequently, the second transistor 102 and the fourth transistor 104 are turned on, so that the potentials of the first output terminal 26 and the second output terminal 27 fall in a short period of time (see FIG. 4A).

[0068]

In the fifth period 55, the potential of the fifth input terminal 25 (i.e., SROUT3) is kept at H level, whereby the potential of the node B is kept. Thus, the second transistor 102, the fourth transistor 104, and the sixth transistor 106 are kept on, so that the potentials of the first output terminal 26 and the second output terminal 27 are kept at L level (see FIG. 4B).

[0069]

In the sixth period 56, the fifth input terminal 25 (i.e., SROUT3) becomes L level, so that the eighth transistor 108 is turned off. At this time, the node B is made to be in a floating state while keeping the potential. Thus, the second transistor 102, the fourth transistor 104, and the sixth transistor 106 are kept on (see FIG. 4C).

5 [0070]

Note that the potential of the node B falls due to an off-state current of a transistor, for example. However, a transistor with a sufficiently low off-state current (e.g., a transistor including an oxide semiconductor) does not have such a problem; thus, the fall in the potential of the node B can be suppressed.

10 [0071]

The threshold voltage of a transistor including silicon is controlled by doping, but the threshold voltage of a transistor including a wide-gap semiconductor such as an oxide semiconductor cannot be controlled by doping. Thus, in the transistor including a wide-gap semiconductor, a current might flow between a source and a drain even when a bias is not applied to a gate (even when the gate and the source have the same potential). However, in the pulse signal output circuit described in this embodiment, the channel length of the tenth transistor 110 is made longer than the channel length of the third transistor 103 and longer than the channel length of the fourth transistor 104, whereby the amount of a leakage current generated from the node B can be suppressed; thus, the potential of the node B can be kept stably. Further, the channel length of the sixth transistor 106 is made longer than the channel length of the third transistor 103 and longer than the channel length of the fourth transistor 104, whereby the amount of a leakage current generated from the node A can be suppressed; thus, bootstrap operation in the node A can be made stable. That is to say, with the structure of this embodiment, the potential of the node A and the potential of the node B can be kept for a long period of time; thus, even when the structure is used for a circuit with low frequency, for example, a malfunction can be prevented.

[0072]

Note that in order to further suppress the fall in the potential of the node B, a capacitor 120 having one electrode electrically connected to the node B may be additionally provided, as illustrated in FIG. 5A. The other electrode of the capacitor 120 may be electrically connected to the first power supply line 31, for example.

[0073]

Further, the fall in the potential of the node B can be further suppressed by using a sixth transistor 106 or a tenth transistor 110 having a multi-gate structure where at least two gates are arranged in series, as illustrated in FIG. 5B. Note that although FIG. 5B illustrates an example in which both the sixth transistor 106 and the tenth transistor 110 have multi-gate structures, only one of the sixth transistor 106 and the tenth transistor 110 may have a multi-gate structure. Of course, the structure illustrated in FIG. 5A and the structure illustrated in FIG. 5B may be used in combination.

[0074]

With the use of a transistor having a multi-gate structure as illustrated in FIG. 5B, redundancy of the transistor can be accomplished. Thus, yield of the pulse signal output circuit can be improved.

[0075]

In the case where both CLK2 and CLK3 become H level in a subsequent period, the ninth transistor 109 and the eleventh transistor 111 are turned on, and a potential is supplied to the node B periodically. Therefore, even when a transistor having a comparatively high off-state current is used, a malfunction of the pulse signal output circuit can be prevented.

[0076]

In addition, the shift register of this embodiment is driven by a driving method in which a pulse output from the m -th pulse signal output circuit overlaps with half of a pulse output from the $(m+1)$ -th pulse signal output circuit. Therefore, a wiring can be charged for a longer period of time as compared to the case where the driving method is not used. That is to say, with the driving method, a pulse signal output circuit which withstands a heavy load and operates at high frequency is provided.

[0077]

(Embodiment 2)

In this embodiment, configuration examples of a pulse signal output circuit and a shift register including the pulse signal output circuit, which are different modes from the pulse signal output circuit and the shift register described in the above embodiment, and operation thereof will be described with reference to FIGS. 6A to 6C, FIG. 7, FIGS.

8A to 8C, and FIGS. 9A and 9B.

<Circuit Configuration>

[0078]

First, examples of circuit configurations of a pulse signal output circuit and a
5 shift register including the pulse signal output circuit will be described with reference to
FIGS. 6A to 6C.

[0079]

The configuration of the shift register described in this embodiment is similar
to that of the shift register described in the above embodiment. One of differences
10 between them is that the third input terminal 23 is not provided in the first to n -th pulse
signal output circuits 10₁ to 10 _{n} (see FIGS. 6A to 6C). That is, two types of clock
signals are input to one pulse signal output circuit. The other structures are similar to
those in the above embodiment.

[0080]

15 Since the third input terminal 23 is not provided in the first to n -th pulse signal
output circuits 10₁ to 10 _{n} , the eleventh transistor connected to the third input terminal
23 is not provided (see FIG. 6C). Accordingly, the connection relation in the second
input signal generation circuit is partly changed.

[0081]

20 A specific example of a configuration of the second input signal generation
circuit is as follows.

[0082]

The second terminal of the ninth transistor 109, the second terminal of the
eighth transistor 108, and the first terminal of the tenth transistor 110 are electrically
25 connected to each other and function as the output terminal of the second input signal
generation circuit.

[0083]

The second potential is supplied to the first terminal of the eighth transistor 108
and the first terminal of the ninth transistor 109 through the second power supply line
30 32. The first potential is supplied to the second terminal of the tenth transistor 110
through the first power supply line 31. A pulse signal is input to the gate terminal of

the eighth transistor 108. The gate terminal of the eighth transistor 108 functions as the first input terminal of the second input signal generation circuit and as the fifth input terminal 25 in the pulse signal output circuit. The second clock signal is input to the gate terminal of the ninth transistor 109. The gate terminal of the ninth transistor 109 functions as the second input terminal of the second input signal generation circuit and the second input terminal 22 in the pulse signal output circuit. A pulse signal is input to the gate terminal of the tenth transistor 110. The gate terminal of the tenth transistor 110 functions as the third input terminal of the second input signal generation circuit and the fourth input terminal 24 in the pulse signal output circuit.

[0084]

Note that in the pulse signal output circuit described in this embodiment, a channel length of the sixth transistor 106 is longer than a channel length of the third transistor 103 and longer than a channel length of the fourth transistor 104. Further, a channel length of the tenth transistor 110 is longer than the channel length of the third transistor 103 and longer than the channel length of the fourth transistor 104. Thus, the amount of shifts in the threshold voltage of the sixth transistor 106 and the tenth transistor 110 can be reduced, so that the deterioration can be suppressed.

[0085]

Note that the aforementioned configuration is just an example, and the disclosed invention is not limited thereto.

[0086]

In the following description of this embodiment, in a manner similar to the above embodiment, a node where the gate terminal of the first transistor 101, the gate terminal of the third transistor 103, and the output terminal of the first input signal generation circuit are connected to each other in the pulse signal output circuit illustrated in FIG. 6C is referred to as a node A. In addition, a node where the gate terminal of the second transistor 102, the gate terminal of the fourth transistor 104, and the output terminal of the second input signal generation circuit are connected to each other is referred to as a node B.

[0087]

A capacitor for favorably performing bootstrap operation may be provided between the node A and the first output terminal 26. Furthermore, a capacitor

electrically connected to the node B may be provided in order to hold a potential of the node B.

[0088]

Note that each of the first to tenth transistors 101 to 110 preferably includes an oxide semiconductor. When an oxide semiconductor is included in the transistor, the off-state current of the transistor can be reduced. Further, the on-state current and field-effect mobility of the transistor including an oxide semiconductor can be increased as compared to a transistor including amorphous silicon or the like. Furthermore, the deterioration of the transistor can be suppressed. Thus, an electronic circuit which consumes low power, can operate at high speed, and operates with higher accuracy is realized. Note that the description of the transistor including an oxide semiconductor is omitted here because it is described in detail in an embodiment below.

[0089]

<Operation>

Next, operation of the shift register shown in FIGS. 6A to 6C is described with reference to FIG. 7, FIGS. 8A to 8C, and FIGS. 9A and 9B. Specifically, operation in each of first to fifth periods 51 to 55 in a timing chart illustrated in FIG. 7 is described with reference to FIGS. 8A to 8C and FIGS. 9A and 9B. In the timing chart, CLK1 to CLK4 denote clock signals; SP1 denotes a first start pulse; OUT1 to OUT4 denote outputs from the second output terminals of the first to fourth pulse signal output circuits 10_{_1} to 10_{_4}; nodes A and B denote potentials at the nodes A and B; and SROUT1 to SROUT4 denote outputs from the first output terminals of the first to fourth pulse signal output circuits 10_{_1} to 10_{_4}.

[0090]

Note that in the description below, the first to tenth transistors 101 to 110 are all n-channel transistors. Further, in FIGS. 8A to 8C and FIGS. 9A and 9B, transistors indicated by solid lines mean that the transistors are in a conduction state (on), and transistors indicated by dashed lines mean that the transistors are in a non-conduction state (off).

[0091]

Typical operation of the first pulse signal output circuit 10_{_1} is described. The

configuration of the first pulse signal output circuit 10_{_1} is as described above. Further, relation between signals input and potentials supplied is as described above. Note that in the description below, V_{DD} is used for all the high potentials (also referred to as H levels, H-level signals, or the like) to be supplied to input terminals and power supply lines, and V_{SS} is used for all the low potentials (also referred to as L levels, L-level signals, or the like) to be supplied to input terminals and power supply lines.

[0092]

In the first period 51, SP1 is at H level, so that a high potential is supplied to the gate terminal of the fifth transistor 105 and the gate terminal of the tenth transistor 110 which function as the fourth input terminal 24 in the first pulse signal output circuit 10_{_1}. Thus, the fifth transistor 105 and the tenth transistor 110 are turned on. In addition, since a high potential is supplied to the gate terminal of the seventh transistor 107, the seventh transistor 107 is also turned on (see FIG. 8A).

[0093]

When the fifth transistor 105 and the seventh transistor 107 are turned on, the potential of the node A rises. When the tenth transistor 110 is turned on, the potential of the node B falls. The potential of the second terminal of the fifth transistor 105 is V_{DD} . Therefore, the potential of the first terminal of the fifth transistor 105 becomes $V_{DD} - V_{th105}$, which is a potential obtained by subtracting the threshold voltage of the fifth transistor 105 from the potential of the second terminal. The potential of the gate terminal of the seventh transistor 107 is V_{DD} . Therefore, in the case where V_{th107} , which is the threshold voltage of the seventh transistor 107, is higher than or equal to V_{th105} , the potential of the node A becomes $V_{DD} - V_{th107}$, whereby the seventh transistor 107 is turned off. On the other hand, in the case where V_{th107} is lower than V_{th105} , the potential of the node A rises to $V_{DD} - V_{th105}$ while the seventh transistor 107 is kept on. Hereinafter, the potential of the node A attained in the first period 51 is denoted by V_{AH} . When the potential of the node A reaches V_{AH} , the fifth transistor 105 and the seventh transistor 107 are turned off; thus, the node A is made to be in a floating state while the potential thereof is kept at V_{AH} .

[0094]

When the potential of the node A becomes V_{AH} , the first transistor 101 and the

third transistor 103 are turned on. Here, since CLK1 is at L level, an L-level signal is output from the first output terminal 26 and the second output terminal 27.

[0095]

In the second period 52, the potential of CLK1 is changed from L level to H level. Since the first transistor 101 and the third transistor 103 are on, a potential of the first output terminal 26 and a potential of the second output terminal 27 rise. Further, a capacitance is generated between the gate terminal and the source terminal (or the drain terminal) of the first transistor 101; with the capacitance, the gate terminal and the source terminal (or the drain terminal) thereof are capacitively coupled. Similarly, a capacitance is generated between the gate terminal and the source terminal (or the drain terminal) of the third transistor 103; with the capacitance, the gate terminal and the source terminal (or the drain terminal) thereof are capacitively coupled. Thus, the potential of the node A in a floating state rises as the potential of the first output terminal 26 and the potential of the second output terminal 27 rise (bootstrap operation). The potential of the node A finally becomes higher than $V_{DD} + V_{th101}$, and each of the potential of the first output terminal 26 and the potential of the second output terminal 27 becomes V_{DD} (H level) (see FIG. 7 and FIG. 8B).

[0096]

In the third period 53, CLK2 becomes H level, and the ninth transistor 109 is turned on. Accordingly, the potential of the node B rises. When the potential of the node B rises, the second transistor 102, the fourth transistor 104, and the sixth transistor 106 are turned on and the potential of the node A falls. Therefore, the potential of the first output terminal 26 and the potential of the second output terminal 27 become L level (see FIG. 8C).

[0097]

In the fourth period 54, CLK2 becomes L level, and the ninth transistor 109 is turned off. The fifth input terminal 25 (i.e., SROUT3) becomes H level, and the eighth transistor 108 is turned on. Therefore, the potential of the node A and the potential of the node B are kept, and the potential of the first output terminal 26 and the potential of the second output terminal 27 are kept at L level (see FIG. 9A).

[0098]

In the fifth period 55, the potential of the fifth input terminal 25 (i.e., SROUT3)

becomes L level, whereby the potential of the node B is kept. Thus, the second transistor 102, the fourth transistor 104, and the sixth transistor 106 are kept on, so that the potentials of the first output terminal 26 and the second output terminal 27 are kept at L level (see FIG. 9B).

5 [0099]

Note that the potential of the node B falls due to an off-state current of a transistor, for example. However, a transistor with a sufficiently low off-state current (e.g., a transistor including an oxide semiconductor) does not have such a problem.

[0100]

10 The threshold voltage of a transistor including silicon is controlled by doping, but the threshold voltage of a transistor including a wide-gap semiconductor such as an oxide semiconductor cannot be controlled by doping. Thus, in the transistor including a wide-gap semiconductor, a current might flow between a source and a drain even when a bias is not applied to a gate (even when the gate and the source have the same potential). However, in the pulse signal output circuit described in this embodiment,
15 the channel length of the tenth transistor 110 is made longer than the channel length of the third transistor 103 and longer than the channel length of the fourth transistor 104, whereby the amount of a leakage current generated from the node B can be suppressed; thus, the potential of the node B can be kept stably. Further, the channel length of the
20 sixth transistor 106 is made longer than the channel length of the third transistor 103 and longer than the channel length of the fourth transistor 104, whereby the amount of a leakage current generated from the node A can be suppressed; thus, bootstrap operation in the node A can be made stable. That is to say, with the structure of this embodiment, the potential of the node A and the potential of the node B can be kept for a long period
25 of time; thus, even when the structure is used for a circuit with low frequency, for example, a malfunction can be prevented.

[0101]

Note that in order to further suppress the fall in the potential of the node B, a capacitor 120 having one electrode electrically connected to the node B may be
30 additionally provided, as illustrated in FIG. 10A. The other electrode of the capacitor 120 may be electrically connected to the first power supply line 31, for example.

[0102]

Further, the fall in the potential of the node B can be further suppressed by using a sixth transistor 106 or a tenth transistor 110 having a multi-gate structure where at least two gates are arranged in series, as illustrated in FIG. 10B. Note that although FIG. 10B illustrates an example in which both the sixth transistor 106 and the tenth transistor 110 have multi-gate structures, one of the sixth transistor 106 and the tenth transistor 110 may have a multi-gate structure. Of course, the structure illustrated in FIG. 10A and the structure illustrated in FIG. 10B may be used in combination.

[0103]

With the use of a transistor having a multi-gate structure as illustrated in FIG. 10B, redundancy of the transistor can be accomplished. Thus, yield of the pulse signal output circuit can be improved.

[0104]

In the case where CLK2 becomes H level in a subsequent period, the ninth transistor 109 is turned on, and a potential is supplied to the node B periodically. Therefore, even when a transistor having a comparatively high off-state current is used, a malfunction of the pulse signal output circuit can be prevented.

[0105]

As described above, the structures, methods, and the like described in this embodiment can be combined with any of the structures, methods, and the like described in the other embodiments as appropriate.

[0106]

(Embodiment 3)

In this embodiment, examples of transistors which can be used in the pulse signal output circuit and the shift register described in the above embodiment are described with reference to FIGS. 11A to 11D. There is no particular limitation on the structure of the transistor. For example, a suitable structure such as a top-gate structure, a bottom-gate structure, a staggered structure, or a planar structure can be employed. Alternatively, the transistor may have a single-gate structure in which one channel formation region is formed or a multi-gate structure in which two or more channel formation regions are formed. Alternatively, the transistor may have a structure in which two gate electrode layers are formed over and below a channel region with a gate insulating layer provided therebetween.

[0107]

FIGS. 11A to 11D illustrate examples of the cross-sectional structures of the transistors. The transistors illustrated in FIGS. 11A to 11D each include an oxide semiconductor as a semiconductor. An advantage of the use of an oxide semiconductor is high mobility and low off-state current which can be obtained by a simple low-temperature process.

[0108]

A transistor 410 illustrated in FIG. 11A is an example of a bottom-gate transistor and is also referred to as an inverted-staggered transistor.

10 [0109]

The transistor 410 includes a gate electrode layer 401, a gate insulating layer 402, an oxide semiconductor layer 403, a source electrode layer 405a, and a drain electrode layer 405b which are provided over a substrate 400 having an insulating surface. Further, an insulating layer 407 which is in contact with the oxide semiconductor layer 403 is provided. A protective insulating layer 409 is formed over the insulating layer 407.

[0110]

A transistor 420 illustrated in FIG. 11B is an example of a bottom-gate transistor referred to as a channel-protective (channel-stop) transistor and is also referred to as an inverted-staggered transistor.

20

[0111]

The transistor 420 includes the gate electrode layer 401, the gate insulating layer 402, the oxide semiconductor layer 403, an insulating layer 427 functioning as a channel protective layer, the source electrode layer 405a, and the drain electrode layer 405b which are provided over the substrate 400 having an insulating surface. Further, the protective insulating layer 409 is provided.

25

[0112]

A transistor 430 illustrated in FIG. 11C is an example of a bottom-gate transistor. The transistor 430 includes the gate electrode layer 401, the gate insulating layer 402, the source electrode layer 405a, the drain electrode layer 405b, and the oxide semiconductor layer 403 which are provided over the substrate 400 having an insulating surface. Further, the insulating layer 407 which is in contact with the oxide

30

semiconductor layer 403 is provided. Furthermore, the protective insulating layer 409 is formed over the insulating layer 407.

[0113]

In the transistor 430, the gate insulating layer 402 is provided on and in contact with the substrate 400 and the gate electrode layer 401, and the source electrode layer 405a and the drain electrode layer 405b are provided on and in contact with the gate insulating layer 402. Further, the oxide semiconductor layer 403 is provided over the gate insulating layer 402, the source electrode layer 405a, and the drain electrode layer 405b.

[0114]

A transistor 440 illustrated in FIG. 11D is an example of a top-gate transistor. The transistor 440 includes an insulating layer 437, the oxide semiconductor layer 403, the source electrode layer 405a, the drain electrode layer 405b, the gate insulating layer 402, and the gate electrode layer 401 which are provided over the substrate 400 having an insulating surface. A wiring layer 436a and a wiring layer 436b are provided in contact with the source electrode layer 405a and the drain electrode layer 405b, respectively.

[0115]

In this embodiment, as described above, the oxide semiconductor layer 403 is used as a semiconductor layer. As an oxide semiconductor used for the oxide semiconductor layer 403, an oxide of four metal elements, such as an In-Sn-Ga-Zn-O-based oxide semiconductor; an oxide of three metal elements, such as an In-Ga-Zn-O-based oxide semiconductor, an In-Sn-Zn-O-based oxide semiconductor, an In-Al-Zn-O-based oxide semiconductor, a Sn-Ga-Zn-O-based oxide semiconductor, an Al-Ga-Zn-O-based oxide semiconductor layer, or a Sn-Al-Zn-O-based oxide semiconductor; an oxide of two metal elements, such as an In-Zn-O-based oxide semiconductor, a Sn-Zn-O-based oxide semiconductor, an Al-Zn-O-based oxide semiconductor, a Zn-Mg-O-based oxide semiconductor, a Sn-Mg-O-based oxide semiconductor, or an In-Mg-O-based oxide semiconductor; an In-O-based oxide semiconductor, a Sn-O-based oxide semiconductor, or a Zn-O-based oxide semiconductor can be used. Further, SiO₂ may be added to the oxide semiconductor. Here, for example, an In-Ga-Zn-O-based oxide semiconductor is an oxide including at

least In, Ga, and Zn, and there is no particular limitation on the composition ratio thereof. Furthermore, the In-Ga-Zn-O-based oxide semiconductor may contain an element other than In, Ga, and Zn.

[0116]

5 For the oxide semiconductor layer 403, an oxide semiconductor expressed by a chemical formula of $\text{InMO}_3(\text{ZnO})_m$ ($m > 0$) can be used. Here, M represents one or more metal elements selected from Ga, Al, Mn, or Co. For example, M can be Ga, Ga and Al, Ga and Mn, Ga and Co, or the like.

[0117]

10 The off-state current of the transistor 410, the transistor 420, the transistor 430, and the transistor 440 including the oxide semiconductor layer 403 can be markedly reduced. Thus, when such transistors are used in the pulse signal output circuit and the shift register, the potential of each node can be kept easily, so that the possibility of a malfunction of the pulse signal output circuit and the shift register can be markedly
15 lowered.

[0118]

There is no particular limitation on a substrate which can be used as the substrate 400 having an insulating surface. For example, a glass substrate, a quartz substrate, or the like used for a liquid crystal display device or the like can be used.
20 Alternatively, a substrate where an insulating layer is formed over a silicon wafer may be used, for example.

[0119]

In each of the bottom-gate transistors 410, 420, and 430, an insulating film serving as a base may be provided between the substrate and the gate electrode layer.
25 The insulating layer has a function of preventing diffusion of an impurity element from the substrate, and can be formed to have a single-layer structure or a layered structure including one or more films selected from a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, or a silicon oxynitride film.

[0120]

30 The gate electrode layer 401 can be formed using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material which includes any of these materials as a main

component. The gate electrode layer 401 may have a single-layer structure or a layered structure.

[0121]

The gate insulating layer 402 can be formed using one or more films selected from a silicon oxide film, a silicon nitride film, a silicon oxynitride film, a silicon nitride oxide film, an aluminum oxide film, an aluminum nitride film, an aluminum oxynitride film, an aluminum nitride oxide film, a hafnium oxide film, or the like by a plasma-enhanced CVD method, a sputtering method, or the like. For example, a gate insulating layer with a total thickness of about 300 nm can be formed in such a manner that a silicon nitride film (SiN_y ($y > 0$)) with a thickness of 50 to 200 nm is formed as a first gate insulating layer by plasma-enhanced CVD and a silicon oxide film (SiO_x ($x > 0$)) with a thickness of 5 to 300 nm is stacked over the first gate insulating layer as a second gate insulating layer by a sputtering method.

[0122]

The source electrode layer 405a and the drain electrode layer 405b can be formed using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material which includes any of these materials as a main component. For example, the source electrode layer 405a and the drain electrode layer 405b can have a layered structure of a metal layer including aluminum, copper, or the like and a refractory metal layer including titanium, molybdenum, tungsten, or the like. Heat resistance may be improved with the use of an aluminum material to which an element for preventing generation of hillocks and whiskers (e.g., silicon, neodymium, or scandium) is added.

[0123]

Alternatively, a conductive metal oxide film may be used as a conductive film serving as the source electrode layer 405a and the drain electrode layer 405b (including a wiring layer formed using the same layer as the source electrode layer 405a and the drain electrode layer 405b). Indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), an alloy of indium oxide and tin oxide ($\text{In}_2\text{O}_3\text{-SnO}_2$, which is abbreviated to ITO in some cases), an alloy of indium oxide and zinc oxide ($\text{In}_2\text{O}_3\text{-ZnO}$), any of these metal oxide materials including silicon oxide, or the like can be used as a conductive metal

oxide.

[0124]

The wiring layer 436a and the wiring layer 436b which are in contact with the source electrode layer 405a and the drain electrode layer 405b, respectively, can be formed using a material which is similar to that of the source electrode layer 405a and the drain electrode layer 405b.

[0125]

For each of the insulating layers 407, 427, and 437, an inorganic insulating film such as a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, or an aluminum oxynitride film can be used typically.

[0126]

For the protective insulating layer 409, an inorganic insulating film such as a silicon nitride film, an aluminum nitride film, a silicon nitride oxide film, or an aluminum nitride oxide film can be used.

[0127]

In addition, a planarization insulating film for reducing surface unevenness due to the transistor may be formed over the protective insulating layer 409. For the planarization insulating film, an organic material such as polyimide, acrylic, or benzocyclobutene can be used. Other than such an organic material, a low-dielectric constant material (a low-k material) or the like can be used. Note that the planarization insulating film may be formed by stacking a plurality of insulating films including these materials.

[0128]

As described above, the structures, methods, and the like described in this embodiment can be combined with any of the structures, methods, and the like described in the other embodiments as appropriate.

[0129]

(Embodiment 4)

In this embodiment, an example of a transistor including an oxide semiconductor layer and an example of a manufacturing method thereof will be described in detail with reference to FIGS. 12A to 12E.

[0130]

FIGS. 12A to 12E are cross-sectional views illustrating a manufacturing process of a transistor. A transistor 510 illustrated here is an inverted staggered transistor similar to the transistor 410 illustrated in FIG. 11A.

[0131]

5 An oxide semiconductor used for a semiconductor layer of this embodiment is an i-type (intrinsic) oxide semiconductor or a substantially i-type (intrinsic) oxide semiconductor. The i-type (intrinsic) oxide semiconductor or substantially i-type (intrinsic) oxide semiconductor is obtained in such a manner that hydrogen, which is an n-type impurity, is removed from an oxide semiconductor, and the oxide semiconductor
10 is purified so as to contain as few impurities that are not main components of the oxide semiconductor as possible.

[0132]

Note that the purified oxide semiconductor includes extremely few carriers, and the carrier concentration is lower than $1 \times 10^{14} / \text{cm}^3$, preferably lower than $1 \times 10^{12} / \text{cm}^3$, further preferably lower than $1 \times 10^{11} / \text{cm}^3$. Such few carriers enable a current in
15 an off state (off-state current) to be small enough.

[0133]

Specifically, in the transistor including the above-described oxide semiconductor layer, the off-state current density per $1 \mu\text{m}$ of channel width at room
20 temperature (25°C) can be $100 \text{ zA}/\mu\text{m}$ ($1 \times 10^{-19} \text{ A}/\mu\text{m}$) or lower, or further $10 \text{ zA}/\mu\text{m}$ ($1 \times 10^{-20} \text{ A}/\mu\text{m}$) or lower under conditions where the channel length L of the transistor is $10 \mu\text{m}$ and the source-drain voltage is 3 V .

[0134]

The transistor 510 including the purified oxide semiconductor layer hardly has
25 temperature dependence of an on-state current and also has an extremely small off-state current.

[0135]

A process for manufacturing the transistor 510 over a substrate 505 will be described with reference to FIGS. 12A to 12E.

30 [0136]

First, a conductive film is formed over the substrate 505 having an insulating

surface, and then a gate electrode layer 511 is formed through a first photolithography process. Note that a resist mask used in the photolithography process may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask; thus, manufacturing cost can be reduced.

5 [0137]

As the substrate 505 having an insulating surface, a substrate similar to the substrate 400 described in the above embodiment can be used. In this embodiment, a glass substrate is used as the substrate 505.

[0138]

10 An insulating layer serving as a base may be provided between the substrate 505 and the gate electrode layer 511. The insulating layer has a function of preventing diffusion of an impurity element from the substrate 505, and can be formed of one or more films selected from a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, a silicon oxynitride film, and the like.

15 [0139]

The gate electrode layer 511 can be formed using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material which includes any of these metal materials as a main component. The gate electrode layer 511 can have a single-layer structure or a stacked
20 structure.

[0140]

Next, a gate insulating layer 507 is formed over the gate electrode layer 511. The gate insulating layer 507 can be formed by a plasma-enhanced CVD method, a sputtering method, or the like. The gate insulating layer 507 can be formed of one or
25 more films selected from a silicon oxide film, a silicon nitride film, a silicon oxynitride film, a silicon nitride oxide film, an aluminum oxide film, an aluminum nitride film, an aluminum oxynitride film, an aluminum nitride oxide film, a hafnium oxide film, and the like.

[0141]

30 Further, in order that hydrogen, hydroxyl, and moisture are contained as little as possible in the gate insulating layer 507 and an oxide semiconductor film 530, it is preferable to preheat the substrate 505 over which the gate electrode layer 511 is formed

or the substrate 505 over which the gate electrode layer 511 and the gate insulating layer 507 are formed, in a preheating chamber of a sputtering apparatus as pretreatment for the formation of the oxide semiconductor film 530, so that impurities such as hydrogen and moisture adsorbed on the substrate 505 are eliminated. As an evacuation unit, a
5 cryopump is preferably provided for the preheating chamber. This preheating step may be performed on the substrate 505 over which layers up to and including a source electrode layer 515a and a drain electrode layer 515b are formed. Note that this preheating treatment can be omitted.

[0142]

10 Next, over the gate insulating layer 507, the oxide semiconductor film 530 with a thickness of greater than or equal to 2 nm and less than or equal to 200 nm, preferably greater than or equal to 5 nm and less than or equal to 30 nm is formed (see FIG. 12A).

[0143]

For the oxide semiconductor film 530, any of the four-component metal oxide,
15 the three-component metal oxides, the two-component metal oxides, an In-O-based oxide semiconductor, a Sn-O-based oxide semiconductor, a Zn-O-based oxide semiconductor, and the like, which are described in the above embodiment, can be used.

[0144]

As a target for forming the oxide semiconductor film 530 by a sputtering
20 method, it is particularly preferable to use a target having a composition ratio of In:Ga:Zn = 1:x:y (x is 0 or more and y is more than or equal to 0.5 and less than or equal to 5). For example, a target having a composition ratio of $\text{In}_2\text{O}_3:\text{Ga}_2\text{O}_3:\text{ZnO} = 1:1:2$ [molar ratio] can be used. Alternatively, a target having a composition ratio of $\text{In}_2\text{O}_3:\text{Ga}_2\text{O}_3:\text{ZnO} = 1:1:1$ [molar ratio], a target having a composition ratio of
25 $\text{In}_2\text{O}_3:\text{Ga}_2\text{O}_3:\text{ZnO} = 1:1:4$ [molar ratio], or a target having a composition ratio of $\text{In}_2\text{O}_3:\text{ZnO} = 1:2$ [molar ratio] can be used.

[0145]

In this embodiment, an oxide semiconductor layer having an amorphous structure is formed by a sputtering method using an In-Ga-Zn-O-based metal oxide
30 target.

[0146]

The relative density of a metal oxide in the metal oxide target is greater than or equal to 80 %, preferably greater than or equal to 95 %, and further preferably greater than or equal to 99.9 %. The use of a metal oxide target having high relative density makes it possible to form an oxide semiconductor layer with a dense structure.

5 [0147]

The atmosphere in which the oxide semiconductor film 530 is formed is preferably a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere containing a rare gas (typically, argon) and oxygen. Specifically, it is preferable to use, for example, an atmosphere of a high-purity gas from which an impurity such as hydrogen, water, hydroxyl, or hydride is removed so that the impurity concentration is 1 ppm or lower (preferably the impurity concentration is 10 ppb or lower).

[0148]

In the formation of the oxide semiconductor film 530, for example, a process object is held in a treatment chamber that is kept under reduced pressure and the process object may be heated so that the temperature of the process object is higher than or equal to 100 °C and lower than 550 °C, preferably higher than or equal to 200 °C and lower than or equal to 400 °C. Alternatively, the temperature of the process object in the formation of the oxide semiconductor film 530 may be room temperature (25 °C ± 10 °C). Then, a sputtering gas from which hydrogen, water, and the like are removed is introduced while moisture in the treatment chamber is removed, and the aforementioned target is used, whereby the oxide semiconductor film 530 is formed. The oxide semiconductor film 530 is formed while the process object is heated, so that impurities contained in the oxide semiconductor layer can be reduced. Further, damage due to sputtering can be reduced. In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, a titanium sublimation pump, or the like can be used. Alternatively, a turbo molecular pump provided with a cold trap may be used. By evacuation with the cryopump or the like, hydrogen, water, and the like can be removed from the treatment chamber, whereby the impurity concentration in the oxide semiconductor film 530 can be reduced.

[0149]

The oxide semiconductor film 530 can be formed under the following conditions, for example: the distance between the process object and the target is 170 mm, the pressure is 0.4 Pa, the direct-current (DC) power is 0.5 kW, and the atmosphere is an oxygen atmosphere (the proportion of oxygen is 100 %), an argon atmosphere (the proportion of argon is 100 %), or a mixed atmosphere including oxygen and argon. A pulse-direct current (DC) power source is preferably used because powder substances (also referred to as particles or dust) generated in the film formation can be reduced and the film thickness can be uniform. The thickness of the oxide semiconductor film 530 is greater than or equal to 1 nm and less than or equal to 50 nm, preferably greater than or equal to 1 nm and less than or equal to 30 nm, more preferably greater than or equal to 1 nm and less than or equal to 10 nm. With the oxide semiconductor film 530 having such a thickness, a short-channel effect due to miniaturization can be suppressed. Note that the appropriate thickness differs depending on the oxide semiconductor material to be used, the intended use of the semiconductor device, and the like; therefore, the thickness may be determined in accordance with the material, the intended use, and the like.

[0150]

Note that before the oxide semiconductor film 530 is formed by a sputtering method, a substance attached to a surface where the oxide semiconductor film 530 is to be formed (e.g., a surface of the gate insulating layer 507) is preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated. Here, the reverse sputtering is a method in which ions collide with a process surface so that the surface is modified, in contrast to normal sputtering in which ions collide with a sputtering target. As an example of a method for making ions collide with a process surface, there is a method in which high-frequency voltage is applied to the process surface in an argon atmosphere so that plasma is generated in the vicinity of the process object. Note that an atmosphere of nitrogen, helium, oxygen, or the like may be used instead of an argon atmosphere.

[0151]

Next, the oxide semiconductor film 530 is processed into an island-shaped

oxide semiconductor layer through a second photolithography process. Note that a resist mask used in the photolithography process may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask; thus, manufacturing cost can be reduced.

5 [0152]

In the case where a contact hole is formed in the gate insulating layer 507, a step of forming the contact hole can be performed at the same time as processing of the oxide semiconductor film 530.

[0153]

10 As the etching of the oxide semiconductor film 530, either wet etching or dry etching or both of them may be employed. As an etchant used for wet etching of the oxide semiconductor film 530, a solution obtained by mixing phosphoric acid, acetic acid, and nitric acid or the like can be used. An etchant such as ITO-07N (produced by KANTO CHEMICAL CO., INC.) may also be used.

15 [0154]

Then, heat treatment (first heat treatment) is performed on the oxide semiconductor layer, so that an oxide semiconductor layer 531 is formed (see FIG. 12B). By the first heat treatment, excessive hydrogen (including water and hydroxyl) in the oxide semiconductor layer is removed and a structure of the oxide semiconductor layer is improved, so that defect level in energy gap can be reduced. The temperature of the first heat treatment is, for example, higher than or equal to 300 °C and lower than 20 550 °C, or higher than or equal to 400 °C and lower than or equal to 500 °C.

[0155]

The heat treatment can be performed in such a way that, for example, a process object is introduced into an electric furnace in which a resistance heating element or the like is used and heated at 450 °C under a nitrogen atmosphere for an hour. During the heat treatment, the oxide semiconductor layer is not exposed to the air, in order to prevent contamination by water and hydrogen.

[0156]

30 The heat treatment apparatus is not limited to an electric furnace; the heat treatment apparatus can be an apparatus that heats a process object using thermal

conduction or thermal radiation from a medium such as a heated gas or the like. For example, an RTA (rapid thermal annealing) apparatus such as a GRTA (gas rapid thermal annealing) apparatus or an LRTA (lamp rapid thermal annealing) apparatus can be used. An LRTA apparatus is an apparatus for heating a process object using radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high-pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas. As the gas, an inert gas which does not react with a process object by heat treatment, such as nitrogen or a rare gas such as argon is used.

[0157]

For example, as the first heat treatment, GRTA treatment may be performed in the following manner. The process object is put in an inert gas atmosphere that has been heated, heated for several minutes, and then taken out of the inert gas atmosphere. The GRTA treatment enables high-temperature heat treatment in a short time. Moreover, in the GRTA treatment, even conditions of the temperature that exceeds the upper temperature limit of the process object can be employed. Note that the inert gas may be changed to a gas including oxygen during the process. This is because defect levels in the energy gap due to oxygen deficiency can be reduced by performing the first heat treatment in an atmosphere including oxygen.

[0158]

Note that as the inert gas atmosphere, an atmosphere that contains nitrogen or a rare gas (e.g., helium, neon, or argon) as its main component and does not contain water, hydrogen, or the like is preferably used. For example, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into a heat treatment apparatus is set to 6N (99.9999 %) or more, preferably 7N (99.99999 %) or more (i.e., the impurity concentration is 1 ppm or less, preferably 0.1 ppm or less).

[0159]

In any case, impurities are reduced by the first heat treatment so that the i-type (intrinsic) or substantially i-type oxide semiconductor layer is obtained. Accordingly, a transistor having excellent characteristics can be realized.

[0160]

The above heat treatment (first heat treatment) has an effect of removing hydrogen, water, and the like and thus can be referred to as dehydration treatment, dehydrogenation treatment, or the like. The dehydration treatment or the dehydrogenation treatment can be performed after the formation of the oxide semiconductor film 530 and before the oxide semiconductor film 530 is processed into the island-shaped oxide semiconductor layer. Such dehydration treatment or dehydrogenation treatment may be performed once or more times.

[0161]

The first heat treatment can be performed at any of the following timings instead of the above timing: after formation of a source electrode layer and a drain electrode layer, after formation of an insulating layer over the source electrode layer and the drain electrode layer, and the like.

[0162]

Next, a conductive film to be a source electrode layer and a drain electrode layer (including a wiring formed from the same layer as the source electrode layer and the drain electrode layer) is formed over the gate insulating layer 507 and the oxide semiconductor layer 531. The conductive film used to form the source electrode layer and the drain electrode layer can be formed using any of the materials described in the above embodiment.

[0163]

A resist mask is formed over the conductive film in a third photolithography process, and the source electrode layer 515a and the drain electrode layer 515b are formed by selective etching, and then, the resist mask is removed (see FIG. 12C).

[0164]

Light exposure at the time of formation of the resist mask in the third photolithography process may be performed using ultraviolet light, KrF laser light, or ArF laser light. Note that the channel length (L) of the transistor is determined by the distance between the source electrode layer and the drain electrode layer. Therefore, in light exposure for forming a mask for a transistor with a channel length (L) of less than 25 nm, it is preferable to use extreme ultraviolet light whose wavelength is as short as several nanometers to several tens of nanometers. In light exposure using extreme ultraviolet light, resolution is high and depth of focus is large. For these reasons, the

channel length (L) of the transistor completed later can be greater than or equal to 10 nm and less than or equal to 1000 nm (1 μm), and the circuit can operate at high speed. Moreover, power consumption of the semiconductor device can be reduced by miniaturization.

5 [0165]

In order to reduce the number of photomasks and the number of photolithography processes, the etching step may be performed using a resist mask formed with a multi-tone mask. Since a resist mask formed with a multi-tone mask includes regions of plural thicknesses and can be further changed in shape by performing etching, the resist mask can be used in a plurality of etching steps to provide different patterns. Therefore, a resist mask corresponding to at least two kinds of different patterns can be formed with one multi-tone mask. Thus, the number of light-exposure masks can be reduced and the number of corresponding photolithography processes can also be reduced, whereby simplification of the process can be realized.

15 [0166]

Note that it is preferable that etching conditions be optimized so as not to etch and divide the oxide semiconductor layer 531 when the conductive film is etched. However, it is difficult to obtain etching conditions in which only the conductive film is etched and the oxide semiconductor layer 531 is not etched at all. In some cases, part of the oxide semiconductor layer 531 is etched when the conductive film is etched, whereby the oxide semiconductor layer 531 having a groove portion (a recessed portion) is formed.

20 [0167]

25 Either wet etching or dry etching may be used for the etching of the conductive film. Note that dry etching is preferably used in terms of miniaturization of elements. An etching gas and an etchant can be selected as appropriate in accordance with a material to be etched. In this embodiment, a titanium film is used as the conductive film and an In-Ga-Zn-O based material is used for the oxide semiconductor layer 531; accordingly, in the case of employing wet etching, ammonia hydrogen peroxide (a mixed solution of ammonia, water, and hydrogen peroxide) is used as an etchant.

30 [0168]

Next, plasma treatment using a gas such as N_2O , N_2 , or Ar is preferably performed, so that water, hydrogen, or the like attached to a surface of an exposed portion of the oxide semiconductor layer may be removed. In the case of performing the plasma treatment, an insulating layer 516 serving as a protective insulating film is formed without the oxide semiconductor layer being exposed to the air after the plasma treatment.

[0169]

The insulating layer 516 is preferably formed to a thickness of at least 1 nm by a method through which an impurity such as water or hydrogen is not introduced into the insulating layer 516, such as a sputtering method. When hydrogen is contained in the insulating layer 516, entry of the hydrogen to the oxide semiconductor layer, or extraction of oxygen in the oxide semiconductor layer by the hydrogen is caused, thereby causing the backchannel of the oxide semiconductor layer to have lower resistance (to have an n-type conductivity), so that a parasitic channel may be formed. As the insulating layer 516, a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, or the like is preferably used.

[0170]

In this embodiment, a silicon oxide film is formed to a thickness of 200 nm by a sputtering method as the insulating layer 516. The substrate temperature in deposition may be higher than or equal to room temperature (25 °C) and lower than or equal to 300 °C, and is 100 °C in this embodiment. The silicon oxide film can be deposited by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere containing a rare gas and oxygen. As a target, a silicon oxide target or a silicon target may be used.

[0171]

In order to remove moisture remaining in the deposition chamber of the insulating layer 516 at the same time as deposition of the oxide semiconductor film 530, an entrapment vacuum pump (such as a cryopump) is preferably used. When the insulating layer 516 is deposited in the deposition chamber which is evacuated using a cryopump, the impurity concentration in the insulating layer 516 can be reduced. A turbo molecular pump provided with a cold trap may be used as an evacuation unit for

removing moisture remaining in the deposition chamber used for forming the insulating layer 516.

[0172]

A sputtering gas used for forming the insulating layer 516 is preferably a high-purity gas from which an impurity such as hydrogen or water is removed.

[0173]

Next, second heat treatment is performed in an inert gas atmosphere or an oxygen gas atmosphere. The second heat treatment is performed at a temperature higher than or equal to 200 °C and lower than or equal to 450 °C, preferably higher than or equal to 250 °C and lower than or equal to 350 °C. For example, the heat treatment may be performed at 250 °C for 1 hour in a nitrogen atmosphere. The second heat treatment can reduce variation in electric characteristics of the transistor. By supply of oxygen from the insulating layer 516 to the oxide semiconductor layer 531, an oxygen vacancy in the oxide semiconductor layer 531 is reduced, whereby an i-type (intrinsic) or substantially i-type oxide semiconductor layer can be formed.

[0174]

In this embodiment, the second heat treatment is performed after the formation of the insulating layer 516; however, the timing of the second heat treatment is not limited thereto. For example, the first heat treatment and the second heat treatment may be successively performed, or the first heat treatment may double as the second heat treatment.

[0175]

In the above-described manner, through the first heat treatment and the second heat treatment, the oxide semiconductor layer 531 is purified so as to contain as few impurities that are not main components of the oxide semiconductor layer as possible, whereby the oxide semiconductor layer 531 can become an i-type (intrinsic) oxide semiconductor layer.

[0176]

Through the above-described process, the transistor 510 is formed (see FIG. 12D).

[0177]

It is preferable to further form a protective insulating layer 506 over the insulating layer 516 (see FIG. 12E). The protective insulating layer 506 prevents entry of hydrogen, water, and the like from the outside. As the protective insulating layer 506, a silicon nitride film, an aluminum nitride film, or the like can be used, for example. The formation method of the protective insulating layer 506 is not particularly limited; however, an RF sputtering method is suitable for forming the protective insulating layer 506 because it achieves high productivity.

[0178]

After the formation of the protective insulating layer 506, heat treatment may be further performed at a temperature higher than or equal to 100 °C and lower than or equal to 200 °C for 1 hour to 30 hours in the air.

[0179]

A transistor which includes a purified oxide semiconductor layer and is manufactured in accordance with this embodiment as described above has a characteristic of significantly small off-state current. Therefore, with the use of such a transistor, the potential of a node can be easily kept. The use of such a transistor for a pulse signal output circuit and a shift register can significantly reduce the probability of causing a malfunction of the pulse signal output circuit and the shift register.

[0180]

As described above, the structures, methods, and the like described in this embodiment can be combined with any of the structures, methods, and the like described in the other embodiments as appropriate.

[0181]

(Embodiment 5)

With the use of the shift register whose example is illustrated in Embodiment 1 or Embodiment 2, a semiconductor device having a display function (also referred to as a display device) can be manufactured. Further, part or whole of a driver circuit can be formed over the same substrate as a pixel portion, whereby a system-on-panel can be obtained.

[0182]

As a display element used for the display device, a liquid crystal element (also

referred to as a liquid crystal display element) or a light-emitting element (also referred to as a light-emitting display element) can be used. The light-emitting element includes, in its category, an element whose luminance is controlled by a current or a voltage, and specifically includes, in its category, an inorganic electroluminescent (EL) element, an organic EL element, and the like. Furthermore, a display medium whose contrast is changed by an electric effect, such as electronic ink, can be used.

[0183]

In FIG. 13A, a sealant 4005 is provided so as to surround a pixel portion 4002 provided over a first substrate 4001, and the pixel portion 4002 is sealed between the first substrate 4001 and a second substrate 4006. In FIG. 13A, a scan line driver circuit 4004 and a signal line driver circuit 4003 which are formed over a substrate separately prepared are mounted in a region which is not included in a region surrounded by the sealant 4005 over the first substrate 4001. Further, a variety of signals and potentials are supplied to the signal line driver circuit 4003 which is separately formed, and the scan line driver circuit 4004 or the pixel portion 4002 from flexible printed circuits (FPCs) 4018a and 4018b.

[0184]

In FIGS. 13B and 13C, the sealant 4005 is provided so as to surround the pixel portion 4002 and the scan line driver circuit 4004 which are provided over the first substrate 4001. The second substrate 4006 is provided over the pixel portion 4002 and the scan line driver circuit 4004. Consequently, the pixel portion 4002 and the scan line driver circuit 4004 are sealed together with the display element by the first substrate 4001, the sealant 4005, and the second substrate 4006. In FIGS. 13B and 13C, the signal line driver circuit 4003 which is formed over a substrate separately prepared is mounted in a region which is different from a region surrounded by the sealant 4005 over the first substrate 4001. In FIGS. 13B and 13C, a variety of signals and potentials are supplied to the signal line driver circuit 4003 which is separately formed, and the scan line driver circuit 4004 or the pixel portion 4002 from an FPC 4018.

[0185]

Although FIGS. 13B and 13C each illustrate an example in which the signal line driver circuit 4003 is formed separately and mounted on the first substrate 4001, the present invention is not limited to this structure. The scan line driver circuit may be

separately formed and then mounted, or only part of the signal line driver circuit or part of the scan line driver circuit may be separately formed and then mounted.

[0186]

Note that a connection method of a separately formed driver circuit is not particularly limited, and a chip on glass (COG) method, a wire bonding method, a tape automated bonding (TAB) method, or the like can be used. FIG. 13A illustrates an example in which the signal line driver circuit 4003 and the scan line driver circuit 4004 are mounted by a COG method. FIG. 13B illustrates an example in which the signal line driver circuit 4003 is mounted by a COG method. FIG. 13C illustrates an example in which the signal line driver circuit 4003 is mounted by a TAB method.

[0187]

In addition, the display device includes a panel in which the display element is sealed, and a module in which an IC or the like including a controller is mounted on the panel.

[0188]

Note that a display device in this specification means an image display device, a display device, or a light source (including a lighting device). Furthermore, the display device also includes the following modules in its category: a module to which a connector such as an FPC, a TAB tape, or a TCP is attached; a module having a TAB tape or a TCP at the tip of which a printed wiring board is provided; and a module in which an integrated circuit (IC) is directly mounted on a display element by a COG method.

[0189]

Further, the pixel portion provided over the first substrate includes a plurality of transistors, and the transistors which are illustrated in the aforementioned embodiment as an example can be used for the transistors.

[0190]

In the case where a liquid crystal element is used as the display element, a thermotropic liquid crystal, a low-molecular liquid crystal, a high-molecular liquid crystal, a polymer dispersed liquid crystal, a ferroelectric liquid crystal, an anti-ferroelectric liquid crystal, or the like is used. These liquid crystal materials exhibit a cholesteric phase, a smectic phase, a cubic phase, a chiral nematic phase, an

isotropic phase, or the like depending on conditions.

[0191]

Alternatively, liquid crystal exhibiting a blue phase for which an alignment film is unnecessary may be used. A blue phase is one of liquid crystal phases, which is generated just before a cholesteric phase changes into an isotropic phase while temperature of cholesteric liquid crystal is increased. Since the blue phase appears only in a narrow temperature range, a liquid crystal composition in which several weight percent or more of a chiral agent is mixed is used for a liquid crystal layer in order to improve the temperature range. The liquid crystal composition which includes a liquid crystal showing a blue phase and a chiral agent has a short response time of 1 msec or less, has optical isotropy, which makes the alignment process unneeded, and has a small viewing angle dependence. In addition, an alignment film does not need to be provided and thus rubbing treatment is not necessary. Therefore, electrostatic discharge damage caused by the rubbing treatment can be prevented and defects and damage of the liquid crystal display device in the manufacturing process can be reduced. Thus, productivity of the liquid crystal display device can be increased.

[0192]

The specific resistivity of the liquid crystal material is greater than or equal to $1 \times 10^9 \Omega \cdot \text{cm}$, preferably greater than or equal to $1 \times 10^{11} \Omega \cdot \text{cm}$, still preferably greater than or equal to $1 \times 10^{12} \Omega \cdot \text{cm}$. Note that the specific resistance in this specification is measured at 20 °C.

[0193]

The size of a storage capacitor formed in the liquid crystal display device is set considering the leakage current of the transistor provided in the pixel portion or the like so that charge can be held for a predetermined period. The size of the storage capacitor may be set considering the off-state current of a transistor or the like.

[0194]

For the liquid crystal display device, a twisted nematic (TN) mode, an in-plane-switching (IPS) mode, a fringe field switching (FFS) mode, an axially symmetric aligned micro-cell (ASM) mode, an optically compensated birefringence (OCB) mode, a ferroelectric liquid crystal (FLC) mode, an antiferroelectric liquid

crystal (AFLC) mode, or the like is used.

[0195]

A normally black liquid crystal display device such as a transmissive liquid crystal display device utilizing a vertical alignment (VA) mode is preferable. Some
5 examples are given as a vertical alignment mode. For example, an MVA (multi-domain vertical alignment) mode, a PVA (patterned vertical alignment) mode, an ASV mode, or the like can be employed.

[0196]

Furthermore, the present invention can be applied to a VA liquid crystal display
10 device. The VA liquid crystal display device has a kind of form in which alignment of liquid crystal molecules of a liquid crystal display panel is controlled. In the VA liquid crystal display device, liquid crystal molecules are aligned in a vertical direction with respect to a panel surface when no voltage is applied. Moreover, it is possible to use a method called domain multiplication or multi-domain design, in which a pixel is
15 divided into some regions (subpixels) and molecules are aligned in different directions in their respective regions.

[0197]

In the display device, a black matrix (a light-blocking layer), an optical element (an optical substrate) such as a polarizing element, a retardation element, or an
20 anti-reflection element, and the like are provided as appropriate. For example, circular polarization may be obtained by using a polarizing substrate and a retardation substrate. In addition, a backlight, a side light, or the like may be used as a light source.

[0198]

As a display method in the pixel portion, a progressive method, an interlace
25 method, or the like can be employed. Further, color elements controlled in a pixel at the time of color display are not limited to three colors: R, G, and B (R, G, and B correspond to red, green, and blue, respectively). For example, R, G, B, and W (W corresponds to white); R, G, B, and one or more of yellow, cyan, magenta, and the like; or the like can be used. Further, the sizes of display regions may be different between
30 respective dots of color elements. Note that the disclosed invention is not limited to the application to a display device for color display; the disclosed invention can also be applied to a display device for monochrome display.

[0199]

Alternatively, as the display element included in the display device, a light-emitting element utilizing electroluminescence can be used. Light-emitting elements utilizing electroluminescence are classified according to whether a light-emitting material is an organic compound or an inorganic compound. In general, the former is referred to as an organic EL element, and the latter is referred to as an inorganic EL element.

[0200]

In an organic EL element, by application of voltage to a light-emitting element, electrons and holes are separately injected from a pair of electrodes into a layer containing a light-emitting organic compound, and current flows. The carriers (electrons and holes) are recombined, and thus, the light-emitting organic compound is excited. The light-emitting organic compound returns to a ground state from the excited state, thereby emitting light. Because of such a mechanism, the light-emitting element is called a current-excitation light-emitting element.

[0201]

The inorganic EL elements are classified according to their element structures into a dispersion-type inorganic EL element and a thin-film inorganic EL element. A dispersion-type inorganic EL element has a light-emitting layer where particles of a light-emitting material are dispersed in a binder, and its light emission mechanism is donor-acceptor recombination type light emission that utilizes a donor level and an acceptor level. A thin-film inorganic EL element has a structure where a light-emitting layer is sandwiched between dielectric layers, which are further sandwiched between electrodes, and its light emission mechanism is localized type light emission that utilizes inner-shell electron transition of metal ions.

[0202]

Further, an electronic paper in which electronic ink is driven can be provided as the display device. The electronic paper is also called an electrophoretic display device (electrophoretic display) and has advantages in that it has the same level of readability as regular paper, it has less power consumption than other display devices, and it can be set to have a thin and light form.

[0203]

An electrophoretic display device can have various modes. An electrophoretic display device contains a plurality of microcapsules dispersed in a solvent or a solute, each microcapsule containing first particles which are positively charged and second particles which are negatively charged. By applying an electric field to the microcapsules, the particles in the microcapsules move in opposite directions to each other and only the color of the particles gathering on one side is displayed. Note that the first particles and the second particles each contain pigment and do not move without an electric field. Moreover, the first particles and the second particles have different colors (which may be colorless).

[0204]

Thus, an electrophoretic display device is a display device that utilizes a so-called dielectrophoretic effect by which a substance having a high dielectric constant moves to a high-electric field region.

[0205]

A solution in which the above microcapsules are dispersed in a solvent is referred to as electronic ink. This electronic ink can be printed on a surface of glass, plastic, cloth, paper, or the like. Furthermore, by using a color filter or particles that have a pigment, color display can also be achieved.

[0206]

Note that the first particles and the second particles in the microcapsules may each be formed using a single material selected from a conductive material, an insulating material, a semiconductor material, a magnetic material, a liquid crystal material, a ferroelectric material, an electroluminescent material, an electrochromic material, or a magnetophoretic material or formed using a composite material of any of these.

[0207]

As the electronic paper, a display device using a twisting ball display system can be used. The twisting ball display system refers to a method in which spherical particles each colored in black and white are arranged between a first electrode layer and a second electrode layer which are electrode layers used for a display element, and a potential difference is generated between the first electrode layer and the second electrode layer to control alignment of the spherical particles, so that display is

performed.

[0208]

The pulse signal output circuit illustrated in Embodiment 1 or Embodiment 2 is used for the display device whose example is illustrated as above, whereby the display device can have a variety of functions.

[0209]

As described above, the structures, methods, and the like described in this embodiment can be combined with any of the structures, methods, and the like described in the other embodiments as appropriate.

[0210]

(Embodiment 6)

A semiconductor device disclosed in this specification can be used in a variety of electronic devices (including game machines). Examples of electronic devices are a television set (also referred to as a television or a television receiver), a monitor of a computer or the like, a camera such as a digital camera or a digital video camera, a digital photo frame, a cellular phone handset (also referred to as a cellular phone or a cellular phone device), a portable game machine, a personal digital assistant, an audio reproducing device, a large game machine such as a pinball machine, and the like.

[0211]

FIG. 14A illustrates a laptop personal computer which includes at least the semiconductor device disclosed in this specification as a component. The laptop personal computer includes a main body 3001, a housing 3002, a display portion 3003, a keyboard 3004, and the like.

[0212]

FIG. 14B illustrates a personal digital assistant (PDA) which includes at least the semiconductor device disclosed in this specification as a component. The personal digital assistant includes a display portion 3023, an external interface 3025, operation buttons 3024, and the like in a main body 3021. A stylus 3022 is included as an accessory for operation.

[0213]

The semiconductor device disclosed in this specification can be used as electronic paper. FIG. 14C illustrates an e-book reader which includes the electronic

paper as a component. FIG. 14C illustrates an example of the e-book reader. For example, an e-book reader 2700 includes two housings 2701 and 2703. The housings 2701 and 2703 are combined with each other with a hinge 2711 so that the e-book reader 2700 can be opened and closed with the hinge 2711 used as an axis. With such a structure, the e-book reader 2700 can operate like a paper book.

[0214]

A display portion 2705 and a display portion 2707 are incorporated in the housing 2701 and the housing 2703, respectively. The display portion 2705 and the display portion 2707 may display one image or different images. In the case where the display portion 2705 and the display portion 2707 display different images, for example, a display portion on the right side (the display portion 2705 in FIG. 14C) can display text and a display portion on the left side (the display portion 2707 in FIG. 14C) can display images.

[0215]

FIG. 14C illustrates an example in which the housing 2701 includes an operation portion and the like. For example, the housing 2701 includes a power switch 2721, operation keys 2723, a speaker 2725, and the like. With the operation key 2723, pages can be turned. Note that a keyboard, a pointing device, or the like may be provided on the same surface as the display portion of the housing. Further, an external connection terminal (e.g., an earphone terminal or a USB terminal), a recording medium insertion portion, and the like may be provided on a back surface or a side surface of the housing. Furthermore, the e-book reader 2700 may function as an electronic dictionary.

[0216]

Further, the e-book reader 2700 may transmit and receive data wirelessly. Through wireless communication, desired book data or the like can be purchased and downloaded from an electronic book server.

[0217]

FIG. 14D illustrates a cellular phone which includes at least the semiconductor device disclosed in this specification as a component. The cellular phone includes two housings 2800 and 2801. The housing 2801 includes a display panel 2802, a speaker 2803, a microphone 2804, a pointing device 2806, a camera lens 2807, an external

connection terminal 2808, and the like. In addition, the housing 2800 includes a solar cell 2810 for storing electricity in a personal digital assistant, an external memory slot 2811, and the like. Further, an antenna is incorporated in the housing 2801.

[0218]

5 Further, the display panel 2802 includes a touch panel. A plurality of operation keys 2805 which are displayed as images are indicated by dashed lines in FIG. 14D. Note that the cellular phone includes a DC-DC converter for raising voltage output from the solar cell 2810 to voltage needed in each circuit.

[0219]

10 The display direction of the display panel 2802 is changed as appropriate depending on a usage pattern. Further, since the cellular phone includes the camera lens 2807 on the same surface as the display panel 2802, it can be used as a video phone. The speaker 2803 and the microphone 2804 can be used for videophone calls, recording, playback, and the like as well as voice calls. Furthermore, the housings 2800 and 2801
15 which are developed as illustrated in FIG. 14D can overlap with each other by sliding; thus, the size of the cellular phone can be decreased, which makes the cellular phone suitable for being carried.

[0220]

The external connection terminal 2808 can be connected to an AC adapter and
20 a variety of cables such as a USB cable, and charging and data communication with a personal computer or the like are possible. Further, a large amount of data can be stored and moved by insertion of a storage medium into the external memory slot 2811.

[0221]

Further, the cellular phone may have an infrared communication function, a
25 television reception function, or the like in addition to the above functions.

[0222]

FIG. 14E illustrates a digital video camera which includes at least the semiconductor device disclosed in this specification as a component. The digital video camera includes a main body 3051, a first display portion 3057, an eye piece portion
30 3053, operation switches 3054, a second display portion 3055, a battery 3056, and the like.

[0223]

FIG. 14F illustrates an example of a television set which includes at least the semiconductor device disclosed in this specification as a component. In a television set 9600, a display portion 9603 is incorporated in a housing 9601. The display portion 9603 can display images. Here, the housing 9601 is supported by a stand 9605.

[0224]

The television set 9600 can be operated by an operation switch of the housing 9601 or a remote control. Further, the remote control may include a display portion for displaying data output from the remote control.

[0225]

Note that the television set 9600 includes a receiver, a modem, and the like. With the receiver, general television broadcasts can be received. Further, when the television set is connected to a communication network with or without wires via the modem, one-way (from a transmitter to a receiver) or two-way (between a transmitter and a receiver or between receivers) data communication can be performed.

[0226]

As described above, the structures, methods, and the like described in this embodiment can be combined with any of the structures, methods, and the like described in the other embodiments as appropriate.

This application is based on Japanese Patent Application serial no. 2010-044949 filed with Japan Patent Office on March 2, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A pulse signal output circuit comprising:

a first transistor and a second transistor, a first terminal of the first transistor and a first terminal of the second transistor being electrically connected to a first output
5 terminal;

a third transistor and a fourth transistor, a first terminal of the third transistor and a first terminal of the fourth transistor being electrically connected to a second output terminal;

a fifth transistor; and

10 a sixth transistor,

wherein a first terminal of the fifth transistor, a gate of the first transistor and a gate of the third transistor are electrically connected to each other;

wherein a gate of the fifth transistor, a first terminal of the sixth transistor, a gate of the second transistor and a gate of the fourth transistor are electrically connected
15 to each other; and

wherein a channel of the fifth transistor and a channel of the sixth transistor are each longer than a channel of the third transistor and a channel of the fourth transistor.

2. A pulse signal output circuit comprising:

20 a first transistor and a second transistor, a first terminal of the first transistor and a first terminal of the second transistor being electrically connected to a first output terminal;

a third transistor and a fourth transistor, a first terminal of the third transistor and a first terminal of the fourth transistor being electrically connected to a second
25 output terminal;

a first input signal generation circuit comprising a fifth transistor; and

a second input signal generation circuit comprising a sixth transistor,

wherein a first terminal of the fifth transistor, a gate of the first transistor and a gate of the third transistor are electrically connected to each other;

30 wherein a gate of the fifth transistor, a first terminal of the sixth transistor, a gate of the second transistor and a gate of the fourth transistor are electrically connected to each other; and

wherein a channel of the fifth transistor and a channel of the sixth transistor are each longer than a channel of the third transistor and a channel of the fourth transistor.

3. A pulse signal output circuit according to claim 2, wherein a second terminal
5 of the fifth transistor and a second terminal of the sixth transistor are electrically connected to a power supply line.

4. A pulse signal output circuit according to claim 2, further comprising a
10 capacitor electrically connected between the gate and a second terminal of the second transistor.

5. A pulse signal output circuit according to claim 2, wherein any one of the
15 fifth transistor and the sixth transistor is a transistor having a multi-gate structure where at least two gates are arranged in series.

6. A pulse signal output circuit according to claim 2, wherein any one of the
transistors includes an oxide semiconductor.

7. A shift register circuit including a pulse signal output circuit according to
20 claim 2.

8. An electronic device including a pulse signal output circuit according to
claim 2.

25 9. A pulse signal output circuit comprising:
a first transistor and a second transistor, a first terminal of the first transistor
and a first terminal of the second transistor being electrically connected to a first output
terminal;

30 a third transistor and a fourth transistor, a first terminal of the third transistor
and a first terminal of the fourth transistor being electrically connected to a second
output terminal;

a first input signal generation circuit comprising a fifth transistor and a sixth

transistor; and

a second input signal generation circuit comprising a seventh transistor, an eighth transistor and a ninth transistor,

5 wherein a first terminal of the fifth transistor, a first terminal of the sixth transistor, a gate of the first transistor and a gate of the third transistor are electrically connected to each other;

10 wherein a gate of the sixth transistor, a first terminal of the seventh transistor, a first terminal of the eighth transistor, a first terminal of the ninth transistor, a gate of the second transistor and a gate of the fourth transistor are electrically connected to each other; and

wherein a channel of the sixth transistor and a channel of the ninth transistor are each longer than a channel of the third transistor and a channel of the fourth transistor.

15 10. A pulse signal output circuit according to claim 9,

wherein a first power supply line is electrically connected to a second terminal of the fifth transistor, a second terminal of the seventh transistor and a second terminal of the eighth transistor;

20 wherein a second power supply line is electrically connected to a second terminal of the sixth transistor, a second terminal of the ninth transistor, a second terminal of the second transistor and a second terminal of the fourth transistor;

wherein a pulse signal line is electrically connected to a gate of the fifth transistor and a gate of the ninth transistor;

25 wherein a first clock signal line is electrically connected to a second terminal of the first transistor and a second terminal of the third transistor;

wherein a second clock signal line is electrically connected to a gate of the eighth transistor; and

wherein an input line is electrically connected to a gate of the seventh transistor.

30

11. A pulse signal output circuit according to claim 9, further comprising a tenth transistor configured to control an electrical connection of the first terminal of the

fifth transistor and the first terminal of the sixth transistor to the gate of the first transistor and the gate of the third transistor,

wherein a gate of the tenth transistor is electrically connected a second terminal of the fifth transistor.

5

12. A pulse signal output circuit according to claim 9, further comprising an eleventh transistor having a first terminal electrically connected to a second terminal of the eighth transistor,

10 wherein a gate of the eleventh transistor is electrically connected to a clock signal line.

13. A pulse signal output circuit according to claim 9, further comprising a capacitor electrically connected between the gate and a second terminal of the second transistor.

15

14. A pulse signal output circuit according to claim 9, wherein any one of the sixth transistor and the ninth transistor is a transistor having a multi-gate structure where at least two gates are arranged in series.

20 15. A pulse signal output circuit according to claim 9, wherein any one of the transistors includes an oxide semiconductor.

16. A shift register circuit including a pulse signal output circuit according to claim 9.

25

17. An electronic device including a pulse signal output circuit according to claim 9.

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FIG. 1A

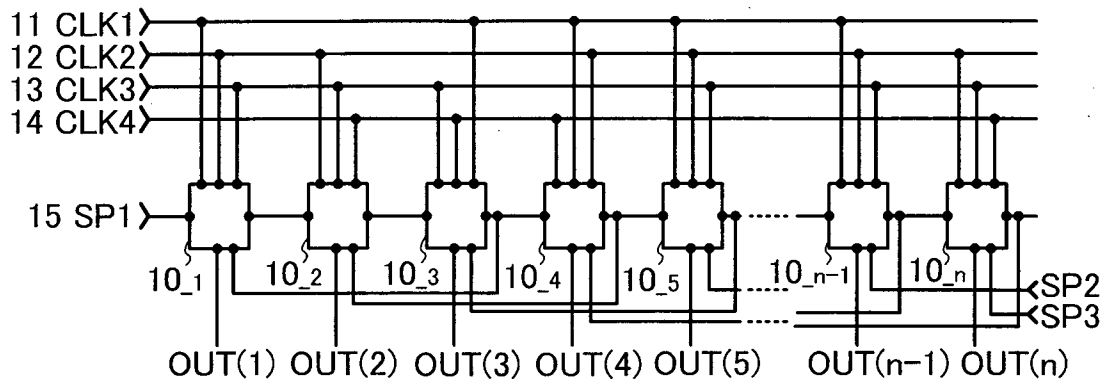


FIG. 1B

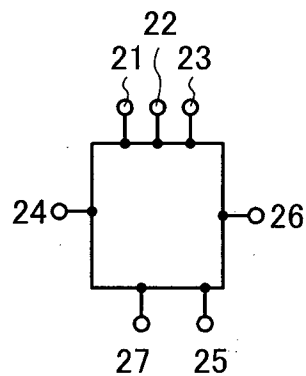


FIG. 1C

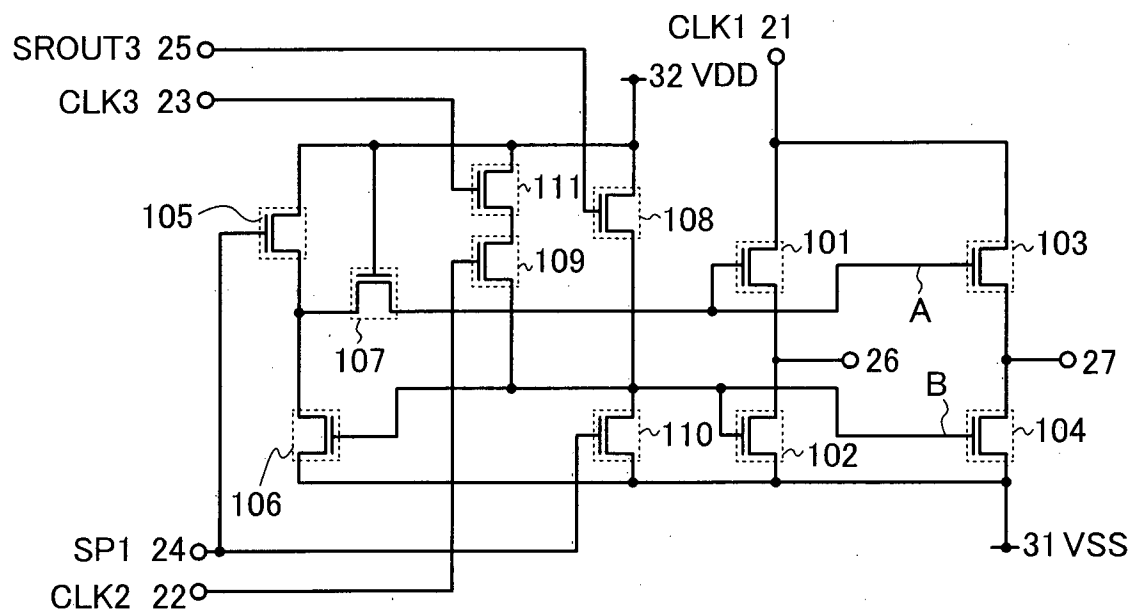
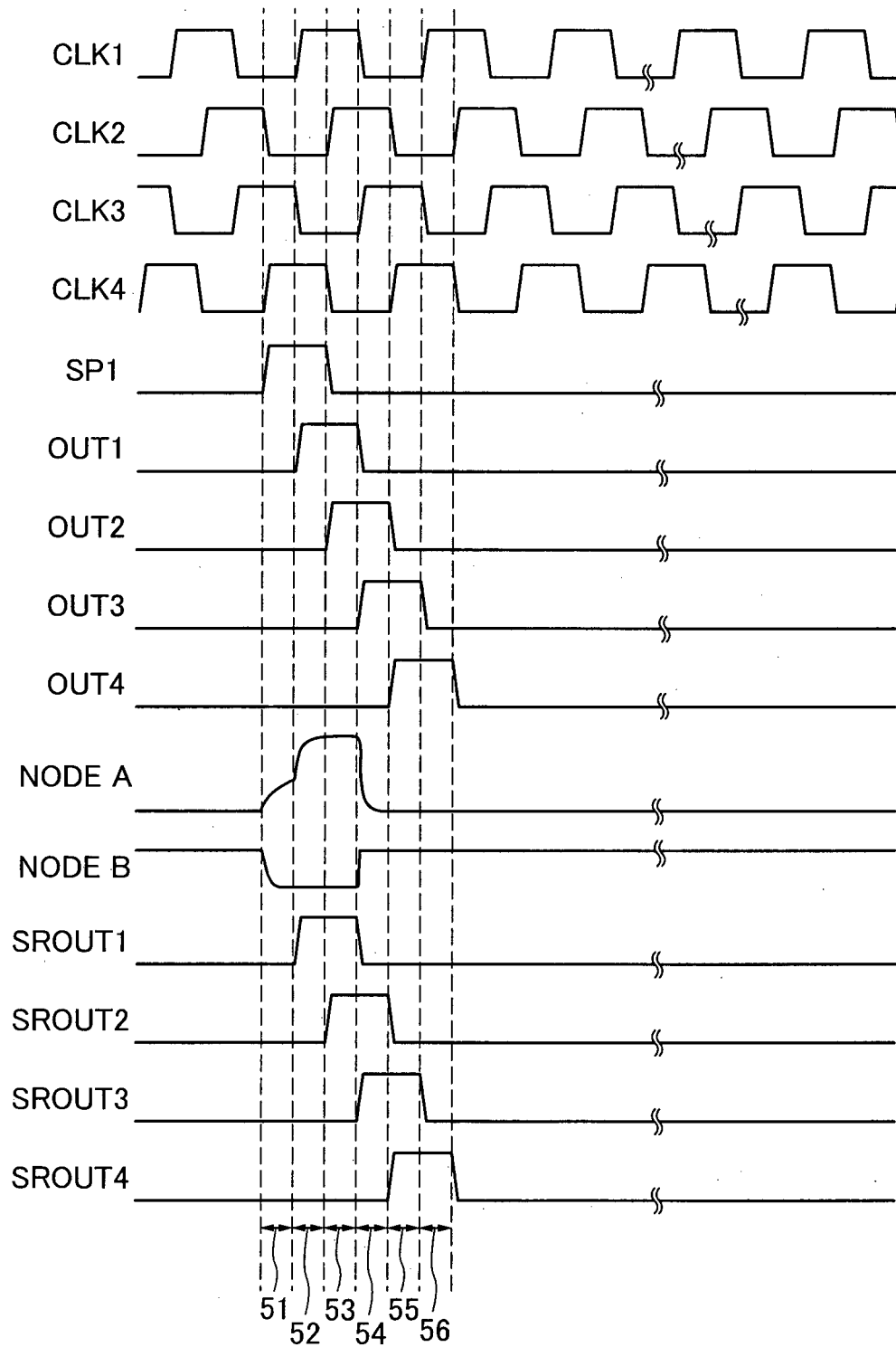
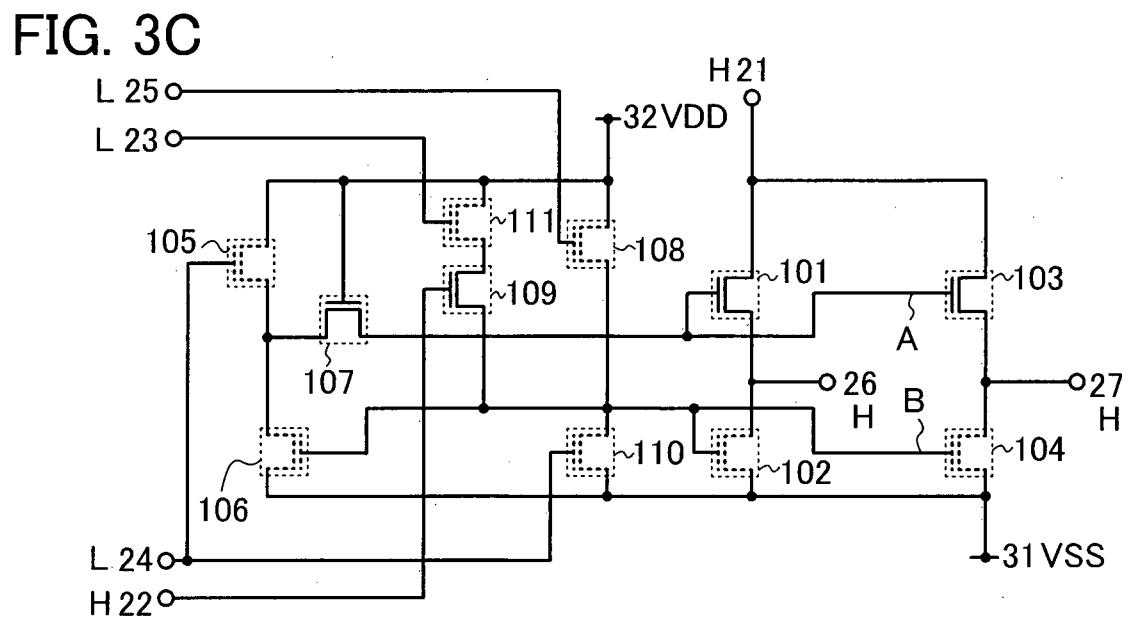
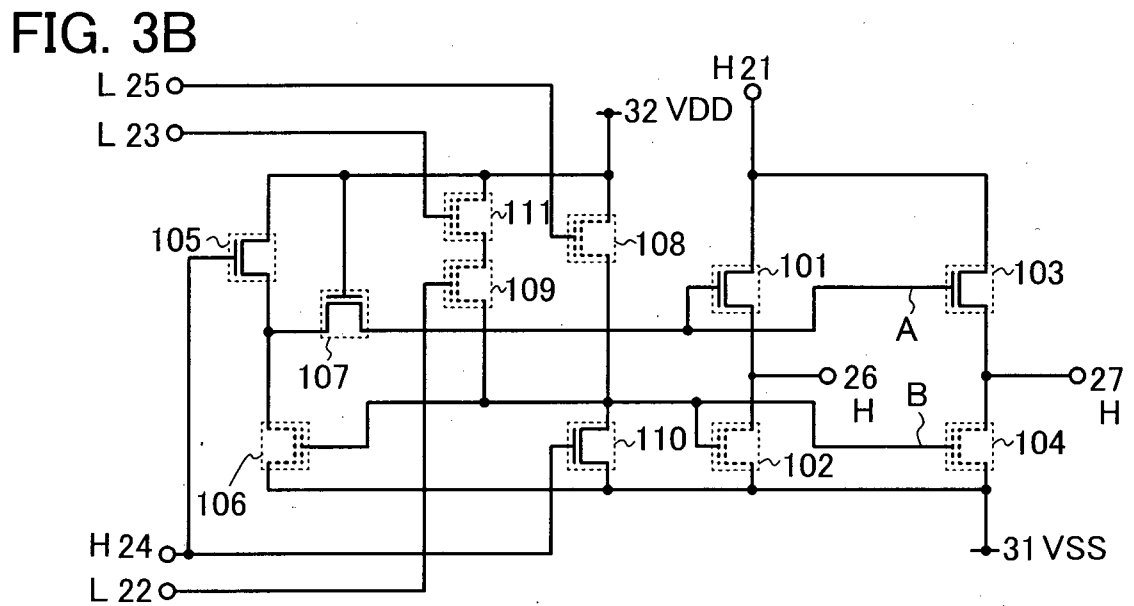
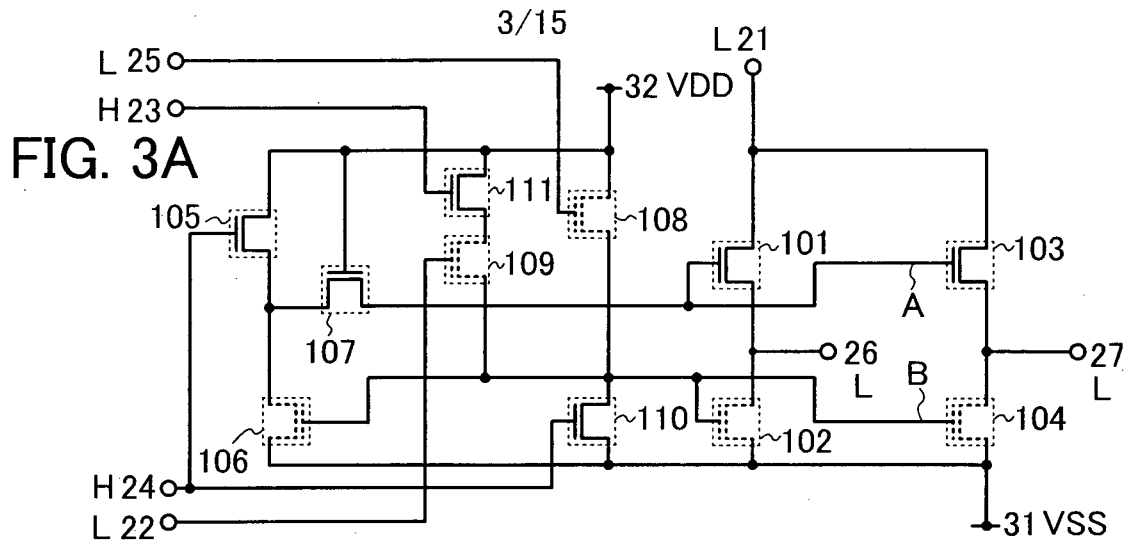


FIG. 2





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FIG. 4A

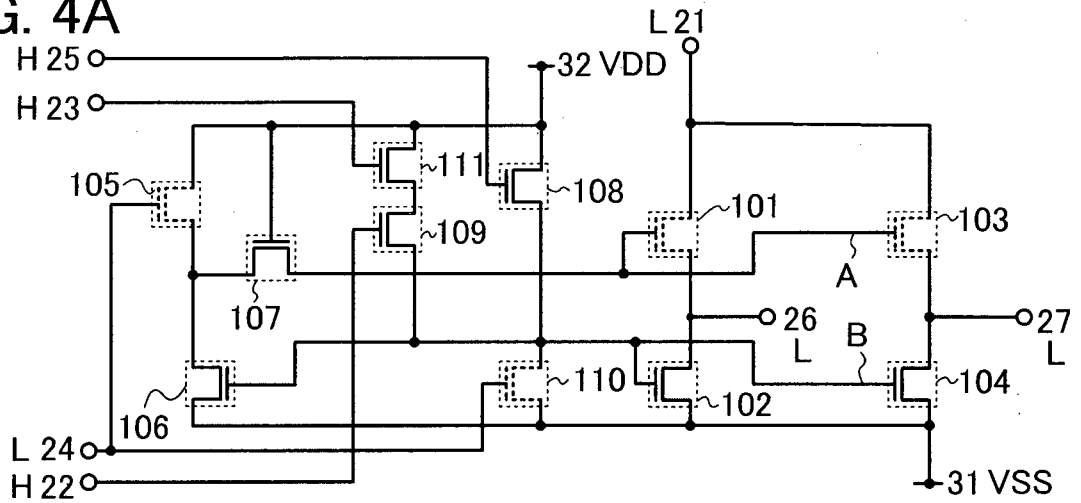


FIG. 4B

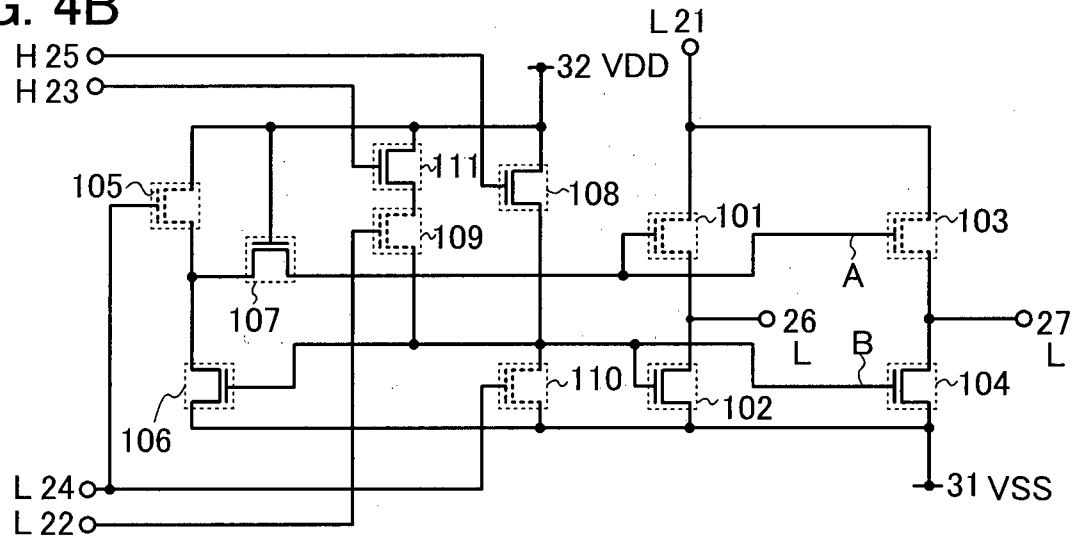
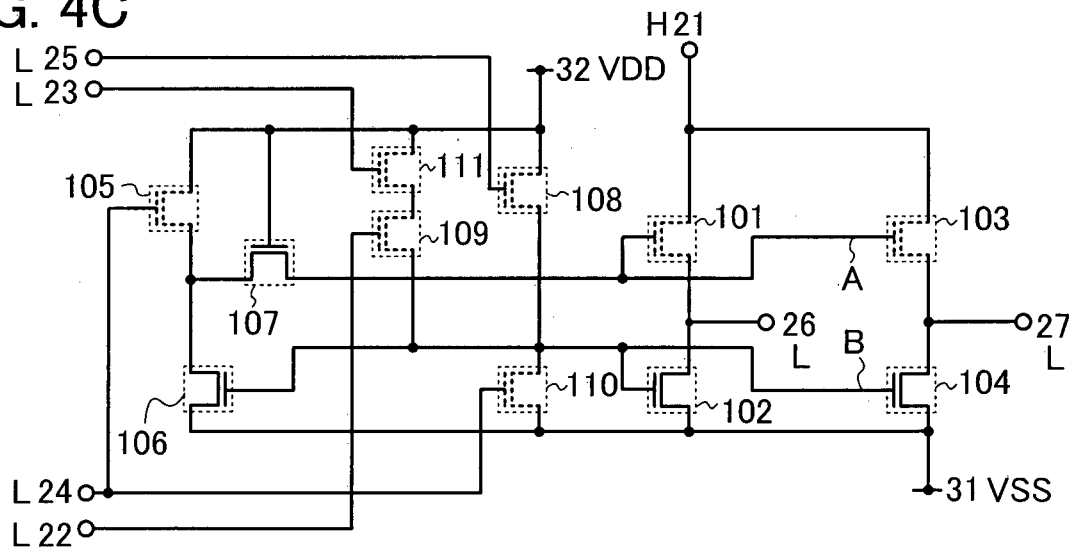


FIG. 4C



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FIG. 5A

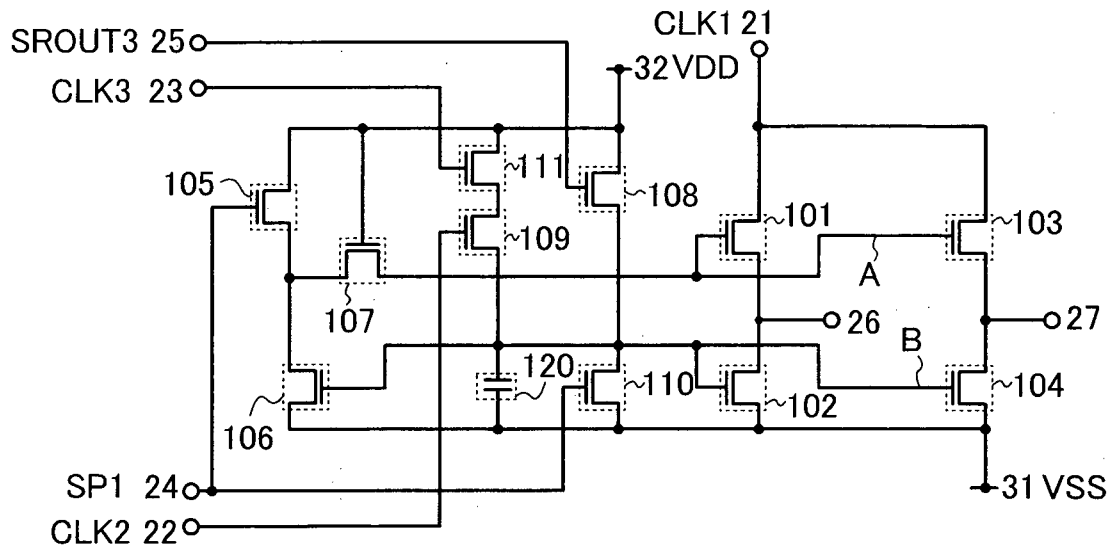
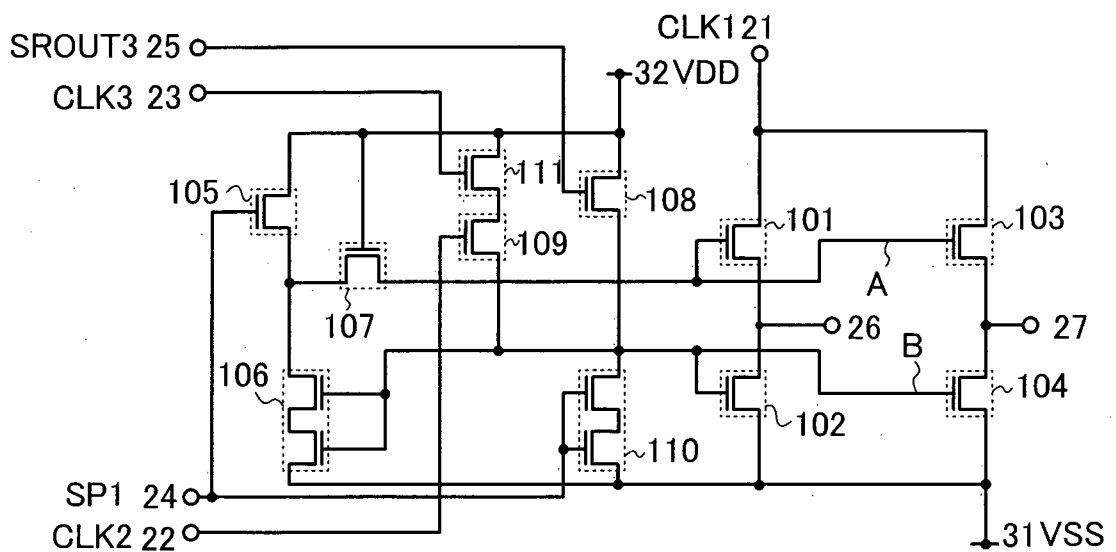


FIG. 5B



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FIG. 6A

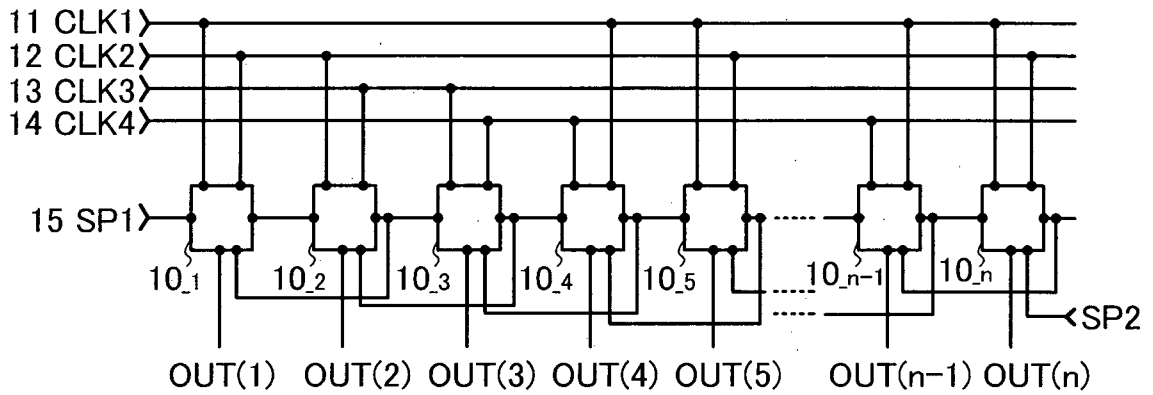


FIG. 6B

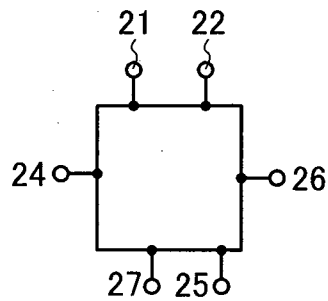


FIG. 6C

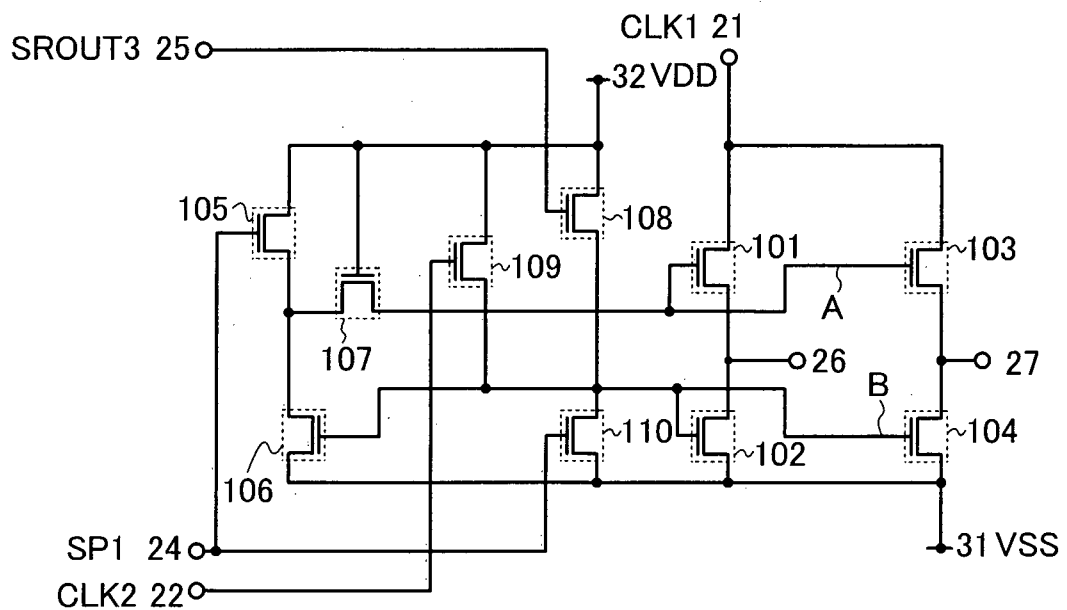
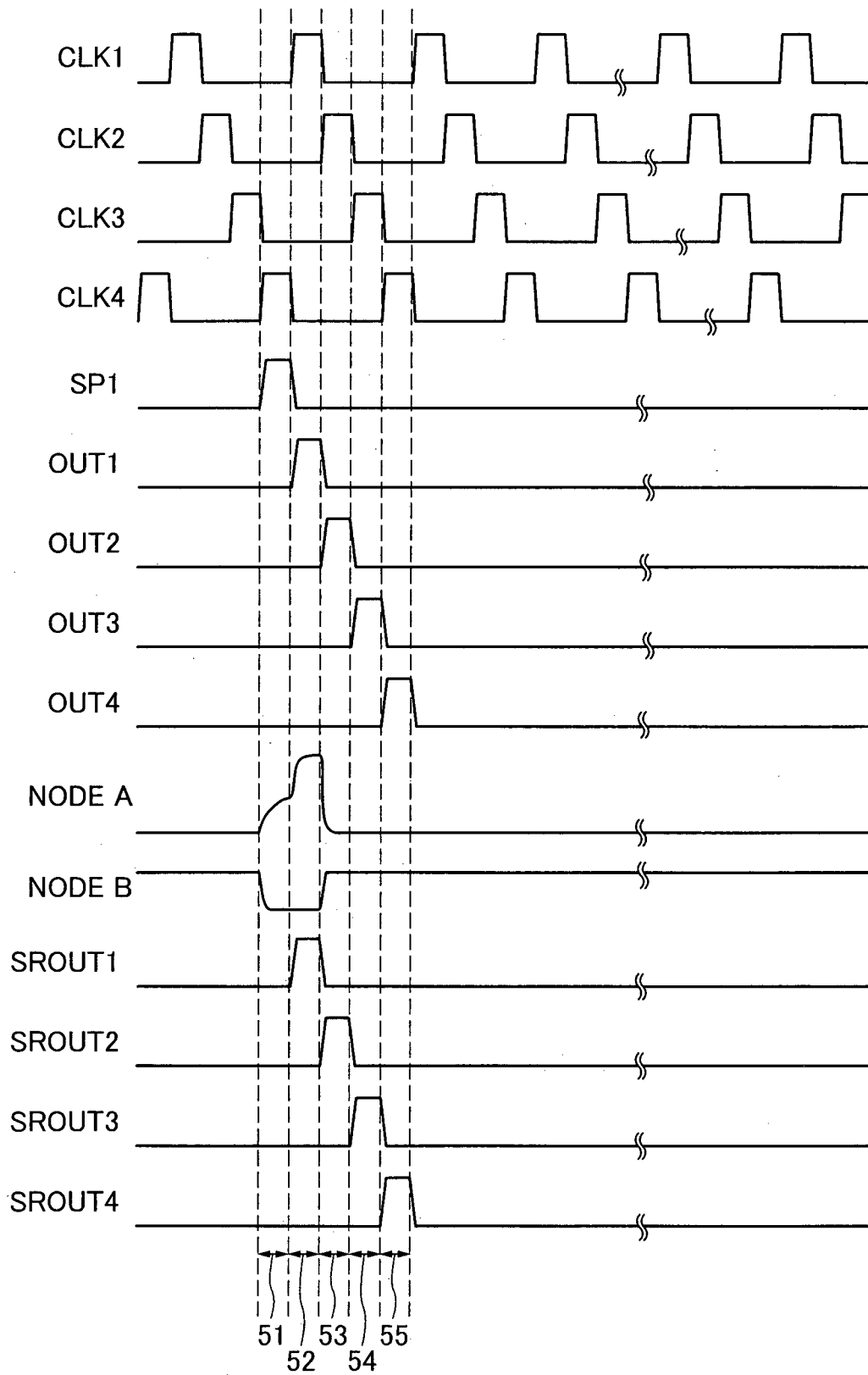


FIG. 7



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FIG. 8A

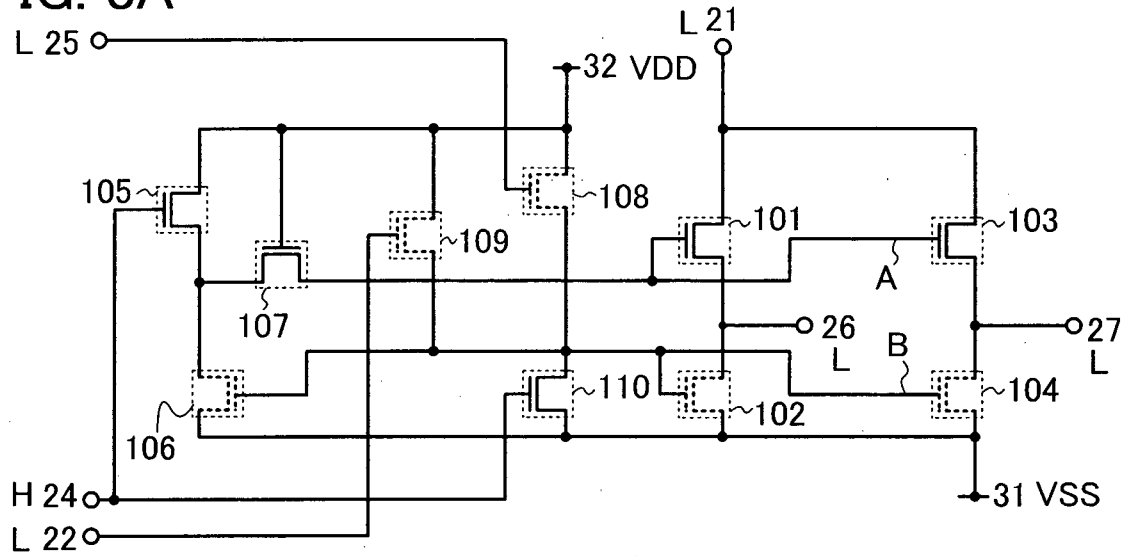


FIG. 8B

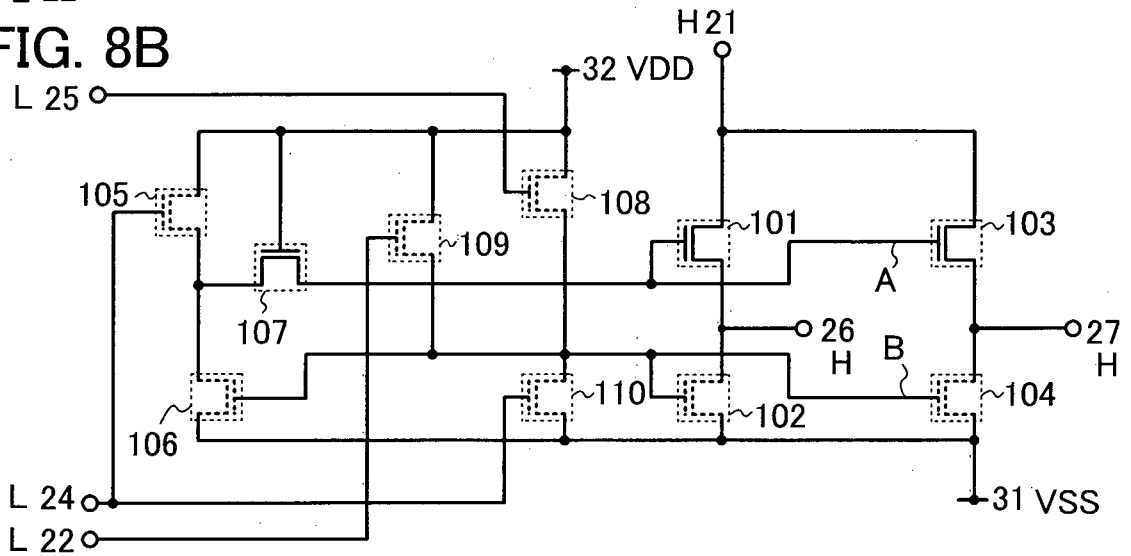
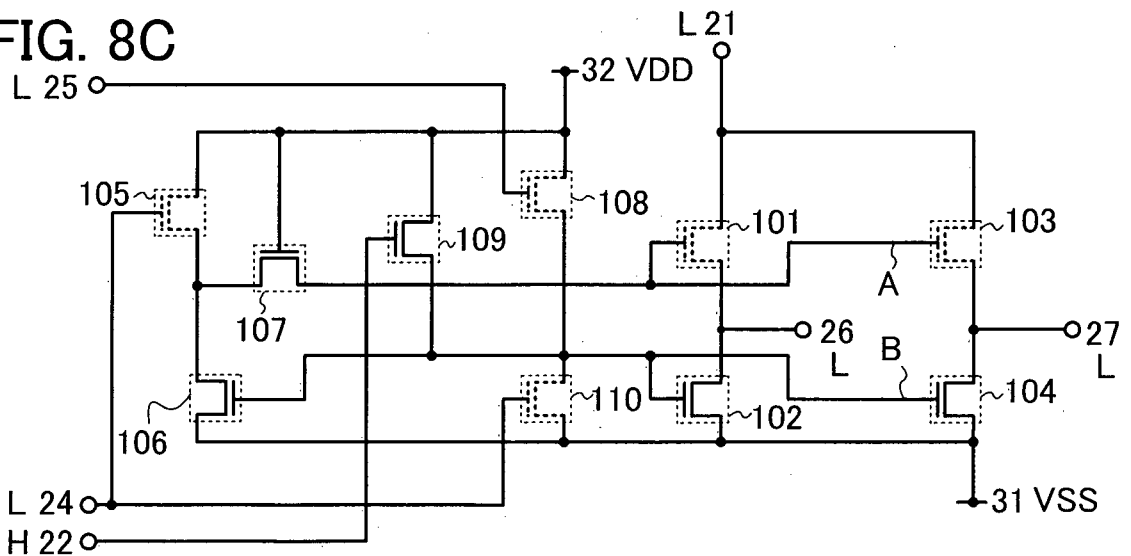


FIG. 8C



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FIG. 9A

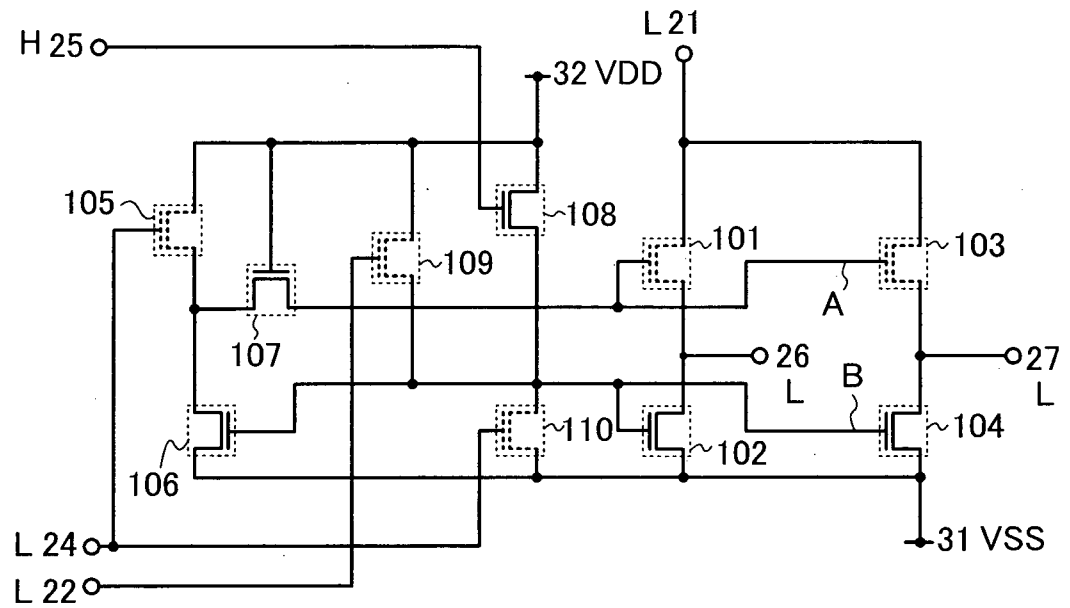
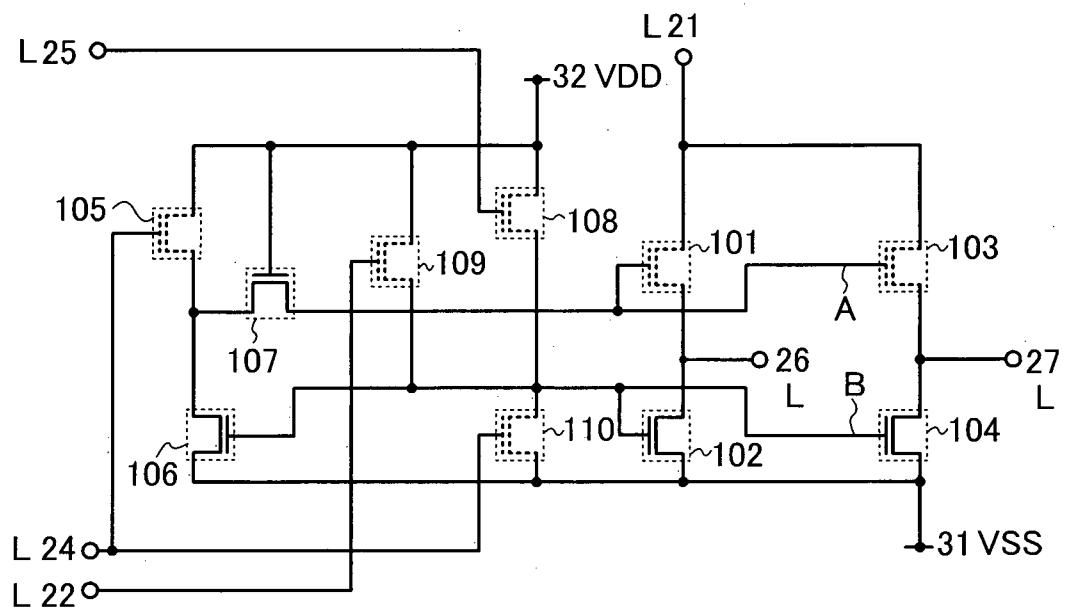


FIG. 9B



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FIG. 10A

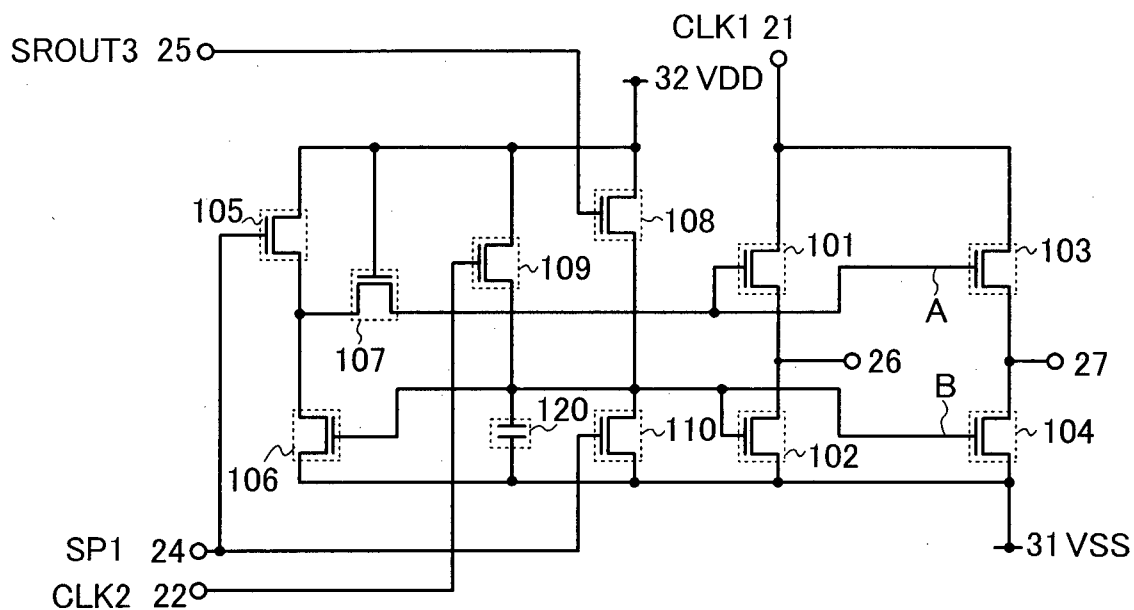
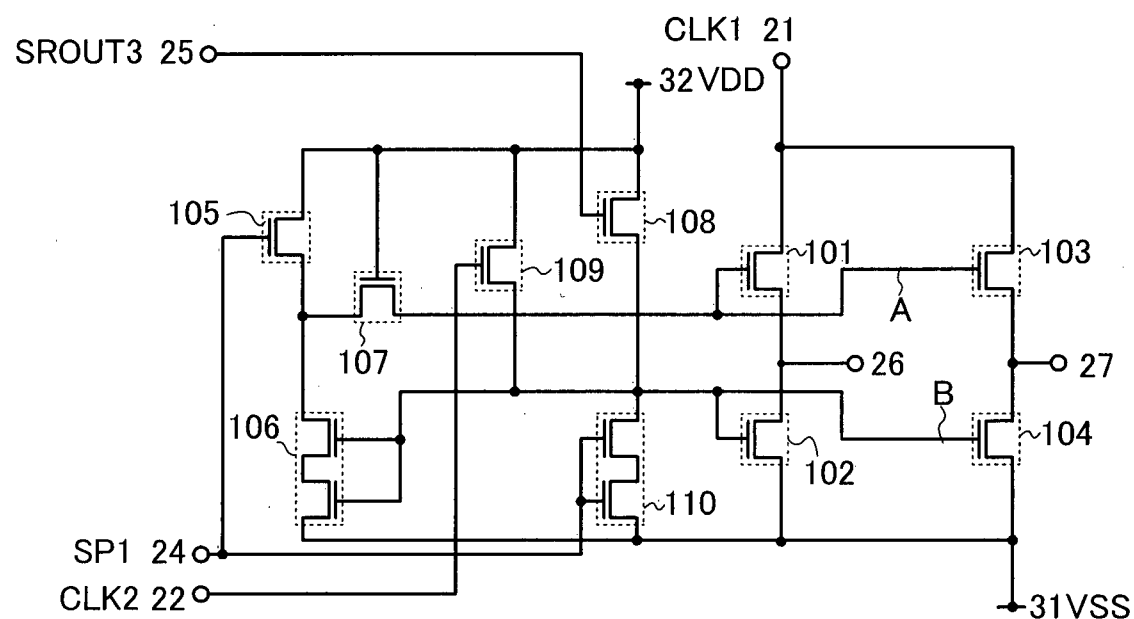


FIG. 10B



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FIG. 11A

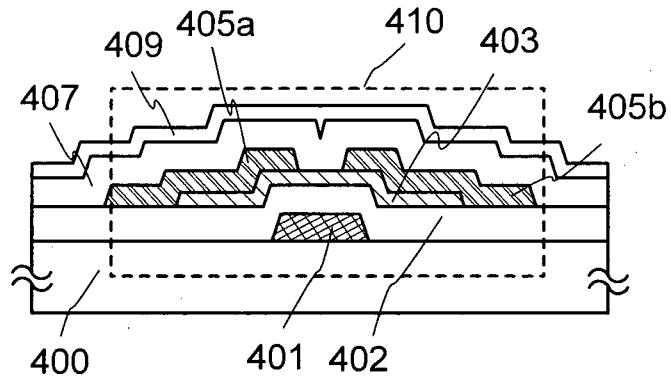


FIG. 11B

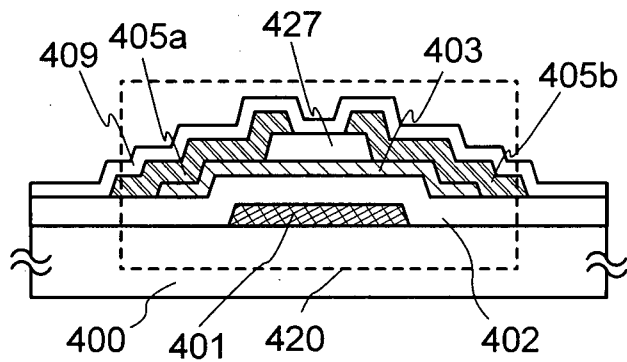


FIG. 11C

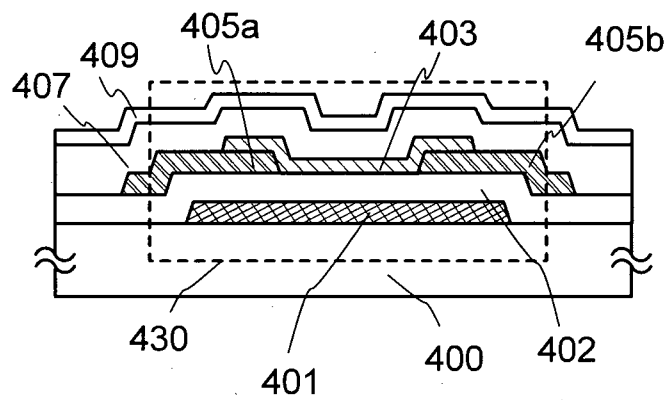
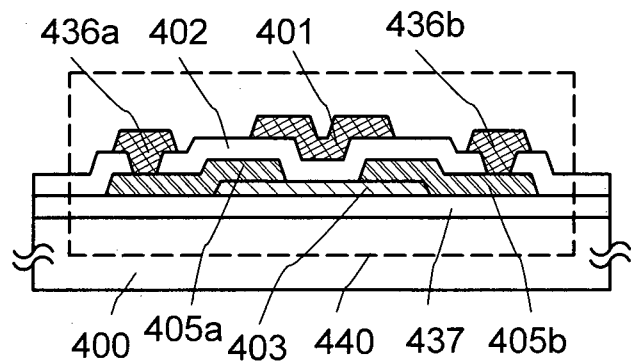


FIG. 11D



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FIG. 12A

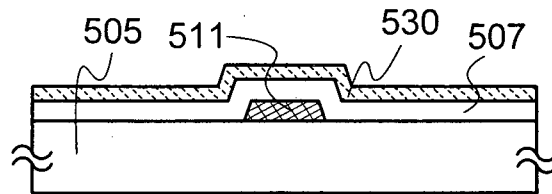


FIG. 12B

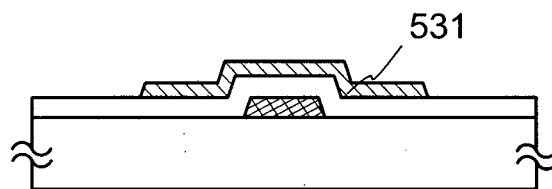


FIG. 12C

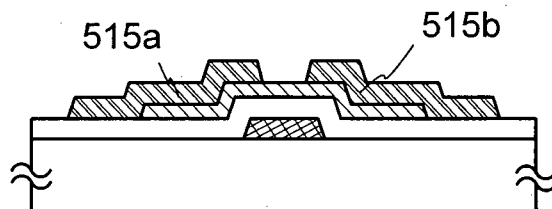


FIG. 12D

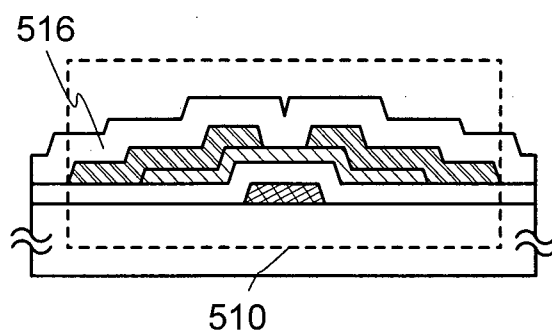
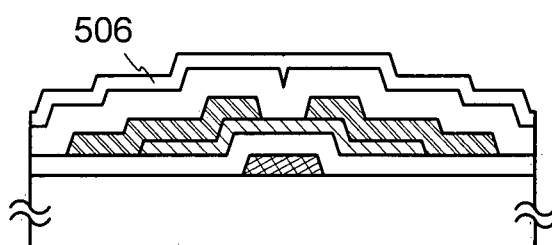


FIG. 12E



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FIG. 13A

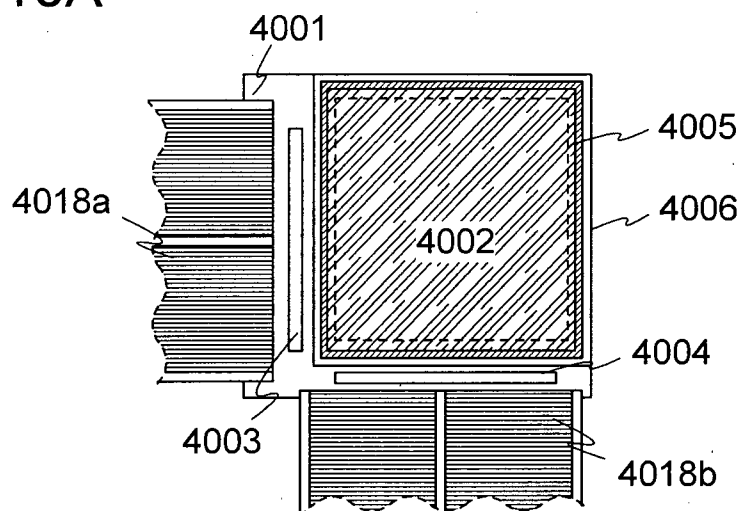


FIG. 13B

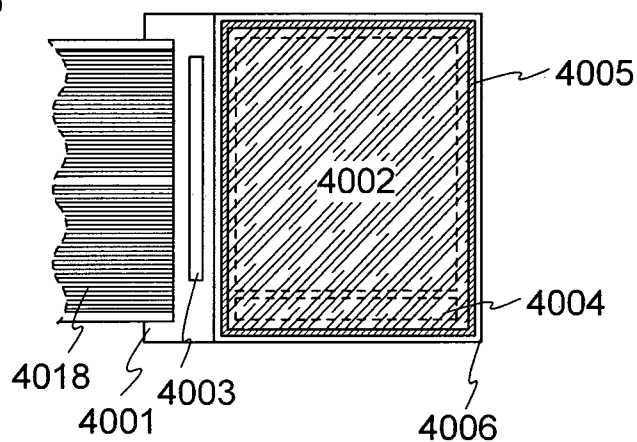
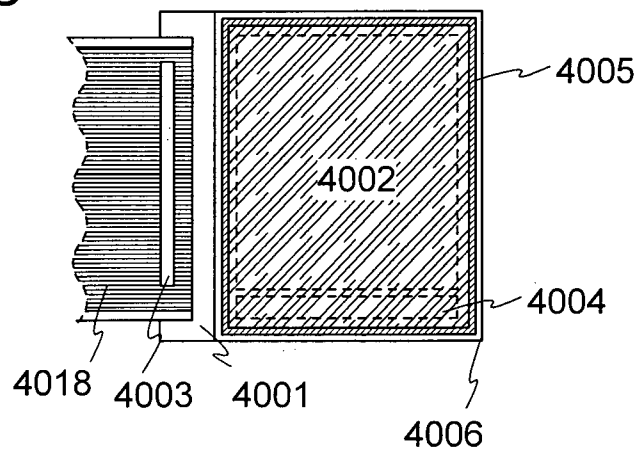


FIG. 13C



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FIG. 14A

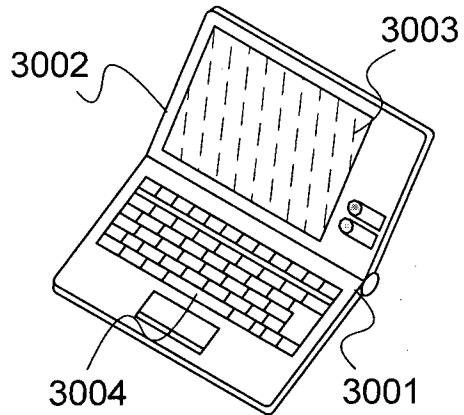


FIG. 14B

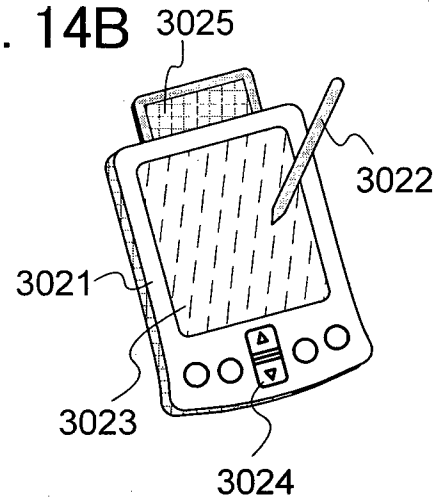


FIG. 14C

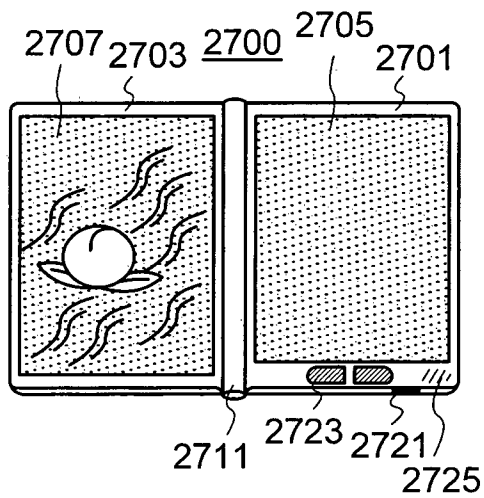


FIG. 14D

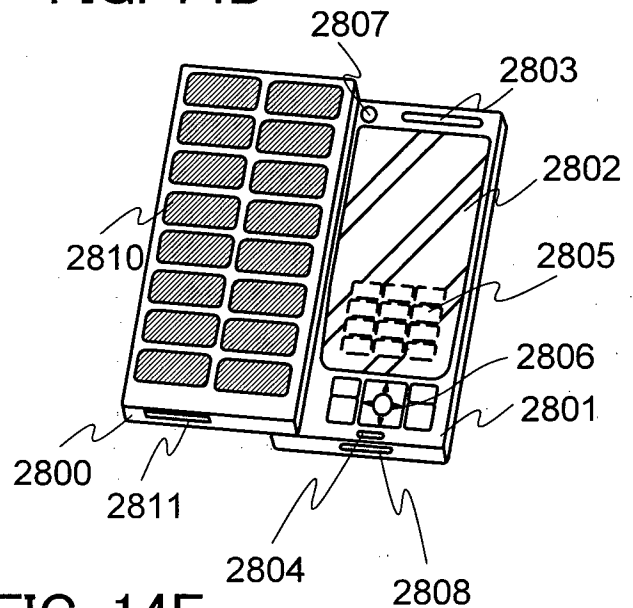


FIG. 14E

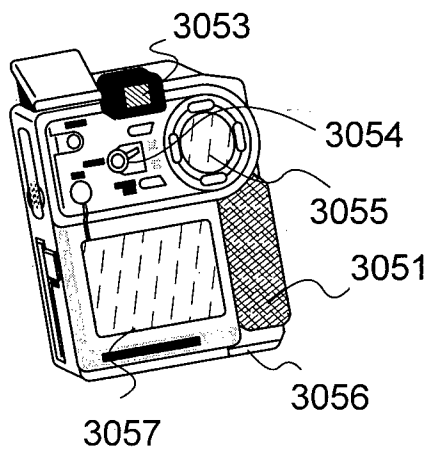
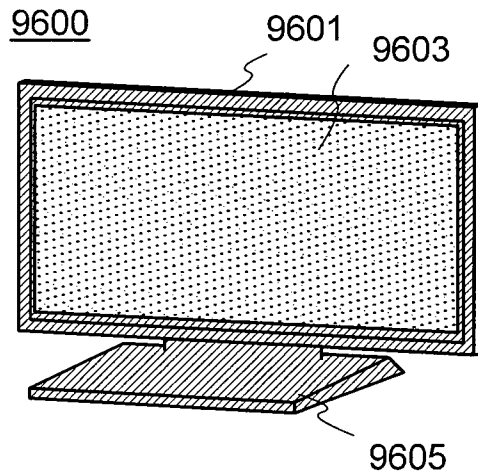


FIG. 14F



REFERENCE NUMERALS

11: signal line, 12: signal line, 13: signal line, 14: signal line, 21: input terminal, 22: input terminal, 23: input terminal, 24: input terminal, 25: input terminal, 26: output terminal, 27: output terminal, 31: power supply line, 32: power supply line, 51: period, 52: period, 53: period, 54: period, 55: period, 56: period, 101: transistor, 102: transistor, 103: transistor, 104: transistor, 105: transistor, 106: transistor, 107: transistor, 108: transistor, 109: transistor, 110: transistor, 111: transistor, 120: capacitor, 400: substrate, 401: gate electrode layer, 402: gate insulating layer, 403: oxide semiconductor layer, 405a: source electrode layer, 405b: drain electrode layer, 407: insulating layer, 409: protective insulating layer, 410: transistor, 420: transistor, 427: insulating layer, 430: transistor, 436a: wiring layer, 436b: wiring layer, 437: insulating layer, 440: transistor, 505: substrate, 506: protective insulating layer, 507: gate insulating layer, 510: transistor, 511: gate electrode layer, 515a: source electrode layer, 515b: drain electrode layer, 516: insulating layer, 530: oxide semiconductor film, 531: oxide semiconductor layer, 2700: e-book reader, 2701: housing, 2703: housing, 2705: display portion, 2707: display portion, 2711: hinge, 2721: power switch, 2723: operation key, 2725: speaker, 2800: housing, 2801: housing, 2802: display panel, 2803: speaker, 2804: microphone, 2805: operation key, 2806: pointing device, 2807: camera lens, 2808: external connection terminal, 2810: solar cell, 2811: external memory slot, 3001: main body, 3002: housing, 3003: display portion, 3004: keyboard, 3021: main body, 3022: stylus, 3023: display portion, 3024: operation button, 3025: external interface, 3051: main body, 3053: eye piece portion, 3054: operation switch, 3055: second display portion, 3056: battery, 3057: first display portion, 4001: substrate, 4002: pixel portion, 4003: signal line driver circuit, 4004: scan line driver circuit, 4005: sealant, 4006: substrate, 4018: FPC, 9600: television set, 9601: housing, 9603: display portion, 9605: stand

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/052795

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H03K3/356 (2006.01) i, H03K19/0175 (2006.01) i, H03K19/0944 (2006.01) i,
H03K23/44 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H03K3/356, H03K19/0175, H03K19/0944, H03K23/44

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2008-122939 A (KABUSHIKIKAISHA HANDOUTAI ENERUGI-KENKYUUSHO) 2008.05.29, Whole document, Figure 1 & US 2008/02588998 A1	1-17
A	JP 2004-226429 A (KABUSHIKIKAISHA HANDOUTAI ENERUGI-KENKYUUSHO) 2004.08.12, Whole document, Figure 1 & US 2004/0140839 A1 & US 2005/0062515 A1 & US 2006/0280279 A1	1-17



Further documents are listed in the continuation of Box C.



See patent family annex.

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“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

01.04.2011

Date of mailing of the international search report

12.04.2011

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3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

Authorized officer

Masaru Ishida

Telephone No. +81-3-3581-1101 Ext. 3596

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