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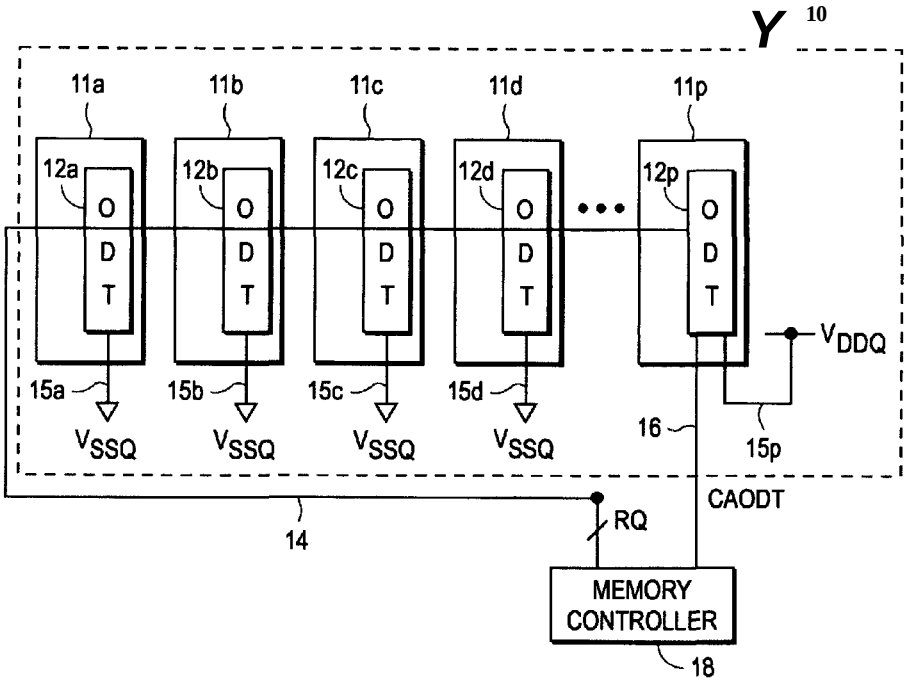

(57) Abstract: A system includes a plurality of memory devices arranged in a fly-by topology, each of the memory devices having on-die termination (ODT) circuitry for connection to an address and control (RQ) bus. The ODT circuitry has at least one input for controlling termination of one or more signal lines of the RQ bus. Application of a first logic level to the at least one input enables termination of the one or more signal lines. Application of a second logic level to the at least one input disables termination of the one or more signal lines.

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DYNAMIC ON-DIE TERMINATION OF ADDRESS AND COMMAND SIGNALS

TECHNICAL FIELD

[0001] This disclosure relates generally to the field of semiconductor memories and memory systems.

BACKGROUND

[0002] High-speed, readily-expandable memory systems consisting of groups of memory devices or modules are commonly used to store data in computers and other electronic devices. Bits of data are typically stored in semiconductor memory cells on the memory device, with the data being transmitted along data signals lines or data bus connected to the memory modules. To avoid undesirable signal reflections on the data bus, the memory device typically includes some sort of termination circuitry for the data bus lines.

[0003] So-called "fly-by" memory modules topologies are being increasingly used for DRAM memory module applications. "Fly-by" memory modules can be terminated either at the hosting motherboard or at the module itself. This scheme often uses extra printed circuit board (PCB) area devoted to termination of the command, address, and control signals (i.e., "RQ" signal or bus lines) on each module in the system, resulting in less area being available for DRAM packages. Also typical memory systems expend significant power for the command, address, and control signals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The present invention will be understood more fully from the detailed description that follows and from the accompanying drawings, which however, should not be taken to limit the invention to the specific embodiments shown, but are for explanation and understanding only.

[0005] Figure 1 illustrates an example memory system with memory devices that employ ODT circuitry.

[0006] Figure 2A & 2B are example ODT circuits that may be used in the memory system of Figure 1.

[0007] Figure 3 illustrates an example method of operation for the memory system of Figure 1.

[0008] Figure 4 illustrates an example memory module with ODT circuitry that provides multiple termination impedance values.

[0009] Figure 5 is a table that illustrates example termination impedance values corresponding to various input pin logic levels for the memory module shown in Figure 4.

[001 0] Figure 6 illustrates another example memory system with memory modules that employ ODT circuitry.

DESCRIPTION OF EXAMPLE EMBODIMENTS

[001 1] In the following description specific details are set forth, such as device types, system and circuit configurations, component values, signaling methods, etc., in order to provide a thorough understanding of the disclosure herein. However, persons having ordinary skill in the relevant arts will appreciate that these specific details may not be needed to practice the embodiments described.

[0012] In the context of the present application, a memory "module" refers to an assembly of memory chips or devices (i.e., semiconductor dies) arranged on a substrate or printed circuit board (PCB) in association with a memory system. A memory module may thus be considered a memory subsystem. The term "data bus" is used throughout to denote data (DQ) signal lines, timing reference signals, and data masking control bits (DM) by which data is communicated to one or more memory modules. Similarly, the term "address / command bus" is used herein to denote the signal lines that carry command, address and control (RQ or CAC) information for communications between a memory controller and one or more memory modules. The term "memory controller", as used herein, refers to a broad class of generic and application-specific processing devices that are capable of reading data from, and writing data to, one or more memory modules.

[001 3] In accordance with one embodiment, each memory device or module of a memory system arranged in a fly-by connection topology includes ODT circuitry for selectively terminating one or more of the RQ signal lines. The RQ signals comprise the command, address, control, and clock signals that may be used to write data to the individual memory cells of the modules, and also to read data stored therein. In a typical configuration, the last device of every module connected to the RQ bus has one or more RQ lines terminated by connecting an ODT enable pin to the appropriate voltage supply rail of the device or module.

[0014] Other embodiments may also utilize register control, either as an override, or as a replacement, for the enable pin configuration method. For example, in one embodiment register fields may be utilized to override the RQ ODT enable. In a specific implementation, a register bit may allow the clock lines to be discretely terminated on the device or module, while the RQ signals (or a subset thereof) are terminated with ODT circuitry.

[0015] Figure 1 illustrates an example memory module 10 comprising a plurality of DDR3 memory devices 11 arranged in a fly-by (also known as a multi-drop) connection topology, each of the memory devices comprising a single semiconductor chip or die that includes ODT circuitry 12. For example, Figure 1 shows 16 memory devices 1la-p, each with a respective ODT circuit 12a-p that may be utilized to selectively terminate any or all of the RQ signal lines on RQ bus 14. Each of memory devices 11 also includes an ODT termination pin 15, which is tied to either VDDQ or VSSQ in the module layout, depending on the device's location on RQ bus 14. By way of example, Figure 1 illustrates ODT circuit 12p of the last memory device (i.e., device 1Ip) on RQ bus 14 being enabled by connection of ODT termination pin 15p to the positive voltage supply rail, VDDQ. The remaining ODT circuits 12a-o are shown having their respective ODT termination pins 15a-o connected to the negative voltage supply rail, VSSQ, which disables termination on devices 1la-o.

[001 6] It is appreciated that the last device (i.e., device 1Ip) is the one electrically furthest from the memory controller 18. In the fly-by (or multi-drop) connection topology, each control and address (CA) signal is routed from a controller pin to a pin on each DRAM

device. The propagation time from the controller to each memory device is different depending on the physical position of the memory device in the module. In the example of Figure 1, device 1Ip is the last memory device in the topology, and therefore experiences the longest CA signal propagation time. It is appreciated that chip select (CS) signals may also be routed with the same fly-by connection topology as the CA signals in the example memory module of Figure 1.

[0017] Memory controller 18 is shown driving the signal lines of bus 14, as well as driving a control / address ODT signal line 16 (labeled "CAODT") connected to ODT circuit 12p. The CAODT control signal pin may be utilized to actively enable and disable a subset (or all) of the RQ signal line terminations. For instance, CAODT pin 16 may be actively driven by memory controller 18 to enable or disable ODT circuit 12p at certain times depending on the transactions been performed in memory system 10. By way of example, when memory controller 18 drives CAODT pin 16 to a logical high level (e.g., VDDQ), ODT circuit 12p is enabled or turned on, such that the impedance for a subset (or all) of the signals at the end of RQ bus 14 is set to a predetermined value. The timing for enabling and disabling the ODT circuitry on the RQ signal lines may be the same is that for the data group signal lines.

[001 8] Practitioners in the art will appreciate that the impedance value of the termination may be determined by signal integrity studies, and may be different for different "classes" of signals. For example, the chip select signal lines may have a different impedance value as compared to the address signal lines. In the case where memory controller 18 drives CAODT pin 16 to a logical low level (e.g., VSSQ), ODT circuit 12p is disabled or turned off, e.g., a high impedance value for the signal lines terminating at the end of RQ bus 14. It should be further understood that CAODT signal line 16 may be included on RQ bus 14.

[0019] In one embodiment, a subset of the RQ signals is terminated at all times by ODT circuit 12p in device l ip. The RQ signals that are terminated at all times include the external clock signals (CK / CKN) and the chip reset signal (RESETN). In the example of

Figure 1, the subset of the RQ signals on bus 14 that are not terminated, unless memory locations in device 1Ip are being immediately addressed, include the address lines (A[15:0]); bank address (BA[2:0]); chip select (CS[3:0]); clock enable (CKE); row address strobe (RASN); column address strobe (CASN); and write enable (WEN). The termination circuits for these latter signal lines may be dynamically controlled by CAODT pin 16. In other words, the foregoing subset of signal lines may be dynamically controlled such that the impedance value at the end of the RQ bus for these signals depends upon the operations being performed. Termination is normally disabled for non-addressed devices.

[0020] Practitioners in the art will appreciate that dynamically controlling (enabling/disabling) the termination at the end of the RQ bus for a subset of signal provides a significant power saving advantage. In one implementation, for example, disabling the termination on most of the RQ pins during extended idle times on the RQ bus, or while in a power-down mode, may save about 30OmW per memory device.

[0021] Figure 2A illustrates an example ODT circuit 20 that may be used in the memory system of Figure 1. ODT circuit 20 comprises a switch 24 coupled in series with resistor 21 between positive voltage supply rail VDDQ and signal line termination node 23. Similarly, a resistor 32 and switch 25 are coupled in series between node 23 and negative supply voltage rail VSSQ. (It is appreciated that switches 24 & 25 may also be located between node 23 and respective resistors 21 & 32.) The signal line has a characteristic impedance shown by element 28 driven by a driver 29 associated with the memory controller. Both resistors 21 and 32 are shown having the same resistance value, R, such that when both switches 24 & 25 are closed the equivalent resistance terminating the signal line is R/2, with the voltage at node 23 being (VDDQ-VSSQ)/2. With switches 24 & 25 both open, termination is off (e.g., high impedance). Consistent with the example of Figure 1, switches 24 & 25 may both be simultaneously controlled by CAODT pin 16.

[0022] Figure 2B illustrates another example ODT circuit 30 that may be used in the memory system of Figure 1 to achieve dynamic termination with multiple impedance values. ODT circuit 30 resembles the ODT circuit of Figure 2A, except with three parallel arranged

circuit legs. Each leg comprises a switch 34 coupled in series with a resistor 31 between VDDQ and signal line termination node 33. Each leg also includes a resistor 42 and switch 35 coupled in series between node 33 and VSSQ. Resistors 31a & 42a have a resistance R; resistors 31b & 42b have a resistance R/2; and resistors 31c & 42c have a resistance R/4.

[0023] Switches 34 and 35 of may be selectively opened / closed in order to implement various different termination impedance values applied to different command, control, and address signals of selected memory devices. For instance, in one embodiment, the termination impedance of a signal line may be selected to be "strong" by closing of all of switches 34 & 35, "weak" by closing only switches 34a, 34b, 35a and 35b, or "off by leaving all of switches 34 & 35 open, depending on signal integrity considerations. In the example of Figure 2B the characteristic impedance is shown by element 38, with the signal line being driven by a driver 39 associated with the memory controller. Switches 34 & 35 in each leg may both be simultaneously controlled by a different CAODT pin or bit value in a register field.

[0024] In a specific embodiment, multi-value RQ termination is supported for memory device by selecting different values of address, control, and command signal line termination impedance to be employed. For instance, multi-value RQ termination may be controlled by three different register fields. A first register field may be used to set an alternate value of termination to be used, while a second register field determines how the alternate value is enabled. A third register field may be used to set a nominal impedance to be used for termination. According to one method of control, the CAODT control pin selects the nominal value of impedance when driven high, and the alternate value of impedance when driven low.

[0025] A second method of controlling / selecting multiple termination values for an RQ signal line utilizes the CAODT control pin and an ALTCAODT control pin. Figure 4 illustrates an example memory device 11 with ODT circuitry 12 that provides for multiple termination impedance values using the CAODT and an ALTCAODT control pins. Figure 5 is a table that illustrates example termination impedance values corresponding to various

input pin logic levels for the memory device shown in Figure 4. As can be seen, when CAODTEN is high (enabled), a logical high value applied to the CAODT control pin enables a nominal impedance value. On the other hand, when ALTCAODT is high, the alternate impedance value is enabled. When CAODTEN and ALTCAODT are both low, termination is off (i.e., a high impedance state).

[0026] It is appreciated that in another embodiment the CAODTEN pin may be controlled via a configuration bit. Setting of the configuration bit to "1", for example, may be equivalent to statically enabling the address on the termination, i.e., hard-tying the CAODTEN pin high.

[0027] Figure 3 illustrates an example method of operation for the memory system of Figure 1. The process begins at block 41, wherein prior to addressing a selected memory device the termination value of selected RQ lines is enabled for the selected memory device. It is appreciated that, in certain situations, termination values may be enabled for more than one device. For instance, depending where the addressed device is electrically located on the RQ bus, it may be appropriate to disable termination on the addressed device, while simultaneously enabling termination on an adjacent device, in order to achieve optimal signal integrity. In other words, termination of the individual RQ signal lines may be dynamically controlled by the memory controller rather than being statically enabled. Furthermore, in certain cases, termination may specifically be disabled in instances where the terminated device is being addressed and enabled when it is not being addressed. In still other situations, termination may be enabled except during full bus idle conditions or power down states. In other embodiments, each of the memory devices arranged in the fly-by topology may have termination enabled with respect to the RQ signal lines, with the termination impedance value changing during addressing of specific devices.

[0028] Once the appropriate termination values have been applied to a subset (or all) of RQ signal lines on the selected memory device(s), the RQ lines may be driven to the appropriate voltage levels for addressing the memory locations within the device (block 42). After data has been written / read from the addressed location, termination is disabled for the

subset of RQ lines at the specified device(s) (block 43). As discussed previously, disabling termination has the salutary effect of reducing quiescent power consumption in the memory system.

[0029] Figure 6 illustrates another example memory system 59 with four memory modules 60a-60d, each module comprising a plurality of memory devices (e.g., DRAM chips) 61. Each of the memory devices 61 include ODT circuitry 62, with each of the memory devices of the modules being coupled with a memory controller 68. As in the case of the example of Figure 1, the respective ODT circuits 62 of memory devices 61 may be utilized to selectively terminate any or all of the RQ signal lines on RQ bus 64. In this example, the RQ bus lines are shown coupled with the memory devices of each module in a stub bus connection topology. In the stub bus connection topology the RQ lines are routed to each module by splitting off of a main bus. In this embodiment, the RQ signals are split off of the main bus and then routed onto each individual module. After being routed past each individual DRAM in a "fly-by" topology, the RQ signals are then optionally terminated by the memory device farthest (electrically) from the controller.

[0030] Each of memory devices 61 of each module 60 also includes an ODT termination on/off pin 65, which is tied to either VDD or VSS in the module layout, depending on the location of the device in the module. Tying termination pin 65 to VDD enables termination for that device. Conversely, tying pin 65 low to VSS disables termination at that device. In the example of Figure 6, only the ODT circuit 62p of the last memory device 61p in each memory module 60 is enabled by connection of ODT termination pin 65p to the positive voltage supply rail, VDD. The remaining ODT circuits 62a-o of the other memory devices 61 on each of modules 60a-60d have their respective ODT termination pins 65 connected to the negative voltage supply rail, VSS, which disables termination on those devices.

[0031] A termination impedance value for each device 61p of modules 60a-60d may be selected via CAODT pins 66a-66d, respectively. For example, the ODT circuitry may be configured such that raising CAODT pin 66 to a high voltage potential (logical "1") result in

a nominal termination impedance, whereas lowering pin 66 to a logical "0" voltage produces an alternate (or high) impedance at that device. Multiple CAODT pins (e.g., CAODT & ALTCAODT) for each device may be utilized for setting a variety of different termination impedance values at devices 62p.

[0032] In the same manner as described in conjunction with Figure 1, memory controller 68 may be utilized to actively drive all, or a subset, of the RQ signal lines of bus 64, as well as driving CAODT signal lines 66a-66d connected to ODT circuits 62p of respective modules 60a-60d. CAODT pin 66 may thus be used to selectively enable or disable ODT circuit 61p of a selected module at certain times depending on the transactions being performed in memory system 59. For example, when a write transaction is initiated to module 60d, the termination on modules 60a-c may be enabled to eliminate reflections from those trace stubs. The termination on module 60d may remain disabled in order to allow a full signal swing on that module. Similarly, where the termination circuitry on devices 61 supports multiple values of termination impedance, a write operation to module 60d may be best achieved having a "strong" termination enabled in modules 60a-c (e.g. low impedance) while module 60d has a "weak" termination (e.g. higher impedance) enabled. In another example, the termination on module 60d may be enabled on a write to module 60d, while the terminations on all other modules are disabled. In still another example, a write to module 60d may be best achieved by having modules 60a-c "weakly" terminated (e.g. high impedance), while enabling a "strong" termination (e.g. lower impedance) on module 60d.

[0033] In another embodiment, termination of the last device of each of a plurality of memory modules may be implemented utilizing a termination component device (or several devices) separate from the memory chips and actively controlled by memory controller 68.

[0034] It is also appreciated that the foregoing termination examples are applicable to buffered memory systems configured with a single buffer on each module or multiple buffers paired with one or more memory devices in a fly-by fashion.

[0035] In still another embodiment, instead of employing the "stub bus" routing scheme shown in Figure 6, a "serpentine" routing scheme may be used in which the address

lines are routed onto and off of each module in turn. In this latter connection topology, only the ODT circuit of the last memory device of the last memory module is enabled.

[0036] It should be understood that elements of the present invention may also be provided as a computer program product which may include a machine-readable medium having stored thereon instructions which may be used to program a computer (e.g., a processor or other electronic device) to perform a sequence of operations. Alternatively, the operations may be performed by a combination of hardware and software. The machine-readable medium may include, but is not limited to, floppy diskettes, optical disks, CD-ROMs, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, magnet or optical cards, propagation media or other type of media/machine-readable medium suitable for storing electronic instructions. For example, elements of the present invention may be downloaded as a computer program product, wherein the program may be transferred from a remote computer or telephonic device to a requesting process by way of data signals embodied in a carrier wave or other propagation medium via a communication link (e.g., a modem or network connection).

[0037] Additionally, although the present invention has been described in conjunction with specific embodiments, numerous modifications and alterations are well within the scope of the present invention. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

We claim:

1. A system comprising:

a plurality of memory devices arranged in a fly-by topology, each of the memory devices having on-die termination (ODT) circuitry for connection to an address and control (RQ) bus, the ODT circuitry having at least one input for controlling termination of one or more signal lines of the RQ bus;

wherein application of a first logic level to the at least one input enables termination of the one or more signal lines, and application of a second logic level to the at least one input disables termination of the one or more signal lines.

2. The system of claim 1 wherein the RQ bus includes command and clock signal lines.

3. The system of claim 1 wherein the at least one input comprises first and second inputs, the first input for enabling the ODT circuitry, and the second input for selectively terminating the one or more signal lines.

4. The system of claim 3 wherein in a normal configuration, the first input of all of the memory devices, except a last memory device, is coupled to the second logic level, with the first input of the last memory device being coupled to the first logic level.

5. The system of claim 3 further comprising:

a memory controller that drives the RQ bus, the memory controller being coupled to the second input of the last memory device, the last memory device being electrically farthest among the memory devices from the memory controller on the RQ bus.

6. A system comprising:

a plurality of memory devices arranged in a fly-by topology, each of the memory devices having on-die termination (ODT) circuitry connected to a subset of signal lines of an address and control (RQ) bus, the ODT circuitry comprises a plurality of identical circuits, each of the identical circuits being connected to a corresponding one of the subset of signal lines;

wherein, responsive to input, the ODT circuitry either being disabled, or enabled to terminate each of the subset of signal lines of the RQ bus with one of a plurality of different impedance values.

7. The system of claim 6 wherein the plurality of different impedance values includes a first and a second impedance value.

8. The system of claim 6 wherein the plurality of different impedance values includes a first, a second, and a third impedance value.

9. The system of claim 6 wherein, when disabled, the ODT circuitry consumes essentially zero power.

10. The system of claim 6 wherein the input comprises a first input that enables the ODT circuitry, and a second input that terminates the subset of signal lines with a nominal impedance value.

11. The system of claim 10 wherein the input further comprises a third input that terminates the subset of signal lines with an alternate impedance value.

12. The system of claim 6 wherein the subset of signal lines excludes clock signal lines.

13. The system of claim 6 wherein the subset of signal lines includes address and bank address signal lines.

14. The system of claim 6 wherein the subset of signal lines includes row address strobe, column address strobe, and write enable signal lines.

15. A system comprising:

a plurality of memory devices arranged in a fly-by topology, each of the memory devices having on-die termination (ODT) circuitry connected to a subset of signal lines of an address and control (RQ) bus, the ODT circuitry comprises a plurality of identical circuits, each of the identical circuits being connected to a corresponding one of the subset of signal lines;

a memory controller connected to the memory devices via the RQ bus, the ODT circuitry of each memory device being coupled to the memory controller via control lines the RQ bus, the memory controller being operable to selectively enable / disable termination of the subset of signal lines in one or more of the memory devices via the control lines.

16. The system of claim 15 wherein the memory control is further operable to selectively terminate the subset of signal lines in the one or more of the memory devices with one of a plurality of different impedance values.

17. The system of claim 16 wherein the plurality of different impedance values includes a nominal impedance value, an alternate impedance value, and a high impedance value, the high impedance value corresponding to disabled termination.

18. The system of claim 15 wherein, when selectively disabled, the ODT circuitry consumes essentially zero power.

19. The system of claim 15 wherein the subset of signal lines excludes clock signal lines.

20. The system of claim 15 wherein the subset of signal lines includes address and bank address signal lines.

21. The system of claim 15 wherein the subset of signal lines includes row address strobe, column address strobe, and write enable signal lines.

22. A method comprising:

enabling on-die termination (ODT) circuitry in a memory device, the ODT circuitry being connected of a subset of signal lines of an address and control (RQ) bus, the memory device being one of a plurality of memory devices arranged in a fly-by topology;

terminating the subset of signal lines in the memory device with one of a plurality of impedance values.

23. The method of claim 22 further comprising:

enabling ODT circuitry in a different one of the memory devices; and

terminating the subset of signal lines in the different one of the memory devices with a different impedance value.

24. The method of claim 22 wherein the ODT circuitry comprises a plurality of identical circuits, each of the identical circuits being connected to a corresponding one of the subset of signal lines.

25. The method of claim 22 further comprising:

accessing data stored in the memory device; and

enabling the ODT circuitry in the memory device.

26. A memory device comprising:

a plurality of an address and control (RQ) lines;

on-die termination (ODT) circuitry coupled to the RQ lines, the ODT circuitry having at least one input for controlling termination of one or more of the RQ lines;

wherein application of a first logic level to the at least one input enables termination of the one or more signal lines, and application of a second logic level to the at least one input disables termination of the one or more signal lines.

27. The memory device of claim 26 wherein the RQ lines further comprise command and clock signal lines.

28. The memory device of claim 26 wherein the at least one input comprise a plurality of input pins for selecting one of a plurality of impedance values terminating the one or more of the RQ lines.

29. The memory device of claim 26 wherein the one or more of the RQ lines includes address and bank address signal lines.

30. The memory device of claim 26 wherein the one or more of the RQ lines includes row address strobe, column address strobe, and write enable signal lines.

31. A memory module comprising:

a plurality of memory devices connected in a fly-by topology to an address and control (RQ) bus;

termination circuitry associated with a last one of the memory devices in the fly-by topology, the termination circuitry having at least one input pin for controlling termination of a set of signal lines of the RQ bus with an impedance value.

32. The memory module of claim 31 further comprising a buffer associated with the last one of the memory devices, the termination circuitry being included in the buffer.

33. The memory module of claim 31 wherein the at least one input pin comprises a plurality of input pins for selecting the impedance value from a plurality of different impedance values.

34. The memory module of claim 31 wherein the set of signal lines of the RQ bus comprise command and clock signal lines.

35. The memory module of claim 31 wherein the set of signal lines of the RQ bus comprise address and bank address signal lines.

36. The memory module of claim 31 wherein the set of signal lines of the RQ bus comprise row address strobe, column address strobe, and write enable signal lines.

37. A memory system comprising:

an address and control (RQ) bus;

a plurality of memory modules, each memory module comprising a plurality of memory devices each of which is coupled to the RQ bus in a fly-by topology, a last one of the memory devices of each memory module having termination circuitry that includes input pins for selecting one of a plurality of impedance values to terminate a set of signal lines of the RQ bus;

a memory controller operable to drive the RQ bus and to selectively terminate the set of signal lines in each module by controlling the input pins of the termination circuitry of the last one of the memory devices of each memory module.

38. The memory system of claim 37 wherein the plurality of impedance values includes a nominal, an alternate, and a high impedance value.

39. The memory system of claim 37 wherein the set of signal lines of the RQ bus comprise row address strobe, column address strobe, and write enable signal lines.

40. The method of managing power consumption in a memory system, comprising:

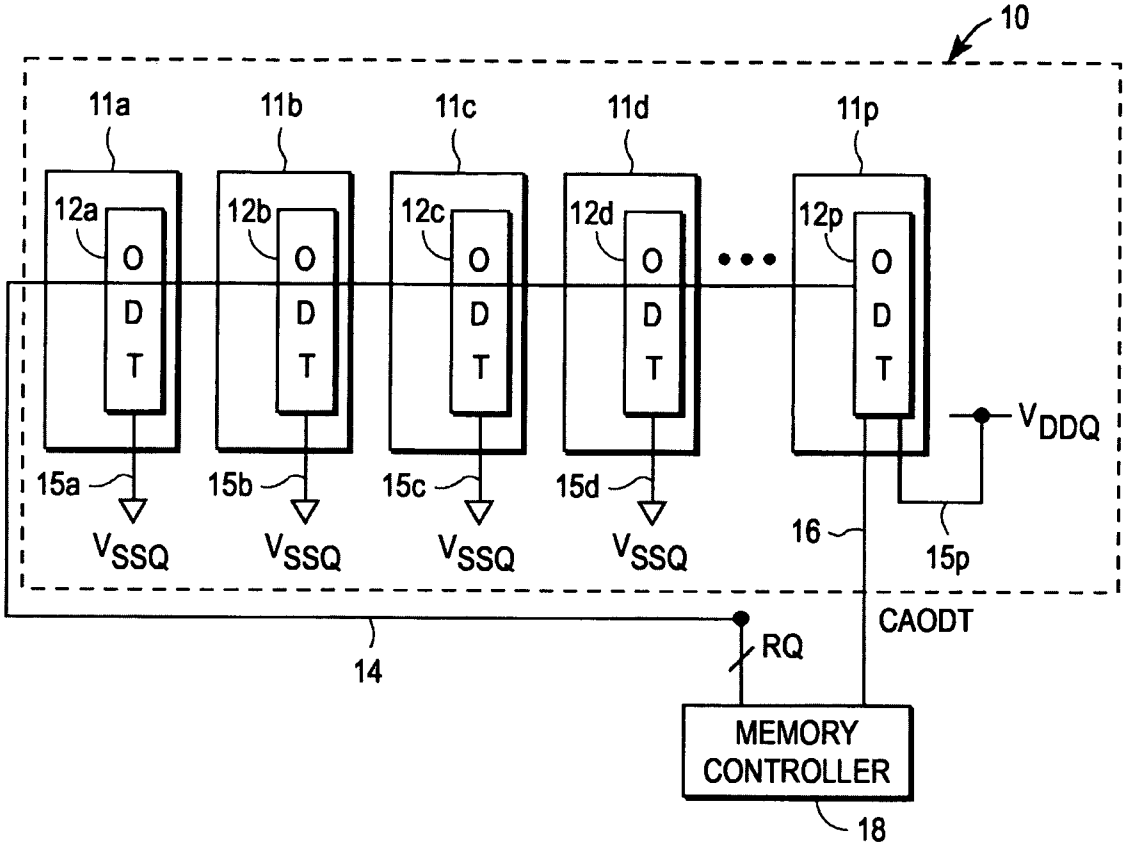
in a first time period, during which memory commands are transmitted from a memory controller to memory devices in memory modules, enabling on-chip termination devices on the memory devices; and

in a second time period, during which memory commands are not transmitted from the memory controller to the memory devices, disabling the on-chip termination devices on the memory devices so as to reduce power consumption in the memory system.

41. The method of claim 40, wherein the on-chip termination devices, when enabled, terminate command signal lines on which the memory commands are transmitted.

42. The method of claim 40, wherein the on-chip termination devices, when enabled, terminate command, address and control signal lines.

43. The method of claim 40, wherein, in the first time period, memory commands are transmitted from the memory controller to the memory devices in memory modules and data is transmitted between the memory controller and memory devices, and in the second time period, memory commands are not transmitted from the memory controller to the memory devices in memory modules and data is not transmitted between the memory controller and memory devices.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T
15a
15b
15c
15d
15p
16
V_{SSQ}
V_{DDQ}
14
RQ
CAODT
MEMORY CONTROLLER
18

FIG. 1

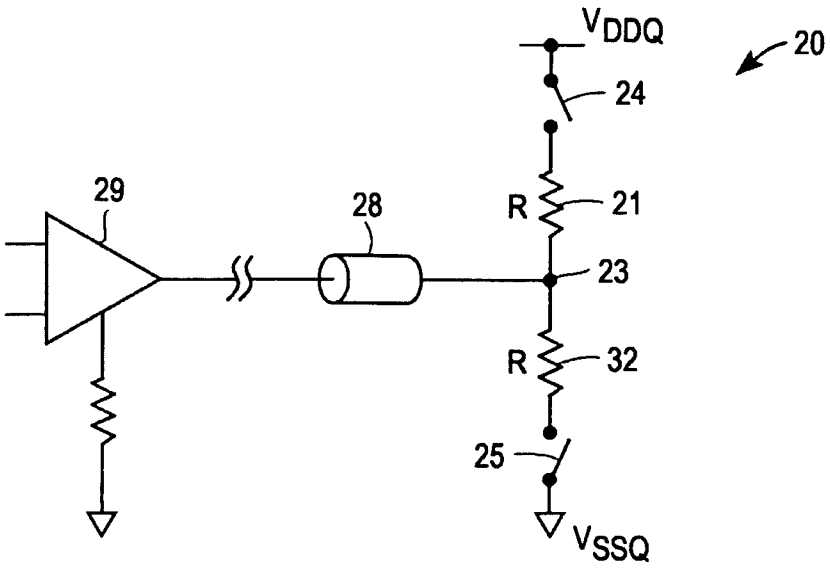
VDDQ
20
24
29
28
R
21
23
R
32
25
VSSQ

FIG. 2A

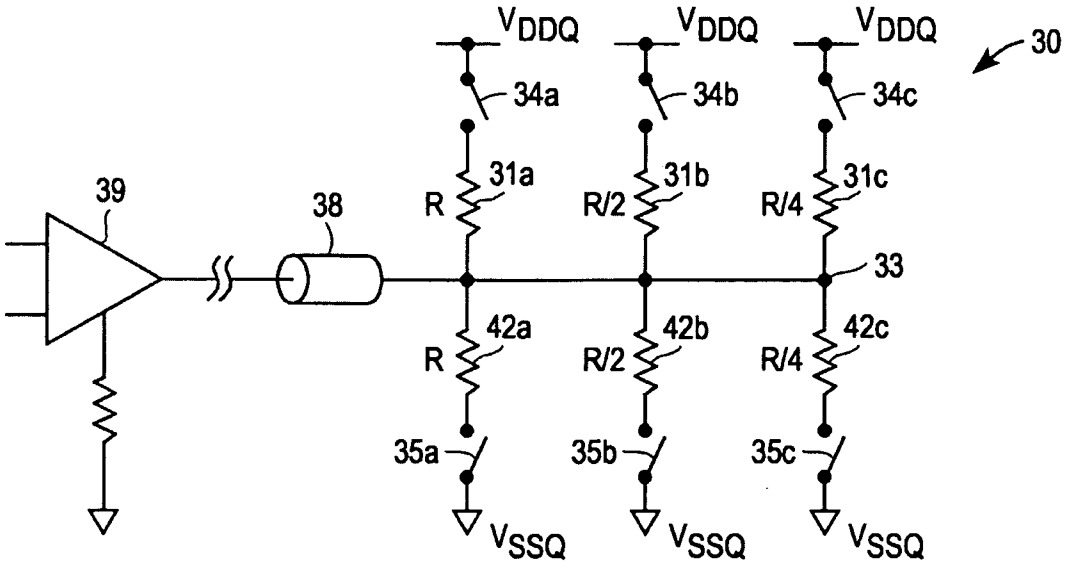
VDDQ
VDDQ
VDDQ
30
34a
34b
34c
39
38
R
31a
R/2
31b
R/4
31c
33
R
42a
R/2
42b
R/4
42c
35a
35b
35c
VSSQ
VSSQ
VSSQ

FIG. 2B

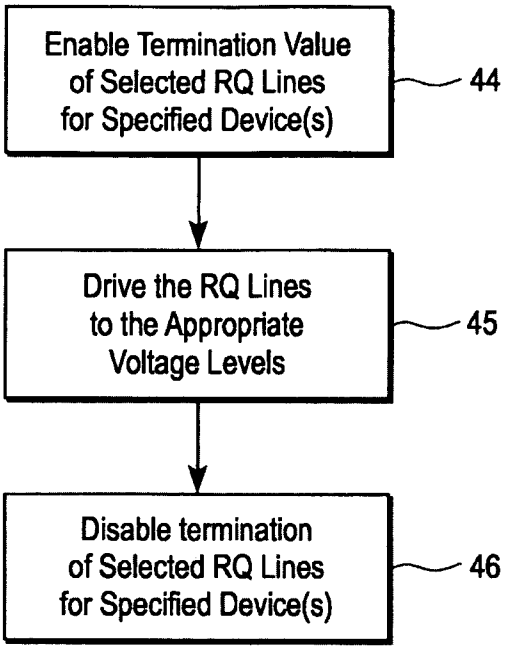
Enable Termination Value of Selected RQ Lines for Specified Device(s)
44
Drive the RQ Lines to the Appropriate Voltage Levels
45
Disable termination of Selected RQ Lines for Specified Device(s)
46

FIG. 3

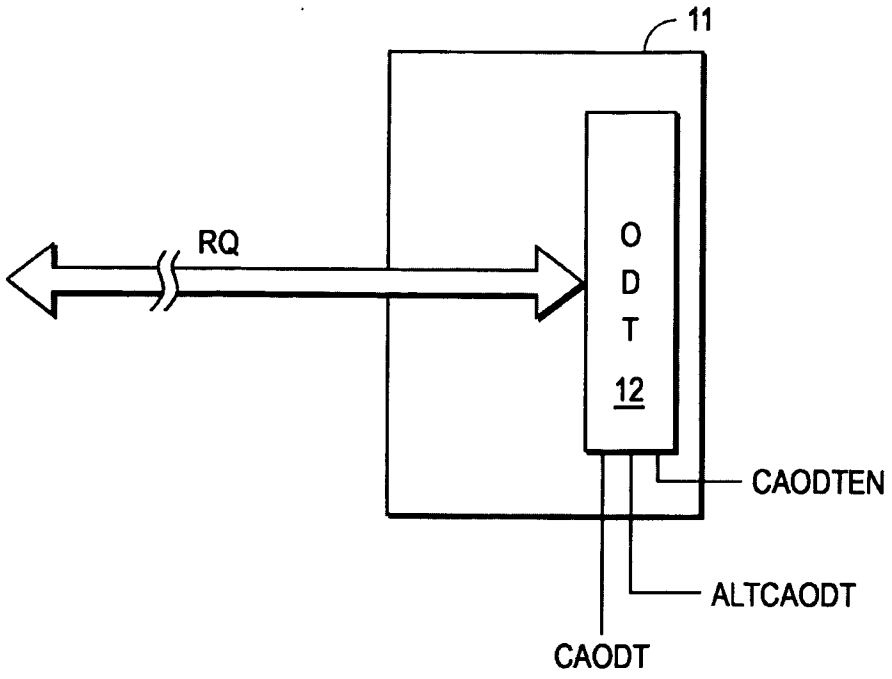

FIG. 4

CAODTEN	CAODT	ALT CAODT	
VSSQ (Disable)	D/C	D/C	Termination Off
VDDQ (Enable)	I	O	Nominal Z
	O	I	Alternate Z
	O	O	High Z

FIG. 5

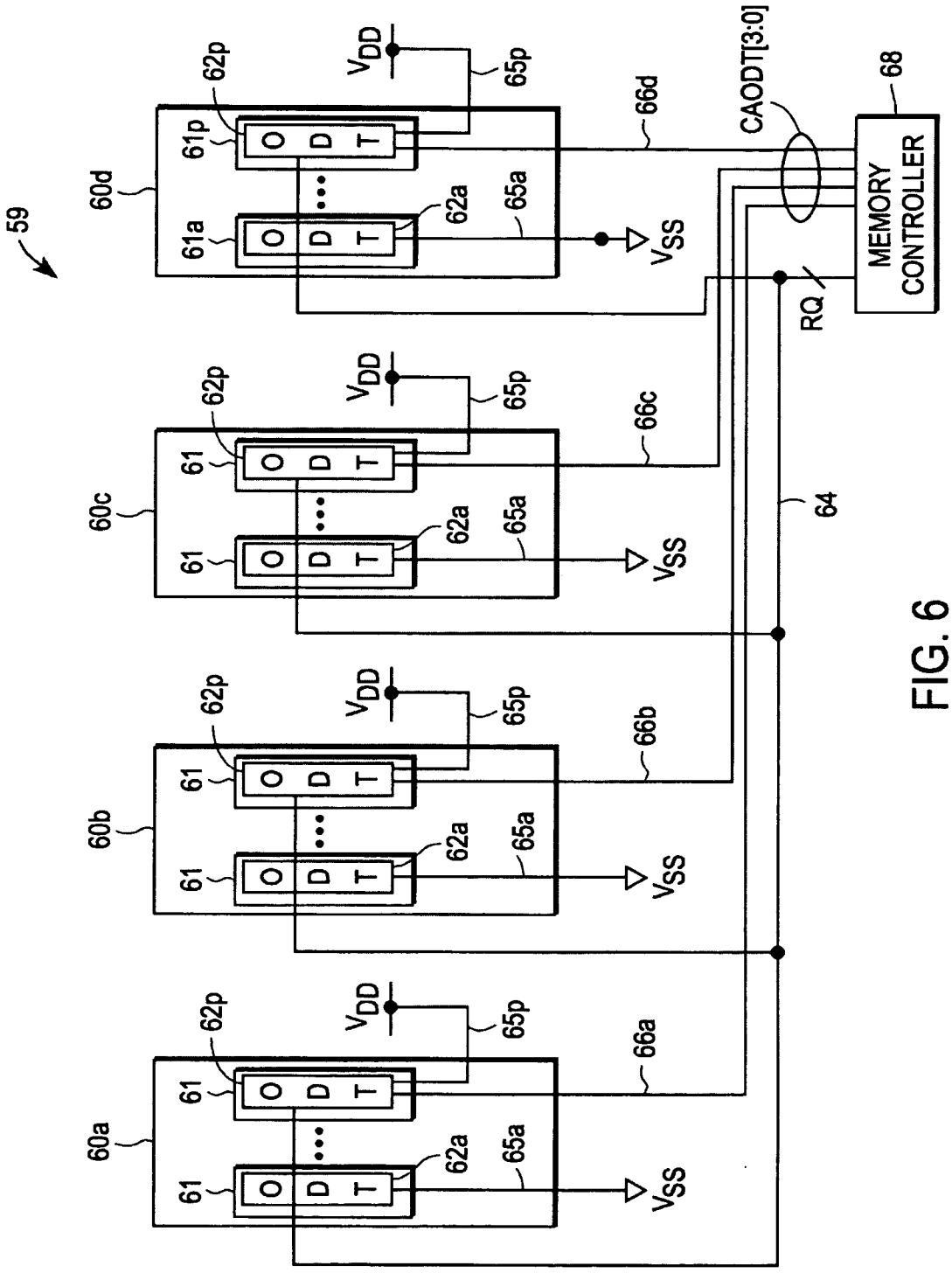
59
60d
60c
60b
60a
61p
61a
61
62p
62a
65p
65a
66d
66c
66b
66a
64
68
CAODT[3:0]
RQ
MEMORY CONTROLLER
VDD
VSS
O
D
T

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/088245

A. CLASSIFICATION OF SUBJECT MATTER
INV. G1105/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
GIIC

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal , WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/100837 A1 (LEE JUNG-BAE [KR]) 27 May 2004 (2004-05-27)	1,3-7,9, 10,15, 16,18, 22-26, 31,37,40
Y	paragraph [0005] - paragraph [0015]; figures 1,2	2,8, 11-14, 17, 19-21, 27-30, 32-36, 38,39, 41-43
	paragraph [0030] - paragraph [0057]; figures 3-9	

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents .

"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

'T' later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search	Date of mailing of the international search report
9 May 2008	02/06/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Balaguer Lopez, J

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C(Contlπuatlon) DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	US 2005/225353 Al (KWON DAE H [KR] KWON DAE HAN [KR]) 13 October 2005 (2005-10-13) paragraph [0017] - paragraph [0022]; figure 2	11,17, 28,32, 33,38
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A	US 2003/043681 Al (JANZEN JEFFERY W [US] ET AL) 6 March 2003 (2003-03-06) paragraph [0015] - paragraph [0027]; figures 1-4	1-43
A	US 2005/212551 Al (SO BYUNG-SE [KR] ET AL) 29 September 2005 (2005-09-29) paragraph [0062] - paragraph [0079]; figure 5	1-43

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Information on patent family members

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