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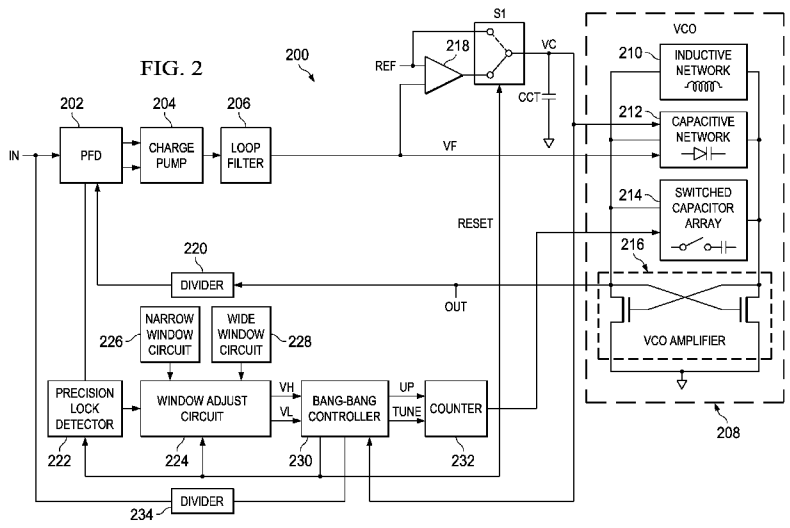
[Continued on next page]

(54) **Title**: PHASE LOCKED LOOP (PLL) WITH ANALOG AND DIGITAL FEEDBACK CONTROLS

FIG. 2



(57) **Abstract**: A phase locked loop (PLL 200), such as employed in a synthesizer, has two continuous (analog) control loops and one digital on-off ("bang-bang") control loop. The control loop of PLL 200 provides additional discrete time controls for a voltage controlled oscillator (VCO 208). The control loop measures the coarse voltage (VC) and input signal (IN) to adjust the switched capacitor array (214) to help decrease settling time. Precision lock detector (222) monitors input phase error, while narrow window circuit (226) and wide window circuit (228) specify a voltage window. Based on lock detection from the precision lock detector (222) and a voltage window from the narrow and wide window circuits (226, 228), a window adjust circuit 224 sets threshold voltages VH, VL for the on-off (bang-bang) controller 230.

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PHASE LOCKED LOOP (PLL) WITH ANALOG AND DIGITAL FEEDBACK CONTROLS

[0001] The invention relates generally to a phase locked loop (PLL) and, more particularly, to improvements in PLL feedback controls.

BACKGROUND

[0002] Phase locked loops (PLLs) are commonly used in synthesizer subsystems. An example of a conventional PLL 100 using continuous calibration is shown in FIG. 1. The PLL 100 is generally comprised of a phase/frequency detector (PFD) 202, charge pump 204, loop filter 206, a dual gain voltage controlled oscillator (VCO) 102, divider 220, amplifier 218, and calibration capacitor CCT. In this configuration, there are two separate analog loops, a low bandwidth loop (formed with the error amplifier 218 and VCO 102) and a high bandwidth loop (formed with divider 220 and VCO 102) so that the low bandwidth loop can apply a coarse tuning voltage VC to the VCO 102 and that the high bandwidth loop can apply a fine tuning voltage VF to VCO 102.

[0003] In operation, the high bandwidth loop operates as a conventional single path PLL, providing a low tuning gain characteristic for VCO 102 with the application of the fine tuning voltage VF to VCO 102, whereas the low bandwidth loop allows for the provision of a wide frequency tuning range characteristic. In particular with the low bandwidth loop, trans-conductance error amplifier 218 amplifies the difference between the fine tuning voltage VF (output from loop filter 206) and reference voltage REF, and this difference is applied as a current to capacitor CCT so as to generate coarse tuning voltage VC, which is applied to VCO 102 for the wide VCO tuning bandwidth. The low frequency loop will coarsely tune the wideband VCO to within a range where the high bandwidth loop becomes operational. This is accomplished by providing continuous (but low frequency) correction to the VCO 102. Because the low bandwidth loop can only track low frequency changes in the input signal, this loop will have little direct influence on the spur level and wide band phase noise performance of the PLL 100.

[0004] The high bandwidth loop does not operate until the VCO is tuned to a frequency that falls within the VCO fine frequency input tuning range, where the fine VCO tuning gain becomes non zero. The high bandwidth loop is generally responsible for setting the generally relevant noise characteristics. In the conventional single loop PLL the tradeoff between tuning range and noise performance is tightly coupled. The use of two loops effectively decouples this

trade-off, allowing PLL 100 to offer better performance over other conventional single path PLLs."

[0005] A drawback of this configuration, however, is the slow settling time of PLL 100. Generally, the slow settling time can be attributed to the low bandwidth, coarse tuning loop. Another drawback is the size of capacitor CCT, which is often very large in order to suppress the noise of amplifier 218. Due to these drawbacks, there are some systems where PLL 100 is undesirable. Therefore, there is a need for a PLL with improved performance characteristics.

[0006] Some other conventional circuits are described in: Wu et al., "A 4.2 GHz PLL Frequency Synthesizer with an Adaptively Tuned Coarse Loop", IEEE 2007 Custom Integrated Circuits Conference, pp. 547-550; Nonis et al., " Modeling, Design and Characterization of a New Low-Jitter Analog Dual Tuning LC-VCO PLL Architecture", IEEE Journal of Solid-State Circuits, Vol. 40, No. 6, June 2005, pp. 1303-1309; Perrott et al., "A 2.5-Gb/s Multi-Rate 0.25-μm CMOS Clock and Data Recovery Circuit Utilizing a Hybrid Analog/Digital Loop Filter and All-Digital Referenceless Frequency Acquisition", IEEE Journal of Solid-State Circuits, Vol. 41, No. 12, December 2006, pp. 2930-2944; U.S. Patent No. 6,658,748; U.S. Patent No. 6,952,124; U.S. Patent No. 7,015,763; U.S. Patent No. 7,133,485; U.S. Patent No. 7,301,407; U.S. Patent No. 7,385,452; U.S. Patent Publ. No. 2002/0008593; U.S. Patent Publ. No. 2003/0141936; U.S. Patent Publ. No. 2005/0212609; U.S. Patent Publ. No. 2005/0212614; U.S. Patent Publ. No. 2007/0057736; and datasheet for Texas Instruments Incorporated clock generator part no. CDCE421.

SUMMARY

[0007] An example embodiment of the invention, accordingly, provides an apparatus. The apparatus comprises a voltage controlled oscillator (VCO) having: a capacitive network that receives a first tuning voltage that is based at least in part on an input signal; and a switched capacitor array that is coupled to the capacitive network; an amplifier that receives the first tuning voltage and a reference voltage, wherein the amplifier amplifies the difference between the reference voltage and the first tuning voltage; a switch that receives the reference voltage and the amplified difference between the reference voltage and the first tuning voltage; a calibration capacitor that receives the output from the switch and generates a second tuning voltage; and a control loop that receives the input signal and the second tuning voltage, wherein the controller loop controls the switch so as to apply the reference voltage to the calibration capacitor when the

apparatus resets, and wherein the control loop controls the switched capacitor array so as to adjust the capacitance of the VCO to generally maintain phase and frequency lock.

[0008] In accordance with an example embodiment of the invention, the VCO further comprise an inductive network that is coupled to the capacitive network; and a VCO amplifier that is coupled to the capacitive network.

[0009] In accordance with an example embodiment of the invention, the control loop further comprises a precision lock detector; a window adjust circuit that is coupled to the precision lock detector; a narrow window circuit that is coupled to the window adjust circuit; a wide window adjust circuit that is coupled to the window adjust circuit; a divider that receives the input signal; a bang-bang controller that is coupled to the window adjust circuit and the divider; and a counter that is coupled to the bang-bang controller and the switched capacitor array.

[0010] In accordance with an example embodiment of the invention, the bang-bang controller further comprises a first comparator that having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first comparator is coupled to the switch, and wherein the second input terminal of the first comparator is coupled to the window adjust circuit; and a second comparator that having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the second comparator is coupled to the switch, and wherein the second input terminal of the second comparator is coupled to the window adjust circuit.

[0011] In accordance with an example embodiment of the invention, the bang-bang controller further comprises a first inverter that is coupled to the divider; a first flip-flop that is coupled to the output terminal of the first comparator and to the divider; a second inverter that is coupled between the first flip-flop and the counter; a second flip flop that is coupled to the first flip-flop and the first inverter; a third flip-flop that is coupled to the output terminal of the second comparator and the divider; a fourth flip-flop that is coupled to the third flip-flop and the first inverter; a first logic gate that is coupled to each of the third and fourth flip-flops and to the counter; and a second logic gate that is coupled to each of the first and second flip-flops and to the switch.

[0012] In accordance with an example embodiment of the invention, the first, second, third, and fourth flip-flops are D flip-flops.

[0013] In accordance with an example embodiment of the invention, the first and second logic gates are OR gates.

[0014] In accordance with an example embodiment of the invention, the switch is a multiplexer.

[0015] In accordance with an example embodiment of the invention, the switch is a single-pole double-throw switch.

[0016] In accordance with an example embodiment of the invention, an apparatus is provided. The apparatus comprises a phase/frequency detector (PFD) that receives an input signal; a charge pump that is coupled to the PFD; a loop filter that is coupled to the charge pump, wherein the loop filter generates a first tuning voltage; an amplifier that receives the first tuning voltage and a reference voltage; a switch having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal receives the reference voltage, and wherein the second input terminal is coupled to the amplifier; a calibration capacitor that is coupled to the output terminal of the switch, wherein the calibration capacitor generates a second tuning voltage; a VCO having: an inductive network that is coupled to the capacitive network; a capacitive network that is coupled to the inductive network, wherein the capacitive network is coupled to the loop filter and calibration capacitor so as to receive the first and second tuning voltages; a switched capacitor array that is coupled to the inductive network; and a VCO amplifier that is coupled to the inductive network; a divider that is coupled to the VCO and the PFD; and a control loop that receives the input signal and that is coupled to the switch, the calibration capacitor, and the switched capacitor array, wherein the controller loop controls the switch so as to apply the reference voltage to the calibration capacitor when the apparatus resets, and wherein he control loop controls the switched capacitor array so as to adjust the capacitance of the VCO to generally maintain phase and frequency lock.

[0017] In accordance with an example embodiment of the invention, an apparatus is provided. The apparatus comprises a PFD that receives an input signal; a charge pump that is coupled to the PFD; a loop filter that is coupled to the charge pump, wherein the loop filter generates a first tuning voltage; an amplifier that receives the first tuning voltage and a reference voltage; a switch having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal receives the reference voltage, and wherein the second input terminal is coupled to the amplifier; a calibration capacitor that is coupled to the output terminal

of the switch, wherein the calibration capacitor generates a second tuning voltage; a VCO having: an inductive network that is coupled to the capacitive network; a capacitive network that is coupled to the inductive network, wherein the capacitive network is coupled to the loop filter and calibration capacitor so as to receive the first and second tuning voltages; a switched capacitor array that is coupled to the inductive network; and a VCO amplifier that is coupled to the inductive network; a first divider that is coupled to the VCO and the PFD; and a control loop having: a precision lock detector that is coupled to the PFD; a first comparator that having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first comparator is coupled to the switch, and wherein the second input terminal of the first comparator is coupled to the window adjust circuit; a second comparator that having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the second comparator is coupled to the switch, and wherein the second input terminal of the second comparator is coupled to the window adjust circuit; a second divider that receives the input signal; a first inverter that is coupled to the second divider; a first D flip-flop that is coupled to the output terminal of the second comparator and to the divider; a second inverter that is coupled to the D first flip-flop; a second D flip flop that is coupled to the first D flip-flop and the first inverter; a third D flip-flop that is coupled to the output terminal of the third comparator and the divider; a fourth D flip-flop that is coupled to the third D flip-flop and the first inverter; a first OR gate that is coupled to each of the third and fourth D flip-flops; a second OR gate that is coupled to each of the first and second D flip-flops and to the second input terminal of the first comparator; and a counter that is coupled to the second inverter, the second OR gate, and the switched capacitor array.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Example embodiments are described with reference to accompanying drawings, wherein:

[0019] FIG. 1 is a circuit diagram of an example of a conventional PLL employing continuous calibration;

[0020] FIG. 2 is a circuit diagram of an example of a PLL with continuous and discrete controls in accordance with an example embodiment of the invention; and

[0021] FIG. 3 is a circuit diagram of a more detailed example of the bang-bang controller of FIG. 2.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0022] In FIG. 2, the reference numeral 200 generally designates a PLL in accordance with an example embodiment of the invention. PLL 200 is generally comprised of PFD 202, charge pump 204, loop filter 206, VCO 208, amplifier 218, switch S1, divider 220, and a control loop. The VCO 208 is generally comprised of an inductive network 210, a capacitive network 212, a switched capacitor array 214, and a VCO amplifier 216. The control loop is generally comprised of precision lock detector 222, narrow window circuit 226, wide window circuit 228, window adjust circuit 224, bang-bang controller 230, counter 232, and divider 234.

[0023] Generally, the PFD 202, charge pump 204, loop filter 206, VCO 208, and divider 220 operate as a high bandwidth loop to generate an output signal OUT from input signal similar to the high bandwidth loop of PLL 100. PFD 202 compares a feedback signal from divider 220 to the input signal IN to generate up and down signals for charge pump 204. The output from the charge pump 204 is filtered by loop filter 206 to generate a fine tuning voltage VF for capacitive network 212 of VCO 208, which operates an inductor-capacitor (LC) VCO. Additionally, amplifier 218 and calibration capacitor CCT generally operate as part of a low bandwidth loop similar to the low bandwidth loop of PLL 100.

[0024] In operation, though, the control loop of PLL 200 provides additional discrete time controls for VCO 208, which is unavailable with PLL 100. Typically, the control loop measures the coarse voltage VC and input signal IN so as to adjust the switched capacitor array 214 (which is generally comprised of metal-insulator-metal (MIM) capacitors) to generally assist in decreasing the settling time of PLL 200 (compared to PLL 100). This is generally accomplished by setting operational window(s) and making adjustments to the capacitor array when the PLL 200 is outside one of the operational windows.

[0025] Turning first to the precision lock detector 222, window adjust circuit 224, narrow window circuit 226, and wide window circuit 228, these circuits generally set an operational window for the PLL 200. Precision lock detector 222 is generally a very high accuracy lock detector that monitors the input phase error, while each of the narrow window circuit 226 and wide window circuit 228 specify a voltage window. For example, the narrow voltage window for the narrow window circuit 226 can be between about 0.8V and about 1.0V, while the wide voltage window for the wide window circuit 228 can be between about 0.5V to about 1.5V. Based on the lock detection from precision lock detector 222 and the voltage window from

circuit 226 and/or 228, the window adjust circuit 224 can set threshold voltages VH and VL for the bang-bang controller 230 to correspond to the wide voltage window or the narrow voltage window.

[0026] The term "bang-bang controller" is used to refer to an on-off controller (also called "hysteresis controller") that switches abruptly between two states based upon a monitored condition going above a high threshold value or going below a low threshold value. The term is often used in connection with control of a circuit that accepts a binary input, one state of which corresponds to an "on" state and one state of which corresponds to an "off" state.

[0027] When the PLL 200 is reset (which generally occurs when the coarse tuning voltage VC is outside of the wide voltage window or narrow voltage window, depending on which of the voltage windows is being used), the bang-bang controller 230 asserts a reset signal RESET for the precision lock detector 222, window adjust circuit 224, and switch S1. During reset, the precision lock detector 222 and window adjust circuit 224 reset the threshold voltages VH and VL to generally correspond to the narrow voltage window set by the narrow voltage window circuit 226, and switch S1 (which may be a single-pole double-throw switch or a multiplexer) is set to apply reference voltage REF to calibration capacitor CCT, the capacitive network (which is generally comprised of varactors). The time period for which RESET is asserted is determined by the period of the sampling clock signal provided by divider 234. During the reset period, capacitor CCT is charged to voltage VC=VREF. The voltage VREF is intended to be centered within the window set by VH and VL causing outputs of comparators 312 and 310 to be "0". Once VC is re-centered, the next rising edge of the sampling clock will end the RESET event, causing the bang-bang controller 230 to set switch S1 to apply the output of amplifier 218 to capacitor CCT, thus re-enabling the low bandwidth loop. A RESET event will also cause the bang-bang controller 230 to provide an up signal UP and a positive pulse on tune signal TUNE to clock counter 232, which controls the switched capacitor array 214. The logic level of signal UP determines whether the counter increments or decrements and whether the VCO frequency increases or decreases. If the RESET event was caused by VC rising above VH, then signal UP= logic HIGH and the VCO digital tuning frequency is increased. If the RESET event is caused by VC dropping below VL then UP=logic LOW and the digital tuning frequency word is decreased. So long as VC is between VL and VH, there will be no reset events and no positive edges on TUNE or any adjustment of counter 232.

[0028] At the end of the RESET period, the low bandwidth loop is again operational but with a new digital tuning word applied to the VCO. The loop will attempt to adjust VC to acquire phase lock with the new digital tuning word. If signal VC again crosses VH or VL another RESET event will occur and the digital tuning word will be adjusted accordingly. This process will repeat until the loop acquires phase lock with VC settled to a voltage between VL and VH using the narrow window settings. After the precision lock detector 222 senses phase lock has been attained, the window adjust circuit 224 adjusts the threshold voltages to correspond to the wide voltage window.

[0029] A reason for having two voltage windows is that it is often desirable to generally prevent the control loop from continuing to adjust (i.e., over a specified frequency or temperature range) once initial digital lock is achieved to avoid perturbation of the PLL 200 and resettling in the continuous (low bandwidth and high bandwidth) loops. This situation could occur if the coarse tuning voltage VC should settle on the edge of the narrow voltage window during initial lock. Under this condition it may take only a small amount of noise or temperature drift to trigger the band-band control loop. This condition can be generally avoided by adding hysteresis through the inclusion and use of the wide voltage window.

[0030] Turning to FIG 3, an example of the bang-bang controller can be seen in more detail. Typically, threshold voltages VH and VL (which generally correspond to the narrow voltage window or the wide voltage window) are applied to the negative input terminal of comparator 312 and the positive input terminal of 310, respectively, while the coarse tuning voltage VC is applied to the positive and negative input terminals of comparators 312 and 310. The output of comparators 312 and 310 are latched by D flip-flops 314 and 318 and 316 and 320. It is noted that flip-flops 314 and 318 are triggered by the rising edge of the sampling clock 234 while flip-flops 316 and 320 are triggered by the falling edge of the sampling clock 234 due to the inverter 322 thus making available (half sampling period) delayed versions of the comparator output signals for generation of the RESET, UP controls as well as the TUNE pulse for the counter 232 clock input.

[0031] When the tuning voltage VC rises above threshold voltage VH, the comparator 312 outputs a "1". This output is latched by D flip-flops 314 and 316 at the rising and falling edges of the sampling clock 234, respectively. Alternatively, if the coarse tuning voltage falls below threshold voltage VL, comparator 310 outputs a "1", which is latched by D flip-flop 318

and 320. Based on a "1" from comparator 312 or 314, OR gate 324 outputs a logic high signal or "1", which corresponds to an assertion of the reset signal RESET and a need to increment or decrement counter 232 and switched capacitor array 214 (so as to increase or decrease the VCO frequency). The decision to increment or decrement is based on the output of flip-flop 314 (a delayed sample of comparator 312), where a logic high output indicates the VH threshold has been crossed and that the VCO is too low in frequency. This indication is passed through inverter 328 to create signal UP which is applied to the UP/Down control of counter 232. Counter 232 also requires a positive going clock edge for up/down adjustment to take place. This is provided by the output of OR gate 326, corresponding to the tune pulse signal TUNE. A rising edge on TUNE occurs only once during any sampling period and only if VC should rise above VH or fall below VL. Furthermore, the half sampling period delay introduced by flip-flops 316 and 320 enables proper timing of the TUNE clock edge relative to signal UP (the counter up/down control) in order to ensure reliable operation of the counter 232.

[0032] It is noted that reliable operation of the band-bang controller 230 depends greatly on the robustness of the precision lock detector 222 which in turn relies on having low DC offset in the PFD 202 and charge pump 204. In the conventional single loop PLL, the charge pump output voltage is free to settle at any voltage within the supply rails resulting in sub-optimal DC offset performance. On the other hand, PLL's incorporating the low bandwidth loop will settle with charge pump voltage (VF) equal to voltage REF, which is typically placed at mid supply voltage, due to the high gain in amplifier 218. This is an advantageous condition as it greatly improves matching in the up/down current sources within the charge pump that are responsible for the offset problem. This in turn allows for the design of a higher precision lock detector than is possible using the single loop architecture. This important benefit of the low band width loop has been leveraged in implementing the bang-bang controller algorithm of PLL 200.

[0033] As a result of the configuration of PLL 200, several advantages over conventional PLLs can be realized. The total analog tuning range of VCO 208 can be reduced though the use of digitally controlled MIM capacitors within the switched capacitor array 214, and there is reduction in the fine and coarse tuning gains for VCO 208. Additionally, phase noise of VCO 208 can be improved by adjusting the ratio of non-linear tuning capacitors (e.g., varactors) to linear tuning capacitor (e.g., MIM capacitors). There is also a reduction of reference spurs and harmonics as well as the ability to reduce the VCO current for a given phase noise and reduce

current elsewhere within PLL 200 where current constrains the noise performance. There is also a decrease sensitivity to parastics, and the settling time is reduced over PLL 100.

[0034] Embodiments having different combinations of one or more of the features or steps described in the context of example embodiments having all or just some of such features or steps are intended to be covered hereby. Those skilled in the art will appreciate that many other embodiments and variations are also possible within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a voltage controlled oscillator (VCO) having:

a capacitive network that receives a first tuning voltage that is based at least in part on an input signal; and

a switched capacitor array that is coupled to the capacitive network;

an amplifier that receives the first tuning voltage and a reference voltage, wherein the amplifier amplifies the difference between the reference voltage and the first tuning voltage;

a switch that receives the reference voltage and the amplified difference between the reference voltage and the first tuning voltage;

a calibration capacitor that receives the output from the switch and generates a second tuning voltage; and

a control loop that receives the input signal and the second tuning voltage, wherein the controller loop controls the switch so as to apply the reference voltage to the calibration capacitor when the apparatus resets, and wherein the control loop controls the switched capacitor array so as to adjust the capacitance of the VCO to generally maintain phase and frequency lock.

2. The apparatus of Claim 1, wherein the VCO further comprises:

an inductive network that is coupled to the capacitive network; and

a VCO amplifier that is coupled to the capacitive network.

3. The apparatus of Claim 1, wherein the control loop further comprises:

a precision lock detector;

a window adjust circuit that is coupled to the precision lock detector;

a narrow window circuit that is coupled to the window adjust circuit;

a wide window adjust circuit that is coupled to the window adjust circuit;

a divider that receives the input signal;

an on-off controller that is coupled to the window adjust circuit and the divider; and

a counter that is coupled to the on-off controller and the switched capacitor array.

4. The apparatus of Claim 3, wherein the on-off controller further comprises:

a first comparator that having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first comparator is coupled to the switch, and wherein the second input terminal of the first comparator is coupled to the window adjust circuit; and

a second comparator that having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the second comparator is coupled to the switch, and wherein the second input terminal of the second comparator is coupled to the window adjust circuit.

5. The apparatus of Claim 4, wherein the on-off controller further comprises:

a first inverter that is coupled to the divider;

first flip-flop that is coupled to the output terminal of the first comparator and to the divider;

a second inverter that is coupled between the first flip-flop and the counter;

a second flip flop that is coupled to the first flip-flop and the first inverter;

a third flip-flop that is coupled to the output terminal of the second comparator and the divider;

a fourth flip-flop that is coupled to the third flip-flop and the first inverter;

a first logic gate that is coupled to each of the third and fourth flip-flops and to the counter; and

a second logic gate that is coupled to each of the first and second flip-flops and to the switch.

6. The apparatus of Claim 5, wherein the first, second, third, and fourth flip-flops are D flip-flops.

7. The apparatus of Claim 5, wherein the first and second logic gates are OR gates.

8. The apparatus of Claim 1, wherein the switch is a multiplexer.

9. An apparatus comprising:

a phase/frequency detector (PFD) that receives an input signal;

a charge pump that is coupled to the PFD;

a loop filter that is coupled to the charge pump, wherein the loop filter generates a first tuning voltage;

an amplifier that receives the first tuning voltage and a reference voltage;

a switch having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal receives the reference voltage, and wherein the second input terminal is coupled to the amplifier;

a calibration capacitor that is coupled to the output terminal of the switch, wherein the calibration capacitor generates a second tuning voltage;

a VCO having:

an inductive network that is coupled to the capacitive network;

a capacitive network that is coupled to the inductive network, wherein the capacitive network is coupled to the loop filter and calibration capacitor so as to receive the first and second tuning voltages;

a switched capacitor array that is coupled to the inductive network; and

a VCO amplifier that is coupled to the inductive network;

a divider that is coupled to the VCO and the PFD; and

a control loop that receives the input signal and that is coupled to the switch, the calibration capacitor, and the switched capacitor array, wherein the controller loop controls the switch so as to apply the reference voltage to the calibration capacitor when the apparatus resets, and wherein he control loop controls the switched capacitor array so as to adjust the capacitance of the VCO to generally maintain phase and frequency lock.

10. The apparatus of Claim 9, wherein the divider is first divider, and wherein the control loop further comprises:

a precision lock detector that is coupled to the PFD;

a window adjust circuit that is coupled to the precision lock detector;

a narrow window circuit that is coupled to the window adjust circuit;

a wide window adjust circuit that is coupled to the window adjust circuit;

a second divider that receives the input signal;

an on-off controller that is coupled to the window adjust circuit and the second divider; and

a counter that is coupled to the bang-bang controller and the switched capacitor array.

11. The apparatus of Claim 10, wherein the bang-bang controller further comprises:

a first comparator that having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first comparator is coupled to the switch, and wherein the second input terminal of the first comparator is coupled to the window adjust circuit; and

a second comparator that having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the second comparator is coupled to the switch, and wherein the second input terminal of the second comparator is coupled to the window adjust circuit.

12. The apparatus of Claim 11, wherein the bang-bang controller further comprises:

a first inverter that is coupled to the divider;

a first flip-flop that is coupled to the output terminal of the first comparator and to the divider;

a second inverter that is coupled between the first flip-flop and the counter;

a second flip flop that is coupled to the first flip-flop and the first inverter;

a third flip-flop that is coupled to the output terminal of the second comparator and the divider;

a fourth flip-flop that is coupled to the third flip-flop and the first inverter;

a first logic gate that is coupled to each of the third and fourth flip-flops and to the counter; and

a second logic gate that is coupled to each of the first and second flip-flops and to the switch.

13. The apparatus of Claim 12, wherein the first, second, third, and fourth flip-flops are D flip-flops; and wherein the first and second logic gates are OR gates.

14. An apparatus comprising:

a PFD that receives an input signal;

a charge pump that is coupled to the PFD;

a loop filter that is coupled to the charge pump, wherein the loop filter generates a first tuning voltage;

an amplifier that receives the first tuning voltage and a reference voltage;

a switch having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal receives the reference voltage, and wherein the second input terminal is coupled to the amplifier;

a calibration capacitor that is coupled to the output terminal of the switch, wherein the calibration capacitor generates a second tuning voltage;

a VCO having:

an inductive network that is coupled to the capacitive network;

a capacitive network that is coupled to the inductive network, wherein the capacitive network is coupled to the loop filter and calibration capacitor so as to receive the first and second tuning voltages;

a switched capacitor array that is coupled to the inductive network; and

a VCO amplifier that is coupled to the inductive network;

a first divider that is coupled to the VCO and the PFD; and

a control loop having:

a precision lock detector that is coupled to the PFD;

a first comparator that having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the first comparator is coupled to the switch, and wherein the second input terminal of the first comparator is coupled to the window adjust circuit;

a second comparator that having a first input terminal, a second input terminal, and an output terminal, wherein the first input terminal of the second comparator is coupled to

the switch, and wherein the second input terminal of the second comparator is coupled to the window adjust circuit;

a second divider that receives the input signal;

a first inverter that is coupled to the second divider;

a first D flip-flop that is coupled to the output terminal of the second comparator and to the divider;

a second inverter that is coupled to the D first flip-flop;

a second D flip flop that is coupled to the first D flip-flop and the first inverter;

a third D flip-flop that is coupled to the output terminal of the third comparator and the divider;

a fourth D flip-flop that is coupled to the third D flip-flop and the first inverter;

a first OR gate that is coupled to each of the third and fourth D flip-flops;

a second OR gate that is coupled to each of the first and second D flip-flops and to the second input terminal of the first comparator; and

a counter that is coupled to the second inverter, the second OR gate, and the switched capacitor array.

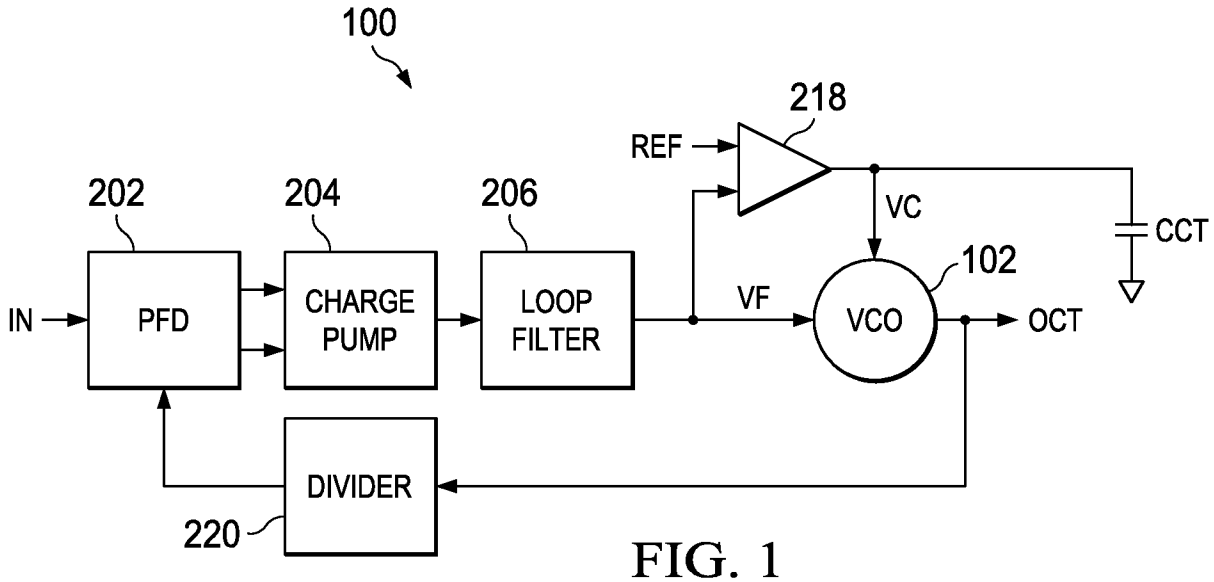

FIG. 1
(PRIOR ART)

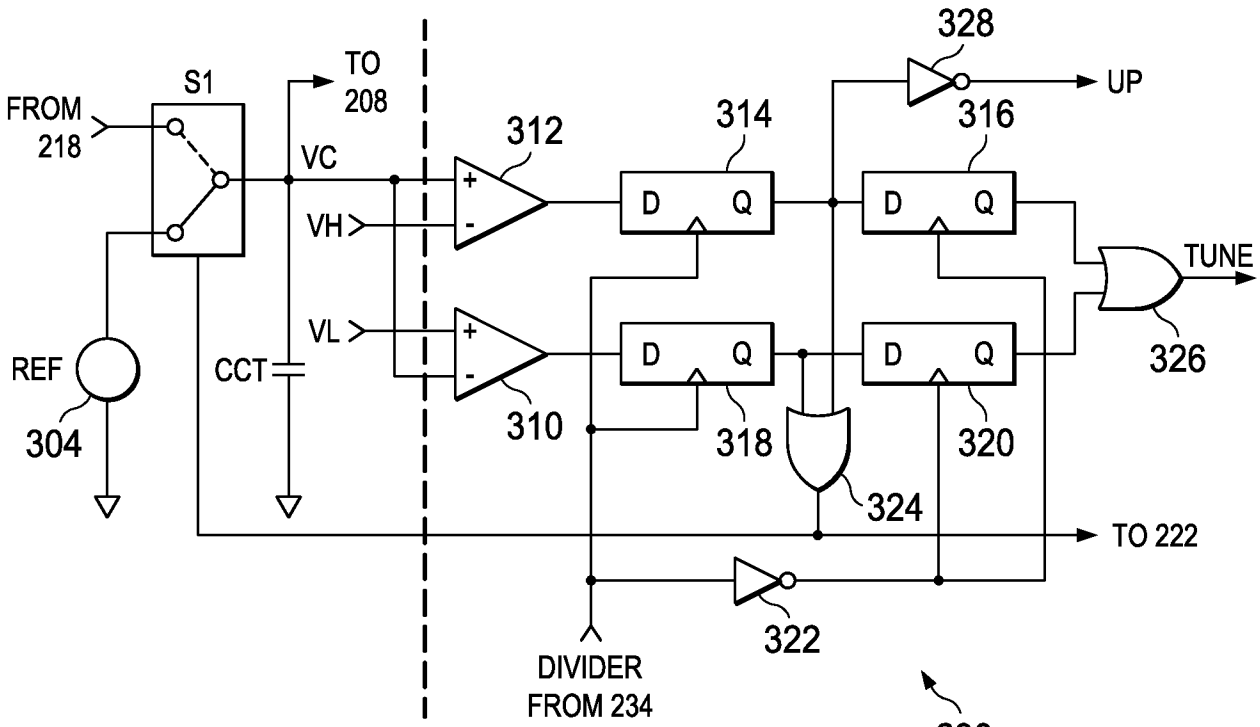

FIG. 3

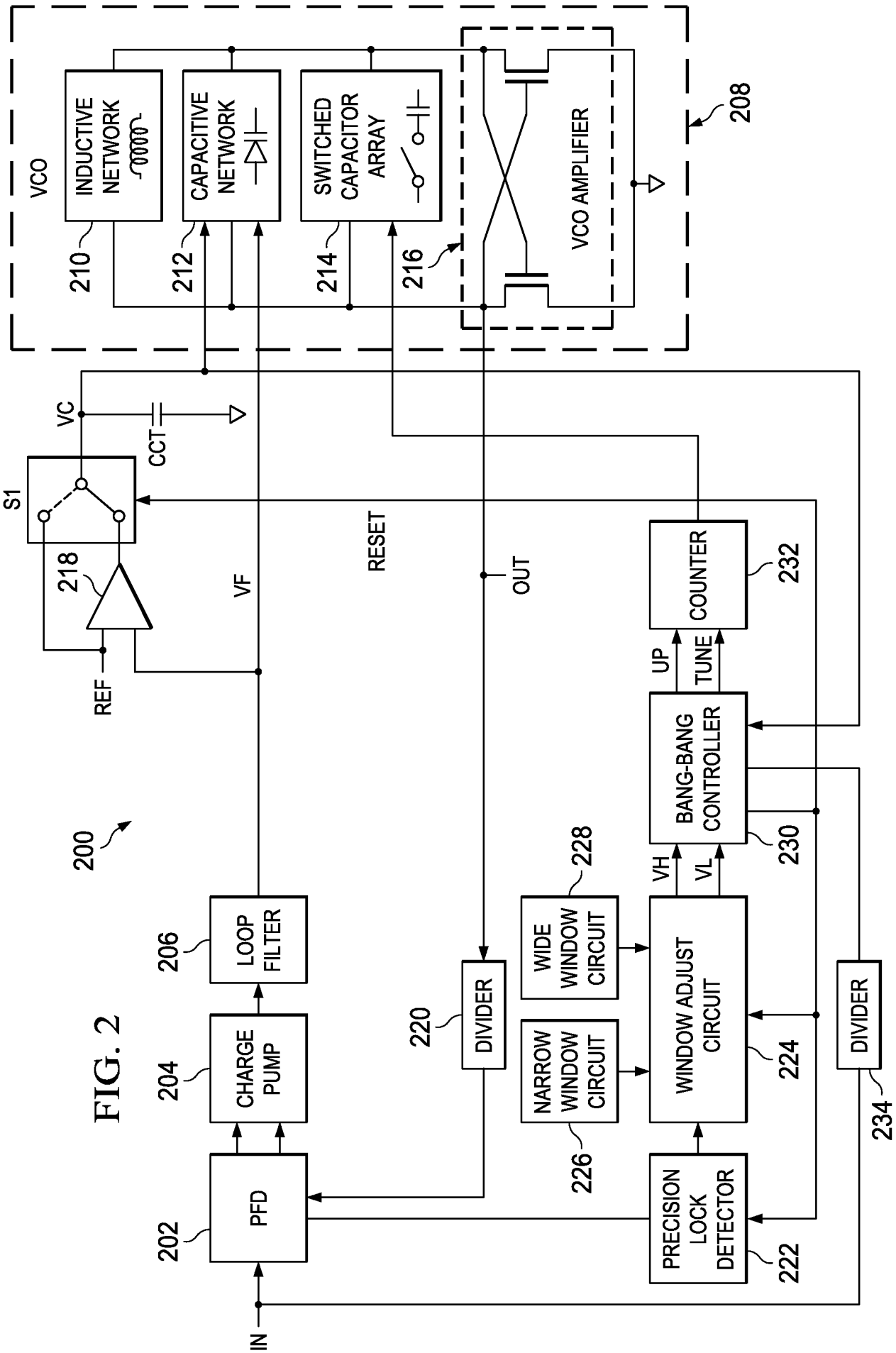
VCO
INDUCTIVE NETWORK
CAPACITIVE NETWORK
SWITCHED CAPACITOR ARRAY
VCO AMPLIFIER
208
210
212
214
216
VC
CCT
S1
218
REF
VF
RESET
OUT
COUNTER
232
UP
TUNE
BANG-BANG CONTROLLER
230
VH
VL
228
WIDE WINDOW CIRCUIT
NARROW WINDOW CIRCUIT
226
WINDOW ADJUST CIRCUIT
224
DIVIDER
220
DIVIDER
234
LOOP FILTER
206
CHARGE PUMP
204
PFD
202
PRECISION LOCK DETECTOR
222
IN
200

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/062022

A. CLASSIFICATION OF SUBJECT MATTER

H03L 7/099(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03L 7/099; H03D 3/24; H03L 7/06; H04B 1/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: switch, capacitor, array, phase, lock, control, reference

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7138839 B2 (Zachan et al.) 21 November 2006 See abstract; Fig 2; column 4, line 44-column 6, line 49	1-14
A	US 7010285 B2 (Dhuna) 07 March 2006 See abstract; Fig 4a, 4b; column 4, line 23-column 7, line 4	1-14
A	US 6952124 B2 (Pham) 04 October 2005 See abstract; Fig 3; column 3, line 1-column 4, line 19	1-14
A	US 7133485 B1 (Baird et al.) 07 November 2006 See abstract; Fig 2; column 4, line 57-column 5, line 35	1-14

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 AUGUST 2011 (08.08.2011)	**09 AUGUST 2011 (09.08.2011)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer KIM, Ki Wan Telephone No. 82-42-481-5682

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2010/062022

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