STRUCTURE AND METHOD OF FORMING SILICIDE ON FINS

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ABSTRACT

Embodiments of the invention provide a semiconductor structure and a method of forming a semiconductor structure. Embodiments of the semiconductor structure have a plurality of fins on a substrate. The semiconductor has, and the method achieves, a silicide layer formed on and substantially surrounding at least one epitaxial region formed on a top portion of the plurality of fins. Embodiments of the present invention provide a method and structure for forming a conformal silicide layer on the epitaxial regions that are formed on the top portion of unmerged fins of a finFET.
STRUCTURE AND METHOD OF FORMING SILICIDE ON FINS

FIELD OF THE INVENTION

The present invention relates generally to semiconductor fabrication, and more particularly, to a structure and method for forming silicide on semiconductor fins.

BACKGROUND

As integrated circuits continue to scale downward in size, the finFET (fin field effect transistor) is becoming attractive for use with modern semiconductor devices. In a finFET, the channel is formed by a semiconductor vertical fin (as compared with a planar channel in a conventional CMOS), and a gate electrode is located and wrapped around the vertical fin. Creating a contact with the fin having the proper density is of serious concern for device operation. Reducing contact resistance is critical to improvement of speed of device operation. It is therefore desirable to have improved methods and structures to improve finFET performance.

SUMMARY

In one aspect, embodiments of the present invention provide a method of forming a semiconductor structure, having the steps of: forming a plurality of silicon fins on a silicon substrate; depositing a high-K dielectric layer on the silicon substrate adjacent to each fin of the plurality of fins; forming at least one epitaxially grown silicon region on an upper portion of each fin of the plurality of fins, wherein the plurality of fins are unmerged; depositing a seed metal layer on the high-K dielectric layer; depositing an interspersing fill metal on the seed metal layer and on the at least one epitaxially grown silicon region; and forming a silicide of the interspersing fill metal on the at least one epitaxially grown silicon regions.

In another aspect, embodiments of the present invention provide a method of forming a semiconductor structure, having the steps of: forming a plurality of silicon fins on a silicon substrate; depositing a high-K dielectric layer on the substrate adjacent to each fin of the plurality of fins; forming at least one epitaxially grown silicon region on an upper portion of each fin of the plurality of fins, wherein the plurality of fins are unmerged; forming a metal gate on the silicon substrate; depositing a seed metal layer on the high-K dielectric layer; depositing an interspersing fill metal on the seed metal layer; depositing a metal layer comprised of the interspersing fill metal on the at least one epitaxially grown silicon region; and forming a silicide of the interspersing fill metal on the at least one epitaxially grown silicon region.

In yet another aspect, embodiments of the present invention provide a semiconductor structure, having a silicon substrate; a plurality of silicon fins formed in the silicon substrate; an epitaxial region formed on a top portion of each of the plurality of fins, wherein the plurality of fins are unmerged; and a silicide layer formed on, and substantially surrounding, each epitaxial region.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate several embodiments of the present teachings and together with the description, serve to explain the principles of the present teachings.
FIG. 19 is a semiconductor structure as viewed along line Z-Z' of FIG. 1, after subsequent processing steps of depositing a second layer of ILD.

FIG. 20 is a flowchart indicating process steps for embodiments of the present invention.

DETAILED DESCRIPTION

Illustrative embodiments will now be described more fully herein with reference to the accompanying drawings, in which embodiments are shown. This disclosure may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete and will fully convey the scope of this disclosure to those skilled in the art. In the description, details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the presented embodiments.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of this disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. Furthermore, the use of the terms "a", "an", etc., do not denote a limitation of quantity, but rather denote the presence of at least one of the referenced items. The term "set" is intended to mean a quantity of at least one. It will be further understood that the terms "comprises" and/or "comprising," or "includes" and/or "including," when used in this specification, specify the presence of stated features, regions, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, regions, integers, steps, operations, elements, components, and/or groups thereof.

Reference throughout this specification to "one embodiment," "an embodiment," "embodiments," "exemplary embodiments," "some embodiments," or similar language means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment," "in an embodiment," "in embodiments," "in some embodiments," and similar language throughout this specification may, but do not necessarily, all refer to the same embodiment.

The terms "overlaying" or "atop," "positioned on," "positioned atop," or "disposed on," "underlying," "beneath" or "below" mean that a first element, such as a first structure (e.g., a first layer) is present on a second element, such as a second structure (e.g., a second layer) wherein intervening elements, such as an interface structure (e.g. interface layer) may be present between the first element and the second element.

Embodiments of the present invention provide an improved method of finFET fabrication and corresponding structure. There are various applications where it is desirable to have unmerged fins (fins that are not joined together by an epitaxial region), for example in SRAM applications. Proper contact formation is important to reduce resistance and improve device operation speed. Epitaxial regions are formed on the upper portion of fins to provide a larger contact surface. However, prior art processes cannot form a good conformal silicide on the epitaxial regions of unmerged fins. Embodiments of the present invention provide a method and structure for forming a conformal silicide layer on the epitaxial regions that are formed on the top portion of unmerged fins of a finFET.

FIG. 1 is a perspective view of an example fin type field effect transistor (finFET) semiconductor structure 100. The semiconductor structure 100 comprises a silicon substrate 102 having thereon fins 104a and 104b, which are formed from an SOI layer. Further shown is a gate 106. It should be recognized that although two fins and one gate is shown, in some embodiments, more or fewer fins per transistor may be present. In some embodiments, the plurality of fins each have a pitch ranging from about 20 nanometers (nm) to about 60 nm. In some embodiments, the fins each have a thickness ranging from about 5 nm to about 20 nm. It should be recognized that the pitch range and thickness range are examples, and any suitable pitch or thickness is included within the scope of the invention.

FIG. 2 is a semiconductor structure as viewed along line X-X' of FIG. 1, after subsequent processing steps of forming a first silicon oxide layer 108 over the silicon substrate. To form the structure, a hard mask of silicon nitride is deposited on the substrate, and fins then formed using industry standard techniques, such as sidewall image transfer (SIT), resulting in the fins 102a, 102b with a hard mask layer 110 disposed over each fin.

FIG. 3 is a semiconductor structure as viewed along line X-X' of FIG. 1, after subsequent processing steps of forming a high-K dielectric layer 112 over the first silicon oxide layer 108 and the silicon nitride hard mask layer 110 over the fins 102a and 102b. In some embodiments, the high-K dielectric layer 112 is hafnium oxide (HfO2). In some embodiments, the high-K layer is zirconium dioxide (ZrO2). In some embodiments, the high-K dielectric layer 112 is deposited by a horizontal deposition process, such as physical vapor deposition. With a horizontal deposition process, the high-K dielectric layer 112 deposits on horizontal surfaces adjacent to fins 104a and 104b, but does not substantially deposit on the sides of the fins 104a and 104b.

FIG. 4 is a semiconductor structure as viewed along line X-X' of FIG. 1, after subsequent processing steps of forming a second silicon oxide layer 114 over the high-K dielectric layer 112. In some embodiments, the second silicon oxide layer is deposited via a chemical vapor deposition process, and then planarized (e.g. via a chemical mechanical polish process), followed by a recess, such as a chemical oxide removal (COR) process.

FIG. 5 is a semiconductor structure as viewed along line X-X' of FIG. 1, after subsequent processing steps of removing various layers. In some embodiments, the high-K dielectric layer 112 and the hard mask 110 are removed from over the fins 102a and 102b.

FIG. 6 is a semiconductor structure as viewed along line X-X' of FIG. 1, after a subsequent processing step of removing the second silicon oxide layer 114 (FIG. 5) and then depositing a conformal oxide layer 116 over the fins 102a and 102b and the high-K dielectric layer 112. In some embodiments, the deposition is performed by a chemical vapor deposition process.

FIG. 7 is a semiconductor structure as viewed through the gate, along line Y-Y' of FIG. 1, after subsequent processing steps of depositing a polysilicon material and patterning it to form gate 118. In some embodiments, the gate 118 is formed by etching using a reactive ion etch process. It should be recognized that any suitable etch may be substi-
the first metal layer 130 comprises aluminum. In some embodiments, the first metal layer 130 comprises titanium.

[0047] FIG. 15 is a semiconductor structure as viewed along line X-X’ of FIG. 1, after subsequent processing steps of depositing a second metal layer 132 over the epitaxial regions 121. In some embodiments, the second metal layer 132 comprises at least one of nickel or platinum. In embodiments, the second metal layer 132 may be formed of the same material as metal layer 130. In some embodiments, the second metal layer 132 may be formed from a different material as metal layer 130. In some embodiments, the deposition is performed by physical vapor deposition.

[0048] FIG. 16 is a semiconductor structure as viewed along line X-X’ of FIG. 1, after subsequent processing steps of annealing the structure to form silicide regions 134, and, optionally, then removing a portion of at least one of the noble metal seed layer 128 and the first metal layer 130. In some embodiments, the annealing is performed at approximately 400-600 degrees Celsius for a duration of approximately 5 to 60 seconds. The metal layers (128 and 130 of FIG. 14) are removed from the structure, leaving a silicide layer 134 formed on the surfaces of the epitaxial regions 121. In some embodiments, the removing may be done by an etching process using aqua regia (nitro-hydrochloric acid). In some embodiments, the silicide is nickel silicide. As a result of this process, the silicide regions 134 formed on, and substantially surrounding, each epitaxial region 121.

[0049] FIGS. 17-19 show views of a semiconductor structure after depositing a second interlayer dielectric (ILD) 136. FIG. 17 is a semiconductor structure as viewed along line X-X’ of FIG. 1, after subsequent processing steps of depositing a second inter-layer dielectric 136. FIG. 18 is a semiconductor structure as viewed along line Y-Y’ of FIG. 1, after subsequent processing steps of depositing a second inter-layer dielectric 136. FIG. 19 is a semiconductor structure as viewed along line Z-Z’ of FIG. 1, after subsequent processing steps of depositing a second inter-layer dielectric 136.

[0050] FIG. 20 is a flowchart of a method according to exemplary embodiments of the present invention. At 202, a first silicon oxide layer is deposited over the silicon substrate. At 204, a high-K layer is deposited over the first silicon oxide layer by a horizontal deposition process. At 206, a second silicon oxide layer is formed over the high-K layer. At 208, the first silicon oxide layer and high-K layer are removed from over the fins of the FinFET. At 210, the second silicon oxide layer is removed. At 212, a conformal oxide layer is deposited. At 214, a dummy gate is formed. At 216, gate spacers are formed. At 218, an ILD is deposited. At 220, a replacement metal gate process is performed. At 222, the ILD is removed. At 224, a noble seed metal layer is deposited and grown. At 226, a first metal layer is deposited over the seed layer. At 228, a second metal layer is deposited over the epitaxial regions. Typically, the material used in step 228 is a similar material to that used in step 226. For example, if nickel is used in step 226, then nickel may also be used in step 228, even though the deposition processes are different for those two steps. At 230, annealing is performed to form silicide. At 232, optionally, at least one seed metal layer, the first metal layer, and second metal layer is removed.

[0051] While the invention has been particularly shown and described in conjunction with exemplary embodiments, it will be appreciated that variations and modifications will occur to those skilled in the art. For example, although the illustrative embodiments are described herein as a series of acts or events, it will be appreciated that the present invention...
is not limited by the illustrated ordering of such acts or events unless specifically stated. Some acts may occur in different orders and/or concurrently with other acts or events apart from those illustrated and/or described herein, in accordance with the invention. In addition, not all illustrated steps may be required to implement a methodology in accordance with the present invention. Furthermore, the methods according to the present invention may be implemented in association with the formation and/or processing of structures illustrated and described herein as well as in association with other structures not illustrated. Therefore, it is to be understood that the appended claims are intended to cover all such modifications and changes that fall within the true spirit of the invention.

1. - 16. (canceled)

17. A semiconductor structure, comprising
   a silicon substrate;
   a plurality of silicon fins formed in the silicon substrate;
   an epitaxial region formed on a top portion of each of the
   plurality of fins, wherein the plurality of fins are
   unmerged; and
   a silicide layer formed on, and substantially surrounding,
   each epitaxial region.

18. The semiconductor structure of claim 17, wherein the
    silicide layer comprises nickel silicide.

19. The semiconductor structure of claim 17, wherein the
    plurality of fins have a pitch ranging from about 20 nanometers to about 60 nanometers.

20. The semiconductor structure of claim 17, wherein the
    plurality of fins each have a thickness ranging from about 5 nanometers to about 20 nanometers.

21. The semiconductor structure of claim 17, further comprising a high-K dielectric layer on the silicon substrate adjacent to each fin of the plurality of fins.

22. The semiconductor structure of claim 21, wherein the
    high-K dielectric layer comprises HfO2.

23. The semiconductor structure of claim 21, wherein the high-K dielectric layer comprises ZrO2.

24. The semiconductor structure of claim 21, further comprising an interlayer dielectric (ILD) formed on the high-K dielectric layer and a top portion of the silicide layer.

25. The semiconductor structure of claim 17, wherein the silicide layer comprises tungsten silicide.

26. A semiconductor structure, comprising
   a silicon substrate;
   a plurality of silicon fins formed in the silicon substrate;
   a metal gate formed on the silicon substrate;
   an epitaxial region formed on a top portion of each of the
   plurality of fins, wherein the plurality of fins are
   unmerged; and
   a silicide layer formed on, and substantially surrounding,
   each epitaxial region.

27. The semiconductor structure of claim 25, wherein the silicide layer comprises nickel silicide.

28. The semiconductor structure of claim 25, wherein the silicide layer comprises tungsten silicide.

29. The semiconductor structure of claim 25, wherein the plurality of fins have a pitch ranging from about 20 nanometers to about 60 nanometers.

30. The semiconductor structure of claim 25, wherein the plurality of fins each have a thickness ranging from about 5 nanometers to about 20 nanometers.

31. The semiconductor structure of claim 25, further comprising a high-K dielectric layer on the silicon substrate adjacent to each fin of the plurality of fins.

32. The semiconductor structure of claim 30, wherein the high-K dielectric layer comprises HfO2.

33. The semiconductor structure of claim 30, wherein the high-K dielectric layer comprises ZrO2.

34. The semiconductor structure of claim 30, further comprising an interlayer dielectric (ILD) formed on the high-K dielectric layer and a top portion of the silicide layer.

35. The semiconductor structure of claim 25, further comprising a nitride cap on the top and sides of the metal gate.

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