



(51) International Patent Classification:
G06F 9/44 (2006.01) **G06F 17/50** (2006.01)
G06F 11/34 (2006.01)

(21) International Application Number:
PCT/US2010/030219

(22) International Filing Date:
7 April 2010 (07.04.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/433,203 30 April 2009 (30.04.2009) US

(71) Applicant (for all designated States except US): **SYNOPTICS, INC.** [US/US]; 700 E. Middlefield Road, Mountain View, CA 94043 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **SOVIANI, Cristian** [RO/US]; 3500 Granada Avenue #180, Santa Clara, California 95051 (US). **HELAIHEL, Rachid, N.** [LB/US]; 750 N. Shoreline Blvd. #136, Mountain View, California

94043 (US). **RAHMAT, Khalid** [US/US]; 44609 Parkmeadow Drive, Fremont, California 94539 (US).

(74) Agent: **YAO, Shun**; Park, Vaughan & Fleming LLP, 2820 Fifth Street, Davis, California 95618-7759 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,

[Continued on next page]

(54) Title: EFFICIENT EXHAUSTIVE PATH-BASED STATIC TIMING ANALYSIS USING A FAST ESTIMATION TECHNIQUE

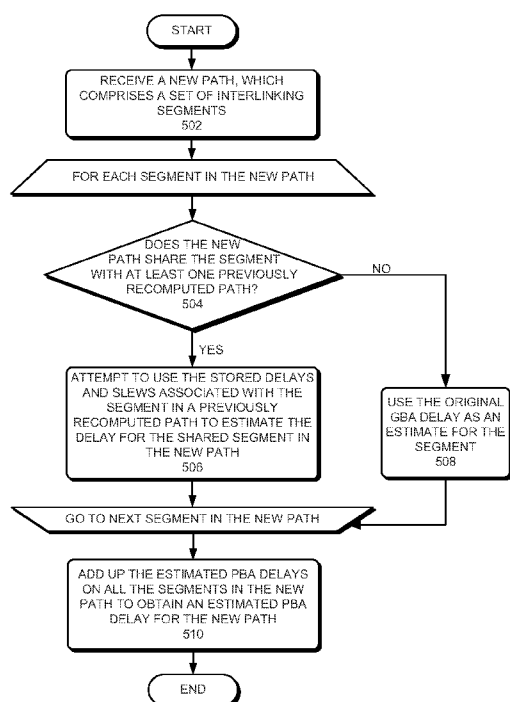


FIG. 5

(57) Abstract: Techniques and systems are described for performing efficient path-based static timing analysis (STA) in a circuit design. During operation, the system identifies a set of paths within the circuit design, wherein each path includes one or more segments. For a path in the set of paths, the system determines if at least one segment in the path is shared with a different path which was previously computed by performing a path-based STA, wherein the at least one segment in the different path is associated with previously computed path-based timing information. If so, the system then performs an estimation of a path-based delay for the path based at least on the path-based timing information associated with the shared segment in the different path. Otherwise, the system computes a path-based delay for the path by performing a path-based STA on the path.



MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
ML, MR, NE, SN, TD, TG).

— *before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments (Rule 48.2(h))*

Published:

— *with international search report (Art. 21(3))*

(88) Date of publication of the international search report:

13 January 2011

A. CLASSIFICATION OF SUBJECT MATTER**G06F 9/44(2006.01)i, G06F 11/34(2006.01)i, G06F 17/50(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 9/44; G06F 17/50; G06F 9/45

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal), NDSL, Google & Keywords: circuit design, IC layout, timing analysis, STA, static, path-based, delay, slack, shar*, common

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7278126 B2 (SUN, Y et al.) 02 October 2007 See figures 3,9; column 5, lines 36-67, column 7, lines 50-55, column 13, lines 13-24, column 15, lines 10-17, column 4, lines 42-44.	1-25
A	US 2008-0209372 A1 (BUCK, NATHAN C. et al.) 28 August 2008 See summary; figure 1; claim 1.	1-25
A	US 2008-0270962 A1 (CHADWICK, THOMAS B. et al.) 30 October 2008 See figure 2; claim 1.	1-25
A	US 7404163 B2 (CHADWICK, JR. THOMAS B. et al.) 22 July 2008 See summary; figure 2; claim 1.	1-25
A	Agarwal, A. et al. 'Path-Based Statistical Timing Analysis Considering Inter- and Intra-Die Correlations.' In:Proc. TAU, pp.16-21, 2002 See abstract.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

12 NOVEMBER 2010 (12.11.2010)

Date of mailing of the international search report

12 NOVEMBER 2010 (12.11.2010)

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
Government Complex-Daejeon, 139 Seonsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

YOON, Hye Sook

Telephone No. 82-42-481-8370



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2010/030219

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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