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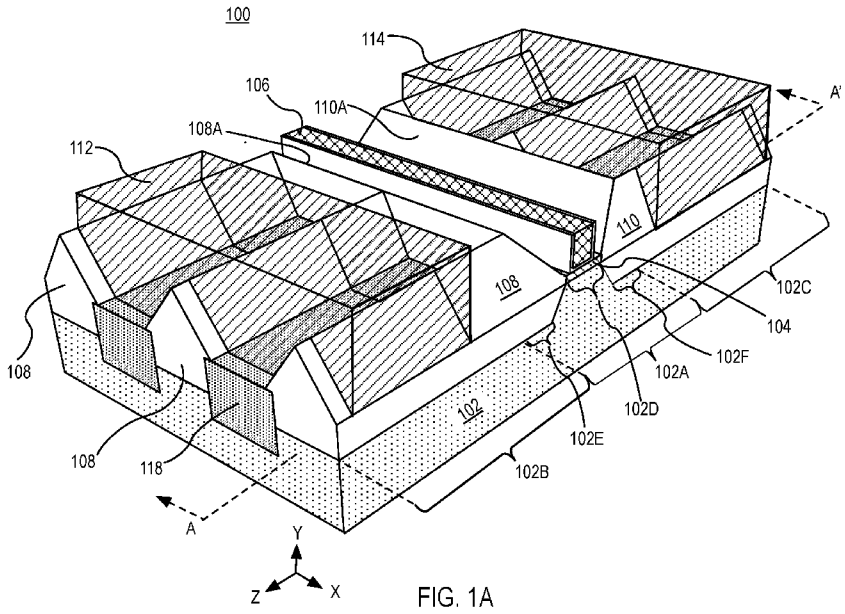


FIG. 1A

(57) Abstract: A device including a III-N material is described. In an example, the device has terminal structure having a first group III-Nitride (III-N) material. The terminal structure has a central body and a first plurality of fins, and a second plurality of fins, opposite the first plurality of fins. A polarization charge inducing layer is above a first portion of the central body. A gate electrode is above the polarization charge inducing layer. The device further includes a source structure and a drain structure, each including impurity dopants, on opposite sides of the gate electrode and on the plurality of fins, and a source contact on the source structure and a drain contact on the drain structure.

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GROUP III-NITRIDE (III-N) DEVICES WITH REDUCED CONTACT RESISTANCE AND THEIR METHODS OF FABRICATION

BACKGROUND

In the fields of wireless communication and power management, various components can be implemented using solid-state devices. For example, in radio frequency (RF) communication, the RF front-end is a generic term for the circuitry between an antenna and a digital baseband system. Such RF front-end components may include one or more diodes in conjunction with one or more transistors, such as one or more field-effect transistors (FETs). Due, in part, to their large bandgap and high mobility, gallium nitride (GaN) and other group III-nitride (III-N) materials are suited for integrated circuits for applications such as high-frequency and high-power.

For many non-silicon materials, it can be challenging to provide doped semiconductor material suitable for making a good ohmic contact. Contact structures and techniques to reduce contact resistance and sheet resistance may advantageously reduce overall device resistance to enhance device performance and/or reduce device power consumption.

BRIEF DESCRIPTION OF THE DRAWINGS

The material described herein is illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, elements illustrated in the figures are not necessarily drawn to scale. For example, the dimensions of some elements may be exaggerated relative to other elements for clarity. Also, various physical features may be represented in their simplified "ideal" forms and geometries for clarity of discussion, but it is nevertheless to be understood that practical implementations may only approximate the illustrated ideals. For example, smooth surfaces and square intersections may be drawn in disregard of finite roughness, corner-rounding, and imperfect angular intersections characteristic of structures formed by nanofabrication techniques. Further, where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

Figure 1A illustrates an isometric view of a group III-N transistor having a source and drain structures with enhanced surface area, in accordance with embodiments of the present disclosure.

Figure 1B illustrates a plan view of a terminal structure with a first and a second plurality of fins, in accordance with embodiments of the present disclosure.

Figure 1C illustrates a cross-sectional view of a contact structure in contact with a source structure having sidewalls that intersect at an apex, in an accordance with an embodiment of the present disclosure.

Figure 1D illustrates a cross-sectional view of a contact structure in contact with a source structure having sidewalls that intersect over a spacer separating portions of the source structure, in an accordance with an embodiment of the present disclosure

Figure 1E illustrates a cross-sectional view of a contact structure in contact with a source structure having an upper surface area with corrugation, in an accordance with an embodiment of the present disclosure.

Figure 1F illustrates a cross-sectional view of a group III-N transistor having a source structure and a drain structure with enhanced surface area, in an accordance with an embodiment of the present disclosure.

Figures 2A illustrates a plan view of a patterned polarization charge inducing layer on a patterned III-N material, in an accordance with an embodiment of the present disclosure.

Figures 2B illustrates a cross-sectional view of a patterned polarization charge inducing layer on a patterned III-N material, in an accordance with an embodiment of the present disclosure.

Figure 3A illustrates a plan view of the structure of Figure 2A following the formation of isolation structures surrounding the patterned polarization charge inducing layer and the patterned III-N material.

Figure 3B illustrates a plan view of the structure of Figure 2B following the formation of isolation structures surrounding the patterned polarization charge inducing layer and the patterned III-N material.

Figure 4A illustrates a plan view of the structure of Figure 3A following the formation of trenches in portions of the polarization charge inducing layer, and in portions of the III-N material adjacent to the isolation structures.

Figure 4B illustrates a cross-sectional view of the structure of Figure 3B following the formation of trenches in portions of the polarization charge inducing layer, and in portions of the III-N material adjacent to the isolation structures.

Figure 5A illustrates a plan view of the structure of Figure 4A following the formation of drain structures and source structures in the trenches.

Figure 5B illustrates a cross-sectional view of the structure of Figure 4B following the formation of drain structures and source structures in the trenches.

Figure 5C illustrates a cross-sectional view of a source structure formed on a plurality of fins.

Figure 6A illustrates a plan view of the structure of Figure 5A following the deposition of a dielectric layer on the source structure, drain structure and on the polarization charge inducing layer.

Figure 6B illustrates a cross-sectional view of the structure of Figure 5B following the deposition of a dielectric layer on the source structure, drain structure and on the polarization charge inducing layer.

Figure 7A illustrates a plan view of the structure of Figure 6A following the formation of an opening in the dielectric layer over a portion of the polarization charge inducing layer.

Figure 7B illustrates a cross-sectional view of the structure of Figure 6B following the formation of an opening in the dielectric layer over a portion of the polarization charge inducing layer.

Figure 8A illustrates a plan view of the structure of Figure 7A following the formation of a gate in the opening and on the polarization charge inducing layer.

Figure 8B illustrates a cross-sectional view of the structure of Figure 7B following the formation of a gate in the opening and on the polarization charge inducing layer

Figure 9A illustrates a plan view of the structure of Figure 8A following the formation of drain and source contact openings above the drain structures and source structures.

Figure 9B illustrates a cross-sectional view of the structure of Figure 8B following the formation of drain and source contact openings above the drain structures and source structures.

Figure 10A illustrates a plan view of the structure of Figure 9A following the formation of drain contact and source contact in the openings.

Figure 10B illustrates cross-sectional views of the structure of Figure 9Bfollowing the formation of drain contact and source contact in the openings.

Figure 10C illustrates a cross-sectional view of a source contact formed on a source structure formed on a plurality of fins.

Figure 11 is a functional block diagram of a group III-N SoC implementation of a mobile computing platform, in accordance with an embodiment of the present disclosure.

Figure 12 illustrates a computing device in accordance with embodiments of the present disclosure.

Figure 13 illustrates an integrated circuit structure in accordance with embodiments of the present disclosure.

DESCRIPTION OF THE EMBODIMENTS

Devices including III-N materials for logic, SoC and memory applications and their methods of fabrication are described. In the following description, numerous specific details are

set forth, such as novel structural schemes and detailed fabrication methods in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known features, such as enhancement mode operations associated with group III-N devices, are described in lesser detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as "upper", "lower", "above", and "below" refer to directions in the drawings to which reference is made. Terms such as "front", "back", "rear", and "side" describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

In the following description, numerous details are set forth. However, it will be apparent to one skilled in the art, that the present disclosure may be practiced without these specific details. In some instances, well-known methods and devices are shown in block diagram form, rather than in detail, to avoid obscuring the present disclosure. Reference throughout this specification to "an embodiment" or "one embodiment" or "some embodiments" means that a particular feature, structure, function, or characteristic described in connection with the embodiment is included in at least one embodiment of the disclosure. Thus, the appearances of the phrase "in an embodiment" or "in one embodiment" or "some embodiments" in various places throughout this specification are not necessarily referring to the same embodiment of the disclosure. Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

As used in the description and the appended claims, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will also be understood that the term "and/or" as used herein refers to and encompasses any and all possible combinations of one or more of the associated listed items.

The terms "coupled" and "connected," along with their derivatives, may be used herein to describe functional or structural relationships between components. It should be understood that

these terms are not intended as synonyms for each other. Rather, in particular embodiments, "connected" may be used to indicate that two or more elements are in direct physical, optical, or electrical contact with each other. "Coupled" may be used to indicated that two or more elements are in either direct or indirect (with other intervening elements between them) physical or electrical contact with each other, and/or that the two or more elements co-operate or interact with each other (e.g., as in a cause an effect relationship).

The terms "over," "under," "between," and "on" as used herein refer to a relative position of one component or material with respect to other components or materials where such physical relationships are noteworthy. For example, in the context of materials, one material or material disposed over or under another may be directly in contact or may have one or more intervening materials. Moreover, one material disposed between two materials may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first material "on" a second material is in direct contact with that second material/material. Similar distinctions are to be made in the context of component assemblies.

As used throughout this description, and in the claims, a list of items joined by the term "at least one of" or "one or more of" can mean any combination of the listed terms. For example, the phrase "at least one of A, B or C" can mean A; B; C; A and B; A and C; B and C; or A, B and C.

In the fields of wireless communication and power management, various components can be implemented using solid-state devices. For example, in radio frequency (RF) communication, the RF front-end is a generic term for the circuitry between an antenna and a digital baseband system. Such RF front-end components may include one or more transistors, such as one or more field-effect transistors (FETs). Due, in part, to their large bandgap and high mobility, gallium nitride (GaN) and other III-N materials are suited for integrated circuits for applications such as high-frequency and high-power. However, optimizing power efficiency of RF-front end components and minimizing energy loss during operation is highly desirable. Devices such as transistors fashioned from III-N materials, may be susceptible to energy loss from various sources such as from conduction and switching losses. The latter is affected by the transition between "on" and "off" states during device operation. In particular, transitioning between on and off states of the transistor may be affected by resistances within the device. Device resistances include internal resistances associated carrier mobility within the channel material, and external resistances between the channel material and external contacts associate with source and drain resistances and metal-semiconductor junction resistances. III-N channels generally have high carrier mobility, but to fully capitalized on this attribute, external resistance should be

minimized. Thus, pathways to minimize contact resistance are especially attractive for practical realization of devices based on III-N materials.

In an embodiment of the present disclosure, a device, such as a transistor including a III-N material, has a central body and a first plurality of fins adjacent to a first side of the central body, and a second plurality of fins adjacent to a second side of the central body. A gate is disposed above the III-N material. The device further includes a source structure and a drain structure each having an impurity dopant on opposite sides of the gate electrode. In an embodiment, the source structure is epitaxially grown above the first plurality of fins, and the drain structure is epitaxially grown above the second plurality of fins. A source contact is disposed on the source structure and a drain contact is disposed on the drain structure. The inventors have discovered that when the epitaxially grown source and drain structures are formed on fins that are fashioned from a III-N material, the 3D nature of epi growth, is more pronounced leading to a larger effective surface area than that obtained from a single continuous source or a drain structure spanning a same foot print as the fin structure. The source and drain contacts, consequently have a larger area to contact the epitaxially grown 3D source and drain structures, respectively. An effective increase in contact area between the source contact and the source structure and between the drain contact and the drain structure can reduce the contact resistance of the transistor by as much as 70%. By reducing the contact resistance of the transistor, the external resistance of a III-N transistor may be reduced.

Figure 1A illustrates an isometric view of a device 100, such as a group III-N transistor, having a terminal structure 102 that includes a first III-N material, in an accordance with an embodiment of the present disclosure. Figure 1B illustrates a plan view layout of the terminal structure 102 along a line A-A' of the isometric view in Figure 1A. In one embodiment, the terminal structure 102 has a central body 102A, a first plurality of fins including individual fins 102B and a second plurality of fins including individual fins 102C. In the illustrated embodiment, three fins are shown, but there can be any number of such fins (e.g., ranging from two to thousands). The fins have a length, L_F, that is between 500nm to 1000nm.

Referring again to the isometric view in Figure 1A, a polarization charge inducing layer 104 is disposed above an uppermost surface of a central body portion 102D. In an embodiment, the polarization charge inducing layer 104 includes a second III-N material. The device 100 further includes a gate 106 above the polarization charge inducing layer 104. A source structure 108 and a drain structure 110, each including a third III-N material with an impurity dopant, are disposed on opposite sides of the gate 106. The source structure 108 is above a central body portion 102E and above the fins 102B. The drain structure 110 is disposed above a third portion 102F of the central body 102A and above the fins 102C. As an example, the third portion 102F

of the central body 102A, similarly, has a relatively flat lower surface and a sloped sidewall opposite to the sidewall 105 as illustrated in figure 1A. The device 100 further includes a source contact 112 on the source structure 108, and a drain contact 114 on the drain structure 110. The region between each of the fins 102B, and between each of the fins 102C is occupied by a spacer 118.

Referring to Figure 1C, in an embodiment, each source structure 108 above each fin 102A has a pair of sidewalls 116A and 116B that are sloped. In the illustrated embodiment, the sidewalls 116A and 116B extend onto portions 120 of the spacer 118. In other embodiments, the sidewalls 116A and 116B do not extend onto the spacer 118. In another example, the sidewall 116A from one source structure 108 can meet an adjacent sidewall 116B from another source structure 108, but not overlap. When adjacent sidewalls overlap, the contact area from a 3D source structure may diminish.

The slope of each of the sidewalls 116A or 116B depends on the material of the source structure 108. In one example, each sidewall 116A and 116B has an angle that is approximately 60 degrees with respect to an uppermost surface of the fin 102B. In one such example, the sidewalls 116A and 116B intersect at an apex as is depicted in Figure 1C. Furthermore, in the illustrated embodiment, the sidewalls 116A and 116B intersect at an apex, but the sidewall 116A of one source structure 108 does not intersect with a neighboring sidewall 116B from a neighboring source structure 108. In other embodiments, an upper portion of the source structure 108 can have curvature indicated by dashed lines 117.

In the embodiment illustrated in Figure 1C, the source contact 112 has an area of contact with the source structure 108, where the area of contact has a first dimension, in the X-Y plane and a second dimension along the Z direction (into the page). In an embodiment, the first dimension of the area of contact has a magnitude that is given by the sum of a length, $L_{S,\ of}$ each of the $_{sloped}$ sidewalls 116A and 116B of the source structure 108. In an embodiment, the sum of the length $L_{S\ of}$ all of the sidewalls 116A and 116B is greater than a combined width, W_S, where W_S, is approximately equal to the sum of the width, W_F, of each of the fins 102B and the sum of the individual width, W_S, of the spacer 118 between each of the fins 102B, i.e.

$$\sum L_S > W_S \qquad (1)$$

$$W_S = \sum W_F + \sum W_{SP} \qquad (2)$$

It is to be appreciated that in the illustrated embodiment, the relative magnitude of the W_F and W_{SP} will determine if the source structure 108 can actually provide a contact area advantage. In one example, where sidewalls 116A and 116B are sloped at approximately 60 degrees, and the width, W_{SP}, of each spacer 118 is equal to or less than the width, W_F, of the fin 102B, relationship (1) is satisfied. In other embodiments, when sidewalls 116A and 116B are sloped at

60 degrees relative to an uppermost surface of the fin 102B, the width, W_{SP}, of each spacer 118 can be up to two times the width, W_F, of each fin 102B for relation (1) to be satisfied. In yet another embodiment, when the sidewalls 116A and 116B are sloped at an angle that is less than 60 degrees but greater than 30 degrees, the width, W_{SP}, of each spacer 118 can be equal to or less than the width, W_F, of each fin 102B to obtain a contact area advantage.

In an embodiment, each fin 102B has a width, W_F, between 100nm – 500nm and the source structure 108 has a height, H_S, between 80nm-430nm, and each of the spacers 118 has a width between 50nm-100nm. In, one such embodiment, the length, L_S, of sidewall 116A and 116B is between 100nm-500nm.

In an example, the sidewall 116A from one source structure 108 can meet a neighboring sidewall 116B from neighboring source structure 108 on the spacer 118, as is depicted in the cross-sectional illustration of Figure 1D. In one such example, the length, L_S of the sidewall 116A and 116B of the source structure 108 in Figure 1D is greater compared to the length, L_S of the sidewall 116A and 116B of the source structure 108 depicted in Figure 1C. A source structure depicted in Figure 1D can offer a greater contact area for the source contact 116 as compared to the contact area from the source contact 116 depicted in Figure 1C.

It is to be appreciated that an increased contact area from a 3D source structure may provide diminishing returns when a sidewall 116A from one source structure 108 depicted in Figure 1D, merges further with a neighboring sidewall 116B from neighboring source structure 108. While the combined length, L_S, of each sidewall 116A and 116B of a source structure 108 having multiple merged sidewalls may be increased, other factors such as increased intrinsic resistance of the source structure 108 may outweigh, benefits obtained from a surface area increase.

Referring again to Figure 1A, the source contact 112 has a second dimension (in a plane that is into the page) that is approximately equal to a length of the fin 102B. To further increase the area of contact between the source contact 112 and the source structure 108, the source contact 112 can extend over the entire source structure 108. In one such example, the source contact 112 is also in contact with a source structure sidewall 108A, adjacent to the gate 106. Similarly, in the illustrative embodiment, the drain contact 114 extends along a portion of the fin 102C. To further increase a contact area between the drain contact 114 and the drain structure 110, the drain contact 114 can extend over the entire drain structure 110. In one such example, the drain contact 114 is also in contact with a drain structure sidewall 110A.

In one or more embodiments, the drain structure 110 has one or more or all of the features of the source structure 108 and the drain contact 114 has one or more or all of the features of the source contact 112 described above in the various embodiments.

An embodiment where the sidewalls 116A or 116B of the source structure 108 do not intersect at an apex is illustrated in Figure 1E. The source structure 108, in such an example, is characterized by an uppermost surface 122 that is corrugated, where the corrugation is between 10nm-50nm. Corrugation of the uppermost surface 122 may result in a larger surface area for source contact 112 compared to an uppermost surface that is not corrugated. In one such example, the fin 102B has a width, W_F, that is at least 100nm and the height, H_S, of the source structure 108 is between 50nm-70nm and the sidewalls 116A and 116B have a slope of approximately 60 degrees (relative to lowermost surface of the source structure 108).

In an embodiment, the first III-N material includes a gallium nitride (GaN). In one such embodiment, the first III-N material has a relatively high carrier mobility, (greater than 500 cm^2 V^{-1}). The first III-N material may be a substantially un-doped III-N material (i.e., O_2 impurity concentration minimized) for minimal impurity scattering. In other embodiments, the first III-N material includes one or more ternary alloys of GaN, such as AlGaN, AlInN, or a quaternary alloy of GaN including at least one group III element and nitrogen, such as $In_xAl_yGa_{1-x-y}N$, where x ranges from 0.01-0.1 and y ranges from 0.01-0.1. Depending on applications, the first III-N material has a material thickness approximately in the range of 100nm -5um.

In an embodiment, the source structure 108 and drain structure 110, have uppermost surfaces that are above the level of the polarization charge inducing layer 104 and the spacer 118. In an embodiment, the source structure 108, drain structure 110 include a third III-N material that is lattice matched to the first III-N material of the terminal structure 102. In one exemplary embodiment where the terminal structure 102 includes a material such as GaN the source structure 108, drain structure 110 includes a single crystal of InGaN. In the illustrative embodiment, the source structure 108 and the drain structure 110 include faceted crystals having sidewalls, such as sidewalls 116A and 116B, that are approximately 60 degrees with respect to an uppermost surface of the first or the second plurality of fins.

In an exemplary embodiment, the third III-N material includes an impurity dopant such as an n-type dopant or an n+ dopant. Examples of an n-type dopant includes a material such as Si or Ge. In one embodiment, the n-type dopant material is silicon. As a further example, the silicon n-type dopant may have a n-dopant density of at least $1e19/cm^3$. Doping of the source structure 108 can reduce the bandgap between the source contact 112 and the source structure 108. Likewise, doping of the drain structure 110 can reduce the bandgap between drain contact 114 and the drain structure 110. A reduced bandgap may lead to a reduced contact resistance of the device 100. In an embodiment, a combination of the height and length of the source structure 108 and drain structure 110, the n-type dopant density, and 3D faceted sidewalls help to achieve a specific contact resistance value that is less than 200 ohms. In an embodiment, the source

structure 108 and the drain structure 110 each includes a third III-N material having an indium content that increases from 1% to 10%, where the higher indium content is proximate to the source contact 112 and drain contact 114, respectively. A higher indium content at an interface between the source structure 108 and the source contact 112 and between the drain structure 110 and the drain contact 114 may reduce the bandgap even further.

In an embodiment, the source contact 112, and the drain contact 114 each include a multi-layer stack. In an embodiment, the multi-layer stack includes two or more distinct layers of metal such as a layer of Ti, Ru or Al and a conductive cap on the layer of metal. The conductive cap may include a material such as W or Cu.

Examples of the spacer 118 may include any material that is sufficiently strong to provide electrical isolation such as, but not to, limited silicon dioxide, silicon nitride, silicon oxynitride, carbon doped nitride and carbon doped oxide.

Figure 1F illustrates a cross-sectional view (normal to the Y-Z plane) of the device 100, in an accordance with an embodiment of the present disclosure. In an embodiment, the gate 106 includes a gate dielectric layer 106A and a gate electrode 106B. In the illustrated embodiment, the gate dielectric layer 106A is between the polarization charge inducing layer 104 and the gate electrode 106B and also on sidewalls of the gate electrode 106B.

In an embodiment, the polarization charge inducing layer 104 includes a suitable second III-N material which induces strain in the first III-N material 102, below an interface between the second III-N material and the first III-N material. In an embodiment, the polarization charge inducing layer 104 includes a strain inducing material such as but not limited to $Al_zGa_{1-z}N$, $Al_wIn_{1-w}N$, or AlN, where Z ranges from 0.2-0.3 and W ranges from 0.7-0.85. One combination includes a polarization charge inducing layer 104 that is AlGaN and a first III-N material 102 that is GaN. In one such combination, the AlGaN polarization charge inducing layer 104 has a bandgap (3.7 eV) that is wider than the bandgap of the GaN III-N material 102 (3.4 eV), facilitating a quantum well at the interface between the AlGaN polarization charge inducing layer 104 and the GaN III-N material 102. In an embodiment, the polarization charge inducing layer 104 introduces a polarization difference in an upper interface 126 between terminal structure 102 and the polarization charge inducing layer 104, creating a conducting sheet of charge known as a 2-dimensional electron gas (2DEG – represented by dashed lines 124) in the terminal structure 102. The presence of the 2DEG leads to current conduction between the source structure 108 and the drain structure 110 in the device 100. By negatively biasing the gate relative to the drain contact 110, the 2DEG is turned off.

The gate dielectric layer 106A may have a high relative permittivity (i.e., dielectric constant, K). In some high-K gate dielectric embodiments, the gate dielectric layer 106A is a

metal oxide (e.g., including oxygen and one or more metals, such as, but not limited to, aluminum, hafnium, zirconium, tantalum or titanium). In another embodiment, the gate dielectric layer 106A includes a silicon dioxide or a silicon nitride. In some examples, the gate dielectric layer 106A has a thickness between 2nm and 10 nm.

In an embodiment, the gate electrode 106B includes a metal such as but not limited to Pt, Ni and an alloy such as TiN or TaN. In one such embodiment, the gate electrode 106B has a length, L_G, approximately in the range of 10-30nm. In some embodiments, the gate electrode 106B further includes a work function metal and a gate cap. The work function metal may include a metal such as Pt, Ni, and an alloy such as TiN or TaN and the gate cap may include a metal such as W.

Figures 2A-10A and Figures 2B-10B illustrate plan and cross-sectional views, respectively, representing various operations in a method of fabricating a group III-N transistor, in accordance with embodiments of the present disclosure. In the illustrative embodiments, the plan view illustrations are not drawn to scale with the cross-sectional illustrations. Furthermore, all cross-sectional views in Figures 2B-10B, unless otherwise specified, are taken along a line A-A' in the plan view illustrations in Figures 2A-10A.

Figures 2A-2B illustrate a plan view and a cross sectional view, respectively of a patterned polarization charge inducing layer 204 on a patterned first III-N material 202 formed above a substrate 200, in an accordance with an embodiment of the present disclosure.

Referring to Figure 2B, in an embodiment, the first III-N material 202 is grown on the substrate 200 by a metal organic chemical vapor deposition (MOCVD) process at a temperature in the range of 1000-1100 degrees Celsius. In an embodiment, the first III-N material 202 has a material composition that is the same or substantially the same as the first III-N material utilized in terminal structure 102. In an embodiment, the III-N material 202 is a GaN layer. In an embodiment, the GaN III-N material 202 is grown to a thickness that is approximately in the range of 100nm-5 micrometers. The first III-N material 202 may have a defect density less than (1e10/cm2) when grown to a sufficient thickness, such as a thickness of at least 100nm.

In an embodiment, the polarization charge inducing layer 204 is formed on the first III-N material 202. The polarization charge inducing layer 204 may be formed using a MOCVD process and grown immediately after the growth of the first III-N material 202. In an embodiment, the polarization charge inducing layer 204 is grown by a MOCVD process at a temperature in the range of 1000-1100 degrees Celsius. Depending on the embodiment, the polarization charge inducing layer 204 includes a material such as but not limited to AlN, AlInN or $Al_yGa_{1-y}N$ (where y is 0.24-0.36) and the first III-N material includes a material such as but not limited to InGaN or GaN. The polarization charge inducing layer 204 may be grown to a

thickness between 3nm and 20nm. In an exemplary embodiment, the polarization charge inducing layer 204 is AlInN. A polarization charge inducing layer 204 having a thickness between 3nm-10nm may induce strain in an uppermost surface of the III-N material 202. The presence of sufficient strain in the first III-N material 202 induces 2DEG (represented by dashed lines 205) in the strained region.

In an embodiment, the substrate 200, includes a semiconductor material such as but not limited to silicon, silicon germanium (Ge) or silicon carbide (SiC). In an exemplary embodiment, the substrate 200 is a silicon substrate having a (100) top surface. A silicon substrate 200 with a (100) top surface enables co-integration of silicon CMOS transistor technology with a III-N material. In a second embodiment, the silicon substrate 200, has a (111) top surface. In embodiments, the first III-N material 202 and the substrate 200 have mismatched lattice structures. The lattice mismatch between the first III-N material 202 and the substrate 200 may be between 15% - 50 %.

An example of an outline 201 of the mask, illustrated in the plan view illustration of Figure 2A, defines the shape of a terminal structure that will be subsequently formed. In an embodiment, a mask (not shown) is formed on the polarization charge inducing layer 204. In one embodiment, a plasma etch process is utilized to etch the polarization charge inducing layer 204 and the first III-N material 202 through an exposed area in the mask. In the illustrative embodiment, the terminal structure, to be formed in a subsequent operation, has two fins in each of the source and drain regions, 206A and 206B, respectively. Referring to the cross-sectional illustration of Figure 2B, an opening 207 is formed sufficiently deep to subsequently define isolation regions. In one embodiment, the opening 207 has a depth between 75nm and 200nm.

Figures 3A and 3B illustrate a plan view and a cross-sectional view, respectively of the structures of Figures 2A and 2B, respectively, following the formation of an isolation layer 210 surrounding the polarization charge inducing layer 204 and the patterned first III-N material 202. In an embodiment, an isolation layer 210 is blanket deposited on the surface of the polarization charge inducing layer 204 and on the patterned first III-N material 202. Examples of the isolation layer 210 may include any material that is sufficiently strong to provide electrical isolation such as, but not to, limited silicon dioxide, silicon nitride, silicon oxynitride, carbon doped nitride and carbon doped oxide. The isolation layer 210 may be deposited by a variety of insulator deposition processes such as but not limited to physical vapor deposition (PVD), chemical vapor deposition (CVD) or plasma enhanced chemical vapor deposition (PECVD) process. Post deposition, the isolation layer 210 is subsequently planarized, for example using a chemical mechanical polish process. In the embodiment depicted in Figure 3B, the CMP process leaves the isolation layer 210 having an uppermost surface that is co-planar or substantially co-

planar with an uppermost surface of the polarization charge inducing layer 204.

Figures 4A and 4B illustrate a plan view and a cross-sectional view, respectively, of the structures of Figures 3A and 3B, respectively following the formation of a terminal structure 212 by patterning portions of the polarization charge inducing layer 204, and portions of the first III-N material 202 adjacent to the isolation layer 210. Referring to Figure 4B, in an embodiment, a mask 214 is formed on a portion of the polarization charge inducing layer 204. The mask 214 may include a material that can withstand high temperature processing such as a silicon oxide or a silicon nitride. In an embodiment, a plasma etch process is utilized to pattern the polarization charge inducing layer 204 and the first III-N material 202 uncovered by the mask 214, to form trenches 215A and 215B as shown in Figure 4B. Patterning of trenches 215A and 215B in the first III-N material 202 forms the terminal structure 212 having a central body 202A, a first plurality of fins 202B adjacent to a first side 211 of the central body 202A, and a second plurality of fins 202C adjacent to a second side 213 of the central body 202A as depicted in the plan view illustration of Figure 4A. In an embodiment, the terminal structure 212, has a sloped sidewalls 202D and an approximately flat lowermost surfaces 202E. The sloped sidewalls 202D may be defined by a linear facet or have sidewall profile that has a compound slope (not depicted).

The cross-sectional illustration of Figure 4A shows an amount of recess, H_R, of the trenches 215A and 215B. In an embodiment, H_R, is between 30nm and 100nm. The trenches 215A and 215B may have a height and width chosen to enable subsequent epitaxial formation of source and drain structures having a contact resistance of less than 200 ohms-micron.

Figures 5A and 5C illustrate plan view and cross-sectional views, of the structures of Figure 4A and 4B, following the formation of source structure 216 in the trench 215A and source structure 218 in the trench 215B. In an embodiment, the source structure 216 and the drain structure 218 include a third III-N material that is the same or substantially the same as the third III-N material of the source structure 108 and drain structure 110, respectively.

As shown in the plan view illustration of Figure 5A, the source structure 216 forms a continuous structure over a portion of the central body 202A and over the first plurality of fins 202B and the drain structure 218 forms a continuous structure over a portion of the central body 202A and over the second plurality of fins 202C. The plan view illustration provides an outline of the spatial extent of the source structure 216 and the drain structure 218. Epitaxial growth of drain structure 218 crystalline material may utilize a variety of techniques and processing chamber configurations. In the illustrated embodiment, in a process known as lateral epitaxial overgrowth (LEO), conditions are engineered to favor advancing a lateral growth face of a nucleated crystal of the source structure 216 and the drain structure 218 to extend over portions

of the isolation layer 210.

As shown in Figure 5B, in an embodiment, the source structure 216 and the drain structure 218 are grown from the exposed, undamaged surface of terminal structure 202 using a metal organic chemical vapor deposition MOCVD process. The MOCVD process may be carried out at process temperatures between 1000 and 1100 degrees Celsius. In an embodiment, the source structure 216 and the drain structure 218, are epitaxially grown sufficiently thick to fill trenches 215A and 215B respectively and extend vertically to a have a height, H_E, as measured from an upper surface of the fin structure 202A and 202B, respectively. Examples of the height H_E is between 60nm-100nm. In the illustrated example, the LEO process causes a sidewall of the source structure 216 to overgrow laterally onto an isolation layer surface 210 and causes a sidewall of the drain structure 218 to overgrow laterally onto an isolation layer surface 210. Figure 5B represents an embodiment of the source structure 216 and the drain structure 218 having corrugated upper surfaces 216D and 218D, respectively. In some examples, the corrugation is between 5nm-20nm.

The cross-sectional illustration of Figure 5C, taken along a direction B-B' of the plan view illustration of Figure 5A shows a profile of the source structure 216 that is the same or substantially the same as the profile of the source structure 108 described in Figure 1E. Each portion of the source structure 216 formed over the fins 202B has sidewalls 216A and 216B. In the example illustrated, the different portions of the source structure 216 grown over the first plurality of fins 202B do not merge because of the spacing, W_S, between the individual fins 202B, resulting in a gap, G_S. Extending the epitaxial overgrowth process may cause sidewalls 216A and 216B to reduce the gap, G_S. In an embodiment the gap, G_S, may be reduced to approximately 5nm-10nm. Having a smaller gap, G_S, may be advantageous in increasing the effective area of the source structure 216.

In an embodiment, when the height H_E of the source structure 216 is approximately equal to the fin width, W_F, and when the sidewalls 216A and 216B each have an angle of approximately 60 degrees, the lateral epitaxial process can cause the sidewalls to merge at an apex such as is depicted in the cross-sectional illustration of the source structure 108 in Figure 1C. In a further embodiment, the further extending the LEO process can cause the sidewalls 216A and 216B to merge at an apex as well as merge on the isolation layer surface 210, resulting in a source structure that similar to the source structure 108 depicted above in the cross-sectional illustration of Figure 1D.

It is to be appreciated that drain structure 218D also has one or more features of the source structure 216 such as including lateral epitaxially overgrown sidewalls sloping at approximately 60 degrees and corrugated uppermost surfaces.

The cross-sectional illustration of Figure 5B also depicts an embodiment where the source structure 216 is grown to meet one sidewall of the polarization charge inducing layer 204 and the drain structure 218 is epitaxially grown to meet a second opposing sidewall of the polarization charge inducing layer 204. In such an embodiment, the source structure 216 and the drain structure 218 come into direct contact with the 2DEG (dashed lines 205) under the polarization charge inducing layer 204. In the illustrated example, the presence of the mask 214 prevents the source structure 216 and the drain structure 218 from extending onto the polarization charge inducing layer 204. It is to be appreciated that source sidewall 216C and drain sidewall 218C may also facet at approximately 60 degrees with respect to the plane of the terminal structure 202. Sidewalls 216C and 218C may also provide increased surface area for source and drain contacts to be subsequently formed.

Figures 6A and 6B illustrates a plan view and a cross-sectional view, respectively, of the structure of Figure 5A and 5B, respectively, following the removal of the mask 214 and deposition of a dielectric layer 220 on the source structure 216, drain structure 218 and on the polarization charge inducing layer 204 and on the isolation layer 210. In an embodiment, the dielectric layer 220 includes a material that is the same or substantially the same as the material of the mask 214. In some examples, the dielectric layer 220 is blanket deposited by a physical vapor deposition (PVD) or a chemical vapor deposition (CVD) process and then planarized for subsequent processing.

Figure 7A and 7B illustrate a plan view and a cross-sectional view, respectively, of the structure of Figures 6A and 6B, respectively, following the formation of a gate opening 221 in the dielectric layer 220 over a portion of the polarization charge inducing layer 204. Referring to Figure 7B, in an embodiment, a photoresist mask (not shown) is patterned over the dielectric layer 220, where the pattern defines a location for an opening to be formed relative to the polarization charge inducing layer 204. In one embodiment, a plasma etch process is utilized to form the opening 221 in the dielectric layer 220, selectively to the underlying polarization charge inducing layer 204 as shown in the cross-sectional illustration of Figure 7B taken along the direction A-A' of the plan view illustration of Figure 7A. In an embodiment, gate opening 221 has a width, at the bottom of the opening, W_B, that is approximately between 50nm- 500nm as shown in the cross-sectional illustration. In the exemplary embodiment, the gate opening 221 exposes a portion of the isolation layer 210 as illustrated in the plan view illustration of Figure 7A.

Figure 8A and 8B illustrate a plan view and a cross-sectional view, respectively, of the structure of Figures 7A and 7B, respectively, following the formation of a gate 222 in the gate opening 221 and on a portion of the polarization charge inducing layer 204. Referring to Figure

8B, in an embodiment, a gate dielectric layer 222A is first blanket deposited on a portion of the polarization charge inducing layer 204 exposed by the gate opening 221, and on the dielectric layer 220. The gate dielectric layer 222A is also disposed on sidewalls of the dielectric layer 220 in the gate opening 221. Suitable materials and thicknesses for the gate dielectric layer 222A are same as or substantially the same as the material and thicknesses of the gate dielectric layer 106A. In an embodiment, the gate dielectric layer 222A, is formed by an atomic layer deposition (ALD) process or a PVD process. A gate electrode layer 222B is then blanket deposited on the gate dielectric layer 222A in the gate opening 221. Examples of the gate electrode layer 222B include a material that is the same as or substantially the same as the material of the gate electrode layer 106B described in association with Figure 1F. In an embodiment, the gate electrode 222B includes a layer of a work function metal deposited in the gate opening 221 on the gate dielectric layer 222A and a gate cap layer deposited on the work function metal. After deposition of the gate dielectric layer 222A and the gate electrode layer 222B, a planarization process is performed to remove the gate dielectric layer 222A and the gate electrode layer 222B from an uppermost surface of the dielectric layer 220. In an embodiment, the planarization process includes a chemical mechanical polish process, where the CMP process forms a gate 222 having an uppermost surface that is co-planar or substantially co-planar with the uppermost surface of the dielectric layer 220 as shown in the cross-sectional illustration of Figure 8B.

Figures 9A and 9B illustrate a plan view and a cross-sectional view, respectively, of the structure of Figures 8A and 8B, respectively, following the formation of an opening 223A such as a source contact opening, above the source structure 216 and an opening 223B such as a drain contact opening above the drain structure 218. Referring to Figure 9B, in an embodiment, a photoresist mask (not shown) is patterned over the dielectric layer 220 and the gate 222, where the pattern defines a location for the opening 223A and the opening 223B to be formed relative to the source structure 216 and the drain structure 218, respectively.

In one embodiment, a plasma etch process is utilized to form the opening 223A and opening 223B in the dielectric layer 220, selectively to the underlying source structure 216 and the drain structure 218, respectively. The plasma etch may cause some corner rounding of the corrugated upper surfaces 216E and 218E.

In an embodiment, the opening 223A exposes a portion of the source structure 216 and a portion of the isolation layer 210 laterally surrounding the source structure 216 as shown in the plan view illustration of Figure 9A. In a different embodiment, the opening 223A can be extended to expose a portion of the source contact sidewall 216C or the entire source contact sidewall 216C. In an embodiment, the opening 223A can be large enough to expose an entire upper surface area of source structure 216.

Similarly, in the illustrated embodiment, the opening 223B exposes a portion of the drain structure 218 and a portion of the isolation layer 210 laterally surrounding the source structure 216 as shown in the plan view illustration of Figure 9A. In a different embodiment, the opening 223B can extend to expose a portion of the drain structure sidewall 218C as illustrated in Figure 9B. In a different embodiment, the opening 223B can be large enough to expose an entire upper surface area of drain structure 218.

In an embodiment, the plasma etch process undergoes a clean-up process in order to completely expose the upper surfaces of the source structure 216 and the drain structure 218. In one such embodiment, the plasma etch completely removes the dielectric layer 220 from the region between the source structure 216 and from the region between the drain structure 218 to expose the underlying isolation layer 210 as illustrated in the plan view illustration of Figure 9A. In some embodiments, significant over etch can result in exposure of sidewalls of the patterned first III-N material 202 under sidewalls 216E and 218E of the source structure 216 and drain structure 218, respectively.

Figure 10A and 10B illustrate a plan view and a cross-sectional view, respectively, of the structure of Figures 9A and 9B following the formation of a drain contact 226 in the drain contact opening 223B on the drain structure 218 and a source contact 228 in the source contact opening 223A on the source structure 216.

Referring to Figure 10B, in an embodiment, one or more layers of contact metal are deposited inside each of the openings 223A and 223B on exposed surfaces of the source structure 216 and on exposed surfaces of the drain structure 218, respectively. In the illustrative embodiment, the one or more layers of the contact metal are also blanket deposited on exposed portions of the isolation layer 210 and on the uppermost surface of the dielectric layer 220 and on the gate 222. In an embodiment, the one or more layers of contact metal are deposited using a plasma enhanced chemical vapor deposition (PECVD) or an ALD process. In an embodiment, suitable contact metals include metals such as but not limited to Ti, Al or Ni. In an embodiment, a tungsten capping layer is deposited on the one or more layers of contact metal. In an embodiment, where the tungsten capping layer is deposited on the one or more layers of contact metal, the one or more layers of contact metal is first deposited on the bottom and on the sides of the opening 223A and 223B and the tungsten capping layer is deposited to fill the remaining portion of the openings 223A and 223B. In an embodiment, the one or more layers of contact metal is deposited to a thickness in the range of 10-30nm, and the tungsten capping layer is deposited to fill the remaining portion of each of the openings 223A and 223B.

A planarization process is carried out to remove the one or more layers of contact metal from the uppermost surface of the dielectric layer 220. In one embodiment, the planarization

process includes a chemical mechanical polish (CMP) process. The CMP process removes all the one or more layers of contact metal from the uppermost surfaces of the dielectric layer 220, and from the uppermost surface of the gate 222. The CMP process leaves the one or more layers of contact metal in the openings 223A and 223B to form a source contact 226 and a drain contact 228 as shown in the cross-sectional illustration of Figure 10B.

It is to be appreciated that maximizing a contact area between the source contact 226 and the source structure 216, formed over a plurality of fins, can help to reduce the contact resistance between the source structure 216 and the source contact 226 by as much as 70% compared to a contact resistance between a source contact and a source structure formed over a large first single fin of a planar terminal structure having a central body, and a large second single fin opposite to the large first single fin. It is to be appreciated that maximizing a contact area between the drain contact 228 and the drain structure 218, formed over a plurality of fins, can help to reduce the contact resistance between the drain contact 228 and the drain structure 218 by as much as 70% compared to a contact resistance between a drain contact and a drain structure, formed over the large second single fin of the planar terminal structure. In an embodiment, the contact resistance between the source contact 226 and the source structure 216 or between the drain contact 228 and the drain structure 216 can have a value of less than 200 ohm-micron.

The cross-sectional illustration in Figure 10C taken along a direction B-B' in the Figure 10C illustrates one of the dimensions of the area of contact between the source contact 226 and the source structure 216. The cross-sectional illustration highlights the area advantage obtained through contact between the source structure 216 and sidewalls 216A and 216B of the source structure 216. Additionally, the corrugation in the source structure 216 also enables a larger contact surface to be obtained.

Figure 11 illustrates a system 1100 in which a mobile computing platform 1105 and/or a data server machine 1106 employs an IC including at least one group III-N transistor, such as the device 100 including an epitaxially grown source and drain structures, formed on fins, where the source and drain structures have surface areas that offer a large contact area for a given footprint of the fin, in accordance with embodiments of the present disclosure. The server machine 1106 may be any commercial server, for example including any number of high-performance computing platforms disposed within a rack and networked together for electronic data processing, which in the exemplary embodiment includes a packaged monolithic IC 1150. The mobile computing platform 1105 may be any portable device configured for each of electronic data display, electronic data processing, wireless electronic data transmission, or the like. For example, the mobile computing platform 1105 may be any of a tablet, a smart phone, laptop computer, etc., and may include a display screen (e.g., a capacitive, inductive, resistive, or

optical touchscreen), a chip-level or package-level integrated system 1110, and a battery 1115.

Whether disposed within the integrated system 1110 illustrated in the expanded view 1120, or as a stand-alone packaged chip within the server machine 1106, packaged monolithic IC 1150 includes a memory chip (e.g., RAM), or a processor chip (e.g., a microprocessor, a multi-core microprocessor, graphics processor, or the like) including at least one group III-N transistor, such as the device 100 including an epitaxially grown source and drain structures formed on fins, for example as describe elsewhere herein. The monolithic IC 1150 may be further coupled to a board, a substrate, or an interposer 1160 along with, one or more of a power management integrated circuit (PMIC) 1130, RF (wireless) integrated circuit (RFIC) 1125 including a wideband RF (wireless) transmitter and/or receiver (TX/RX) (e.g., including a digital baseband and an analog front end module further comprises a power amplifier on a transmit path and a low noise amplifier on a receive path), and a controller thereof 1135.

Functionally, PMIC 1130 may perform battery power regulation, DC-to-DC conversion, etc., and so has an input coupled to battery 1115 and with an output providing a current supply to other functional modules. As further illustrated, in the exemplary embodiment, RFIC 1125 has an output coupled to an antenna (not shown) to implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. In alternative implementations, each of these board-level modules may be integrated onto separate ICs coupled to the package substrate of the monolithic IC 1150 or within a single IC coupled to the package substrate of the monolithic IC 1150.

Figure 12 is a functional block diagram of a computing device 1200, arranged in accordance with at least some implementations of the present disclosure. Computing device 1200 may be found inside platform 1100, for example, and further includes a motherboard 1202 hosting a number of components, such as but not limited to a processor 1201 (e.g., an applications processor) and one or more communications chips 1204, 1205. Processor 1201 may be physically and/or electrically coupled to motherboard 1202. In some examples, processor 1201 includes an integrated circuit die packaged within the processor 1201. In general, the term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. A device or component of computing device 1200 may include transistor(s) or transistor structure(s) such as III-N devices 100 including a terminal

structure having a central body and a first plurality of fins, and a second plurality of fins, opposite the first plurality of fins integrated with or without silicon CMOS transistors.

In various examples, one or more communication chips 1204, 1205 may also be physically and/or electrically coupled to the motherboard 1202. In further implementations, communication chips 1204 may be part of processor 1201. Depending on its applications, computing device 1200 may include other components that may or may not be physically and electrically coupled to motherboard 1202. These other components may include, but are not limited to, volatile memory (e.g., DRAM) 1207, 1208, non-volatile memory (e.g., ROM) 1210, a graphics processor 1212, flash memory, global positioning system (GPS) device 1213, compass 1214, a chipset 1206, an antenna 1216, a power amplifier 1209, a touchscreen controller 1211, a touchscreen display 1217, a speaker 1215, a camera 1203, and a battery 1218, as illustrated, and other components such as a digital signal processor, a crypto processor, an audio codec, a video codec, an accelerometer, a gyroscope, and a mass storage device (such as hard disk drive, solid state drive (SSD), compact disk (CD), digital versatile disk (DVD), and so forth), or the like.

Communication chips 1204, 1205 may enables wireless communications for the transfer of data to and from the computing device 1200. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. Communication chips 1204, 1205 may implement any of a number of wireless standards or protocols, including but not limited to those described elsewhere herein. As discussed, computing device 1200 may include a plurality of communication chips 1204, 1205. For example, a first communication chip may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

As used in any implementation described herein, the term "module" refers to any combination of software, firmware and/or hardware configured to provide the functionality described herein. The software may be embodied as a software package, code and/or instruction set or instructions, and "hardware", as used in any implementation described herein, may include, for example, singly or in any combination, hardwired circuitry, programmable circuitry, state machine circuitry, and/or firmware that stores instructions executed by programmable circuitry. The modules may, collectively or individually, be embodied as circuitry that forms part of a larger system, for example, an integrated circuit (IC), system on-chip (SoC), and so forth.

Figure 13 illustrates an integrated circuit structure 1300 that includes one or more

embodiments of the disclosure. The integrated circuit (IC) structure 1300 is an intervening structure used to bridge a first substrate 1302 to a second substrate 1304. The first substrate 1302 may be, for instance, an integrated circuit die. The second substrate 1304 may be, for instance, a memory module, a computer mother, or another integrated circuit die. The integrated circuit die may include one or more devices such as a III-N device 100 (transistor) including a terminal structure having a central body and a first plurality of fins, and a second plurality of fins, opposite the first plurality of fins, and source and drain structures on respective first and second plurality of fins, where the source and drain structures are designed for enhanced contact surface area and reducing contact resistance, for example. Generally, the purpose of an integrated circuit (IC) structure 1300 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an integrated circuit (IC) structure 1300 may couple an integrated circuit die to a ball grid array (BGA) 1306 that can subsequently be coupled to the second substrate 1304. In some embodiments, the first and second substrates 1302/1304 are attached to opposing sides of the integrated circuit (IC) structure 1300. In other embodiments, the first and second substrates 1302/1304 are attached to the same side of the integrated circuit (IC) structure 1300. And in further embodiments, three or more substrates are interconnected by way of the integrated circuit (IC) structure 1300.

The integrated circuit (IC) structure 1300 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the integrated circuit (IC) structure 1300 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-N, group III-V and group IV materials.

The integrated circuit (IC) structure 1300 may include metal interconnects 1308 and via 1310, including but not limited to through-silicon vias (TSVs) 1310. The integrated circuit (IC) structure 1300 may further include embedded devices 1314, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, group III-N transistors such as a III-N device 100 including a terminal structure having a central body and a first plurality of fins, and a second plurality of fins, opposite the first plurality of fins, one or more magnetic tunnel junction or resistive random-access devices, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the integrated circuit (IC) structure 1300. In accordance with embodiments of the present disclosure, apparatuses or processes disclosed herein may be used in the fabrication of integrated circuit (IC)

structure 1300.

While certain features set forth herein have been described with reference to various implementations, this description is not intended to be construed in a limiting sense. Hence, various modifications of the implementations described herein, as well as other implementations, which are apparent to persons skilled in the art to which the present disclosure pertains are deemed to lie within the spirit and scope of the present disclosure.

Thus, embodiments of the present disclosure include group III-Nitride (III-N) devices with reduced contact resistance and their methods of fabrication.

In first examples, a device includes a terminal structure having a first group III-Nitride (III-N) material, where the terminal structure has a central body and a first plurality of fins, and a second plurality of fins, opposite the first plurality of fins, a polarization charge inducing layer above a first portion of the central body, where the polarization charge inducing layer includes a second III-N material, a gate electrode above the polarization charge inducing layer, a source structure and a drain structure including a third III-N material with an impurity dopant on opposite sides of the gate electrode, the source structure above a second portion of the central body and above the first plurality of fins, the drain structure above a third portion of the central body and above the second plurality of fins, a source contact on the source structure and a drain contact on the drain structure.

In second examples, for any of first examples, the bottom electrode, each fin in the first or the second plurality of fins has a width between 100nm – 500nm and a length between 0.5 micrometer and 1 micrometer.

In third examples, for any of the first through second examples, a spacing between each successive fin in the first or the second plurality of fins is less than the width of the fin.

In fourth examples, for any of the first through third examples, the number of fins in the first and the second plurality of fins is between 2-1000.

In fifth examples, for any of the first through fourth examples, the source contact has an area of contact over the first plurality of fins, wherein the area of contact has a first dimension that is greater than a combined width of the first plurality of fins summed with the combined width of the spacing between the first plurality of fins, and wherein the source contact has a second dimension that is approximately equal to a length of the fins.

In sixth examples, for any of the first through fifth examples, the drain contact has an area of contact on the drain structure, wherein the area of contact has a first dimension that is greater than a combined width of the second plurality of fins and the combined width of the spacing between the second plurality of fins and, wherein the drain contact has a second dimension that is approximately equal to the length of the second plurality of fins

In seventh examples, for any of the first through sixth examples, the source structure and a drain structure include of faceted crystals having sidewalls that are approximately 60 degrees with respect to an uppermost surface of the first or the second plurality of fins.

In eighth examples, for any of the first through seventh examples, the sidewalls intersect to form an apex.

In ninth examples, for any of the first through eighth examples, the source structure and a drain structure each have an uppermost surface that is corrugated and wherein the corrugation is between 10nm-50nm.

In tenth examples, for any of the first through ninth examples, the first III-N material includes a gallium nitride (GaN) and the second III-N material includes a III-N material that includes aluminum.

In eleventh examples, for any of the first through tenth examples, the source structure and the drain structure each includes a III-N material having an indium content that increases from 1% to 10%.

In twelfth examples, for any of the first through eleventh examples, the source structure and the drain structure each include a material that is lattice matched to the first III-N material and an n-type impurity dopant.

In thirteenth examples, for any of the first through twelfth examples, the device further includes a gate dielectric layer between the gate electrode and the polarization charge inducing layer.

In fourteenth examples, for any of the first through thirteenth examples, the gate electrode comprises a work function layer and a gate metal cap.

In fifteenth examples, a method of fabricating a semiconductor structure includes forming a layer having a first group III-nitride (III-N) material on a substrate. The method further includes forming a polarization charge inducing layer including a second III-N material above the first layer and patterning the layer including the first III-N material and the polarization charge inducing layer and forming a central body, a first plurality of fins adjacent to a first side of the central body, and a second plurality of fins adjacent to a second side of the central body, opposite the first side. The method further includes forming an isolation between the first plurality of fins and between the second plurality of fins. The method further includes forming a first trench and a second trench, laterally separated from the first trench, in the first III-N semiconductor material. The method further includes forming a source structure in the first trench and a drain structure in the second trench and forming a gate dielectric layer on the polarization charge inducing layer. The method further includes forming a gate electrode on the gate dielectric layer and forming a source contact on the source structure and a drain contact on

the drain structure.

In sixteenth examples, for any of the fifteenth examples, the method of forming the isolation includes depositing an electrically insulating layer on the patterned polarization charge inducing layer, between the first and the second plurality of fins and on the layer comprising the first III-N material between the first and the second plurality of fins, and planarizing the electrically insulating layer and removing it from an uppermost surface of the polarization charge inducing layer.

In seventeenth examples, for any of the fifteenth through sixteenth examples, the method of forming the first recess and a second recess includes removing polarization charge inducing layer from above the first and the second plurality of fins and from a portion of the central body.

In eighteenth examples, for any of the fifteenth through seventeenth examples, the method of forming the source structure includes growing a third III-N material in the first recess and on the first III-N material, and forming the drain structure includes growing the third III-N material in the second recess and on the first III-N material, wherein the growing includes forming crystal structures with slanted sidewalls.

In nineteenth examples, for any of the fifteenth through eighteenth examples, the growing includes a merging of slanted sidewalls to form an apex.

In twentieth examples, a system includes a processor and a radio transceiver coupled to the processor, wherein the transceiver includes a group III-Nitride (III-N) transistor. The III-N transistor includes a terminal structure having a first group III-Nitride (III-N) material, where the terminal structure has a central body and a first plurality of fins, and a second plurality of fins, opposite the first plurality of fins, a polarization charge inducing layer above a first portion of the central body, where the polarization charge inducing layer includes a second III-N material, a gate electrode above the polarization charge inducing layer, a source structure and a drain structure including a third III-N material with an impurity dopant on opposite sides of the gate electrode, the source structure above a second portion of the central body and above the first plurality of fins, the drain structure above a third portion of the central body and above the second plurality of fins, a source contact on the source structure and a drain contact on the drain structure.

In twenty first examples, for any of the twentieth examples, each fin in the first or the second plurality of fins has a width between 100nm – 500nm and a length between 0.5 micrometer and 1 micrometer.

In twenty second examples, for any of the twentieth examples, a spacing between each successive fin in the first or the second plurality of fins is less than the width of the fin.

In twenty third examples, for any of the twentieth through twenty second examples, the

source contact has an area of contact on the first plurality of fins, wherein the area of contact has a first dimension that is greater than a combined width of the first plurality of fins summed with the combined width of the spacing between the first plurality of fins, and wherein the source contact has a second dimension that is approximately equal to a length of the fins.

In twenty fourth examples, for any of the twentieth through twenty third examples, the source structure and a drain structure include of faceted crystals having sidewalls that are approximately 60 degrees with respect to an uppermost surface of the first or the second plurality of fins.

In twenty fifth examples, for any of the twentieth through twenty fourth examples, the source structure and a drain structure each have an uppermost surface that is corrugated and wherein the corrugation is between 10nm-50nm.

Claims

What is claimed is:

1. A device comprising:

a terminal structure comprising a first group III-Nitride (III-N) material, the terminal structure having a central body, a first plurality of fins, and a second plurality of fins opposite the first plurality of fins;

a polarization charge inducing layer above a first portion of the central body, the polarization charge inducing layer comprising a second III-N material;

a gate electrode above the polarization charge inducing layer;

a source structure and a drain structure comprising a third III-N material with an impurity dopant on opposite sides of the gate electrode, the source structure above a second portion of the central body and above the first plurality of fins, the drain structure above a third portion of the central body and above the second plurality of fins;

a source contact on the source structure; and

a drain contact on the drain structure.

2. The device of claim 1, wherein each fin in the first or the second plurality of fins has a width between 100nm – 500nm and a length between 0.5 micrometer and 1 micrometer.

3. The device of claim 2, where a spacing between each successive fin in the first or the second plurality of fins is less than the width of the fin.

4. The device of claim 2, wherein the number of fins in the first and the second plurality of fins is between 2-1000.

5. The device of any of claims 1-4, wherein the source contact has an area of contact over the first plurality of fins, wherein the area of contact has a first dimension that is greater than a combined width of the first plurality of fins summed with the combined width of the spacing between the first plurality of fins, and wherein the source contact has a second dimension that is approximately equal to a length of the fins.

6. The device of any of claims 1-4, wherein the drain contact has an area of contact on the drain structure, wherein the area of contact has a first dimension that is greater than a combined width

of the second plurality of fins and the combined width of the spacing between the second plurality of fins and, wherein the drain contact has a second dimension that is approximately equal to the length of the second plurality of fins.

7. The device of any of claims 1-6, wherein the source structure and a drain structure comprise of faceted crystals having sidewalls that are approximately 60 degrees with respect to an uppermost surface of the first or the second plurality of fins.

8. The device of claim 7, wherein the sidewalls intersect at an apex.

9. The device of claim of any of claims 1-8, wherein the source structure and the drain structure each include a material that is lattice matched to the first III-N material and an n-type impurity dopant.

10. The device of any of claims 1-9, wherein the source structure and a drain structure each have an uppermost surface that is corrugated and wherein the corrugation is between 10nm-50nm.

11. The device of any of claims 1-10, wherein the source structure and the drain structure each comprises a III-N material having an indium content that increases from 1% to 10%.

12. The device of any of claims 1-11, wherein the first III-N material includes a gallium nitride (GaN) and the second III-N material includes a III-N material that includes aluminum.

13. The device of any of claims 1-12, further comprising a gate dielectric layer between the gate electrode and the polarization charge inducing layer.

14. The device of any of claims 1-13, wherein the gate electrode comprises a work function layer and a gate metal cap.

15. A method of fabricating a semiconductor structure, the method comprising:

forming a layer comprising a first group III-nitride (III-N) semiconductor material on a substrate;

forming a polarization charge inducing layer comprising a second III-N material above the first layer;

patterning the layer comprising the first III-N material and the polarization charge

inducing layer and forming a central body, a first plurality of fins adjacent to a first side of the central body, and a second plurality of fins adjacent to a second side of the central body, opposite the first side;

forming an isolation between the first plurality of fins and between the second plurality of fins;

forming a first trench and a second trench, laterally separated from the first trench, in the first III-N material;

forming a source structure in the first trench and a drain structure in the second trench;

forming a gate dielectric layer on the polarization charge inducing layer;

forming a gate electrode on the gate dielectric layer; and

forming a source contact on the source structure and a drain contact on the drain structure

16. The method of claim 15, wherein forming the isolation comprises depositing an electrically insulating layer on the patterned polarization charge inducing layer, between the first and the second plurality of fins and on the layer comprising the first III-N material between the first and the second plurality of fins, and planarizing the electrically insulating layer and removing it from an uppermost surface of the polarization charge inducing layer.

17. The method of claim 15, wherein forming the first recess and a second recess comprises removing polarization charge inducing layer from above the first and the second plurality of fins and from a portion of the central body.

18. The method of any of claims 15-17, wherein forming the source structure comprises growing a third III-N material in the first recess and on the first III-N material, and forming the drain structure comprises growing the third III-N material in the second recess and on the first III-N material, wherein the growing comprises forming crystal structures with slanted sidewalls.

19. The method of claim 18, wherein the growing comprises a merging of the slanted sidewalls to form an apex.

20. A system comprising:

a processor; and

a radio transceiver coupled to the processor, wherein the transceiver includes a group III-Nitride (III-N) transistor comprising:

a terminal structure comprising a first group III-Nitride (III-N) material, the terminal structure having a central body, a first plurality of fins, and a second plurality of fins opposite the first plurality of fins;

a polarization charge inducing layer above a first portion of the central body, the polarization charge inducing layer comprising a second III-N material;

a gate electrode above the polarization charge inducing layer;

a source structure and a drain structure comprising a third III-N material with an impurity dopant on opposite sides of the gate electrode, the source structure above a second portion of the central body and above the first plurality of fins, the drain structure above a third portion of the central body and above the second plurality of fins;

a source contact on the source structure; and

a drain contact on the drain structure.

21. The system of claim 20, wherein each fin in the first or the second plurality of fins has a width between 100nm – 500nm and a length between 0.5 micrometer and 1 micrometer.

22. The system of any of claims 20-21, where a spacing between each successive fin in the first or the second plurality of fins is less than the width of the fin.

23. The system of any of claims 20-22, wherein the source contact has an area of contact on the first plurality of fins, wherein the area of contact has a first dimension that is greater than a combined width of the first plurality of fins summed with the combined width of the spacing between the first plurality of fins, and wherein the source contact has a second dimension that is approximately equal to a length of the fins.

24. The system of claim 20, wherein the source structure and a drain structure comprise of faceted crystals having sidewalls that are approximately 60 degrees with respect to an uppermost surface of the first or the second plurality of fins.

25. The system of any of claims 20-24, wherein the source structure and a drain structure each have an uppermost surface that is corrugated and wherein the corrugation is between 10nm-50nm.

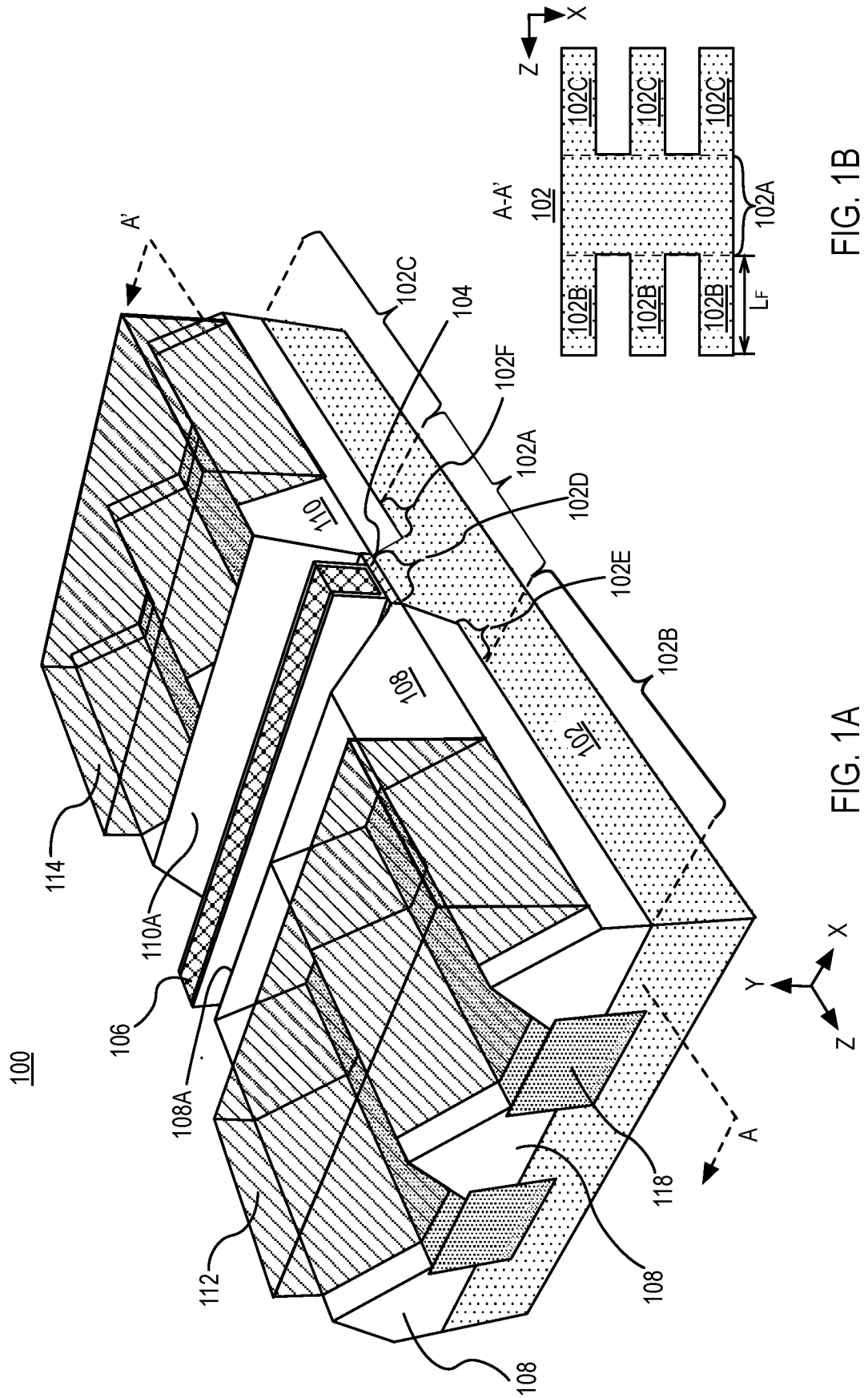

100
A'
A
102C
104
102F
102A
102D
102E
102B
110
108
102
114
110A
106
108A
112
118
X
Y
Z

FIG. 1A

A-A'
102
102C
102B
102A
L_F
X
Z

FIG. 1B

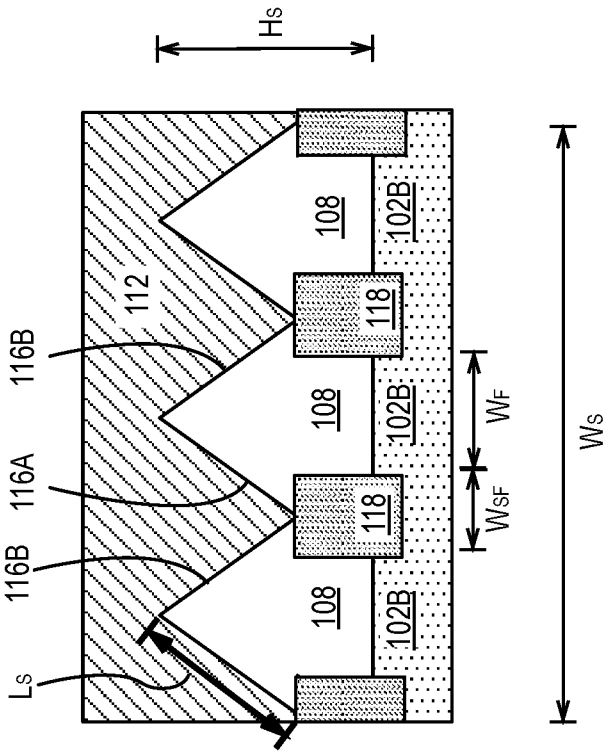

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116A
116B
Ls
108
102B
118
WF
WSF
Ws

FIG. 1D

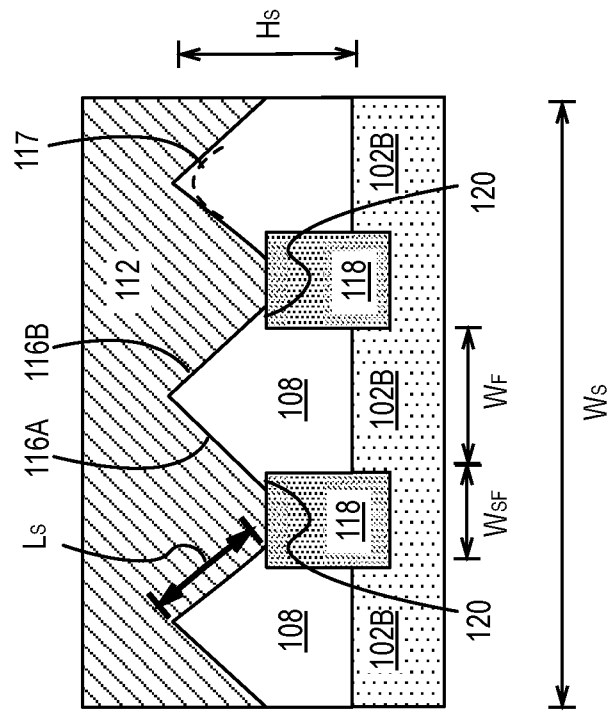
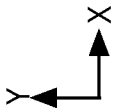

Hs
117
112
116B
116A
Ls
108
102B
118
120
WF
WSF
Ws

FIG. 1C


X
Y

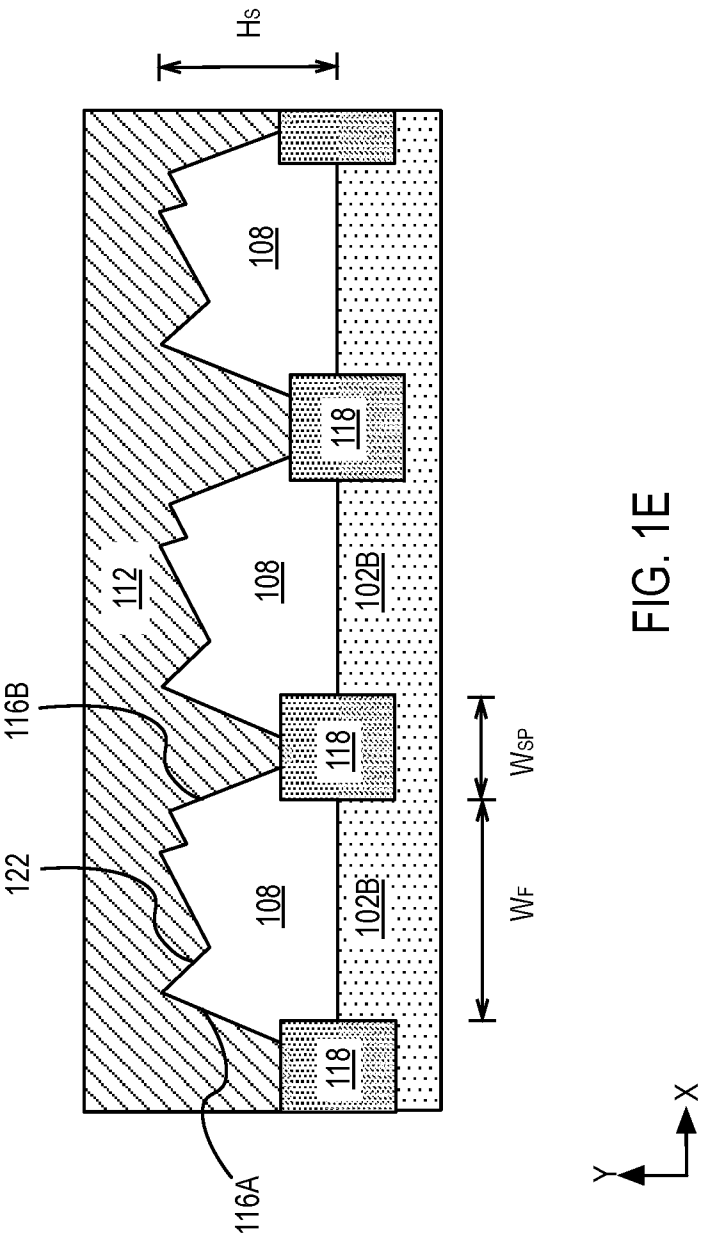


FIG. 1E

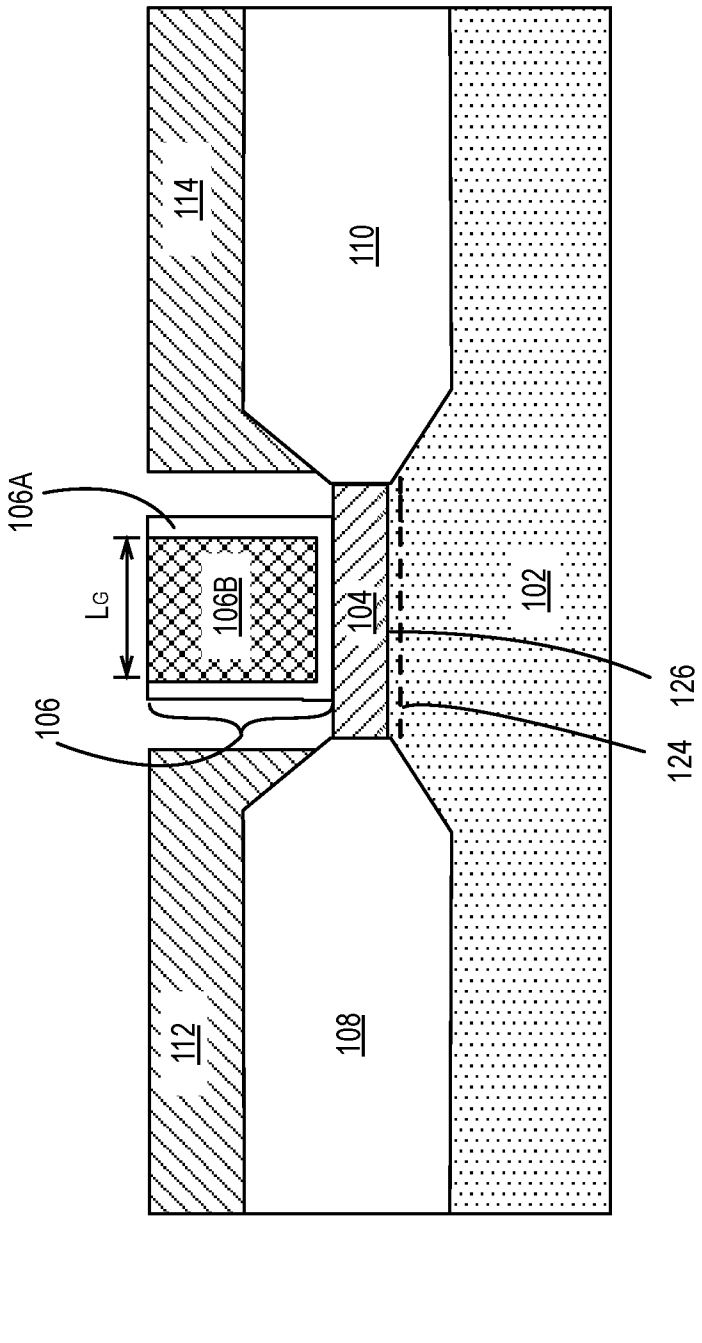


FIG.1F

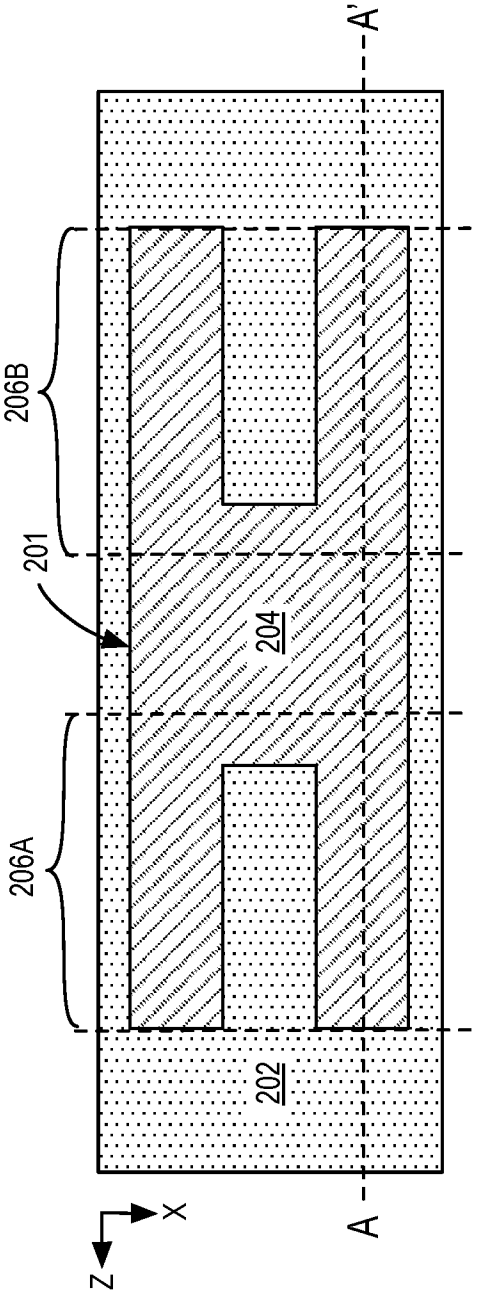


FIG. 2A

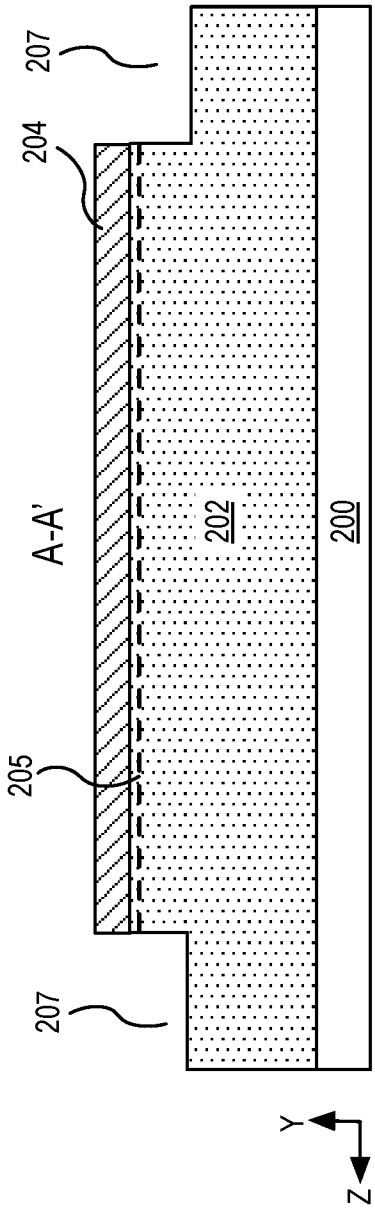


FIG. 2B

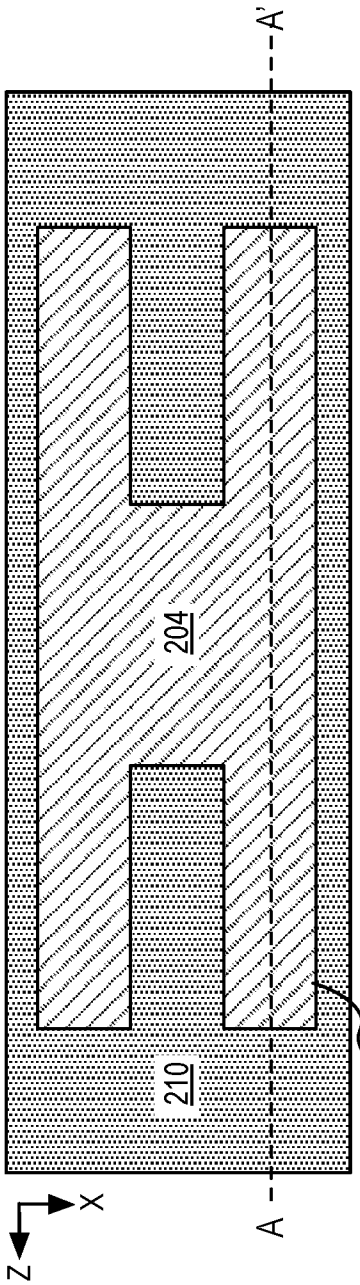


FIG. 3A

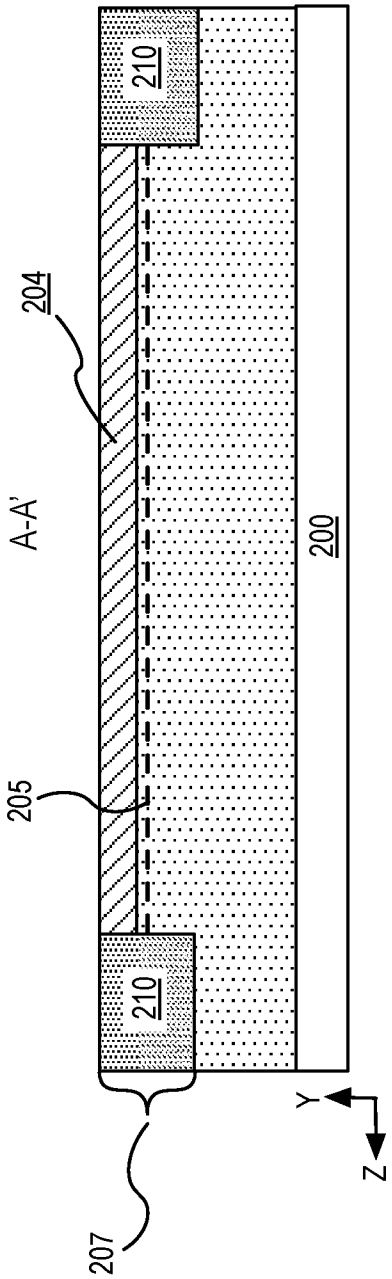


FIG. 3B

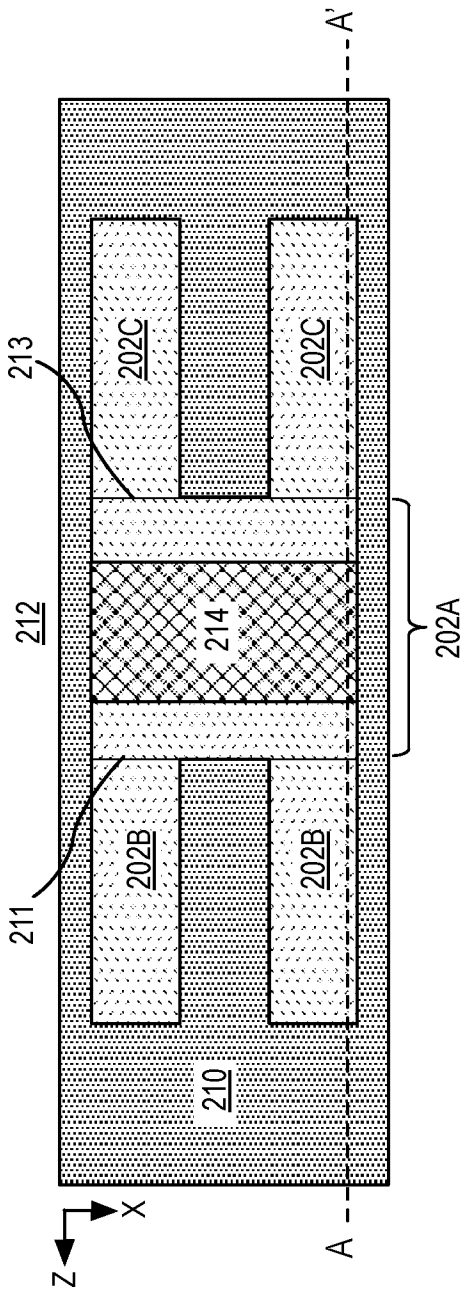

A'
213
202C
202C
212
214
202A
211
202B
202B
210
A
X
Z

FIG. 4A

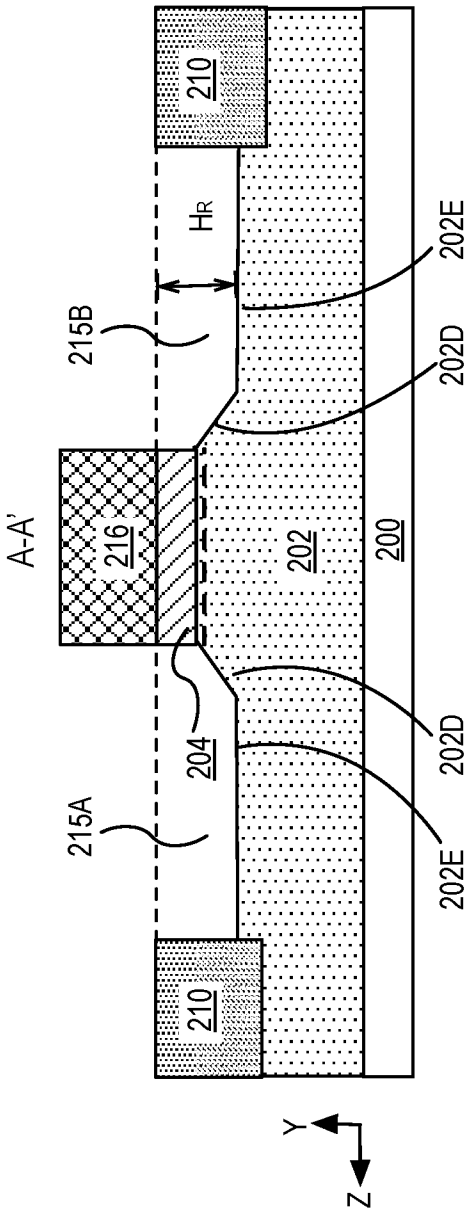

210
H_R
202E
215B
202D
A-A'
216
202
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204
202D
215A
202E
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Y
Z

FIG. 4B

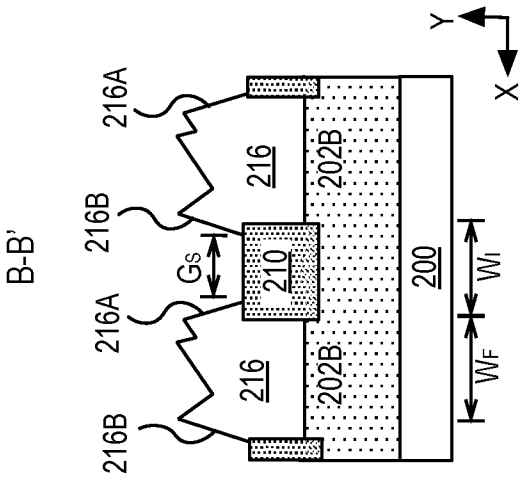


FIG. 5C

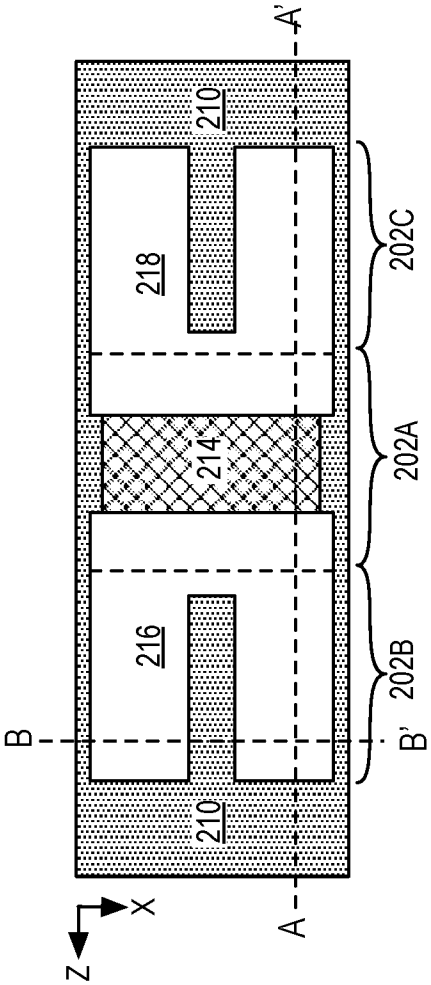


FIG. 5A

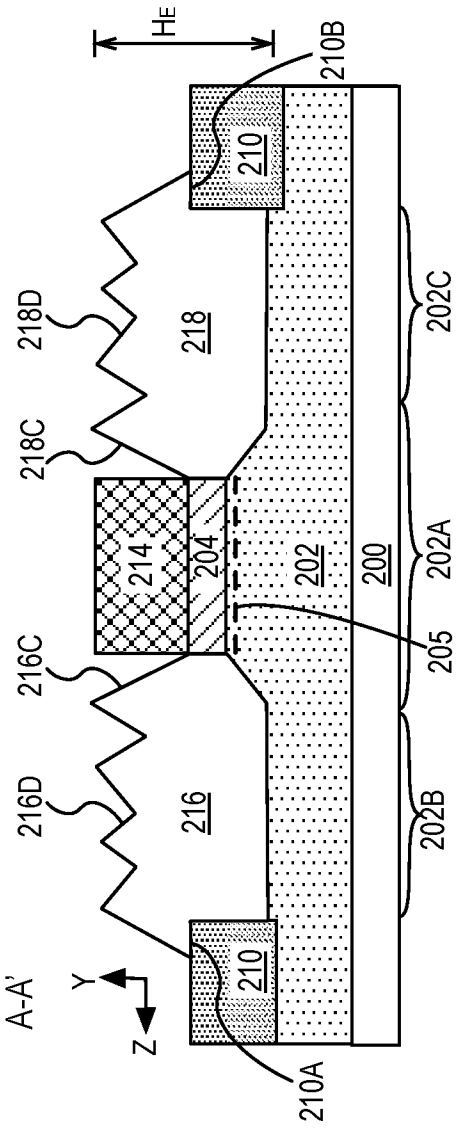


FIG. 5B

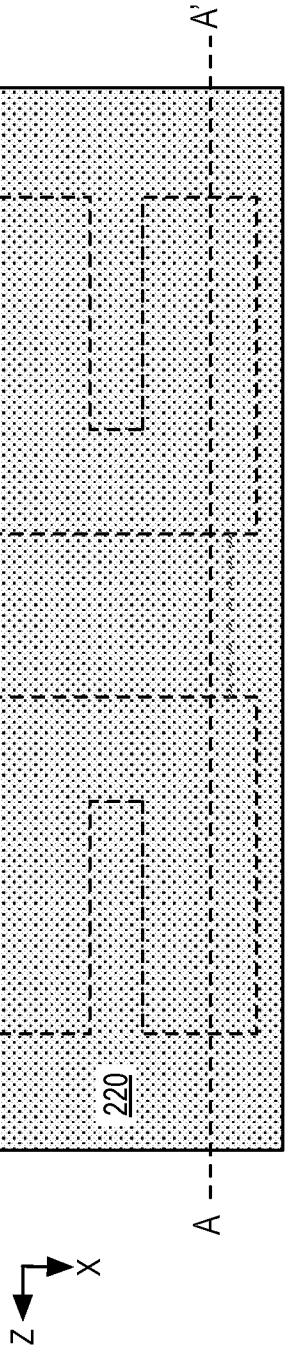


FIG. 6A

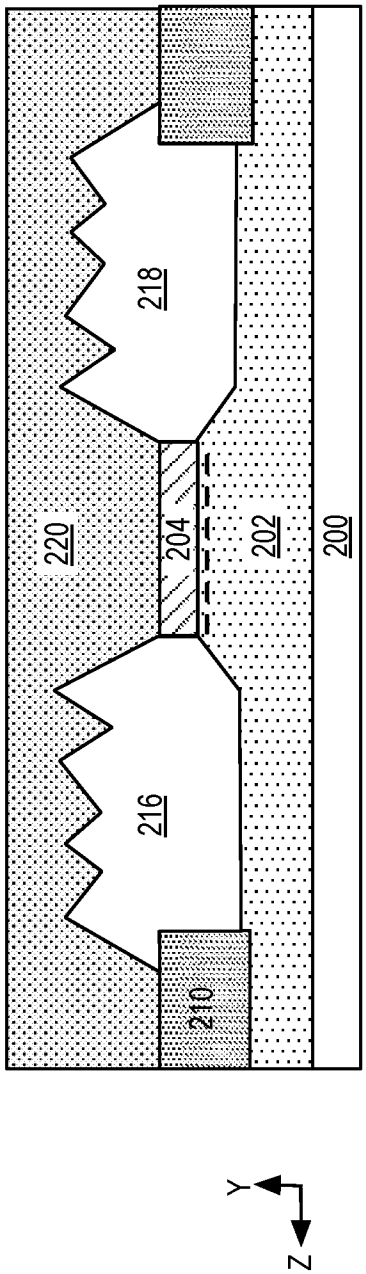


FIG. 6B

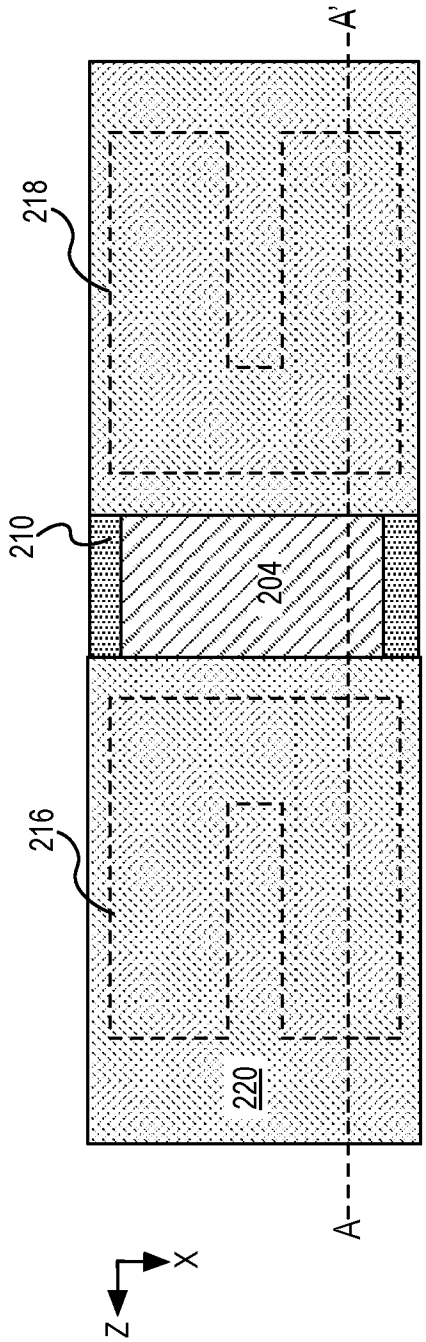


FIG. 7A

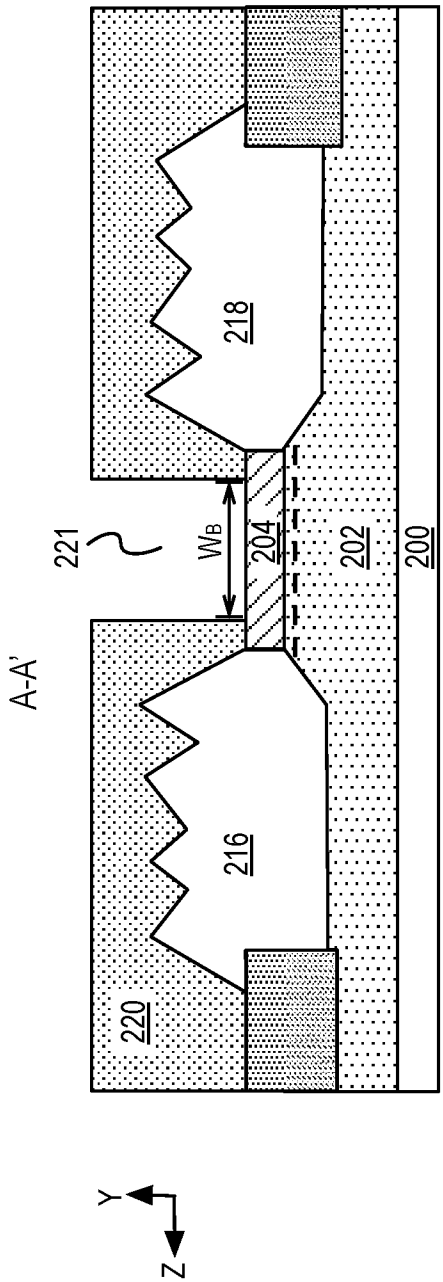


FIG. 7B

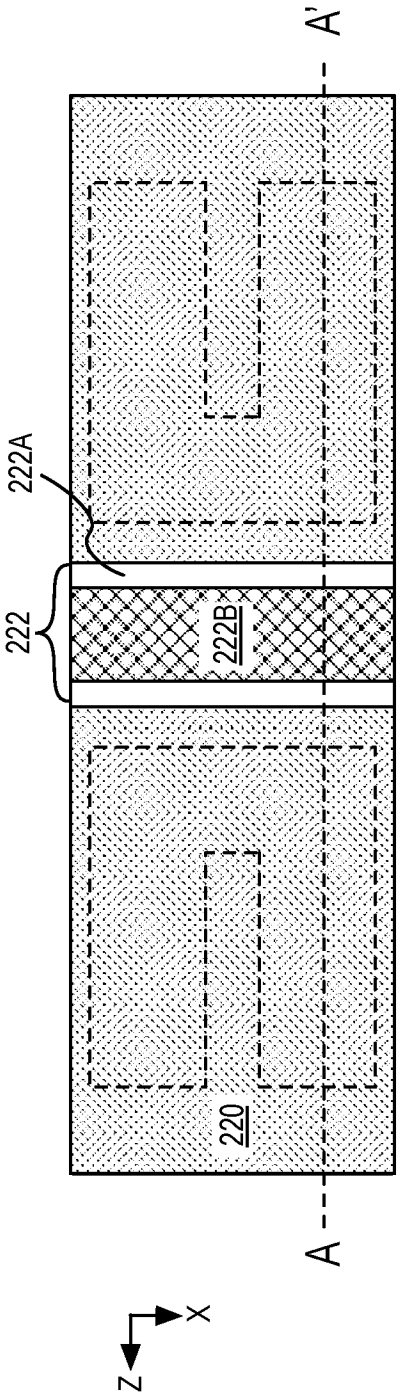

A'
222A
222
222B
220
A
X
Z

FIG. 8A

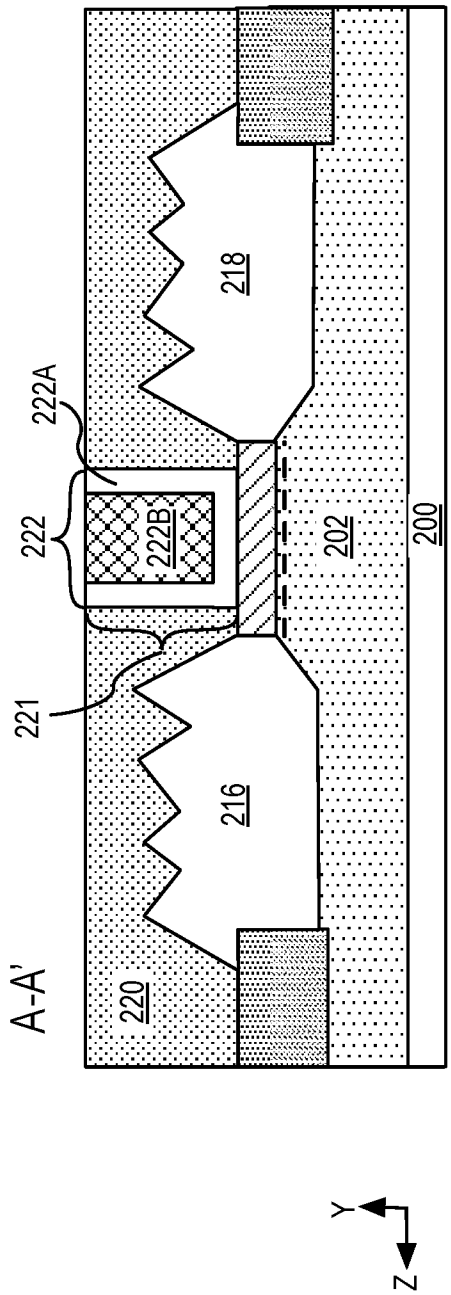

218
222A
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222B
202
200
221
216
A-A'
220
Y
Z

FIG. 8B

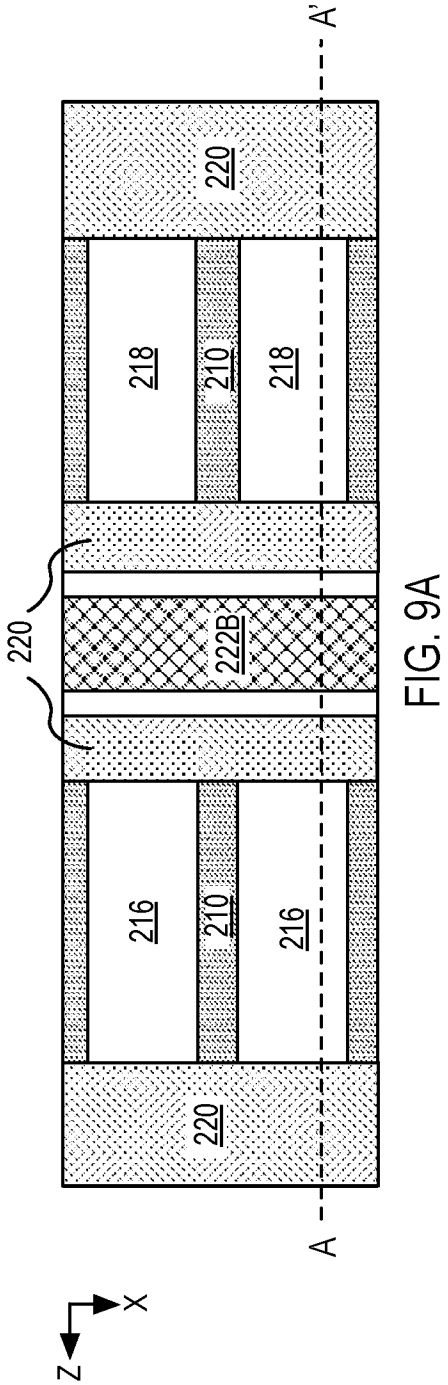

A'
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218
220
222B
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216
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A
Z
X

FIG. 9A

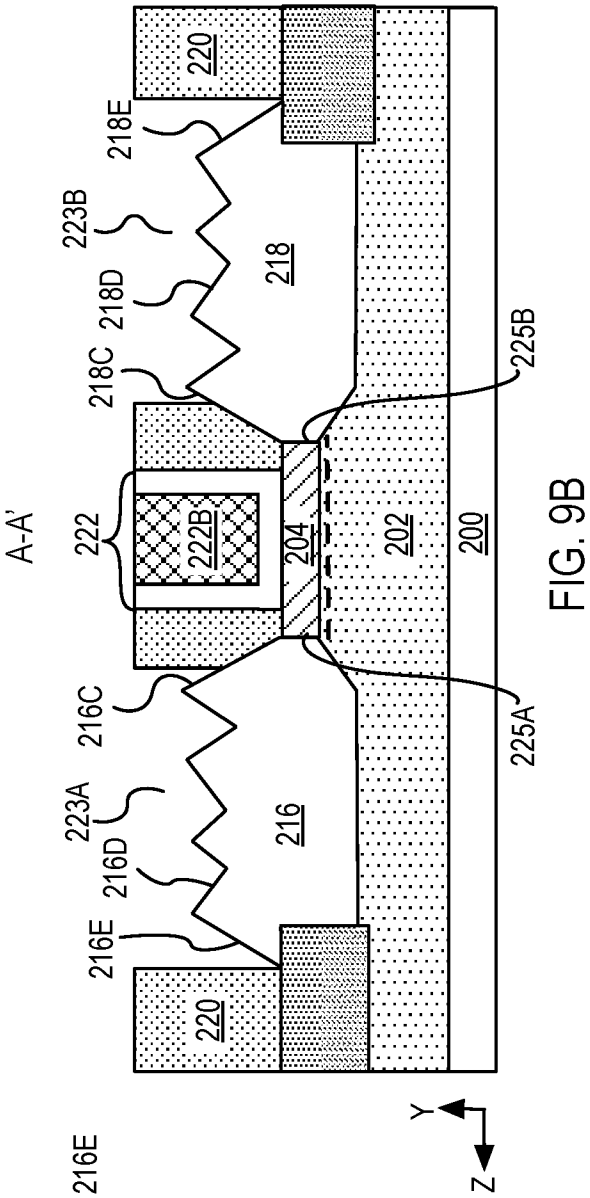

A-A'
220
218E
223B
218D
218C
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225B
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222B
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FIG. 9B

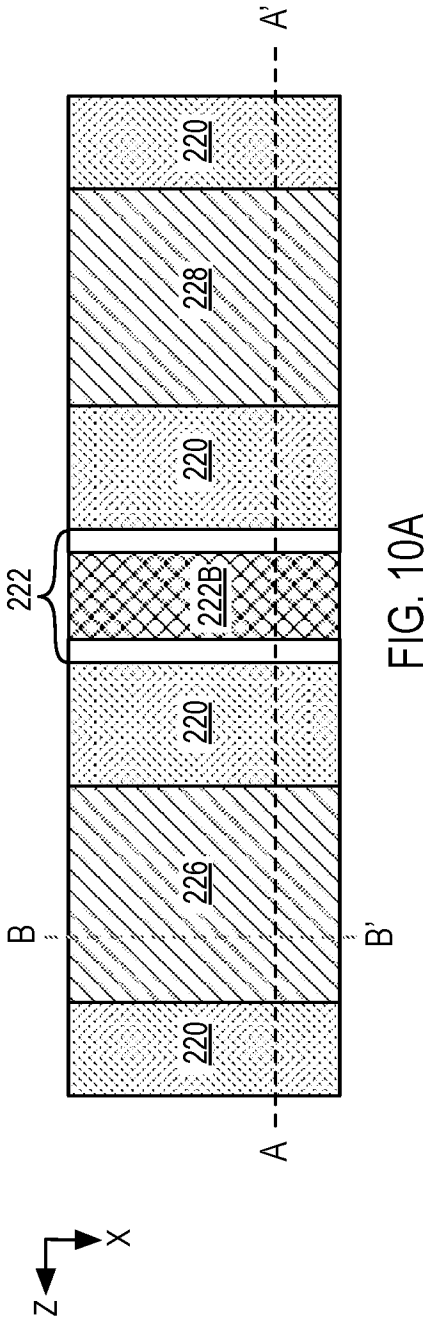


FIG. 10A

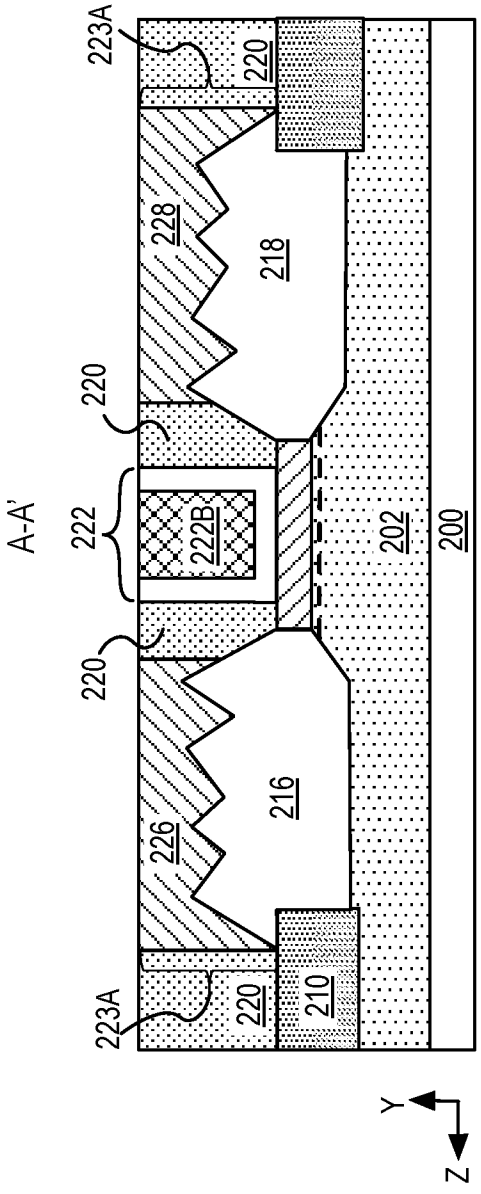


FIG. 10B

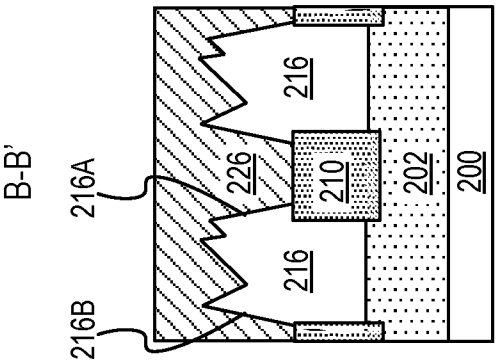


FIG. 10C

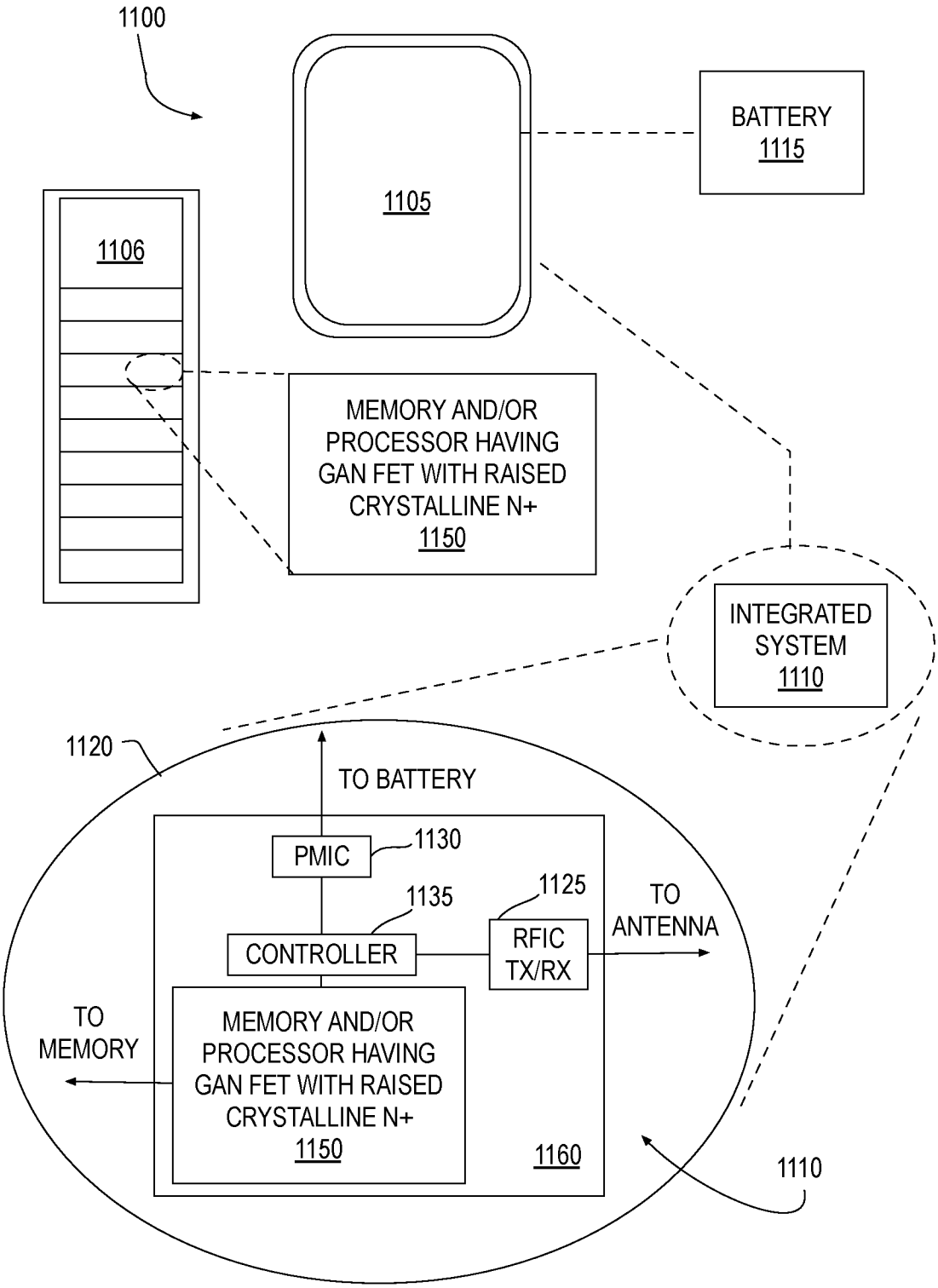

1100
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BATTERY
1115
1106
MEMORY AND/OR
PROCESSOR HAVING
GAN FET WITH RAISED
CRYSTALLINE N+
1150
INTEGRATED
SYSTEM
1110
1120
TO BATTERY
PMIC
1130
1135
1125
TO
ANTENNA
CONTROLLER
RFIC
TX/RX
TO
MEMORY
MEMORY AND/OR
PROCESSOR HAVING
GAN FET WITH RAISED
CRYSTALLINE N+
1150
1160
1110

FIG. 11

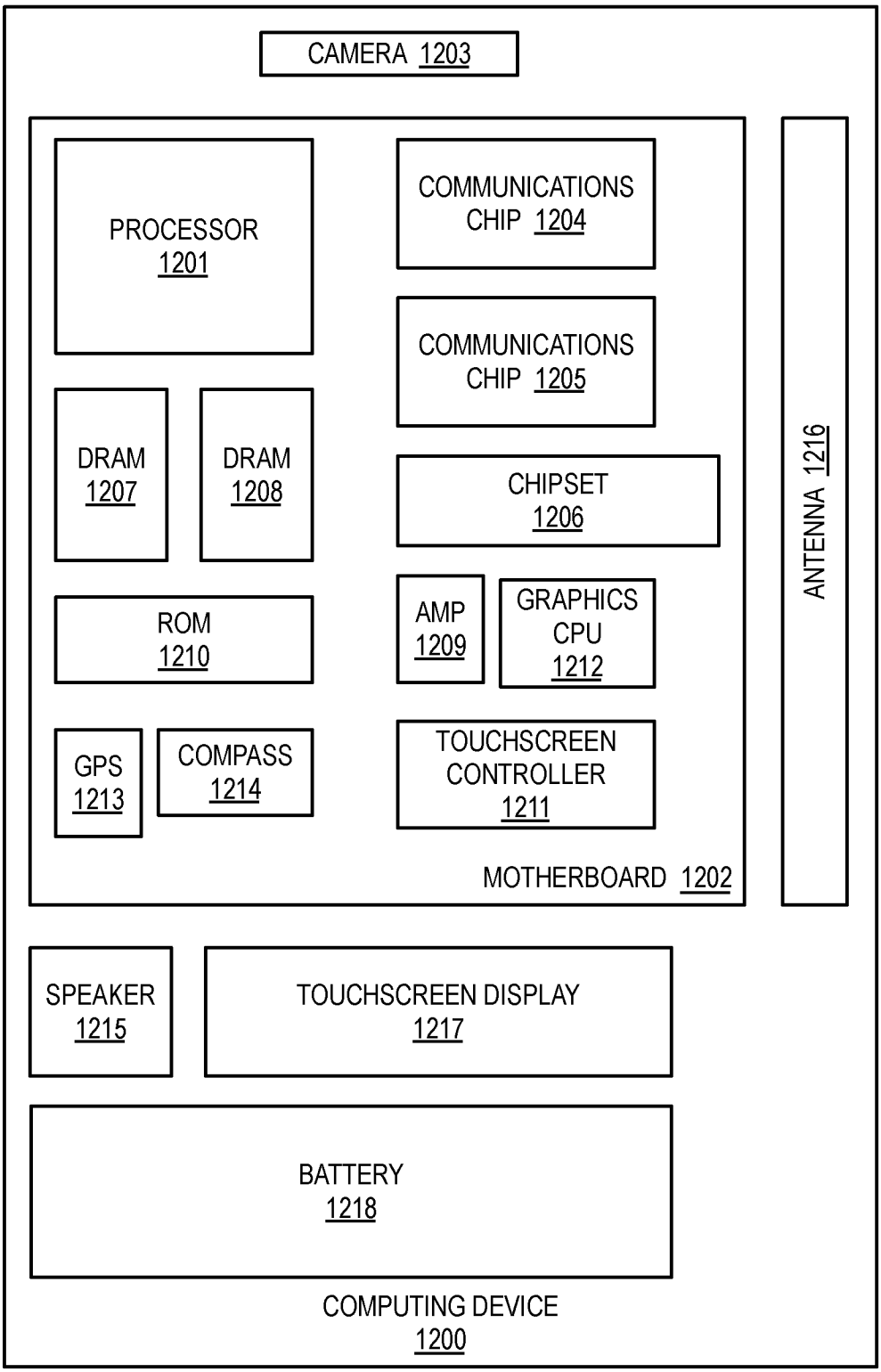

CAMERA 1203
PROCESSOR 1201
COMMUNICATIONS CHIP 1204
COMMUNICATIONS CHIP 1205
DRAM 1207
DRAM 1208
CHIPSET 1206
ROM 1210
AMP 1209
GRAPHICS CPU 1212
GPS 1213
COMPASS 1214
TOUCHSCREEN CONTROLLER 1211
MOTHERBOARD 1202
ANTENNA 1216
SPEAKER 1215
TOUCHSCREEN DISPLAY 1217
BATTERY 1218
COMPUTING DEVICE 1200

FIG. 12

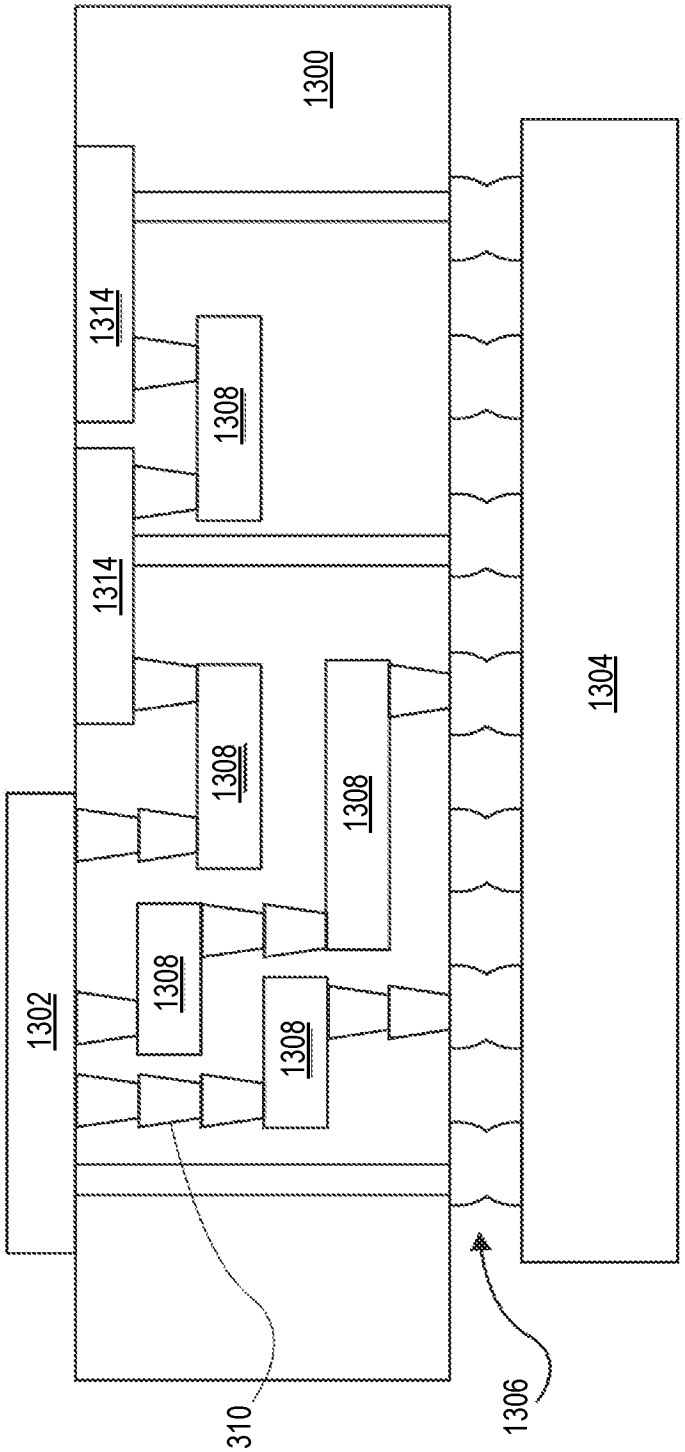


FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/054471

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 21/8234(2006.01)i, H01L 29/66(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/78; H01L 29/778; H01L 27/088; H01L 29/94; H01L 29/66; H01L 29/423; H01L 21/8234

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: transistor, group III-Nitride, charge inducing layer, gate, source/drain

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2016-209263 A1 (INTEL CORPORATION) 29 December 2016 See page 4, lines 15-33; page 6, line 18 - page 13, line 31; page 16, lines 17-25; claims 1, 20, 22; and figures 1, 2A-2F, 5.	1-6,15-22,24
Y	US 9240410 B2 (THEN et al.) 19 January 2016 See column 4, line 60 - column 5, line 5; and figures 2A-2C.	1-6,15-22,24
A	US 8530978 B1 (CHU et al.) 10 September 2013 See figures 1, 5.	1-6,15-22,24
A	US 2006-0197129 A1 (WOHLMUTH) 07 September 2006 See figures 1A-1C.	1-6,15-22,24
A	US 2015-0340482 A1 (SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC) 26 November 2015 See figures 1, 5, 6B.	1-6,15-22,24

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 June 2018 (28.06.2018)	**28 June 2018 (28.06.2018)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
LEE, Myung Jin
Telephone No. +82-42-481-8474

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/054471

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 8
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
The claim 8 is not clear under PCT Article 6 because it refers to claim 7, which do not comply with PCT Rule 6.4(a)

3. ☒ Claims Nos.: 7,9-14,23,25
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required addtional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2017/054471

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