UNIT AND METHOD FOR SYNCHRONOUS RECTIFICATION CONTROL

START

301: Measuring current I

302: Outputting a high value for V1 or for V2 based on current I

303: Generating SQ1 and SQ2 based on Q1, Q2, V1 and V2

END

Fig. 11
UNIT AND METHOD FOR SYNCHRONOUS RECTIFICATION CONTROL

FIELD OF INVENTION

Implementations described herein relate generally to a synchronous rectification control unit and a method for controlling synchronous rectification. In particular is herein described a mechanism for generating first and second synchronous pulse width modulation, PWM, control signals usable for controlling switching a power switch.

BACKGROUND OF INVENTION

Power switches, for example switches being realised by use of MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) or other suitable types of transistors, are used in a large number of circuits today. For example, such power switches are used power converters, which may be implemented as half bridge power converters or full bridge power converters. E.g. full bridge power converter circuits may include a synchronous side and a non-synchronous side. In such a circuit, the non-synchronous side is the side to which the original/non-converted signal/power is inputted, and the synchronous side is the side where the manipulated/converted signal/power is outputted. This can also be expressed as the synchronous rectification side is defined as a side of the circuit, at which side the synchronous rectification power switches are located. Correspondingly, the non-synchronous rectification side is defined as side of the circuit, at which side the main power switches are located.

Thus, for a bidirectional circuit, the non-synchronous side of the circuit can correspond to different physical sides of the circuit, depending on in which direction the signal/power should be manipulated/converted, since the original
signal/power is input to the non-synchronous side. Correspondingly, the synchronous side of the circuit can correspond to different physical sides of the circuit, depending on in which direction the signal/power should be manipulated/converted, since the manipulated/converted signal/power is output from the synchronous side.

Circuits including such power switches, e.g. power transforming circuits or the like, can be utilised in a large variety of units, e.g. in a User Equipment (UE), also known as a mobile station, wireless terminal and/or mobile terminal enabled to communicate wirelessly in a wireless communication network, sometimes also referred to as a cellular radio system. Such circuits can also be utilised in a radio network node, or base station, e.g., a Radio Base Station (RBS), which in some networks may be referred to as "eNB", "eNodeB", "NodeB" or "B node", depending on the technology and/or terminology used.

Switching of the power converters in such circuits aims at being as power efficient as possible. MOSFETs, and other transistors being used for realising the power switches, generally have a lower electrical resistance when the switch is closed/conducting than when the switch is open/non-conducting. As a non-limiting example can be mentioned that a MOSFET switch has a voltage drop over the switch corresponding to the body diode voltage of the MOSFET, which can be e.g. 0.7 Volt, when the switch is open. When the MOSFET switch is closed, the voltage drop over the switch is much lower, e.g. 0.01 Volt according to a non-limiting example. Therefore, to achieve as high power efficiency as possible, as much power as possible should flow through the closed switch, which has the lower voltage drop.
Conventional synchronous rectification has been suggested for improving the power efficiency of circuits by controlling switching of the power switches being included in the circuits. Today, a number of conventional synchronous rectification control solutions have been proposed. One such solution utilizes a current transformer, which is placed on the synchronous rectification side of the circuit. The voltage drop across the current transformer is measured. Based on the measured voltage drop signal, a control circuit creates appropriate pulses to turn-on and turn-off power switches on the synchronous rectification side of the circuit.

However, the conventional solutions generally have poor efficiency, since a relatively large portion of the power flows through the body diode of the power switches when the switch is open. Also, the conventional solutions have high implementation complexity, which adds to production costs for the circuits.

**SUMMARY OF INVENTION**

It is therefore an object to solve at least some of the above mentioned disadvantages and to improve the power efficiency and to lower the implementation complexity of circuits including a synchronous side and a non-synchronous side.

According to a first aspect, the object is achieved by a synchronous rectification control unit including:

- a voltage pulse generation circuit configured to:
  - measure a current $I$ in a circuit including a power switch;
  - output a logic high value for a first voltage $V_I$ if said current $I$ has a positive change rate adjacent to a value of zero for said current $I$; and
  - output a logic high value for a second voltage $V_2$ if
said current $I$ has a negative change rate adjacent to a value of zero for said current $I$;
- a control algorithm circuit configured to generate a first and second synchronous pulse width modulation, PWM, control signal $SQ_1$ and $SQ_2$ based on a first and a second non-synchronous PWM control signal $Q_1$ and $Q_2$, and based on said first voltage $VI$ and said second voltage $V_2$, said first and second synchronous PWM control signals $SQ_1$ and $SQ_2$ being usable for controlling switching of said power switch.

The synchronous rectification control unit can provide a high power efficiency and low power dissipation losses. The synchronous rectification control unit can generate the first and second synchronous PWM control signals $SQ_1$ and $SQ_2$ based on continuous or discontinuous AC current waveforms, or based on continuous or discontinuous rectified AC current waveforms, which results in more flexibility for the current measurement. The synchronous rectification control unit can be implemented with very low addition to the circuit complexity.

The synchronous rectification control unit further provides an inherent current shoot-through protection, a fast transient response, and low power dissipation. Also, the need for PWM resources are minimized by the synchronous rectification control unit.

In a first possible implementation form of the synchronous rectification control unit according to the first aspect, said current $I$ is a rectified alternating current $I_{AC\_rect}$, and said control algorithm circuit is configured to generate a logic high value for said first synchronous PWM control signal $SQ_1$ if said first voltage $VI$ has a logic high value and said first non-synchronous PWM control signal $Q_1$ has a logic high value.
The logic high value of the first voltage $V_I$ indicates that the body diode of the power switch in the synchronous rectification side starts the conduction. Thus, the logical high value of the first voltage $V_I$ is an indicator to turn-on the power switch in the synchronous rectification side in order to avoid diode conduction and to increase the efficiency. Moreover, the first non-synchronous PWM control signal $Q_1$ is taken into account in order to guarantee that the first synchronous PWM control signal $SQ_1$ (and not the second synchronous PWM control signal $SQ_2$) is chosen.

In a second possible implementation form of the synchronous rectification control unit according to the first aspect as such or according to any of the preceding implementation forms of the first aspect, said current $I$ is a rectified alternating current $I_{AC\_rect}$, and said control algorithm circuit is configured to generate a logic low value for said first synchronous PWM control signal $SQ_1$ if at least one of said first voltage $V_I$ and said first non-synchronous PWM control signal $Q_1$ has a logic low value, and if said second voltage $V_2$ has a logic high value or if said second non-synchronous PWM control signal $Q_2$ has a logic high value.

The logic high value of the second voltage $V_2$ indicates that the body diode of the power switch in the synchronous rectification side stops the conduction. Thus, the logic high value of the second voltage $V_2$ is an indicator to turn-off the power switch in the synchronous rectification side in order to avoid current-shoot through. Also, the second non-synchronous PWM control signal $Q_2$ is taken into account in order to guarantee that current-shoot through will not happen. Thus, the utilization of the second non-synchronous PWM control signal $Q_2$ results in a current shoot-through protection, which guarantees appropriate operation of the circuit.
In a third possible implementation form of the synchronous rectification control unit according to the first aspect as such or according to any of the preceding implementation forms of the first aspect, said current \( I \) is a rectified alternating current \( I_{AC \_rect} \), and said control algorithm circuit is configured to generate a previous value for said first synchronous PWM control signal \( SQ1 \) if at least one of said first voltage \( V1 \) and said first non-synchronous PWM control signal \( Q1 \) has a logic low value, and if both said second voltage \( V2 \) and said second non-synchronous PWM control signal \( Q2 \) has a logic low value.

Hereby, the first synchronous PWM control signal \( SQ1 \) is set to a correct previous value, i.e. logic high or logic low, which makes the system robust and insensitive to circuit disturbances. Also, during the time period when this implementation form is performed, the values of the signals in the circuit, i.e. of \( Q1, V1, Q2 \) and \( V2 \) can be logic low, which means the energy consumed is minimized.

In a fourth possible implementation form of the synchronous rectification control unit according to the first aspect as such or according to any of the preceding implementation forms of the first aspect, said current \( I \) is a rectified alternating current \( I_{AC \_rect} \), and said control algorithm circuit is configured to generate a logic high value for said second synchronous PWM control signal \( SQ2 \) if said first voltage \( V1 \) has a logic high value and said second non-synchronous PWM control signal \( Q2 \) has a logic high value.

The logic high value of the first voltage \( V1 \) indicates that the body diode of the power switch in the synchronous rectification side starts the conduction. Thus, the logic high value of the first voltage \( V1 \) is an indicator to turn-on the
power switch in the synchronous rectification side in order to avoid diode conduction and to increase the efficiency. Also the second non-synchronous PWM control signal Q2 is taken into account in order to guarantee that the second synchronous PWM control signal SQ2 (and not the first synchronous PWM control signal SQ1) is chosen.

In a fifth possible implementation form of the synchronous rectification control unit according to the first aspect as such or according to any of the preceding implementation forms of the first aspect, said current I is a rectified alternating current $I_{AC}$, e.t, and said control algorithm circuit is configured to generate a logic low value for said second synchronous PWM control signal SQ2 if at least one of said first voltage $V_I$ and said second $Q_2$ non-synchronous PWM control signal has a logic low value, and if said second voltage $V_2$ has a logic high value or if said first non-synchronous PWM control signal $Q_1$ has a logic high value.

The logic high value of the second voltage $V_2$ indicates that the body diode of the power switch in the synchronous rectification side stops the conduction. Thus, the logic high value of the second voltage $V_2$ is an indicator to turn-off the power switch in the synchronous rectification side in order to avoid current-shoot through. Also, the first non-synchronous PWM control signal $Q_1$ is taken into account in order to guarantee that current-shoot through will not happen. Thus, the utilization of the first non-synchronous PWM control signal $Q_1$ results in a protection, such that the appropriate operation of the circuit is guaranteed.

In a sixth possible implementation form of the synchronous rectification control unit according to the first aspect as such or according to any of the preceding implementation forms
of the first aspect, said current $I$ is a rectified alternating current $I_{AC\text{-rect}}$, and said control algorithm circuit is configured to generate a previous value for second synchronous PWM control signal $SQ2$ if at least one of said first voltage $V_I$ and said second non-synchronous PWM control signal $Q2$ has a logic low value, and if both said second voltage $V_2$ and said first non-synchronous PWM control signal $Q1$ has a logic low value.

Hereby, it is guaranteed that the second synchronous PWM control signal $SQ2$ is set to a correct value, e.g. logic high or logic low, which makes the system robust and insensitive to circuit disturbances. Also, during the time period when this implementation form is performed, the logic values of the signals in the circuit, i.e. $Q1$, $V_I$, $Q2$ and $V2$ can be low, which means that the energy consumed is minimized.

In a seventh possible implementation form of the synchronous rectification control unit according to the first aspect as such, said current $I$ is an alternating current $I_{AC}$, and said control algorithm circuit is configured to generate a logic high value for said first synchronous PWM control signal $SQ1$ if said first voltage $V_I$ has a logic high value and said first non-synchronous PWM control signal $Q1$ has a logic high value.

Here, the first non-synchronous PWM control signal $Q1$ is taken into account in order to guarantee that the first synchronous PWM control signal $SQ1$ is chosen, and not the second synchronous PWM control signal $SQ2$. Then the logic high value of the first voltage $V_I$ indicates that the body diode of the power switch in the synchronous rectification side starts the conduction. Thus, the logic high value of the first voltage $V_I$ is an indicator to turn-on the power switch $SQ1$ in the
synchronous rectification side in order to avoid diode conduction and increase the power efficiency.

In a eighth possible implementation form of the synchronous rectification control unit according to the first aspect as such or according to the seventh possible form of the first aspect, said current \( I \) is an alternating current \( I_{AC} \), and said control algorithm circuit is configured to generate a logic low value for said first synchronous PWM control signal SQ1 if at least one of said first voltage \( V_I \) and said first non-synchronous PWM control signal \( Q_1 \) has a logic low value, and if said second voltage \( V_2 \) has a logic high value or if said second non-synchronous PWM control signal \( Q_2 \) has a logic high value.

The high value of the second voltage \( V_2 \) indicates that the body diode of the power switch in the synchronous rectification side stops the conduction. Thus, the logic high value of the second voltage \( V_2 \) is an indicator to turn-off the power switch SQ1 in the synchronous rectification side in order to avoid current-shoot through. Therefore, the utilization of the second non-synchronous PWM control signal \( Q_2 \) results in a circuit protection and guarantees that current-shoot through will not happen. Hereby, an appropriate operation of the circuit is guaranteed.

In a ninth possible implementation form of the synchronous rectification control unit according to the first aspect as such or according to any of the seventh or eighth possible implementation forms of the first aspect, said current \( I \) is a alternating current \( I_{AC} \), and said control algorithm circuit is configured to generate a previous value for said first synchronous PWM control signal SQ1 if at least one of said first voltage \( V_I \) and said first non-synchronous PWM control
signal $Q_1$ has a logic low value, and if both said second voltage $V_2$ and said second non-synchronous PWM control signal $Q_2$ has a logic low value.

Hereby, it is guaranteed that the first synchronous PWM control signal $SQ_1$ is set to a correct previous value, i.e. logic high or logic low, which makes the system robust and insensitive to circuit disturbances. Moreover, during the time period when this implementation form is performed, the values of the signals in the circuit, e.g. $Q_1$, $V_1$, $Q_2$ and $V_2$ can be low, which means that the energy consumed is as little as possible.

In a tenth possible implementation form of the synchronous rectification control unit according to the first aspect as such or according to any of the seventh, eighth or ninth possible implementation forms of the first aspect, said current $I$ is an alternating current $I_{AC}$, and said control algorithm circuit is configured to generate a logic high value for said second synchronous PWM control signal $SQ_2$ if said second voltage $V_2$ has a logic high value and said second non-synchronous PWM control signal $Q_2$ has a logic high value.

Here, the second non-synchronous PWM control signal $Q_2$ is taken into account in order to guarantee that the first synchronous PWM control signal $SQ_1$ is chosen, and that the second synchronous PWM control signal $SQ_2$ is not chosen. The logic high value of the second voltage $V_2$ indicates that the body diode of the power switch $SQ_2$ in the synchronous rectification side starts the conduction. Thus, the logic high value of the second voltage $V_2$ is an indicator to turn-on the power switch $SQ_2$ in the synchronous rectification side in order to avoid diode conduction and increase the power efficiency.
In a eleventh possible implementation form of the synchronous rectification control unit according to the first aspect as such or according to any of the seventh, eighth, ninth or tenth possible implementation forms of the first aspect, said current I is an alternating current $I_{AC}$, and said control algorithm circuit is configured to generate a logic low value for said second synchronous PWM control signal $SQ2$ if at least one of said second voltage $V2$ and said second non-synchronous PWM control signal $Q2$ has a logic low value, and if said first voltage $VI$ has a logic high value or if said first non-synchronous PWM control signal $Q1$ has a logic high value.

The logic high value of the first voltage $VI$ indicates that the body diode of the power switch $SQ2$ in the synchronous rectification side stops the conduction. Thus, the logic high value of the first voltage $VI$ is an indicator to turn-off the power switch $SQ2$ in the synchronous rectification side in order to avoid current-shoot through. Moreover, the first non-synchronous PWM control signal $Q1$ is taken into account in order to guarantee that current-shoot through will not happen. Thus, the usage of the first non-synchronous PWM control signal $Q1$ here acts as protection, such that appropriate operation of the circuit is guaranteed.

In a twelfth possible implementation form of the synchronous rectification control unit according to the first aspect as such or according to any of the seventh, eighth, ninth, tenth or eleventh possible implementation forms of the first aspect, said current I is an alternating current $I_{AC}$, and said control algorithm circuit is configured to generate a previous value for said second synchronous PWM control signal $SQ2$ if at least one of said second voltage $V2$ and said second non-synchronous PWM control signal $Q2$ has a logic low value, and
if both said first voltage $V_I$ and said first non-synchronous PWM control signal $Q_1$ has a logic low value.

Hereby, it is guaranteed that the second synchronous PWM control signal $SQ_2$ is set to a correct previous value, i.e. logic high or logic low, which makes the system robust and insensitive to circuit disturbances. Moreover, during the time period when this implementation form is performed, the values of the signals in the circuit $Q_1$, $VI$, $Q_2$ and $V_2$ can be low, which means that the energy consumed is as little as possible.

According to a second aspect, the object is achieved by a method for controlling synchronous rectification, comprising:
- measuring a current $I$ in a circuit including a power switch;
- outputting:
  - a logic high value for a first voltage $V_I$ if said current $I$ has a positive change rate adjacent to a value of zero for said current $I$, or
  - a logic high value for a second voltage $V_2$ if said current $I$ has a negative change rate adjacent to a value of zero for said current $I$; and
- generating a first and a second synchronous pulse width modulation, PWM, control signals $SQ_1$ and $SQ_2$ based on a first and a second non-synchronous PWM control signal $Q_1$ and $Q_2$, and based on said first voltage $V_I$ and said second voltage $V_2$, said first and second synchronous PWM control signals $SQ_1$ and $SQ_2$ being usable for controlling switching of said power switch.

The synchronous rectification control method can provide a high power efficiency and low power dissipation losses. The synchronous rectification control method can generate the first and second synchronous PWM control signals $SQ_1$ and $SQ_2$ based on continuous or discontinuous AC current waveforms, or
based on continuous or discontinuous rectified AC current waveforms, which results in more flexibility for the current measurement. The synchronous rectification control method can be implemented with very low addition to the circuit complexity.

The synchronous rectification control method further provides an inherent current shoot-through protection, a fast transient response, and low power dissipation. Also, the need for PWM resources are minimized by the synchronous rectification control method.

In a first possible implementation form of the method for controlling the synchronous rectification according to the second aspect, said current I is a rectified alternating current $I_{AC, \text{rect}}$, and said control algorithm circuit is generating a logic high value for said first synchronous PWM control signal $SQ1$ if said first voltage $VI$ has a logic high value and said first non-synchronous PWM control signal $Q1$ has a logic high value.

The logic high value of the first voltage $VI$ indicates that the body diode of the power switch in the synchronous rectification side starts the conduction. Thus, the logical high value of the first voltage $VI$ is an indicator to turn-on the power switch in the synchronous rectification side in order to avoid diode conduction and to increase the efficiency. Moreover the first non-synchronous PWM control signal $Q1$ is taken into account in order to guarantee that the first synchronous PWM control signal $SQ1$ (and not the second synchronous PWM control signal $SQ2$) is chosen.

In a second possible implementation form of the method for controlling the synchronous rectification according to the second aspect as such or according any of the preceding
implementation forms of the first aspect, said current $I$ is a rectified alternating current $\text{lAc}_{\text{rect}}$, and said control algorithm circuit is generating a logic low value for said first synchronous PWM control signal $\text{SQ1}$ if at least one of said first voltage $V_1$ and said first non-synchronous PWM control signal $Q_1$ has a logic low value, and if said second voltage $V_2$ has a logic high value or if said second non-synchronous PWM control signal $Q_2$ has a logic high value.

The logic high value of the second voltage $V_2$ indicates that the body diode of the power switch in the synchronous rectification side stops the conduction. Thus, the logic high value of the second voltage $V_2$ is an indicator to turn-off the power switch in the synchronous rectification side in order to avoid current-shoot through. Also, the second non-synchronous PWM control signal $Q_2$ is taken into account in order to guarantee that current-shoot through will not happen. Thus, the utilization of the second non-synchronous PWM control signal $Q_2$ results in a current shoot-through protection, which guarantees appropriate operation of the circuit.

In a third possible implementation form of the method for controlling the synchronous rectification according to the second aspect as such or according any of the preceding implementation forms of the first aspect, said current $I$ is a rectified alternating current $\text{lAc}_{\text{rect}}$, and said control algorithm circuit is generating a previous value for said first synchronous PWM control signal $\text{SQ1}$ if at least one of said first voltage $V_1$ and said first non-synchronous PWM control signal $Q_1$ has a logic low value, and if both said second voltage $V_2$ and said second non-synchronous PWM control signal $Q_2$ has a logic low value.
Hereby, the first synchronous PWM control signal SQ1 is set to a correct previous value, i.e. logic high or logic low, which makes the system robust and insensitive to circuit disturbances. Also, during the time period when this implementation form is performed, the values of the signals in the circuit, i.e. of Q1, VI, Q2 and, V2 can be logic low, which means the energy consumed is minimized.

In a fourth possible implementation form of the method for controlling the synchronous rectification according to the second aspect as such or according any of the preceding implementation forms of the first aspect, said current I is a rectified alternating current \( I_{AC\_rect} \), and said control algorithm circuit is generating a logic high value for said second synchronous PWM control signal SQ2 if said first voltage VI has a logic high value and said second non-synchronous PWM control signal Q2 has a logic high value.

The logic high value of the first voltage VI indicates that the body diode of the power switch in the synchronous rectification side starts the conduction. Thus, the logic high value of the first voltage VI is an indicator to turn-on the power switch in the synchronous rectification side in order to avoid diode conduction and to increase the efficiency. Also the second non-synchronous PWM control signal Q2 is taken into account in order to guarantee that the second synchronous PWM control signal SQ2 (and not the first synchronous PWM control signal SQ1) is chosen.

In a fifth possible implementation form of the method for controlling the synchronous rectification according to the second aspect as such or according any of the preceding implementation forms of the first aspect, said current I is a rectified alternating current \( I_{AC\_ext} \), and said control
algorithm circuit is generating a logic low value for said second synchronous PWM control signal SQ2 if at least one of said first voltage VI and said second non-synchronous PWM control signal Q2 has a logic low value, and if said second voltage V2 has a logic high value or if said first non-synchronous PWM control signal Q1 has a logic high value.

The logic high value of the second voltage V2 indicates that the body diode of the power switch in the synchronous rectification side stops the conduction. Thus, the logic high value of the second voltage V2 is an indicator to turn-off the power switch in the synchronous rectification side in order to avoid current-shoot through. Also, the first non-synchronous PWM control signal Q1 is taken into account in order to guarantee that current-shoot through will not happen. Thus, the utilization of the first non-synchronous PWM control signal Q1 results in a protection, such that the appropriate operation of the circuit is guaranteed.

In a sixth possible implementation form of the method for controlling the synchronous rectification according to the second aspect as such or according any of the preceding implementation forms of the first aspect, said current I is a rectified alternating current $I_{AC\_rect}$, and said control algorithm circuit is generating a previous value for second synchronous PWM control signal SQ2 if at least one of said first voltage VI and said second non-synchronous PWM control signal Q2 has a logic low value, and if both said second voltage V2 and said first non-synchronous PWM control signal Q1 has a logic low value.

Hereby, it is guaranteed that the second synchronous PWM control signal SQ2 is set to a correct previous value, e.g. logic high or logic low, which makes the system robust and
insensitive to circuit disturbances. Also, during the time period when this implementation form is performed, the logic values of the signals in the circuit, i.e. Q1, V1, Q2 and V2 can be low, which means that the energy consumed is minimized.

In a seventh possible implementation form of the method for controlling the synchronous rectification according to the second aspect as such, said current I is an alternating current $I_{AC}$, and said control algorithm circuit is generating a logic high value for said first synchronous PWM control signal SQ1 if said first voltage $V_1$ has a logic high value and said first non-synchronous PWM control signal Q1 has a logic high value.

Here, the first non-synchronous PWM control signal Q1 is taken into account in order to guarantee that the first synchronous PWM control signal SQ1 is chosen, and not the second synchronous PWM control signal SQ2. Then the logic high value of the first voltage $V_1$ indicates that the body diode of the power switch in the synchronous rectification side starts the conduction. Thus, the logic high value of the first voltage $V_1$ is an indicator to turn-on the power switch SQ1 in the synchronous rectification side in order to avoid diode conduction and increase the power efficiency.

In a eighth possible implementation form of the method for controlling the synchronous rectification according to the second aspect as such or according to the seventh possible implementation form of the first aspect, said current I is an alternating current $I_{AC}$, and said control algorithm circuit is generating a logic low value for said first synchronous PWM control signal SQ1 if at least one of said first voltage $V_1$ and said first non-synchronous PWM control signal Q1 has a logic low value, and if said second voltage $V_2$ has a logic
high value or if said second non-synchronous PWM control signal Q2 has a logic high value.

The high value of the second voltage V2 indicates that the body diode of the power switch in the synchronous rectification side stops the conduction. Thus, the logic high value of the second voltage V2 is an indicator to turn-off the power switch SQ1 in the synchronous rectification side in order to avoid current-shoot through. Therefore, the utilization of the second non-synchronous PWM control signal Q2 results in a circuit protection and guarantees that current-shoot through will not happen. Hereby, an appropriate operation of the circuit is guaranteed.

In a ninth possible implementation form of the method for controlling the synchronous rectification according to the second aspect as such or according to any of the seventh or eighth possible implementation forms of the first aspect, said current I is a alternating current $I_{AC}$, and said control algorithm circuit is generating a previous value for said first synchronous PWM control signal SQ1 if at least one of said first voltage VI and said first non-synchronous PWM control signal Q1 has a logic low value, and if both said second voltage V2 and said second non-synchronous PWM control signal Q2 has a logic low value.

Hereby, it is guaranteed that the first synchronous PWM control signal SQ1 is set to the correct previous value, i.e. logic high or logic low, which makes the system robust and insensitive to circuit disturbances. Moreover, during the time period when this implementation form is performed, the values of the signals in the circuit, e.g. Q1, VI, Q2 and V2 can be low, which means that the energy consumed is as little as possible.
In a tenth possible implementation form of the method for controlling the synchronous rectification according to the second aspect as such or according to any seventh, eighth, or ninth possible implementation forms of the first aspect, said current I is an alternating current $I_{AC}$, and said control algorithm circuit is generating a logic high value for said second synchronous PWM control signal SQ2 if said second voltage V2 has a logic high value and said second non-synchronous PWM control signal Q2 has a logic high value.

Here, the second non-synchronous PWM control signal Q2 is taken into account in order to guarantee that the first synchronous PWM control signal SQ1 is chosen, and that the second synchronous PWM control signal SQ2 is not chosen. The logic high value of the second voltage V2 indicates that the body diode of the power switch SQ2 in the synchronous rectification side starts the conduction. Thus, the logic high value of the second voltage V2 is an indicator to turn-on the power switch SQ2 in the synchronous rectification side in order to avoid diode conduction and increase the power efficiency.

In an eleventh possible implementation form of the method for controlling the synchronous rectification according to the second aspect as such or according to any of the seventh, eighth, ninth or tenth possible implementation forms of the first aspect, said current I is an alternating current $I_{AC}$, and said control algorithm circuit is generating a logic low value for said second synchronous PWM control signal SQ2 if at least one of said second voltage V2 and said second non-synchronous PWM control signal Q2 has a logic low value, and if said first voltage VI has a logic high value or if said first non-synchronous PWM control signal Q1 has a logic high value.
The logic high value of the first voltage $V_I$ indicates that the body diode of the power switch SQ2 in the synchronous rectification side stops the conduction. Thus, the logic high value of the first voltage $V_I$ is an indicator to turn-off the power switch SQ2 in the synchronous rectification side in order to avoid current-shoot through. Moreover, the first non-synchronous PWM control signal $Q_l$ is taken into account in order to guarantee that current-shoot through will not happen. Thus, the usage of the first non-synchronous PWM control signal $Q_l$ here acts as protection, such that appropriate operation of the circuit is guaranteed.

In a twelfth possible implementation form of the method for controlling the synchronous rectification according to the second aspect as such or according to any of the seventh, eighth, ninth, tenth or eleventh possible implementation forms of the first aspect, said current $I$ is an alternating current $I_{AC}$, and said control algorithm circuit is generating a previous value for said second synchronous PWM control signal SQ2 if at least one of said second voltage $V_2$ and said second Q2 non-synchronous PWM control signal has a logic low value, and if both said first voltage $V_I$ and said first non-synchronous PWM control signal $Q_l$ has a logic low value.

Hereby, it is guaranteed that the second synchronous PWM control signal SQ2 is set to a correct previous value, i.e. logic high or logic low, which makes the system robust and insensitive to circuit disturbances. Moreover, during the time period when this implementation form is performed, the values of the signals in the circuit $Q_l$, $V_I$, $Q_2$ and $V_2$ can be low, which means that the energy consumed is as little as possible.

According to a third aspect, the object is achieved by a computer program with a program code for performing a method
according to the second aspect when the computer program runs on a computer.

The computer program according to the third aspect has advantages corresponding to the advantages stated above for the second aspect. Further, a computer program with a program code gives flexibility, accuracy, and robustness to environmental conditions. Also, the program code is easily modified and updated.

According to a fourth aspect, the object is achieved by an integrated circuit comprising at least one synchronous rectification control unit according to the first aspect as such or according any of the preceding implementation forms of the first aspect.

The integrated circuit according to the fourth aspect has advantages corresponding to the advantages stated above for the first aspect.

According to a fifth aspect, the object is achieved by a power electronic device having a power converter comprising the synchronous rectification control unit according to the first aspect as such or according any of the preceding implementation forms of the first aspect.

The power electronic device according to the fifth aspect has advantages corresponding to the advantages stated above for the first aspect.

The above described embodiments can achieve high power efficiency for circuits including one or more power switches. Such circuits may include power converters, such as resonant switching power converters.
The synchronous rectification control unit can be connected to the circuit including the one or more power switch in a way that rectified AC currents or AC currents can be utilized by the unit.

The synchronous rectification control algorithm can be implemented by either analogue control circuits or digital control circuits.

Moreover the proposed synchronous rectification control method can be applied e.g. on bi-directional resonant switching power converters.

Other objects, advantages and novel features of the embodiments of the invention will become apparent from the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention are described in more detail with reference to attached drawings illustrating examples of embodiments of the invention in which:

Fig. 1 is a schematic block diagram illustrating a synchronous rectification control unit according to some embodiments.

Fig. 2 is a flow chart diagram illustrating some embodiments.

Figs. 3a-b are block diagrams illustrating some embodiments.

Fig. 4 is a flow chart diagram illustrating some embodiments.

Figs. 5a-b are block diagrams illustrating some embodiments.
Fig. 6 illustrates examples of input and output signals values according to some embodiments.

Fig. 7 illustrates examples of input and output signals values according to some embodiments.

Fig. 8 illustrates examples of input and output signals values according to some embodiments.

Fig. 9 illustrates examples of input and output signals values according to some embodiments.

Fig. 10 is a schematic block diagram illustrating a power converter including a synchronous rectification control unit according to some embodiments.

Fig. 11 is a flow chart diagram illustrating the synchronous rectification control method according some embodiments.

Fig. 12 is a schematic block diagram illustrating a processing circuit implementing the synchronous rectification control method according to some embodiments.

DETAILED DESCRIPTION OF INVENTION

Embodiments of the invention described herein are defined as a synchronous rectification control unit and a method for controlling synchronous rectification, which may be put into practice in the embodiments described below. These embodiments may, however, be exemplified and realised in many different forms and are not to be considered as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete.
Still other objects and features may become apparent from the following detailed description considered in conjunction with the accompanying drawings. It is to be understood, however, that the drawings are designed solely for purposes of illustration and not as a definition of the limits of the herein disclosed embodiments, for which reference is to be made to the appended claims. Further, the drawings are not necessarily drawn to scale and, unless otherwise indicated, they are merely intended to conceptually illustrate the structures and procedures described herein.

Figure 1 schematically illustrates the inner structure of the synchronous rectification control unit 100 implementing the embodiments of the invention.

The synchronous rectification control unit 100 includes a voltage pulse generation circuit 26 and a control algorithm circuit 27. The synchronous rectification control unit 100 has a current I in a circuit 200 including a power switch 50, and first and second non-synchronous PWM control signals Q1 30 and Q2 31 as inputs. The synchronous rectification control unit 100 outputs first and second synchronous PWM control signals SQ1 32 and SQ2 33 being usable for controlling switching of the power switch 50.

The voltage pulse generation circuit 26 is configured to measure/detect the current I. The voltage pulse generation circuit 26 is also configured to output two voltage pulses.

A logic high value for a first voltage VI 28 is output if the measured/detected current I has a positive change rate; dl/dt>0; adjacent/close to a value of zero for the current I. In this document, dl/dt corresponds to the time derivative of the current I, which of course indicates the change rate of...
the current, i.e. if the current $I$ is increasing (positive value) or is decreasing (negative value).

A logic high value for a second voltage $V_{29}$ is output if the current $I$ has a negative change rate; $dI/dt < 0$; adjacent/close to a value of zero for the current $I$.

The first and second voltage pulses $V_{I28}$ and $V_{29}$, and the first and second non-synchronous PWM control signals $Q_{130}$ and $Q_{231}$ are inputs to the control algorithm circuit 27. The control algorithm circuit 27 is configured to generate the first and second synchronous PWM control signals $SQ_{132}$ and $SQ_{233}$. These first and second synchronous PWM control signals $SQ_{132}$ and $SQ_{233}$ are usable for controlling switching of the power switch 50 of the circuit 200.

The control algorithm circuit 27 is configured to generate the first and second synchronous PWM control signals $SQ_{132}$ and $SQ_{233}$, and based on the first and second non-synchronous PWM control signals $Q_{130}$ and $Q_{231}$, and based on the first voltage $VI_{28}$ and the second voltage $V_{29}$ outputted by the voltage pulse generation circuit 26. Thus, the control logic/algorithm implemented in the control algorithm circuit 27 determines values for and generates the first and second synchronous PWM control signals $SQ_{132}$ and $SQ_{233}$ based on the first and second voltage pulses $VI_{28}$ and $V_{29}$, and on the first and second non-synchronous PWM control signals $Q_{130}$ and $Q_{231}$. The control logic/algorithm used for generating the first and second synchronous PWM control signals $SQ_{132}$ and $SQ_{233}$ is explained in detail below.

Switching of the power switch 50 in the circuit 200 is then performed by usage of these generated first and second synchronous PWM control signals $SQ_{132}$ and $SQ_{233}$.
The synchronous rectification control unit 100 according to embodiments of the invention has a number of advantages. The synchronous rectification control unit can provide high power efficiency. The synchronous rectification control unit 100 can further provide the first and second synchronous PWM control signals SQ1 32 and SQ2 33 based on either of AC current waveforms and rectified AC current waveforms, whereas conventional solutions have been restricted to only AC current waveforms. Since both AC and rectified AC current can be utilized by the synchronous rectification control unit 100, more flexibility of the current measurement can be achieved.

Also, the synchronous rectification control unit 100 according to embodiments of the invention presents a simple, very low complex, and still robust solution to the above stated problems.

The synchronous rectification control unit 100 thus utilizes a simple control algorithm for the synchronous rectification, which utilizes narrow pulses for indication of the turn-on and turn-off instances of the power switch. The synchronous rectification control unit 100 further provides an inherent current shoot-through protection, a fast transient response, and low power dissipation.

The invention utilizes a saturable current transformer, e.g. a current sensing circuit including a saturable comparator, for generating the voltage pulses in the voltage pulse generation circuit 26 in combination with an intelligent control method/algorithm/logic for the synchronous rectification control implemented in the control algorithm circuit 27. The utilisation of the saturable current transformer has the effect that the power dissipation losses are reduced.
The first and second synchronous PWM control signals SQ1 and SQ2, are here generated based on non-synchronous first and second non-synchronous control signals Q1 and Q2. Hereby, PWM resources are minimized in the synchronous rectification control unit 100.

Figure 2 is a flowchart illustrating a couple of embodiments for the method/algorithm/logic of the control algorithm circuit 27.

According to an embodiment illustrated in the left branch of figure 2, the current I input to the synchronous rectification control unit 100 is a rectified alternating current $I_{AC\_rect}$. The method/algorithm/logic of the control algorithm circuit 27 corresponding to the left branch in figure 2 is also illustrated in a flip-flop circuit in figure 3a, which is configured to perform the method/algorithm/logic of the control algorithm circuit 27.

The voltage pulse generation circuit 26 is configured to measure the rectified alternating current $I_{AC\_rect}$ and to output the first and second voltages V1 28 and V2 29 as described above.

According to an embodiment, the control algorithm circuit 27 is, based on the inputted first and second non-synchronous PWM control signals Q1 30 and 31, and on the first and second voltages V1 28 and V2 29, configured to generate a logic high value for the first synchronous PWM control signal SQ1 32 if both the first voltage V1 28 and the first non-synchronous PWM control signal Q1 30 have a logic high value. The generated and outputted logic high value for the first synchronous PWM control signal SQ1 32 is then locked to this logic high value.
According to an embodiment, the control algorithm circuit 27 is, based on the inputted first and second non-synchronous PWM control signals Q1 30 and Q2 31 and on the first and second voltages V1 28 and V2 29, configured to generate and output a logic low value for the first synchronous PWM control signal SQ1 32 if at least one of the first voltage V1 28 and the first non-synchronous PWM control signal Q1 30 has a logic low value, and if the second voltage V2 29 has a logic high value or if the second non-synchronous PWM control signal Q2 31 has a logic high value. The outputted logic low value for the first synchronous PWM control signal SQ1 32 is then locked to this logic low value.

According to an embodiment, the control algorithm circuit 27 is, based on the inputted first and second non-synchronous PWM control signals Q1 30 and Q2 31 and on the first and second voltages V1 28 and V2 29, configured to output a previous value for the first synchronous PWM control signal SQ1 32 if at least one of the first voltage V1 28 and the first non-synchronous PWM control signal Q1 30 has a logic low value, and if both the second voltage V2 29 and the second non-synchronous PWM control signal Q2 31 has a logic low value. The outputted previous value for the first synchronous PWM control signal SQ1 32 is then locked to these previous values.

According to an embodiment illustrated in the right branch of figure 2, the current I input to the synchronous rectification control unit 100 is a rectified alternating current $I_{AC, rect}$. The method/algorithm/logic of the control algorithm circuit 27 corresponding to the right branch in figure 2 is also illustrated in a flip-flop circuit in figure 3b, which is configured for performing the method/algorithm/logic of the control algorithm circuit 27.
According to an embodiment, the control algorithm circuit 27 is, based on the inputted first and second non-synchronous PWM control signals Q1 30 and Q2 31 and on the first and second voltages VI 28 and V2 29, configured to generate and output a logic high value for the second synchronous PWM control signal SQ2 33 if the first voltage VI 28 has a logic high value and the second non-synchronous PWM control signal Q2 31 has a logic high value. The outputted logic high value for the second synchronous PWM control signal SQ2 33 is then locked to this logic high value.

According to an embodiment, the control algorithm circuit 27 is, based on the inputted first and second non-synchronous PWM control signals Q1 30 and Q2 31, and on the first and second voltages VI 28 and V2 29, configured to generate and output a logic low value for the second synchronous PWM control signal SQ2 33 if at least one of the first voltage VI 28 and the second non-synchronous PWM control signal Q2 31 has a logic low value, and if the second voltage V2 29 has a logic high value or if the first non-synchronous PWM control signal Q1 30 has a logic high value. The outputted logic low value for the second synchronous PWM control signal SQ2 33 is then locked to this logic low value.

According to an embodiment, the control algorithm circuit 27 is, based on the inputted first and second non-synchronous PWM control signals Q1 30 and Q2 31, and on the first and second voltages VI 28 and V2 29, configured to generate and output a previous value for the second synchronous PWM control signal SQ2 33 if at least one of the first voltage VI 28 and the second non-synchronous PWM control signal Q2 31 has a logic low value, and if both the second voltage V2 29 and the first non-synchronous PWM control signal Q1 30 has a logic low value. The previous value for the second synchronous PWM
control signal SQ2 33 are then locked to these previous values, respectively.

Figure 4 is a flowchart illustrating a couple of embodiments for the method/algorithm/logic of the control algorithm circuit 27.

According to an embodiment illustrated in the left branch of figure 4, the current $I_{AC}$ input to the synchronous rectification control unit 100 is an alternating current $I_{AC}$, i.e. a non-rectified current. The method/algorithm/logic of the control algorithm circuit 27 corresponding to the left branch in figure 4 is also illustrated in a flip-flop circuit in figure 5a, which is configured to perform the method/algorithm/logic of the control algorithm circuit 27.

If the alternating current $I_{AC}$ here is a measured synchronous rectification side current $I_{AC,sec}$ 35, then the synchronous rectification control unit is a synchronous rectification side unit 2 connected to the AC part of the synchronous rectification side 220, as illustrated in figure 10 below.

Correspondingly, if the alternating current $I_{AC}$ here is a measured non-synchronous alternating AC current $I_{AC,non}$ 36, then the synchronous rectification control unit 100 is a non-synchronous rectification side unit 3 connected to the AC part of the non-synchronous rectification side 210, as illustrated in figure 10 below.

According to an embodiment, the control algorithm circuit 27 is, based on the inputted first and second non-synchronous PWM control signals $Q_1$ 30, $Q_2$ 31 and on the first and second voltages $V_1$ 28 and $V_2$ 29, configured to generate and output a logic high value for the first synchronous PWM control signal SQ1 32 if the first voltage $V_1$ 28 has a logic high value and
the first non-synchronous PWM control signal \( Q_{l30} \) has a logic high value. The outputted logic high value for the first synchronous PWM control signal SQ1 32 is then locked to this logic high value.

According to an embodiment, the control algorithm circuit 27 is, based in the inputted first and second non-synchronous PWM control signals \( Q_{l30} \) and \( Q_{231} \), and on the first and second voltages \( V_{I28} \) and \( V_{229} \), configured to generate and output a logic low value for the first synchronous PWM control signal SQ1 32 if at least one of the first voltage \( V_{I28} \) and the first non-synchronous PWM control signal \( Q_{l30} \) has a logic low value, and if the second voltage \( V_{229} \) has a logic high value or if the second non-synchronous PWM control signal \( Q_{231} \) has a logic high value. The outputted logic low value for the first synchronous PWM control signal SQ1 32 is then locked to this logic low value.

According to an embodiment, the control algorithm circuit 27 is, based in the inputted first and second non-synchronous PWM control signals \( Q_{l30} \) and \( Q_{231} \), and on the first and second voltages \( V_{I28} \) and \( V_{229} \), configured to generate and output a previous value for the first synchronous PWM control signal SQ1 32 if at least one of the first voltage \( V_{I28} \) and the first non-synchronous PWM control signal \( Q_{l30} \) has a logic low value, and if both of the second voltage \( V_{229} \) and the second non-synchronous PWM control signal \( Q_{231} \) have logic low values. The previous value for the first synchronous PWM control signal SQ1 32 is then locked to these previous values, respectively.

According to an embodiment illustrated in the right branch of figure 4, the current I input to the synchronous rectification control unit 100 is an alternating current \( I_{AC} \), i.e. a non-
rectified current. The method/algorithm/logic of the control algorithm circuit 27 corresponding to the right branch in figure 4 is also illustrated in a flip-flop circuit in figure 5b, which is configured for performing the method/algorithm/logic of the control algorithm circuit 27.

If the alternating current $I_{AC}$ here is a measured synchronous rectification side current $I_{AC, sec}$ 35, then the synchronous rectification control unit 27 is connected to the AC part of the synchronous rectification side 220, as illustrated in figure 10 below.

Correspondingly, if the alternating current $I_{AC}$ here is a measured non-synchronous alternating AC current $I_{AC, nrs}$ 36, then the synchronous rectification control unit 100 is a non-synchronous rectification side unit 3 connected to the AC part of the non-synchronous rectification side 210, as illustrated in figure 10 below.

According to an embodiment, the control algorithm circuit 27 is, based in the inputted first and second non-synchronous PWM control signals Q1 30 and Q2 31, and on the first and second voltages V1 28 and V2 29, configured to generate and output a logic high value for the second synchronous PWM control signal SQ2 33 if the second voltage V2 29 has a logic high value and the second non-synchronous PWM control signal Q2 31 has a logic high value. The outputted logic high value for the second synchronous PWM control signal SQ2 33 is then locked to this logic high value.

According to an embodiment, the control algorithm circuit 27 is, based in the inputted first and second non-synchronous PWM control signals Q1 30 and Q2 31, and on the first and second voltages V1 28 and V2 29, configured to generate and output a logic low value for the second synchronous PWM control signal
SQ2 33 if at least one of the second voltage V2 29 and the second non-synchronous PWM control signal Q2 31 has a logic low value, and if the first voltage VI 28 has a logic high value or if the first non-synchronous PWM control signal Q1 30 has a logic high value. The outputted logic low value for the second synchronous PWM control signal SQ2 33 is then locked to this logic low value.

According to an embodiment, the control algorithm circuit 27 is, based in the inputted first and second non-synchronous PWM control signals Q1 30 and Q2 31, and on the first and second voltages VI 28 and V2 29, configured to generate and output a previous value for the second synchronous PWM control signal SQ2 33 if at least one of the second voltage V2 29 and the second non-synchronous PWM control signal Q2 31 has a logic low value, and if both of the first voltage VI 28 and the first non-synchronous PWM control signal Q1 30 has a logic low value. The previous value for the second synchronous PWM control signal SQ2 33 is then locked to these previous values, respectively.

Figure 6 is a graph having plots that illustrate example values and waveforms of the first and second non-synchronous PWM control signals Q1 30 and Q2 31, of the current being an alternating current I_{AC, rect}, of the first and second voltage pulses VI 28 and V2 29, and of the generated first and second synchronous PWM control signals SQ1 32 and SQ2 33 being usable for controlling switching of the power switch. The first and second synchronous PWM control signals SQ1 32 and SQ2 33 are here generated in accordance with the flowchart in figure 2 above.

Figure 6 illustrates the operation condition when the rectified alternating current I_{AC, rect} is continuous. According
to the operation condition presented in figure 6, the first voltage pulse VI 28 is created by the voltage pulse generation circuit 26 if the continuous rectified alternating current $I_{AC_{rect}}$ is adjacent/close to zero and has positive change rate. Alternatively, the second voltage pulse V2 29 is created by the voltage pulse generation circuit 26 if the continuous rectified alternating current $I_{AC_{rect}}$ is adjacent/close to zero and has a negative change rate. The synchronous rectification control algorithm is configured to generate the first and second synchronous PWM control signals SQ1 32 and SQ2 33 in order to turn-on or turn-off the power switch is described above in connection with the flowchart in figure 2.

Figure 7 is a graph having plots that illustrate example values and waveforms of the first and second non-synchronous PWM control signals Q1 30 and Q2 31, of the current being a rectified alternating current $I_{AC_{rect}}$, of the first and second voltage pulses VI 28 and V2 29, and of the generated first and second synchronous PWM control signals SQ1 32 and SQ2 33 being usable for controlling switching of the power switch. The first and second synchronous PWM control signals SQ1 32 and SQ2 33 are here generated in accordance with the flowchart in figure 2 above.

Figure 7 illustrates the operation condition when the rectified alternating current $I_{AC_{rect}}$ is discontinuous. According to the operation condition presented in figure 7, the first voltage pulse VI 28 is created by the voltage pulse generation circuit 26 if the discontinuous rectified alternating current $I_{AC_{rect}}$ is adjacent/close to zero and has positive change rate. Alternatively, the second voltage pulse V2 29 is created by the voltage pulse generation circuit 26 if the discontinuous rectified alternating current $I_{AC_{rect}}$ is adjacent/close to zero and has a negative change rate. The
synchronous rectification control algorithm is configured to generate the first and second synchronous PWM control signals SQ1 32 and SQ2 33 in order to turn-on or turn-off the power switch is described above in connection with the flowchart in figure 2.

Figure 8 is a graph having plots that illustrate example values and waveforms of the first and second non-synchronous PWM control signals Q1 30 and Q2 31, of the current being an alternating current $I_{AC}$, of the first and second voltage pulses VI 28 and V2 29, and of the generated first and second synchronous PWM control signals SQ1 32 and SQ2 33 being usable for controlling switching of the power switch. The first and second synchronous PWM control signals SQ1 32 and SQ2 33 are here generated in accordance with the flowchart in figure 4 above.

Figure 8 illustrates the operation condition when the alternating current $I_{AC}$ is continuous. According to the operation condition presented in figure 8, the first voltage pulse VI 28 is created by the voltage pulse generation circuit 26 if the continuous alternating current $I_{AC}$ is adjacent/close to zero and has positive change rate. Alternatively, the second voltage pulse V2 29 is created by the voltage pulse generation circuit 26 if the continuous alternating current $I_{AC}$ is adjacent/close to zero and has a negative change rate. The synchronous rectification control algorithm is configured to generate the first and second synchronous PWM control signals SQ1 32 SQ2 33 and in order to turn-on or turn-off the power switch is described above in connection with the flowchart in figure 4.

Figure 9 is a graph having plots that illustrate example values and waveforms of the first and second non-synchronous
PWM control signals $Q_{l30}$ and $Q_{231}$, of the current being an alternating current $I_{AC}$, of the voltage first and second voltage pulses $V_{I28}$ and $V_{229}$, and of the generated first and second synchronous PWM control signals $SQ_{132}$ and $SQ_{233}$ being usable for controlling switching of the power switch. The first and second synchronous PWM control signals $SQ_{132}$ and $SQ_{233}$ are here generated in accordance with the flowchart in figure 4 above.

Figure 9 illustrates the operation condition when the alternating current $I_{AC}$ is discontinuous. According to the operation condition presented in figure 9, the first voltage pulse $V_{I28}$ is created by the voltage pulse generation circuit 26 if the discontinuous alternating current $I_{AC}$ is adjacent/close to zero and has positive change rate. Alternatively, the second voltage pulse $V_{229}$ is created by the voltage pulse generation circuit 26 if the discontinuous alternating current $I_{AC}$ is adjacent/close to zero and has a negative change rate. The synchronous rectification control algorithm is configured to generate the first and second synchronous PWM control signals $SQ_{132}$ and $SQ_{233}$ in order to turn-on or turn-off the power switch as described above in connection with the flowchart in figure 4.

As is stated above, the synchronous rectification control unit 100 can be used for controlling a power switch in essentially any circuit 200 including such a power switch 50. Such circuits 200 include e.g. half bridge power converters and full bridge converters.

Figure 10 schematically illustrates one non-limiting example of a circuit diagram for a full bridge power converter circuit 200 in which embodiments of the invention could be implemented. It should, however, be noted that the embodiments
of the invention could also be implemented in a large number of other circuits including one or more power switches.

The circuit 200 in figure 10 is thus a schematic illustration of a resonant switching power converter 200 including a synchronous rectification circuit. The resonant switching power converter 200 is separated into a primary side 210 and a secondary side 220 by an isolation transformer 18. The primary side 210 can in this example correspond to the non-synchronous side 210 of the circuit. The secondary side 220 can here correspond to the synchronous side 220 of the circuit.

The transformer 18 has a primary winding 181 with Np number of turns and a secondary winding 182 with Ns number of turns. The primary side 210 of the resonant switching power converter here includes four non-synchronous side power switches 13, 14, 15 and 16, that can be implemented e.g. by use of MOSFETs or other suitable transistors. The primary side 210 further includes a resonant circuit 17, which can include capacitors and inductors arranged in a well known way, and a capacitor 12 which is connected between two primary side terminals 10 and 11. The capacitor 12 is fed with a rectified AC voltage. Thus, a rectified AC voltage, i.e. a voltage where the negative voltage values of an alternative voltage AC have been converted to corresponding positive voltages is connected to the terminals 10 and 11.

The secondary side 220 of the converter includes four non-synchronous side power switches 19, 20, 21 and 22, that can be implemented e.g. by use of MOSFETs or other suitable transistors. The secondary side 220 further includes a capacitor 25, which is connected between two secondary side terminals 23 and 24 and is fed with a rectified AC voltage.
Thus, a rectified AC voltage is connected to the terminals 23 and 24.

A first non-synchronous control signal Ql 30 drives two of the non-synchronous side power switches 13 and 16 during a first half of a switching period such that the first non-synchronous control signal Ql 30 has a logic high value, which means that the two non-synchronous side power switches power switches driven by the first non-synchronous control signal Ql 30 are turned-on. During a second half of the switching period, the first non-synchronous control signal Ql 30 has a logic low value, which means that the two non-synchronous side power switches driven by the first non-synchronous control signal Ql 30 are turned-off.

The second non-synchronous control signal Q2 31 drives two of the non-synchronous side power switches 14 and 15 during the first half of the switching period/cycle such that the second non-synchronous control signal Q2 31 has a logic low value, which means that the two power switches driven by the second non-synchronous control signal Q2 31 are turned-off. During the second half of the switching period, the second non-synchronous control signal Q2 31 has a logic high value, which means that the two power switches driven by the second non-synchronous control signal Q2 31 are turned-on.

Between the first and second non-synchronous control signal signals Ql and Q2, a dead time has been introduced in order to prevent a current shoot-through in the circuit, i.e. a short circuit due to simultaneous turn-on of multiple power switches. In this document, dead time can be defined as the time period during which both the first and second non-synchronous control signal signals Ql and Q2 have a logic low value. Correspondingly, the dead time can be defined as the
time period during which both the first and second synchronous
control signal signals $Q_1$ and $Q_2$ have a logic low value.

On the secondary/synchronous side 220, a first synchronous
control signal $SQ_1$ 3 2 drives the two of the synchronous side
power switches 19 and 22, and a second synchronous control
signal $SQ_2$ 3 3 drives the power switches 20 and 21 in a
corresponding way as the first non-synchronous control signal
$Q_1$ 3 0 and the second non-synchronous control signal $Q_2$ 3 1
drives the four non-synchronous power switches.

Thus, a first synchronous control signal $SQ_1$ 3 2 drives two of
the synchronous side power switches 19 and 22 during a first
half of a switching period such that the first synchronous
control signal $SQ_1$ 3 2 has a logic high value, which means that
the two synchronous side power switches power switches driven
by the first synchronous control signal $SQ_1$ 3 2 are turned-on.

During a second half of the switching period, the first
synchronous control signal $SQ_1$ 3 2 has a logic low value, which
means that the two synchronous side power switches driven by
the first synchronous control signal $SQ_1$ 3 2 are turned-off.

The second synchronous control signal $SQ_2$ 3 3 drives two of the
synchronous side power switches 20 and 21 during the first
half of the switching period such that the second synchronous
control signal $SQ_2$ 3 3 has a logic low value, which means that
the two power switches driven by the second synchronous
control signal $SQ_2$ 3 3 are turned-off. During the second half
of the switching period, the second synchronous control signal
$SQ_2$ 3 3 has a logic high value, which means that the two power
switches driven by the second synchronous control signal $SQ_2$
3 3 are turned-on.
Between the first and second synchronous control signal signals SQ1 and SQ2, a dead time has been introduced in order to prevent a current shoot-through.

The synchronous rectification control unit 100 can, according to different embodiments described above, be implemented in different locations/positions in the full bridge power converter circuit 200 shown in figure 10.

According to an embodiment, the synchronous rectification control unit 100 is connected to the rectified AC bus, also called DC bus, i.e. on the rectified AC part, of the synchronous rectification side 220 between the power switches 19, 20, 21, 22 and the capacitor 25. The synchronous rectification control unit 100 is thus then denoted 1 in figure 10 and is positioned between points 37 and 38 in figure 1. Here, the current I being input to the synchronous rectification control unit 1 is a rectified AC current $I_{Ac,rect}$ 34, which can be continuous or discontinuous, as described above for rectified alternating currents $I_{Ac,rect}$.

According to another embodiment, the synchronous rectification control unit 100 is connected to the AC part of the synchronous rectification side 220 between the transformer 18 and the two of the power switches 21, 22. The synchronous rectification control unit 100 is thus then denoted 2 in figure 10. Here, the current I being input to the synchronous rectification control unit 2 is a synchronous alternating AC current $I_{Ac,syn}$ 35, which can be continuous or discontinuous, as described above for alternating currents $I_{Ac}$. Thus, if the alternating current $I_{Ac}$ used as input to the synchronous rectification control unit 100 is a measured synchronous rectification side current, then the synchronous rectification control unit is the synchronous rectification side unit 2.
According to another embodiment, the synchronous rectification control unit 100 is connected to the AC part of the non-synchronous rectification side 210 between the resonant circuit 17 and the transformer 18. The synchronous rectification control unit 100 is thus then denoted 3 in figure 10. Here, the current I being measured by the synchronous rectification control unit 3 is a non-synchronous alternating AC current $I_{AC,rim}$ 36, which can be continuous or discontinuous, as described above for alternating currents $I_{AC}$.

In the full bridge converter circuit 200, the non-synchronous alternating AC current $I_{AC,rim}$ 36 can be a mirror waveform of the synchronous alternating AC current $I_{AC,sec}$ 35.

The synchronous rectification control units 1, 2, 3 according to these embodiments of the invention can correspond to anyone of the embodiments disclosed in this document, given that they have the suitable input currents. Thus, the operation of the inner structure of the synchronous rectification control unit 100 described above is also valid for each of the synchronous rectification control units 1, 2, 3 disclosed in figure 10, i.e. when the synchronous side rectified alternating current $I_{AC,rect}$ 34 is input to the synchronous rectification control unit 1, when the synchronous side alternating current $I_{AC,sec}$ 35 is input to the synchronous rectification control unit 2, or when the non-synchronous side alternating current $I_{AC,rim}$ 36 is input to the synchronous rectification control unit 3.

Figure 11 is a flow chart illustrating actions of a method 300 method for controlling synchronous rectification.

It is however to be noted that any, some or all of the described actions 301-303, may be performed in a somewhat different chronological order than the enumeration indicates, be performed simultaneously or even be performed in reversed order.
Further, it is to be noted that some actions may be performed in a plurality of alternative manners according to different embodiments. The method 300 may comprise the following actions:

5 Action 301

In a first action 301, a current a current I in a circuit 100 including a power switch 50 is measured.

Action 302

In a second action 302, a logic high value for a first voltage VI 28 is outputted if the current I has a positive change rate adjacent to a value of zero for the current I.

Alternatively, a logic high value for a second voltage V2 29 is outputted if the current I has a negative change rate adjacent to a value of zero for the current I.

15 Action 303

In a third action 303, first and second synchronous pulse width modulation, PWM, control signals SQ1 32 and SQ2 33 are generated based on first and second non-synchronous PWM control signals Q1 30 and Q2 31, and based on the first voltage VI 28 and the second voltage V2 29. The generated first and second synchronous PWM control signals SQ1 32 and SQ2 33 are then usable for controlling switching of the power switch 50 in the circuit 200.

Also, the method for controlling synchronous rectification may be implemented in a circuit 400 schematically illustrated in figure 12. The processing circuit 400 is configured for:

- measuring 301 a current I in a circuit 100 including a power switch 50;
- outputting 302
  - a logic high value for a first voltage V1 28 if the current I has a positive change rate adjacent to a value of zero for said current I, or
  - a logic high value for a second voltage V2 29 if the current I has a negative change rate adjacent to a value of zero for the current I; and
- generating 303 first and second synchronous pulse width modulation, PWM, control signals SQ1 32 and SQ2 33 based on first and second non-synchronous PWM control signals Q1 30 and Q2 31, and based on the first voltage V1 28 and the second voltage V2 29. These first and second synchronous PWM control signals SQ1 32 and SQ2 33 are usable for controlling switching of the power switch 50.

The processing circuit 400 may comprise, e.g., one or more instances of a Central Processing Unit (CPU), a processing unit, a processing circuit, a processor, an Application Specific Integrated Circuit (ASIC), a microprocessor, or other processing logic that may interpret and execute instructions. The herein utilised expression "processing circuit" may thus represent a processing circuitry comprising a plurality of processing circuits, such as, e.g., any, some or all of the ones enumerated above.

The processing circuit 400 may further perform data processing functions for inputting, outputting, and processing of data comprising data buffering and device control functions.

The processing circuit 400 may be connected to at least one memory 401, according to some embodiments. The memory 401 may comprise a physical device utilised to store data or programs, i.e., sequences of instructions, on a temporary or permanent basis. According to some embodiments, the memory 401 may
comprise integrated circuits comprising silicon-based transistors. Further, the memory 401 may be volatile or non-volatile.

The previously described actions 301-303 may be implemented through one or more processing circuits 400, together with computer program code for performing the functions of the actions 301-303. Thus a computer program product, comprising instructions for performing the actions 301-303 may perform the method 300 controlling synchronous rectification, when the computer program product is loaded in a processing circuit 400.

The computer program product mentioned above may be provided for instance in the form of a data carrier carrying computer program code for performing any, at least some, or all of the actions 301-303 according to some embodiments when being loaded into the processing circuit 400. The data carrier may be, e.g., a hard disk, a CD ROM disc, a memory stick, an optical storage device, a magnetic storage device or any other appropriate medium such as a disk or tape that may hold machine readable data in a non transitory manner. The computer program product may furthermore be provided as computer program code on a server and may be downloaded remotely, e.g., over an Internet or an intranet connection.

The terminology used in the detailed description of the embodiments as illustrated in the accompanying drawings is not intended to be limiting of the described method 300 and/or synchronous rectification control unit 100, which instead are limited by the enclosed claims.

As used herein, the term "and/or" comprises any and all combinations of one or more of the associated listed items. In addition, the singular forms "a", "an" and "the" are to be
interpreted as "at least one", thus also possibly comprising a plurality of entities of the same kind, unless expressly stated otherwise. It will be further understood that the terms "includes", "comprises", "including" and/ or "comprising", specifies the presence of stated features, actions, integers, steps, operations, elements, and/ or components, but do not preclude the presence or addition of one or more other features, actions, integers, steps, operations, elements, components, and/ or groups thereof.
CLAIMS

1. A synchronous rectification control unit (100) including:
   - a voltage pulse generation circuit (26) configured to
     - measure a current I in a circuit (200) including a
     - power switch (50);
     - output a logic high value for a first voltage VI (28) if said current I has a positive change rate adjacent to a value of zero for said current I; and
     - output a logic high value for a second voltage V2 (29) if said current I has a negative change rate adjacent to a value of zero for said current I;
   - a control algorithm circuit (27) configured to generate a first and a second synchronous pulse width modulation, PWM, control signal SQ1 (32) and SQ2 (33) based on a first and a second non-synchronous PWM control signal Q1 (30) and Q2 (31), and based on said first voltage VI (28) and said second voltage V2 (29), said first and second synchronous PWM control signals SQ1 (32) and SQ2 (33) being usable for controlling switching of said power switch (50).

2. The synchronous rectification control unit (100) as claimed in claim 1, wherein said current I is a rectified alternating current \( \text{I}_{\text{AC, rect}} \), and said control algorithm circuit (27) is configured to generate a logic high value for said first synchronous PWM control signal SQ1 (32) if said first voltage VI (28) has a logic high value and said first non-synchronous PWM control signal Q1 (30) has a logic high value.

3. The synchronous rectification control unit (100) as claimed in anyone of claim 1-2, wherein said current I is a rectified alternating current \( \text{I}_{\text{AC, rect}} \), and said control algorithm circuit (27) is configured to generate a logic low value for said first synchronous PWM control signal SQ1 (32)
if at least one of said first voltage $V_I$ (28) and said first non-synchronous PWM control signal $Q_1$ (30) has a logic low value, and if said second voltage $V_2$ (29) has a logic high value or if said second non-synchronous PWM control signal $Q_2$ (31) has a logic high value.

4. The synchronous rectification control unit (100) as claimed in anyone of claim 1-3, wherein said current $I$ is a rectified alternating current $I_{AC\text{rect}}$, and said control algorithm circuit (27) is configured to generate a previous value for said first PWM control signal $SQ_1$ (32) if at least one of said first voltage $V_I$ (28) and said first non-synchronous PWM control signal $Q_1$ (30) has a logic low value, and if both said second voltage $V_2$ (29) and said second non-synchronous PWM control signal $Q_2$ (31) has a logic low value.

5. The synchronous rectification control unit (100) as claimed in anyone of claims 1-4, wherein said current $I$ is a rectified alternating current $I_{AC\text{rect}}$, and said control algorithm circuit (27) is configured to generate a logic high value for said second synchronous PWM control signal $SQ_2$ (33) if said first voltage $V_I$ (28) has a logic high value and said second non-synchronous PWM control signal $Q_2$ (31) has a logic high value.

6. The synchronous rectification control unit (100) as claimed in anyone of claim 1-5, wherein said current $I$ is a rectified alternating current $I_{AC\text{rect}}$, and said control algorithm circuit (27) is configured to generate a logic low value for said second synchronous PWM control signal $SQ_2$ (33) if at least one of said first voltage $V_I$ (28) and said second non-synchronous PWM control signal $Q_2$ (31) has a logic low value, and if said second voltage $V_2$ (29) has a logic high value.
value or if said first non-synchronous PWM control signal \( Q_1 \) (30) has a logic high value.

7. The synchronous rectification control unit (100) as claimed in anyone of claim 1-6, wherein said current \( I \) is a rectified alternating current \( I_{\text{AC}} \) and said control algorithm circuit (27) is configured to generate a previous value for and second synchronous PWM control signal \( SQ_2 \) (33) if at least one of said first voltage \( V_1 \) (28) and said second non-synchronous PWM control signal \( Q_2 \) (31) has a logic low value, and if both said second voltage \( V_2 \) (29) and said first non-synchronous PWM control signal \( Q_1 \) (30) has a logic low value.

8. The synchronous rectification control unit (100) as claimed in claim 1, wherein said current \( I \) is an alternating current \( I_{\text{AC}} \) and said control algorithm circuit (27) is configured to generate a logic high value for said first synchronous PWM control signal \( SQ_1 \) (32) if said first voltage \( V_1 \) (28) has a logic high value and said first non-synchronous PWM control signal \( Q_1 \) (30) has a logic high value.

9. The synchronous rectification control unit (100) as claimed in anyone of claims 1 or 8, wherein said current \( I \) is an alternating current \( I_{\text{AC}} \) and said control algorithm circuit (27) is configured to generate a logic low value for said first synchronous PWM control signal \( SQ_1 \) (32) if at least one of said first voltage \( V_1 \) (28) and said first non-synchronous PWM control signal \( Q_1 \) (30) has a logic low value, and if said second voltage \( V_2 \) (29) has a logic high value or if said second non-synchronous PWM control signal \( Q_2 \) (31) has a logic high value.

10. The synchronous rectification control unit (100) as claimed in anyone of claims 1, 8 or 9, wherein said current \( I \)
is a alternating current $I_{AC}$, and said control algorithm circuit (27) is configured to generate a previous value for said first synchronous PWM control signal SQ1 (32) if at least one of said first voltage $V_1$ (28) and said first non-synchronous PWM control signal Q1 (30) has a logic low value, and if both said second voltage $V_2$ (29) and said second non-synchronous PWM control signal Q2 (31) has a logic low value.

11. The synchronous rectification control unit (100) as claimed in anyone of claims 1 or 8-10, wherein said current $I$ is an alternating current $I_{AC}$, and said control algorithm circuit (27) is configured to generate a logic high value for said second synchronous PWM control signal SQ2 (33) if said second voltage $V_2$ (29) has a logic high value and said second non-synchronous PWM control signal Q2 (31) has a logic high value.

12. The synchronous rectification control unit (100) as claimed in anyone of claim 1 or 8-11, wherein said current $I$ is an alternating current $I_{AC}$, and said control algorithm circuit (27) is configured to generate a logic low value for said second synchronous PWM control signal SQ2 (33) if at least one of said second voltage $V_2$ (29) and said second non-synchronous PWM control signal Q2 (31) has a logic low value, and if said first voltage $V_1$ (28) has a logic high value or if said first non-synchronous PWM control signal Q1 (30) has a logic high value.

13. The synchronous rectification control unit (100) as claimed in anyone of claim 1 or 8-12, wherein said current $I$ is an alternating current $I_{AC}$, and said control algorithm circuit (27) is configured to generate a previous value for said second synchronous PWM control signals SQ2 (33) if at least one of said second voltage $V_2$ (29) and said second non-
synchronous PWM control signal Q2 (31) has a logic low value, and if both said first voltage VI (28) and said first non-synchronous PWM control signal Q1 (30) has a logic low value.

14. An integrated circuit comprising at least one of the synchronous rectification control unit (100) according to any of claims 1-13.

15. A power electronic device having a power converter comprising the synchronous rectification control unit (100) according to any of claims 1-13.

16. A method (300) for controlling synchronous rectification, comprising:
   - measuring (301) a current I in a circuit (100) including a power switch (50);
   - outputting (302):
     - a logic high value for a first voltage VI (28) if said current I has a positive change rate adjacent to a value of zero for said current I, or
     - a logic high value for a second voltage V2 (29) if said current I has a negative change rate adjacent to a value of zero for said current I; and
   - generating (303) a first and a second synchronous pulse width modulation, PWM, control signal SQ1 (32) and SQ2 (33) based on a first and a second non-synchronous PWM control signal Q1 (30) and Q2 (31), and based on said first voltage VI (28) and said second voltage V2 (29), said first and second synchronous PWM control signals SQ1 (32) and SQ2 (33) being usable for controlling switching of said power switch (50).
17. A computer program with a program code for performing a method according to claim 16, when the computer program runs on a computer.
Fig. 1
Input:
V1, V2 pulses
Q1, Q2 PWM signals

2/8
Start

V1=High AND Q1=High
Yes
Set and lock SQ1=High
No
V2=High OR Q2=High
Yes
Set and lock SQ1=LOW
No

V1=High AND Q2=High
Yes
Set and lock SQ2=High
No
V2=High OR Q1=High
Yes
Set and lock SQ2=LOW
No

Keep old values of SQ1 SQ2

End

Fig. 2
4/8
Start

Input:
V1, V2 pulses
Q1, Q2 PWM signals

V1=High AND Q1=High
Yes No
Set and lock SQ1=High

V2=High OR Q2=High
Yes No
Set and lock SQ2=High

V2=High AND Q2=High
Yes No
Set and lock SQ2=High

V1=High OR Q1=High
Yes No
Set and lock SQ1=LOW

Keep old values of SQ1, SQ2

End

Fig. 4
Fig. 8

Fig. 9
START

301: Measuring current I

302: Outputting a high value for V1 or for V2 based on current I

303: Generating SQ1 and SQ2 based on Q1, Q2, V1 and V2

END

Fig. 11

401 Memory

400 Processing circuit

Fig. 12
A. CLASSIFICATION OF SUBJECT MATTER

According to International Patent Classification (IPC) or to both national classification and IPC

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
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<td>1-17</td>
</tr>
<tr>
<td>A</td>
<td>US 2014/119063 AI (TSENG P0-JUNG [TW] ET AL) 1 May 2014 (2014-05-01) the whole document</td>
<td>1-17</td>
</tr>
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</tbody>
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Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:
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<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Wo 2007/145388 Al (PSTEK CO LTD [KR]; SE0NG HWANHO [KR]) 21 December 2007 (2007-12-21) the whole document</td>
<td>1-17</td>
</tr>
<tr>
<td>Patent document cited in search report</td>
<td>Publication date</td>
<td>Patent family member(s)</td>
</tr>
<tr>
<td>---------------------------------------</td>
<td>-----------------</td>
<td>-------------------------</td>
</tr>
<tr>
<td>US 6992906</td>
<td>31-01-2006</td>
<td>NONE</td>
</tr>
<tr>
<td>US 2014119063</td>
<td>01-05-2014</td>
<td>CN 103795234 A</td>
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<td></td>
<td>TW 201417467 A</td>
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<tr>
<td></td>
<td></td>
<td>US 2014119063 AI</td>
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<tr>
<td>US 2010118565</td>
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<td></td>
<td>US 2010118565 AI</td>
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<tr>
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<td>CN 103780094 A</td>
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<td>TW 201417472 A</td>
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<td>US 2014112027 AI</td>
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<td>JP 2008035641 A</td>
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<td></td>
<td></td>
<td>US 2008049473 AI</td>
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<tr>
<td>Wo 2007145388</td>
<td>21-12-2007</td>
<td>NONE</td>
</tr>
</tbody>
</table>