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(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventor: **ZHANG, Kevin**; 1807 NW Pentland Street, Portland, OR 97229 (US).

(74) Agent: **MALLIE, Michael, J.**; Blakely Sokoloff Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

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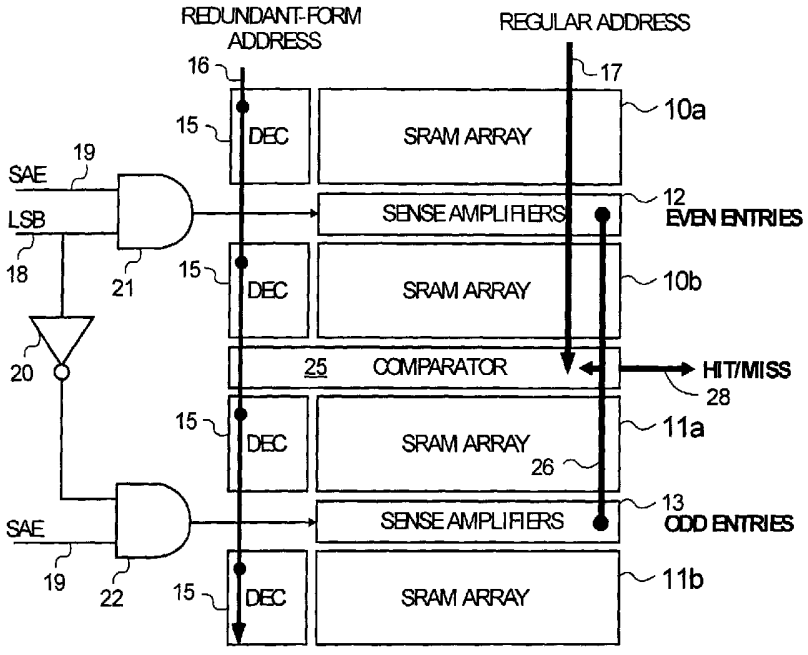
(54) **Title:** TAG DESIGN FOR CACHE ACCESS WITH REDUNDANT-FORM ADDRESS



(57) **Abstract:** A memory and method for accessing data in a memory which uses non redundant-form address decoders is disclosed. Lines in subarrays of the memory are selected using the redundant-form address. The least significant bit of the non redundant-form address is used to selected between these lines. The compare function of the cache memory is then done with a non redundant-form address.

WO 03/001533 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

TAG DESIGN FOR CACHE ACCESS WITH REDUNDANT-FORM ADDRESS

FIELD OF THE INVENTION

[0001] The invention relates to field of memories particularly those using redundant-form addresses.

PRIOR ART AND RELATED ART

[0002] The latency of on-chip caching has become more and more important to the overall performance of microprocessors. To speed up cache access, a redundant-form addressing system is known which permits cache access before the final complete address becomes available. In general, the ordinary binary address is replaced with a more complex address (redundant-form). In effect, address components from an adder are used since these are more quickly available. For instance, these components are not delayed by the carry chain needed to complete the ordinary address. Aspects of this technology are described in PCT Application WO 99/64953; co-pending Application Serial Number 09/532,411 entitled "Shared Cache Word Line Decoder For Redundant And Regular Addresses" filed March 22, 2000; and Application Serial Number 09/538,553 entitled "Cache Column Multiplexing Using Redundant Form Addresses" filed March 29, 2000.

[0003] One problem associated with using redundant-form addresses is that it is costly to do redundant-form tag compares. Substantial additional circuitry is required to handle the redundant-form tag comparison.

[0004] As will be seen, the present invention solves this problem.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] **Figure 1** is a block diagram illustrating an embodiment of the present invention.

[0006] **Figure 2** is a flow diagram illustrating the steps of one embodiment of the present invention.

[0007] **Figure 3** is a timing diagram used in conjunction with the block diagram of **Figure 1**.

DETAILED DESCRIPTION OF THE INVENTION

[0008] A memory is described particularly useful for caching where redundant-form addresses are used. In the following description, embodiments of the invention are described for a cache memory having a particular architecture. It will be apparent to one skilled in the art that the invention may be practiced without these specific embodiments. In other instances, well-known circuits, such as comparators, have not been shown in detail in order not to obscure the present invention.

Overview Of One Embodiment

[0009] The memory array (which includes at least the tag fields and associated data for one embodiment) is first divided into odd and even entries (sometimes also referred herein to as subarrays). A redundant-form address is used by decoders to select a line in both the even and odd subarrays. Also a small differential voltage is developed at the bit lines in the arrays. While this is occurring, the least significant bit (LSB) for the ordinary (non redundant-form address) is generated along with the final (non redundant) address bits. The LSB is used to enable the sense amplifiers associated with one of the odd or even subarrays. The output of the sense amplifiers drive a common data bus, shared by both odd and even subarrays. The tag field of the data from the selected subarray is coupled to a ordinary (non redundant-form) comparator. This allows the tag to be accessed early with a redundant-form address. While the non redundant-form tag bits are being completed, the tag bit lines are activated and subsequently used for developing a hit/miss generation (way select). By doing this, the very costly redundant-form compare is avoided without incurring a speed penalty. Additionally, since only one set of sense amplifiers is selected during the redundant-form access, the sensing power is minimized. Moreover, the shared data buses between the subarrays provides metal trace reduction in the fabrication of an integrated circuit employing the disclosed memory.

Embodiment of Figure 1

[0010] Referring to **Figure 1**, the memory includes an even subarray shown as arrays 10a and 10b and an odd subarrays comprising arrays 11a and 11b.

These are ordinary static random-access memory (SRAM) arrays such as are often found in a cache memory. Arrays 10a and 10b are associated with the sense amplifiers 12. A tag field from array 10a or 10b may be sensed by the amplifiers 12 and coupled to the comparators 25 on data bus 26. Similarly, the arrays 11a and 11b are associated with the sense amplifiers 13. When lines are selected in these arrays, they are sensed by the sense amplifiers 13 with a tag field being coupled to the comparator 25 on data bus 26. It should be noted that the data bus 26 is common to both subarrays; however, as will be seen, only one set of sense amplifiers 12 or 13 are activated at any one time.

[0011] Decoders 15 are redundant-form address decoders which receive the redundant-form address on lines 16 and which select a line or lines in both of the subarrays. These decoders are described in more detail in the references cited in the "Prior Art And Related Art" section of this application.

[0012] The ordinary tag position of the address (that is the non redundant-form address) is coupled on lines 17 to the comparator 25. Within the comparator 25, this address is compared with the stored tag to provide a hit or miss indication on line 28 as is typically done. The comparators, as mentioned previously, are ordinary non redundant-form comparators, and operate on the ordinary address on lines 17 and a tag from the arrays.

[0013] Most typically, the hit/miss signal is coupled to a data array for selecting the data. For instance, in a four-way associative cache, one of four lines of data may be selected.

[0014] The LSB of the ordinary address is coupled to the AND gate 21 and also through inverter 20 to the AND gate 22. A sense amplifier enable signal (SAE) on line 19 is also coupled to the gates 21 and 22. If the LSB is even (a binary 1), the sense amplifiers 12 are selected when SAE is active. On the other hand, if the LSB is odd, the sense amplifiers 13 are selected through the output of the gate 22 when the SAE is active.

[0015] As shown in **Figure 3**, at time 30, assume that a redundant-form address is coupled to the decoders 15. The redundant-form address is decoded during time 31. This causes at lease one line to be selected in each of the subarrays 10 and 11, that is the word lines in both subarrays are turned on. Additionally, in one embodiment, a small differential voltage is developed at the bit lines in the arrays.

[0016] At time 32, the LSB of the ordinary address will have been determined. This bit and its complement are coupled to the gates 21 and 22, respectively. As mentioned, if the LSB is even, then the amplifiers 12 are selected whereas if it is odd, the amplifiers 13 are selected. During time 33, the sense amplifiers can sense the tag field being coupled to the comparator 25 from the selected subarray. At time 34, the ordinary address will become available and is coupled to the comparator 25 on line 17. At time 35, the comparison will have been completed and a hit or miss signal will be provided on the line 28 allowing, for instance, the selection of data from the data array.

Method of the Present Invention

[0017] Referring now to **Figure 2**, the method of the present invention is shown beginning with step **100** where the decoding of the redundant-form memory address occurs. This decoded address is used as mentioned to select one or more lines in the each of the subarrays as shown by step **101**.

[0018] Now as show by step **102**, selected lines from only one of the subarrays is selected based on the redundant-form address, for instance, based on the LSB of the ordinary address signal.

[0019] The tag field selected by step **102** is then compared with the bits of the non redundant-form address to provide a hit or miss signal as indicated by step **103**.

[0020] In the above description, the array was divided into odd and even subarrays, and the least significant bit was used to select between these arrays. In another embodiment, it is possible to use the two least significant bits, or for that matter, any number of least significant bits, and to divide the array for instance, into four subarrays and to select between the four subarrays using the two least significant bits. Also in the above description, it was assumed that the tag field and related data were read from the array at the same time. It is also possible to first compare the tag field with the non redundant-form address and then, for instance, read data based on the status of a hit/miss signal. Other alternate embodiments will be apparent to one skilled in the art.

[0021] Thus, a cache memory implying redundant-form addresses and non redundant-form addresses where the compare function has been described.

CLAIMS

What is claimed:

1. A memory comprising:

a first and a second array;

a redundant-form address decoder coupled to the first and second arrays for selecting a line in each of the first and second arrays;

a circuit for selecting between the selected lines in the first and second arrays based on at least one bit of a non redundant-form memory address.

2. The memory defined by claim 1 wherein the one bit of the non redundant-form memory address is the least significant bit of the address.

3. The memory defined by claim 1 wherein data from the first and second memory arrays are coupled to common lines.

4. The memory defined by claim 1 wherein the circuit for selecting between the selected lines includes first and second sense amplifiers wherein one of the first and second sense amplifiers are activated by the one bit of the non redundant-form memory address.

5. The memory defined by claim 4 wherein the one bit of the non redundant-form memory address is the least significant bit of the address.

6. The memory defined by claim 5 wherein data from the first and second memory arrays are coupled to common lines.

7. The memory defined by claim 6 including a comparator coupled to receive signals from the first and second sense amplifiers and coupled to receive bits of the non redundant-form memory address.

8. The memory defined by claim 7 wherein the comparator provides a hit/miss signal.

9. The memory defined by claim 1 including a comparator for receiving signals from the sense amplifiers and coupled to receive non redundant-form address bits.

10. A memory comprising:

a storage array separated into at least two subarrays;

a redundant-form decoder for selecting at least one line in each of the subarrays in response to redundant-form address bits;

first sense amplifiers coupled to one of the subarrays;

second sense amplifiers coupled to the other of the subarrays;

a selection circuit for selecting data from one of the first and second sense amplifiers in response to at least one bit of a non redundant-form address.

11. The memory defined by claim 10 wherein the one bit of the non redundant-form address is the least significant bit of the address.

12. The memory defined by claim 11 wherein the first and second sense amplifiers are coupled to common output lines.

13. The memory defined by claim 12 including a comparator coupled to receive a tag field from the selected one of the subarrays and non redundant-form address bits.

14. The memory defined by claim 10 including a comparator coupled to receive a tag field from the selected one of the subarrays and non redundant-form address bits.

15. A method for accessing a memory comprising:

selecting first and second data based on a redundant-form address; and

selecting between the first and second data based on at least one bit of a non redundant-form address.

16. The method defined by claim 15 wherein the one bit of the non redundant-form is the least significant bit of the address.

17. The method defined by claim 15 including the step of comparing part of the selected data with bits of non redundant-form address.

18. The memory defined by claim 17 wherein the one bit of the non redundant-form address is the least significant bit.

19. A method comprising the steps of:

decoding a redundant-form memory address;

selecting at least two lines in a memory array based on the decoded redundant-form memory address;

selecting between the two lines based on at least one bit of a non redundant-form memory address;

comparing bits of the non redundant-form memory address with tag bits from the selected line.

20. The memory defined by claim 19 wherein the one bit of the non redundant-form memory address is the least significant bit of the address.

21. The method defined by claim 20 including the step of providing a hit/miss signal.

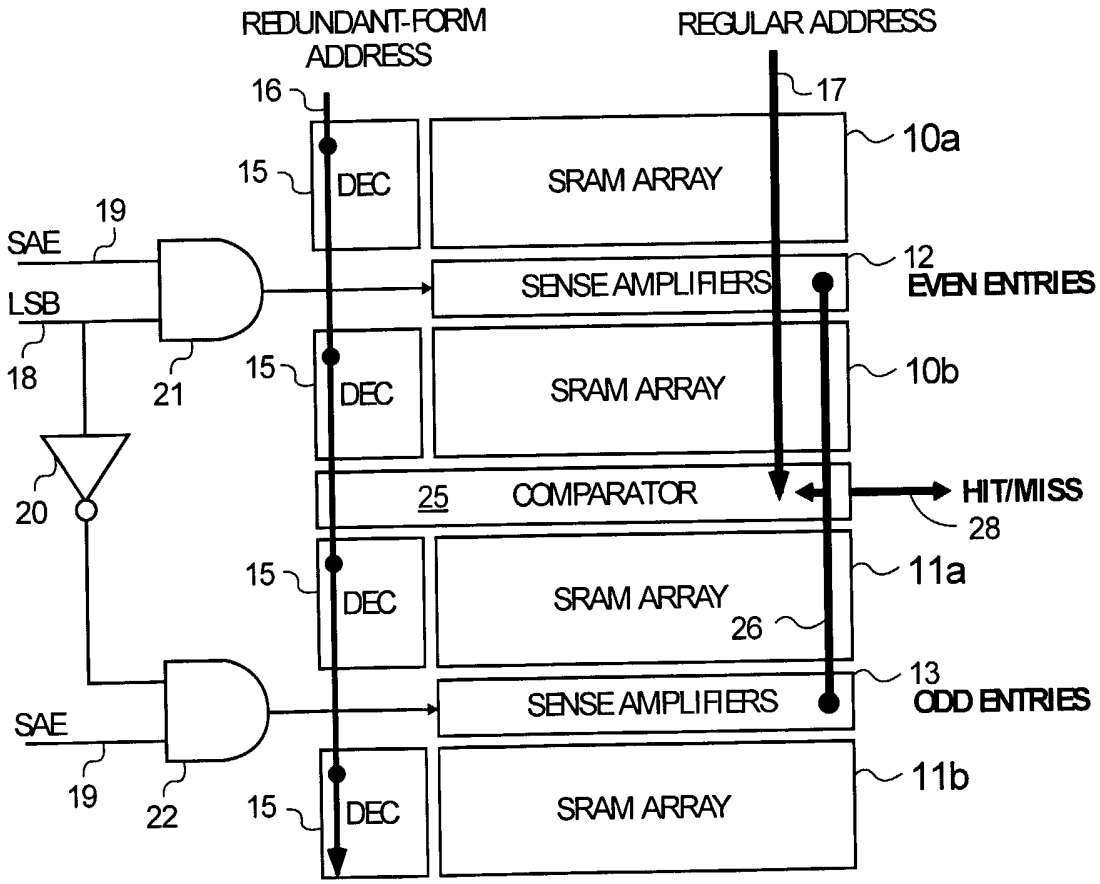

REDUNDANT-FORM ADDRESS
REGULAR ADDRESS
16
17
15
DEC
SRAM ARRAY
10a
19
SAE
LSB
18
21
SENSE AMPLIFIERS
12
EVEN ENTRIES
15
DEC
SRAM ARRAY
10b
20
25
COMPARATOR
HIT/MISS
28
15
DEC
SRAM ARRAY
26
11a
13
SENSE AMPLIFIERS
ODD ENTRIES
SAE
19
22
15
DEC
SRAM ARRAY
11b

FIG. 1

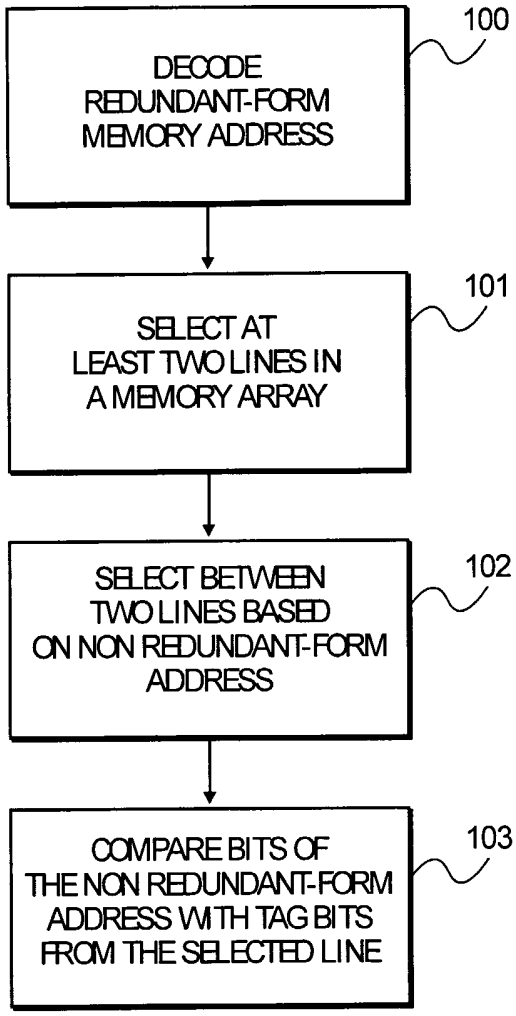

DECODE REDUNDANT-FORM MEMORY ADDRESS
100
SELECT AT LEAST TWO LINES IN A MEMORY ARRAY
101
SELECT BETWEEN TWO LINES BASED ON NON REDUNDANT-FORM ADDRESS
102
COMPARE BITS OF THE NON REDUNDANT-FORM ADDRESS WITH TAG BITS FROM THE SELECTED LINE
103

FIG. 2

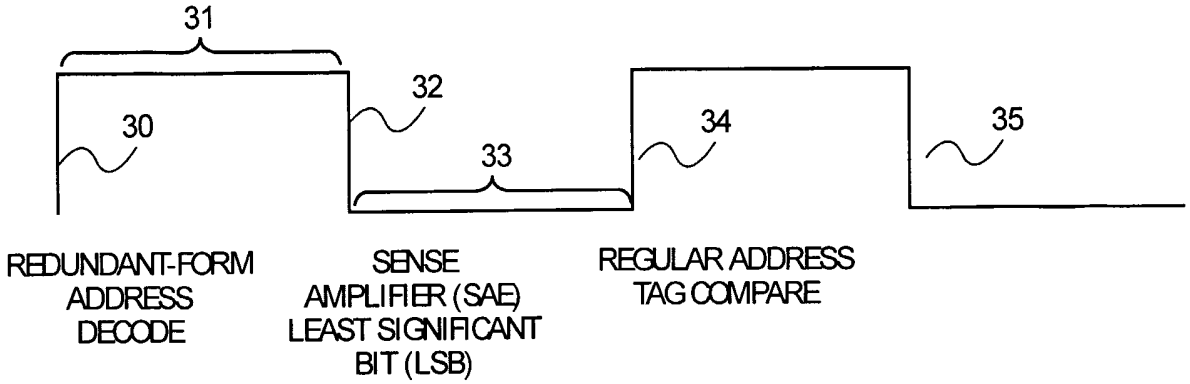

31
32
30
33
34
35
REDUNDANT-FORM ADDRESS DECODE
SENSE AMPLIFIER (SAE) LEAST SIGNIFICANT BIT (LSB)
REGULAR ADDRESS TAG COMPARE

FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 02/18181

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C15/04 G06F12/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 253 203 A (PARTOVI HAMID ET AL) 12 October 1993 (1993-10-12) column 5, line 10 -column 6, line 61; figures 1,3	1-21
A	US 5 353 424 A (PARTOVI HAMID ET AL) 4 October 1994 (1994-10-04) column 7, line 38 -column 8, line 28; figures 3A,3B,4	1-21
A	US 5 890 201 A (MCLELLAN EDWARD J ET AL) 30 March 1999 (1999-03-30) figure 4	1-21
A	US 5 542 062 A (NGO HUY X ET AL) 30 July 1996 (1996-07-30) figure 1	1-21

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
8 October 2002	15/10/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Lindquist, J

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Ir[illegible]ational Application No
PCT/US 02/18181

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5253203 A	12-10-1993	GB 2246001 A ,B	15-01-1992
		JP 2037692 C	28-03-1996
		JP 4227553 A	17-08-1992
		JP 7066350 B	19-07-1995
US 5353424 A	04-10-1994	JP 5225053 A	03-09-1993
US 5890201 A	30-03-1999	US 5568415 A	22-10-1996
		EP 0613089 A1	31-08-1994
		US 5784709 A	21-07-1998
US 5542062 A	30-07-1996	US 5307477 A	26-04-1994
		US 5699551 A	16-12-1997