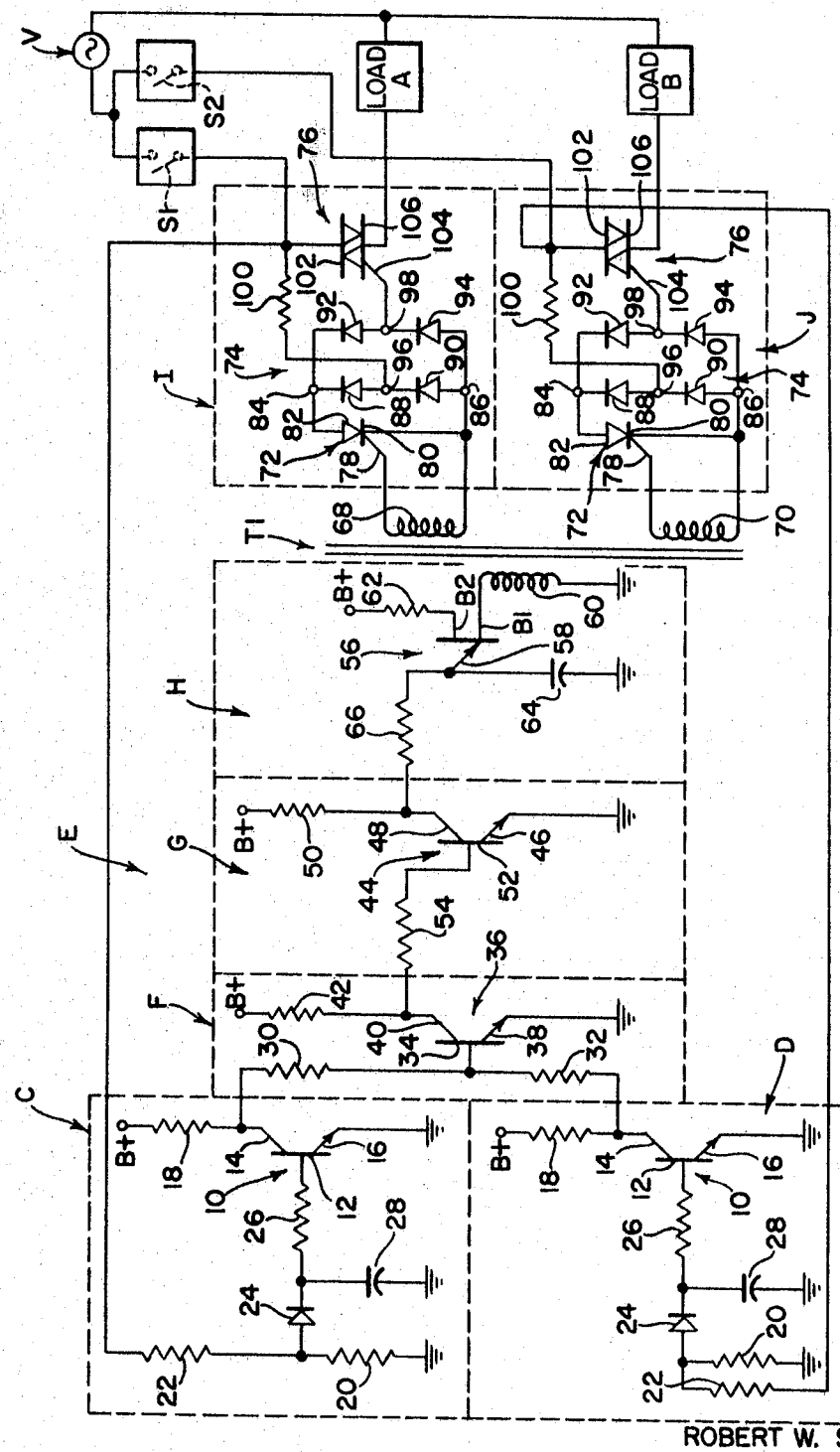
July 22, 1969 R. W. SAMUELSON 3,457,430

ANTICOINCIDENCE LOAD CONTROL CIRCUIT

Filed Dec. 7, 1966



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United States Patent Office 3,457,430 Patented July 22, 1969

3,457,430

ANTICOINCIDENCE LOAD CONTROL CIRCUIT

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Filed Dec. 7, 1966, Ser. No. 599,932
Int. Cl. H02j 3/14, 1/04
U.S. Cl. 307—41 9 Claims

ABSTRACT OF THE DISCLOSURE

An anticoincidence circuit is disclosed herein for use in preventing energization of first and second loads by a common voltage source upon concurrent actuation of first and second actuatable switching means respectively associated with the loads. The anticoincidence circuit includes a pair of normally deenergized static element load switching means, such as triacs, each having load terminals for respectively connecting a first and a second load and an associated actuatable switching means with a common voltage source. A pair of static element load control circuits are provided, each having a normal first condition and a second condition in response to whether an actuation of an associated actuatable switching means has occurred. A common static element control circuit responds to the condition of the static element load control circuit for purposes of controlling energization of the load switching means in such a manner that neither of the loads is energized when both of the actuatable switching means are concurrently actuated.

This invention relates to the art of load control circuits and, more particularly, to an anticoincidence load control circuit for connecting one of a plurality of loads to a common voltage source.

The invention is particularly applicable for connecting one of two alternating current voltage loads across an alternating current voltage source so that only one load is energized by the source at any one time, and the invention will be described with particular reference thereto; although, it will be appreciated that the invention has broader applications.

It is frequently desirable that load control circuits have the capability of connecting only one of a plurality of loads with a voltage source at any one time, and to prevent the occurrence of more than one load being concurrently energized. Thus, for example, intersection traffic signal controllers serve to control switching means for connecting both main street and cross street traffic signal go light across a common alternating current voltage source. It is important for traffic safety that both the main street and the cross street go lights are not concurrently energized. Accordingly, anticoincidence failsafe circuitry is desirable to prevent energization of either of the go lights upon a coincidence in the actuation of both switching means which might cause connection of both go lights to the common voltage source for energization thereby. Such a coincidence might result, for example, from a malfunction in the operation of the traffic signal controller.

Anticoincidence circuitry known heretofore for preventing the occurrence of a plurality of loads from being concurrently energized by a common voltage source have taken the form of banks of electromechanical relays. Thus, such circuits include a large number of moving parts, i.e., relay contacts, which exhibit relatively short operating lifetimes, necessitating frequent maintenance. Since a traffic signal controller normally operates on a twenty-four hour a day basis throughout each year, it is desirable that the controller, as well as an anticoincidence circuit associated therewith, operate with minimum maintenance requirements.

The present invention is directed toward an anticoincidence circuit employing static logic control elements so that the circuit is relatively maintenance free, thereby overcoming the noted disadvantages, as well as others, of anticoincidence circuits known heretofore.

The anticoincidence circuit contemplates the provision of a load control circuit having at least first and second selectively actuatable switching means for respectively connecting first and second loads with a common voltage source.

In accordance with the present invention the anticoincidence circuit comprises first and second static element load switching means respectively associated with the first and second loads for, upon energization, completing an energizing circuit between the associated load and its selectively actuatable switching means and the source; first and second static element load control means associated with the first and second loads, with each control means having a normal first condition and a second condition in response to actuation of the associated actuatable switching means; and, common static element control means responsive to the condition of the first and second control means for controlling energization of the first and second load switching means in such a manner that one of the load switching means is energized when its associated load control means is in its second condition to thereby energize its associated load, and that neither of the load switching means is energized when both their associated load control means are concurrently in their second conditions.

The primary object of the present invention is to provide a static element anticoincidence circuit for preventing concurrent energization of a plurality of loads by a common voltage source.

In accordance with a further object of the present invention, the anti-coincidence circuit employs solid state, static elements in the form of semiconductors which consume low power and, hence, are economical in operation.

These and other objects and advantages of the invention will become apparent from the following description of the preferred embodiment of the invention as read in connection with the accompanying drawings in which:

The single figure is a schematic circuit diagram illustrating the preferred embodiment of the invention.

Referring now to the single figure, there is illustrated a preferred embodiment of the anticoincidence circuit for preventing load A and load B from being concurrently energized by alternating current voltage source V upon actuation of both switches S1 and S2. The anticoincidence circuit generally comprises: a load A static element control circuit and a load B static element control circuit D; a common static element control circuit E comprising a NOR circuit F, a gating circuit G and an oscillator circuit H; a coupling transformer T1; and, a pair of static element load switching circuits including circuit I associated with load A and circuit J associated with load B.

To facilitate the understanding of the static element circuits of the anticoincidence circuit, each of these circuits is briefly explained below.

Load control circuit.—This is a solid state, static element circuit having an input circuit and an output circuit. A ground potential signal, known as a 0 signal, is present at its output circuit so long as an alternating current voltage signal is present at its input circuit. Otherwise, a positive potential signal, known as a 1 signal, is present at its output circuit.

NOR circuit.—This is a single stage, solid state, static element gate having two or more input circuits and one output circuit. A 1 signal is present at its output circuit so long as all of its input circuits receive a 0 signal. If any

of its input circuits receive a 1 signal, a 0 signal is present at its output circuit.

Gating circuit.—This is a single stage, solid state, static element gate having an input circuit and an output circuit. A 0 signal is present at its output circuit so long as a 1 signal is present at its input circuit, and a 1 signal is present at its output circuit so long as a 0 signal is present at its input circuit.

Oscillator circuit.—This is a solid state, static element oscillator circuit having an input circuit and an output circuit. An output frequency signal of a given frequency is present at its output circuit so long as a 1 signal is present at its input circuit.

Load switching circuit.—This is a solid state, static element load switching circuit having an input circuit and an output circuit. The output circuit serves to switch a load across a voltage source, such as an alternating current voltage source, so long as a frequency signal from the oscillator circuit is present at its input circuit.

Load control circuits

The internal circuitry of load control circuits C and D is substantially identical, and, accordingly, only circuit C will be described hereinafter in detail, like components in both circuits being identified in the single drawing with like reference numerals. Control circuit C includes a normally nonconductive NPN transistor **10** having a base **12**, a collector **14** and an emitter **16**. Emitter **16** is directly connected to ground and collector **14** is connected to a B+ voltage supply source through a resistor **18**. The output circuit of load control circuit C is taken between ground and collector **14**.

The onput circuit of load control circuit C is taken across a resistor **20** having one end connected to ground and the other end connected to the voltage source V through a resistor **22** and actuatable switch **S1**. The junction between resistors **20** and **22** is connected to base **12** of transistor **10**, through a diode rectifier **24**, poled as shown in the single drawing, and a resistor **26**. The junction between diode **24** and resistor **26** is connected to ground through a smoothing capacitor **28**. Thus, it will be appreciated that upon closure of switch **S1**, alternating current voltage from source V is applied to the input circuit of circuit C across resistor **20**, where the voltage is rectified and smoothed by rectifier **24** and capacitor **28** so as to provide a positive forward biasing potential to the base **12** of transistor **10**. Circuit D differs from circuit C only insofar that it is associated with load B as opposed to load A, and has its coupling resistor **22** connected to source V through actuatable switch **S2** as opposed to switch **S1**.

NOR circuit

NOR circuit F is a resistor-transistor NOR circuit having two input resistors **30** and **32** respectively connected to the output circuits of circuits C and D. The junction of resistors **30** and **32** is connected to the base **34** of normally conductive NPN transistor **36**. Transistor **36** has its emitter **38** connected directly to ground and its collector **40** connected to a B+ voltage supply source through a resistor **42**. The output circuit of NOR circuit F is taken between the collector **40** of transistor **36** and ground.

Gating circuit

The gating circuit G includes a normally nonconductive NPN transistor **44** having its emitter **46** connected directly to ground and its collector **48** connected to a B+ voltage supply source through a resistor **50**. The input circuit of gating circuit G is taken between ground and base **52** across the output circuit of circuit F. A resistor **54** connects the collector **40** of transistor **36** to the base **52** of transistor **44**. The output circuit of gating circuit G is taken between collector **48** and ground.

Oscillator circuit

The oscillator circuit H is a normally conductive unijunction transistor RC oscillator circuit and includes a unijunction transistor **56** having an emitter **58**, a first base **B1** and a second base **B2**. Base **B1** is connected to ground through a primary winding **60** on transformer T and base **B2** is connected to a B+ voltage supply source through a resistor **62**. Emitter **58** is connected to ground through a timing capacitor **64** and to collector **48** of transistor **44** through a timing resistor **66**.

Static load switching circuits

Static load switching circuits I and J have their input circuits coupled with the output circuit of oscillator circuit H through secondary windings **68** and **70**, respecively, on coupling transformer T. The internal circuitry of circuits I and J is substantially identical, and, accordingly, only circuit I will be described hereinafter in detail, like components in both circuits being identified in the single drawing with like reference numerals. Circuit I generally comprises a silicon controlled rectifier **72**, a full wave bridge rectifier circuit **74** and a bidirectional semiconductive device **76**. The semiconductive device **76** serves as a static switch for switching alternating current loads and may, for example, take the form of General Electric Company's SC40B device. Basically, this device is substantially the equivalent of two silicon controlled rectifiers, each having an anode, a cathode and a gate, and which are connected together in parallel but poled oppositely from each other, i.e., with the anode of one rectifier being connected with the cathode of the other rectifier, and with the two gates being connected in common.

Silicon controlled rectifier **72** includes a gate **78** and a cathode **80** connected across secondary winding **68** on transformer T. The anode **82** of rectifier **72** together with cathode **80** are respectively connected across terminals **84** and **86** of bridge circuit **74**.

The bridge circuit **74** includes four rectifier diodes **88**, **90**, **92** and **94**, poled as shown in the single drawing. Terminals **84** and **86** are respectively connected to the junction of the cathodes of rectifiers **88** and **92** and to the junction of the anodes of rectifiers **90** and **94**. Terminals **84** and **86** may be termed as the input circuit of bridge circuit **74**. The output circuit of bridge circuit **74** is taken across terminals **96** and **98**. Terminals **96** and **98** are respectively connected to the junction of the anode and cathode of rectifiers **88** and **90** and to the junction of the anode and cathode of rectifiers **92** and **94**.

Terminal **96** is connected through a resistor **100** to the junction of one side **102** of the bidirectional, semiconductive device **76** and actuatable switch **S1**. Terminal **98** is connected to the gate **104** on the other side **106** of the semiconductive device **76**.

Load A is connected across voltage source V upon actuation of switch **S1** through the bidirectional static switching device **76** of circuit I. Similarly, load B is connected across voltage source V upon actuation of actuatable switch **S2** through the static alternating current voltage switch **76** of circuit J. For purposes of simplification, selectively actuatable switches **S1** and **S2** are illustrated as normally open, manually actuatable switches. However, it is to be appreciated that switches **S1** and **S2** may take the form of relay contacts of load relays, or they may be transistors. These switches are normally actuated by a master control circuit, such as a traffic controller, for purposes of energizing loads A and B by alternating curcent voltage source V. It is to be appreciated that loads A and B may, for example, take the form of light filaments of go lights of traffic signals.

Operation

Prior to the actuation of switch **S1** or switch **S2**, transistors **10** in circuit C and circuit D are reversed biased. Accordingly, forward biasing potential from the B+ volt-

age supply source in circuit C or circuit D is applied to base 34 of transistor 36 in NOR circuit F. Thus, transistor 36 is normally conductive, whereby a 0 signal is present at its output circuit, i.e., at collector 40. This 0 signal is applied to base 52 of transistor 44 in gating circuit G through resistor 54. Accordingly, transistor 44 is reversed biased and a 1 signal is present at its output circuit, i.e., at collector 48.

The 1 signal on the output circuit of gating circuit G is applied to the input circuit of oscillator circuit H. Thus, capacitor 64 charges toward the value of the B+ voltage supply source through resistors 50 and 66, and when the voltage stored by the capacitor and, hence, the voltage appearing on emitter 58 of unijunction transistor 56, attains a level equal to the peak point voltage of the transistor, the transistor becomes forward biased. Capacitor 64 discharges through the emitter 58 to base B1 of transistor 56, developing a positive potential signal across load winding 60. Transistor 56 then ceases to conduct and capacitor 64 again commences to charge toward the B+ voltage supply source. This operation continues so long as a 1 signal is present at the input circuit of oscillator circuit H, providing an output frequency signal across the oscillator's output circuit, i.e., across primary winding 60. The components of the oscillator H are preferably chosen to provide a pulse frequency on the order of 1,000 cycles per second. This may be referred to as a frequency signal which has a duration corresponding with the 1 signal applied to the input circuit of the oscillator. The transformer T offers a measure of isolation between the oscillator circuit H and the load switching circuits I and J.

When unijunction transistor 56 is conductive the voltage appearing across its output circuit, as taken across primary winding 60, is coupled to secondary windings 68 and 70. Thus, a positive voltage is applied to gate 78 of silicon controlled rectifier 72 in circiuts I and J. However, neither rectifier conducts since positive voltage is not present on its anode in the absence of actuation of switch S1 or switch S2.

Upon actuation of switch S1, alternating current voltage from source V is applied to the input circuit of control circuit C. The alternating current voltage is rectified by diode rectifier 24 and smoothed by capacitor 28 and applied as a positive forward biasing potential to base 12 of transistor 10. Accordingly, transistor 10 is forward biased and conductive so that a ground potential, i.e., a 0 signal exists on its output circuit, taken at collector 14. But, transistor 36 in gating circuit F continues to conduct since transistor 10 in circuit D is still reversed biased. Accordingly, oscillator circuit H continues to develop a frequency signal at its output circuit. This signal provides forward biasing potential for gate 78 of rectifier 72 in circuits I and J, as described hereinbefore. However, anode 82 of rectifier 72 in circuit J does not receive positive voltage from source V since switch S2 is open and, accordingly, circuit J remains nonconductive. Since, however, switch S1 is closed, current flows from source V to circuit I. During the positive half cycle of the alternating current voltage, current flows through switch S1, resistor 100 and through the anode to cathode circuit of rectifier 88 to provide positive voltage on the anode 82 of rectifier 72. Since the frequency of source V is 60 cycles per second and the frequency of oscillator H is on the order of 1,000 cycles per second, rectifier 72 is gated into conduction substantially upon closure of switch S1. Thus, during the positive half cycle of voltage source V, current flows through resistor 100, through the anode to cathode circuit of diode rectifier 88, through the now conductive silicon controlled rectifier 72 from its anode 82 to cathode 80, and through the anode to cathode circuit of diode rectifier 94. This places a positive potential gating signal at terminal 98 which, hence, appears on gate 104 of the bidirectional semiconductive device 76. Thus, device 76 is gated into conduction and current flows during the positive half cycle from source V through device 76, from side 102 to side 106, i.e., through the equivalent of one silicon controlled rectifier from that rectifier's anode to cathode circuit, and thence from side 106 through load A and back to source V.

During the negative half cycle of source V, cathode 80 of rectifier 72 is rendered negative with respect to anode 82 through a circuit including the anode to cathode circuit of rectifier diode 90, terminal 96 and, thence, through resistor 100 and now closed switch S1 to source V. Thus, rectifier 72 is gated into conduction substantially upon commencement of the negative half cycle of source V. Current flows through diode rectifier 92 through the anode to cathode circuit of rectifier 72, the anode to cathode resistor 100, closed switch S1, to source V. This current path provides sufficient gating potential at gate 104 to gate device 76 into conduction, whereupon current flows from source V through load A and, thence, from side 106 to side 102 of device 76, i. e., through the anode to cathode circuit of the equivalent second silicon controlled rectifier within device 76, and, thence, through switch S1 to source V. Accordingly, it is seen that upon actuation of switch S1, semiconductive switching device 76 is gated into conduction so as to switch alternating current voltage source V across load A. Similarly, with switch S1 in its nonactuated position, as shown in the single drawing, actuation of switch S2 will result in a forward biasing gating potential applied to gate 104 of semi-conductive switching device 72 in circuit J to switch source V across load B.

Attention is now directed toward the operation which results upon concurrent actuation of switches S1 and S2. As described hereinbefore, such concurrent actuation of switches S1 and S2 may result from, for example, a malfunction in the operation of a master control circuit, not shown, that controls the operation of switches S1 and S2.

Upon concurrent actuation of switches S1 and S2 alternating current voltage is applied from source V to the input circuits of circuits C and D. Accordingly, transistors 10 in circuits C and D become forward biased, whereupon a ground potential signal, i.e., a 0 signal is present on the output circuits of both circuits C and D. These 0 signals are applied to the input circuit of NOR circuit F whereupon transistor 36 becomes reversed biased and a 1 signal is present on its output circuit. This 1 signal is applied to the input circuit of gating circuit G resulting in a 0 signal being present at its output circuit. This 0 signal is applied to oscillator circuit H whereupon oscillator circuit H ceases to operate, terminating the frequency signal. Accordingly, neither circuit I nor circuit J is conductive, whereby both static switching devices 76 are reversed biased. Thus, neither load A nor load B can be concurrently energized by source V even though both switches S1 and S2 are actuated.

In accordance with a preferred embodiment of the invention, the values and types of various components illustrated in the single drawing are found in Table I.

TABLE I

Component:	Component value or type
Transistor 10	NPN transistor.
Resistor 18	3.9 kilohms.
Resistor 20	3.9 kilohms.
Resistor 22	33 kilohms.
Capacitor 28	1.0 microfarad.
Transistor 36	NPN transistor.
Resistor 30	33 kilohms.
Resistor 32	33 kilohms.
Resistor 42	3.9 kilohms.
Transistor 44	NPN transistor.
Resistor 50	1 kilohm.
Resistor 54	33 kilohms.
Transistor 56	Unijunction transistor.
Resistor 62	100 ohms.
Resistor 66	100 ohms.

TABLE I—Continued

Component:	Component value or type
Timing capacitor **64**	0.25 microfarad.
Rectifier **72**	Silicon controlled rectifier.
Resistor **100**	100 ohms.
Bidirectional semiconductor device **72**	General Electric Company's SC40B.
B+ voltage supply source	+20 volts direct current.
Source V	120 volts, 60 cycles per second.

Although the invention has been shown in connection with a preferred embodiment, it will be readily apparent to those skilled in the art that various changes in form and arrangement of parts may be made to suit requirements without departing from the spirit and scope of the invention as defined by the appended claims.

Having thus described my invention, I claim:

1. An anticoincidence circuit for preventing energization of first and second loads by a common voltage source upon concurrent actuation of first and second actuatable switching means respectively associated with said loads, said anticoincidence circuit comprising:

first and second normally deenergized static element load switching means each having load terminals for respectively connecting a first and a second load and an associated actuatable switching means with a common voltage source;

first and second static element load control means respectively associated with first and second loads, each said control means having a normal first condition and a second condition in response to actuation of an associated actuatable switching means; and,

common static element control means responsive to the condition of said first and second control means for controlling energization of said first and second load switching means in such a manner that one of said load switching means is energized when its associated load control means is in its second condition to thereby energize its associated load and that neither of said load switching means is energized when both said load control means are concurrently in their second conditions.

2. An anticoincidence circuit as set forth in claim **1**, wherein each said load switching means is a bidirectional semiconductive device having first and second electrodes and a control electrode, said first and second electrodes of each device connecting one of said loads across a common alternating current voltage source through a said actuatable switching means, each said device exhibiting a characteristic in that is passes alternating current from said source to said load when a forward biasing signal is applied to its said control electrode.

3. An anticoincidence circuit as set forth in claim **2**, wherein said common control means includes normally energized oscillator means for developing a frequency signal and means for deenergizing said oscillator means when both said static element control means are concurrently in said second condition.

4. An anti-coincidence circuit as set forth in claim **3**, including first and second load switching circuits, each including:

a said bidirectional device; and

means for forward biasing said bidirectional device in response to actuation of said first actuatable switching means and said frequency signal.

5. An anticoincidence circuit as set forth in claim **4**, wherein each said means for forward biasing a said bidirectional device includes a silicon controlled rectifier having its gate to cathode circuit coupled to the output of said oscillator means and its anode to cathode circuit connected between the control electrode of said associated bidirectional device and said associated actuatable switching means.

6. An anticoincidence circuit as set forth in claim **5**, including a first and second diode for respectively connecting said anode to said actuatable switching means and said cathode to said control electrode of said bidirectional device during a first half cycle of said alternating current voltage source for forward biasing said device to pass current from said source in a first direction through said associated load.

7. An anticoincidence circuit as set forth in claim **6**, including third and fourth diodes for respectively connecting said cathode to said actuatable switching means and said anode to said control electrode of said bidirectional device during a second half cycle of said alternating current voltage source for forward biasing said device to pass current from said source in a second direction through said associated load.

8. An anticoincidence circuit as set forth in claim **4**, wherein said oscillator means includes an RC relaxation oscillator circuit having its output circuit connected across a primary winding of a coupling transformer, said transformer having first and second secondary windings for respectively coupling said frequency signal to said first and second load switching circuits for forward biasing a said bidirectional device.

9. An anticoincidence circuit as set forth in claim **3**, wherein said means for deenergizing said oscillator means includes first and second static element ON-OFF switching means each having a normal first and a second stable state condition, said first ON-OFF switching means being in its second condition only in response to both said first and second load control means being in their respective second conditions, said second ON-OFF switching means being in its second condition only in response to said first ON-OFF switching means being in its second condition, and said second ON-OFF switching means being coupled to said oscillator means for deenergizing said oscillator means only when said second ON-OFF switching means is in its second condition.

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U.S. Cl. X.R.

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