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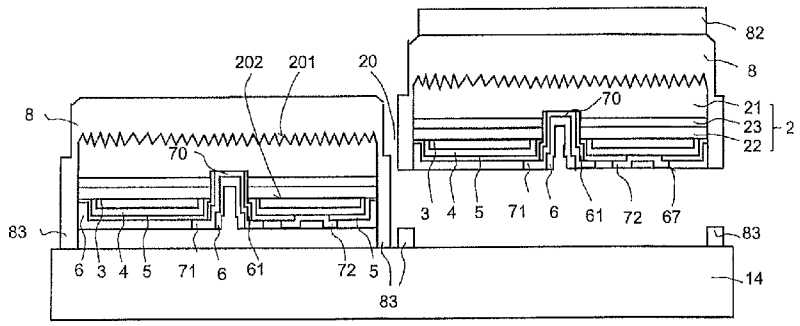
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(54) **Title**: METHOD FOR PRODUCING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT

FIG 13



(57) **Abstract**: A method for producing a plurality of semiconductor components is provided, wherein a semiconductor layer sequence having a first semiconductor layer, a second semiconductor layer and an active region is applied on a substrate. A contact structure is formed for electrically contacting the first and the second semiconductor layers. An auxiliary substrate is applied on the semiconductor layer sequence, so that the semiconductor layer sequence is arranged between the auxiliary substrate and the substrate. In a subsequent step, the substrate is removed from the semiconductor layer sequence. The semiconductor layer sequence is structured into a plurality of semiconductor bodies by forming at least one trench separating the semiconductor bodies. An anchoring layer is formed to cover the trench and vertical surfaces of the semiconductor bodies. A plurality of tethers is formed by structuring the anchoring layer in regions covering the trench. The auxiliary substrate is locally detached from the semiconductor bodies, wherein the tethers remain attached to the auxiliary substrate. At least one semiconductor body is selectively picked up by separating the tethers from the auxiliary substrate. Moreover, a semiconductor component produced by said method is provided.

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Description

Method for producing a semiconductor component and semiconductor component

The invention relates to a method for producing a semiconductor component and to a semiconductor component.

Area lighting using LEDs necessitates a large number of small LEDs to be die bonded on a carrier. This is time-consuming and expensive when using standard methods for producing the LEDs and using standard die bonding techniques.

It is an object of the invention to specify a particularly flexible method for producing a semiconductor component or a plurality of semiconductor components, and furthermore to specify a semiconductor component which can be produced in a simplified and cost-effective manner.

This object is achieved by means of the subject-matter of the independent patent claims. The dependent patent claims relate to further configurations and developments.

In one embodiment of a method for producing a semiconductor component or a plurality of semiconductor components, a substrate is provided. The substrate can be patterned or flat. For example the substrate is radiation-transmissive, in particular transparent. The substrate is, for example, a growth substrate, which may in this case consist inter alia of sapphire or silicon or contain sapphire or silicon.

According to at least one embodiment of the method for producing the semiconductor component, a semiconductor layer sequence having a first semiconductor layer, a second

semiconductor layer and an active region is applied, for instance is grown epitaxially, onto the substrate.

The semiconductor layer sequence comprises a first main surface facing the substrate and a second main surface facing away from the substrate. The first main surface, for example, faces a surface of the substrate. The first and second main surfaces in particular delimit the semiconductor layer sequence in a vertical direction. A vertical direction is understood to mean a direction which is directed transversely, for instance perpendicularly, to a main extension plane of the active region. A lateral direction extends in parallel to the main extension plane of the active region. In particular, the lateral direction and the vertical direction are perpendicular to each other.

For example, the first semiconductor layer is formed as an n-conductive layer and the second semiconductor layer is formed as a p-conductive layer, or vice versa. The active region is disposed for instance between the first semiconductor layer and the second semiconductor layer. In particular, the active region is a pn-junction zone which is provided for generating or detecting electromagnetic radiation during the operation of the semiconductor component.

The semiconductor layer sequence is based, for example, on a III-V compound semiconductor material, which comprises at least one element from main group III, such as for example Al, Ga, In, and one element from main group five, such as for example N, P, As. In particular, the term "III-V compound semiconductor material" encompasses the group of binary, ternary and quaternary compounds, which contain at least one element from main group III and at least one element from

main group five, for example nitride and phosphide compound semiconductors. N-conductive and p-conductive layers may respectively be produced by appropriate doping of the semiconductor material. The semiconductor layer sequence may also be based on a II-VI compound semiconductor material.

According to at least one embodiment of the method, a contact structure comprising at least a first contact area, a second contact area and a via is formed on the side of the second main surface. The via is electrically connected for instance to the first contact area. For electrically contacting the first semiconductor layer, the via may extend from the second main surface throughout the second semiconductor layer and the active region into the first semiconductor layer. It is also possible that the via also extends throughout the first semiconductor layer. The second contact area is electrically connected for instance to the second semiconductor layer.

In particular, the via covers vertical surfaces of a recess which is formed in the semiconductor layer sequence. In lateral directions, the recess is surrounded by the semiconductor layer sequence for instance completely. The recess may extend throughout the second semiconductor layer and the active region as far as into the first semiconductor layer and/or also throughout the first semiconductor layer. The recess may be formed by an etching method, for example by a dry etching method. It is possible that a plurality of recesses and a plurality of vias are formed.

According to at least one embodiment of the method, the semiconductor layer sequence is patterned on a side remote from the substrate, such that a patterned second main surface of the semiconductor layer sequence remote from the substrate

is formed. The second main surface may comprise a plurality of microprisms. In particular, the second main surface is patterned prior to the step of forming the contact structure, for example prior to the forming of the first contact area and the second contact area of the contact structure.

According to at least one embodiment of the method, a mirror layer is applied on the patterned second main surface. The mirror layer in particular reproduces the patterned second main surface at least in places. The first main surface of the semiconductor layer sequence may be formed as a radiation exit area. Radiation emitted in the direction of the second main surface can be reflected towards the first main surface by the mirror layer.

According to at least one embodiment of the method, an auxiliary substrate is applied on the semiconductor layer sequence, so that the semiconductor layer sequence is arranged between the auxiliary substrate and the substrate. The first contact area and the second contact area of the contact structure are arranged in particular completely between the auxiliary substrate and the semiconductor layer sequence. The auxiliary substrate may comprise a polymer, which is particularly suitable for a temporary bonding process due to its temperature-dependent properties.

The auxiliary substrate may be mechanically fixed, in particular temporarily bonded, to the semiconductor layer sequence by a connecting layer. For example, the connecting layer comprises a bonding material which may be applied on the semiconductor layer sequence by a spin coating method. For instance the connecting layer contains a spin-on bonding material which temporarily bonds the auxiliary substrate to

the semiconductor layer sequence, wherein the connecting layer is able to timely release the auxiliary substrate from the semiconductor layer sequence. The connecting layer comprises for instance a thermally decomposable spin-on bonding material having temperature-dependent adhesion. It is also possible to use other suitable materials for the connecting layer. For example, the connecting layer may be formed from a photoresist material. Using a photoresist material, the connecting layer may be dissolved in a simplified manner, for example by means of a photolithography process.

According to at least one embodiment of the method, the substrate is removed from the semiconductor layer sequence. In particular, the auxiliary substrate is applied prior to the process of removing the substrate. The recess and the via or the plurality of recesses and vias may be formed prior to or after removing the substrate.

According to at least one embodiment of the method, the semiconductor layer sequence is structured into a plurality of semiconductor bodies. The semiconductor layer sequence may be divided into a plurality of semiconductor bodies for example by forming at least one or a plurality of trenches separating the semiconductor bodies in the lateral direction. Structuring the semiconductor layer sequence may proceed for example by means of an etching and/or a laser separation method for forming the mesa trench or the plurality of trenches. The trench may extend from the first main surface throughout the semiconductor layer sequence as far as or into the connecting layer or also throughout the connecting layer as far as or into the auxiliary substrate. By way of example, the trench or trenches is/are formed such that the auxiliary

substrate is partially exposed. After structuring the semiconductor layer sequence, the semiconductor bodies arranged on the auxiliary substrate are in particular electrically insulated from one another. It is also possible that the step of structuring the semiconductor layer sequence into a plurality of semiconductor bodies is performed prior to the process of fixing the auxiliary substrate to the semiconductor layer sequence.

According to at least one embodiment of the method, the semiconductor layer sequence is applied onto an unpatterned, for example a flat or a plane, surface of the substrate, so that the first main surface of the semiconductor layer sequence may be unpatterned at first. After removing the substrate, the first main surfaces of the semiconductor bodies may be patterned for example by means of an etching method. It is possible that structuring the semiconductor layer sequence into a plurality of semiconductor bodies and patterning the first main surfaces of the semiconductor bodies are realized in a mutual process step or in two directly consecutive steps. On the other hand, the substrate may be provided with a patterned surface and the semiconductor layer sequence may be applied onto the patterned surface of the substrate. The first main surface of the semiconductor layer sequence is in particular patterned prior to removing the substrate. For example, the first main surface reproduces the patterned surface of the substrate.

According to at least one embodiment of the method, an anchoring layer is applied onto the structured semiconductor layer sequence, wherein the anchoring layer covers the trench or the plurality of trenches and vertical surfaces of the semiconductor bodies. In particular, the anchoring layer is

in direct physical contact with the auxiliary substrate. The anchoring layer can be a dielectric layer which contains for instance silicon, such as silicon oxide or silicon nitride. The anchoring layer can be applied to the semiconductor bodies for example by sputtering or coating, such as chemical or physical vapor deposition. It is also possible that the anchoring layer is formed by a photoresist layer. Using a photoresist material, the anchoring layer can be structured in a simplified manner, for example by means of a photolithography process.

According to at least one embodiment of the method, a plurality of tethers are formed by structuring the anchoring layer in the region covering the trench. In particular, the tethers are formed within the trench or trenches. In this case the tethers are arranged laterally from the active regions of the semiconductor bodies in plan view. The tether or the plurality of tethers may be formed by etching the anchoring layer. A photolithography process may be used for forming the plurality of tethers containing the photoresist material.

According to at least one embodiment of the method, the anchoring layer is structured so that the tethers associated with different semiconductor bodies are disconnected. It is also possible that at least an anchor bar is formed between the semiconductor bodies by structuring the anchoring layer in the region covering the trench or the plurality of trenches, wherein the semiconductor bodies are connected to the anchor bar by the tethers. The anchor bar, for example, extends along at least one trench separating the semiconductor bodies. The anchor bar additionally helps holding the semiconductor bodies in place during the step of

detaching the auxiliary substrate from the semiconductor bodies.

According to at least one embodiment of the method, the auxiliary substrate is locally detached from the semiconductor bodies. Locally detaching the auxiliary substrate from the semiconductor bodies means in particular that the auxiliary substrate is separated from the semiconductor bodies at least in those regions of the auxiliary substrate covered by the active regions or by the semiconductor bodies. The semiconductor bodies, however, may still be connected to the auxiliary substrate indirectly for example by means of the tethers arranged at least partially sideways from the semiconductor bodies. Locally detaching the auxiliary substrate may be achieved by dissolving the mechanical connection between the auxiliary substrate and the semiconductor bodies at the connecting layer, for example by removing the connecting layer or by timely changing the adhesive effect of the connecting layer.

The local detachment of the auxiliary substrate may proceed after the forming of the tethers. During and after the step of locally detaching the auxiliary substrate from the semiconductor bodies, the tethers remain in particular attached directly or indirectly to the auxiliary substrate. In this case, the semiconductor bodies may be held in place at least during the step of locally detaching the auxiliary substrate. After the step of locally detaching the auxiliary substrate from the semiconductor bodies, the auxiliary substrate is separated from the semiconductor bodies at least in those regions of the auxiliary substrate covered by the active regions or by the semiconductor bodies. The auxiliary substrate, however, is preferably mechanically connected to

the semiconductor bodies indirectly by the tethers, in particular in those regions of the auxiliary substrate covered by the tethers.

According to at least one embodiment of the method, at least one semiconductor body having one first semiconductor layer, one second semiconductor layer and one active region together with the associated contact structure is selectively picked out by separating the tethers from the auxiliary substrate. Separating the tethers from the auxiliary substrate may be performed by mechanically breaking the tethers or by releasing or dissolving the tethers from the auxiliary substrate. The at least one semiconductor body may be then separated completely from the auxiliary substrate and transferred to a carrier, such as an interposer or a final board. The semiconductor body, which is mechanically connected to the auxiliary substrate in particular only by means of the tethers, may be selectively removed by a stamp attached to the semiconductor body on the side of its first main surface. By lifting away the semiconductor body from the auxiliary substrate, the tethers attaching the semiconductor body to the auxiliary substrate can be mechanically broken or released, so that the semiconductor body is separated completely from the auxiliary substrate. It is also possible that a plurality of the semiconductor bodies are selectively removed simultaneously or one after another from the auxiliary substrate.

In accordance with at least one embodiment of a method for producing a plurality of semiconductor components each having a semiconductor body, a semiconductor layer sequence is applied on a substrate, wherein the semiconductor layer sequence comprises a first semiconductor layer, a second

semiconductor layer and an active region being disposed between the first and the second semiconductor layers. A contact structure is formed for electrically contacting the first semiconductor layer and the second semiconductor layer. For electrically contacting the first semiconductor layer, by way of example, the contact structure comprises at least one via or a plurality of vias extending throughout the second semiconductor layer and the active region. The semiconductor layer sequence is structured into a plurality of semiconductor bodies by forming at least one trench or a plurality of trenches separating the semiconductor bodies. An auxiliary substrate is applied on the semiconductor layer sequence, so that the semiconductor layer sequence is arranged between the auxiliary substrate and the substrate. In a subsequent step, the substrate is removed from the semiconductor layer sequence. An anchoring layer is applied on the auxiliary substrate to cover the trench or trenches and vertical surfaces of the semiconductor bodies. In a next step, a plurality of tethers are formed by structuring the anchoring layer in regions covering the trench or trenches. After forming the tethers, the auxiliary substrate is locally detached from the semiconductor bodies, while the tethers remain attached to the auxiliary substrate. Each individual semiconductor body or a plurality of the semiconductor bodies may then be selectively picked up from the auxiliary substrate by separating the tethers from the auxiliary substrate, wherein the semiconductor body comprises one first semiconductor layer, one second semiconductor layer and one active region together with one associated contact structure.

Using the tethers' binding to the auxiliary substrate, wherein the tethers connected to the semiconductor bodies are formed after forming a plurality of trenches separating or

isolating the semiconductor bodies from each other, each individual semiconductor body may be held in place by the tethers during the step of locally detaching the auxiliary substrate from the semiconductor bodies. In a subsequent step, the semiconductor bodies may be selectively picked up, for example by a stamp, by breaking or releasing the tethers from the auxiliary substrate. The semiconductor bodies can be transferred one after the other or in a large number simultaneously to a carrier, such as an interposer or a final board.

According to at least one embodiment of the method, the semiconductor component is formed by means of a direct-bonding method, wherein a main body comprising the semiconductor body and the contact structure of the semiconductor component is direct-bonded to the carrier of the semiconductor component. Direct-bonding means that the process of connecting of the main body to the carrier is in particular free of using any adhesive material.

The main body comprises for example an insulating layer which is formed on a side of the semiconductor body facing the first contact area and the second contact area. The main body may have a planar connection surface which delimits the main body in a vertical direction. This planar connection surface may be formed by surfaces, in particular exposed lateral surfaces of the first contact area, the second contact area and the insulating layer.

The carrier may comprise a first contact pad, an insulating pad and a second contact pad laterally separated from the first contact pad by the insulating pad. Preferably the carrier has a planar bonding surface which for example is

formed by surfaces, in particular exposed lateral surfaces, of the first contact pad, the second contact pad and the insulating pad. The planar bonding surface and the planar connecting surface may be brought together directly to form a common interface between the main body and the carrier. The common interface is at least locally planar. The common interface may comprise a hole, where the planar bonding surface and the planar connecting surface are not in direct contact in places. Preferably, the common interface is globally planar. The common interface is in particular free of steps and edges.

By way of example, the common interface is formed partially by a metal-metal-interface, an insulating-insulating-interface and partially by a metal-insulating-interface. The semiconductor component may then be free of an adhesive material at the common interface between the carrier and the main body, wherein the carrier and the main body are fixed to each other in particular at the common interface. In this case, the first contact area and the second contact area may be in direct electrical contact to the first contact pad and the second contact pad, respectively. Using the direct-bonding method, electrical interconnection of the main body and the carrier can be realized without any extra step, such as wire bonding or plating electrical tracks on the main body.

In a direct-bonding method, two bodies, each having a planar surface, are brought together at a suitable pressure and a suitable temperature and are mechanically connected with each other due to van der Waals interactions or hydrogen bonds between the atoms on the planar surfaces. A planar surface is understood to mean a surface which is in particular formed

microscopically flat. For example, such a planar surface has a roughness which is for example smaller than 50 nm, for example smaller than 10 nm, in particular smaller than 1 nm. Preferably, such a planar surface is free of edges. In particular, this bonding technique does not call for the use of any bonding material, such as an adhesive or a soldering material. Apart from that, it is also possible that the carrier and the main body be connected to each other by means of an alternative method using a bonding material.

According to at least one embodiment of the method, prior to the step of direct-bonding the planar bonding surface to the planar surface, the bonding surface and the connection surface are surface-finished and planarized for instance by a plasma cleaning method.

In accordance with at least one embodiment of a semiconductor component, the component has a main body and a carrier. The main body comprises a semiconductor body having a first main surface remote from the carrier and a second main surface facing the carrier. The semiconductor body comprises a first semiconductor layer, a second semiconductor layer and an active region being arranged between the first semiconductor layer and the second semiconductor layer. The main body comprises a contact structure having a via extending from second main surface throughout the second semiconductor layer and the active region for electrically contacting the first semiconductor layer. The contact structure further comprises a first contact area being electrically connected to the via and a second contact area on a side of the second main surface, wherein the first contact area and the second contact area are laterally separated by an insulating layer. The main body comprises a planar connection surface which is

formed by surfaces of the first contact area, the second contact area and the insulating layer. The carrier comprises a planar bonding surface which is in direct contact with the planar connection surface of the main body, so that a common interface between the main body and the carrier is formed, wherein the common interface is free of an adhesive material. The common interface is in particular an overlapping region of the planar connection surface and planar bonding surface.

Preferably, the main body is mechanically fixed to the carrier at the common interface. The common interface is in particular free of macroscopic elevations and depressions or steps and edges. It is possible that a plurality of the main bodies are arranged on a single common carrier. The main bodies may be arranged in the form of a matrix having columns and rows.

Such a semiconductor component may be produced by the methods for producing a semiconductor component described herein. Therefore, features described in connection with the methods for producing a semiconductor component or a plurality of semiconductor components can also be used for the semiconductor component, and vice versa.

According to at least one embodiment of the semiconductor component, the second main surface is patterned and comprises a plurality of microprisms. The semiconductor component comprises for instance a mirror layer which is arranged between second main surface and the carrier and preferably reproduces the patterned second main surface at least in places. The active region is configured for example to generate electromagnetic radiation during operation of the semiconductor component. The electromagnetic radiation may be

coupled out from the semiconductor component at the first main surface. The efficiency of light out-coupling can be increased by means of the patterned mirror layer, since the patterned mirror layer reflects electromagnetic radiation towards the first main surface in various directions resulting in a reduction of negative effects due to total internal reflection at the first main surface.

According to at least one embodiment of the component, the carrier has a rear side remote from the bonding surface, wherein, in vertical direction, the first contact pad and the second contact pad extend from the bonding surface in particular throughout the carrier as far as the rear side. The component may be electrically contacted to an external power source by means of the first and the second contact pads on the rear side.

According to at least one embodiment of the component, phosphor particles and/or scattering particles are embedded in a layer covering the first main surface. Phosphor particles may absorb electromagnetic radiation emitted by the active region and re-emit an electromagnetic radiation having a longer peak wavelength in comparison with the electromagnetic radiation absorbed by the phosphor particles, so that the component may emit white light in total.

The method described herein and the semiconductor component described herein are explained in greater detail below with reference to exemplary embodiments and the associated figures, in which:

Figures 1 through 14 show schematic sectional views of various method stages for producing a plurality of semiconductor components,

Figures 15 and 16 show exemplified embodiments of a semiconductor component,

Figures 17A through 17H show schematic sectional views of various method stages of further embodiments of a method for producing a plurality of semiconductor components, and

Figure 17I shows a further exemplified embodiment of a semiconductor component.

Identical or similar elements, or elements acting in an identical manner, are provided with the same reference numerals in the figures. In each case, the figures are schematic views and are therefore not necessarily true to scale. Rather, comparatively small elements, and in particular layer thicknesses, may be illustrated excessively large for clarification purposes.

In Figure 1, a substrate 9 is provided. The substrate 9 has a surface 91 which is flat. It is also possible that the substrate 9 comprises a patterned surface 91. The substrate 9 is, for example, radiation-transmissive, in particular transparent for electromagnetic radiation in visible, infrared and/or ultraviolet spectral ranges. Alternatively, the substrate 9 can be radiation-opaque. The substrate 9 may comprise gallium nitride or silicon carbide or sapphire. In particular, the substrate 9 is a silicon substrate.

A semiconductor layer sequence 200 is applied onto the surface 91 of the substrate 9. The semiconductor layer

sequence 200 comprises a first semiconductor layer 21, a second semiconductor layer 22 and an active region 23 which is disposed between the first semiconductor layer 21 and the second semiconductor layer 22. The first semiconductor layer 21 may be an n-conductive layer and the second semiconductor layer 22 may be a p-conductive layer, or vice versa. The active region 23, for example, is configured for generating electromagnetic radiation or for absorbing and transforming electromagnetic radiation into electrical signals or energy.

The semiconductor layer sequence 200 may be grown epitaxially on the substrate 9. The semiconductor layer sequence 200 has a first main surface 201 facing the substrate 9 and a second main surface 202 which is remote from the substrate 9. For improving the quality of the epitaxial semiconductor layers of the semiconductor layer sequence 200, the substrate 9 may have a patterned surface 91. Moreover, the semiconductor layer sequence 200 can be grown onto the patterned surface 91 of the substrate 9, so that the first main surface 201 may reproduce the patterned surface 91.

A mirror layer 3 is deposited onto the second main surface 202 remote from the substrate 9. The mirror layer 3 comprises a plurality of subregions being laterally separated from one another. In particular, the mirror layer 3 comprises a plurality of openings 30. Each of the subregions of the mirror layer 3 may be continuous and comprises, for instance, at least one of the openings 30 of the mirror layer 3.

The mirror layer 3 is in particular electrically conductive. In top view, the mirror layer 3 is covered by a connection layer 4 which is, for example, also electrically conductive. The mirror layer 3 and/or the connection layer 4 may contain

a metal such as aluminium, rhodium, palladium, silver, gold or platinum or alloys of these elements.

In Figure 2, a dielectric layer 5, for example a silicon nitride layer or a silicon oxide layer, is applied on the semiconductor layer sequence 200, wherein the dielectric layer 5 covers the connection layer 4 and in particular the semiconductor layer sequence 200 completely.

In Figure 3, a plurality of recesses 24 are formed in regions of the openings 30 of the mirror layer 3. In vertical direction, each recess 24 extends throughout the dielectric layer 5, the second semiconductor layer 22, the active region 23 into the first semiconductor layer 21. The recess 24 forms a blind hole in the semiconductor layer sequence 200, wherein in lateral direction the recess 24 is surrounded by the semiconductor layer sequence 200 for instance completely. The recesses 24 may be formed by an etching method, for example by a dry etching method.

After forming the recesses 24, a passivation layer 61, for example a silicon oxide layer such as SiO2 or a silicon nitride layer, is formed to cover vertical surfaces of the recesses 24. It is possible that the passivation layer 61 covers the recesses 24 and the dielectric layer 5 completely. In a subsequent step, the passivation layer 61 may be partially removed. The passivation layer 61 and the dielectric layer 5 preferably comprise different dielectric materials. By way of example, the dielectric layer 5 contains or mainly consists of silicon nitride and the passivation layer 61 contains or mainly consists of silicon oxide.

In Figure 4 the passivation layer 61 is partially removed, for example by etching, such that the first semiconductor layer 21 is exposed in the regions of the recesses 24. By partially removing the passivation layer 61, the dielectric layer 5 is also at least partially exposed. In a next step, the dielectric layer 5 is removed, for example by etching, in places such that the dielectric layer 5 comprises in addition to first openings 51 in the regions of the recesses 24, a plurality of second openings 52 arranged laterally to the recesses 24. In the second openings 52, an electrically conductive layer such as the connection layer 4 is partially exposed.

In Figure 5, a contact structure 7 comprising a first contact area 71, a second contact area 72 and a via 70 is formed on the side of the second main surface 202 of the semiconductor layer sequence 200. The first contact area 71 and the second contact area 72 are laterally separated and in this way electrically isolated from each other. In vertical direction, the second contact area 72 extends through the second opening 52 of the dielectric layer 5 and is electrically connected to the second semiconductor layer 22 by means of the mirror layer 3 and the connection layer 4. The first contact area 71 is deposited outside the recess 24 and is electrically connected to the via 70, wherein the via 70 is arranged inside the recess 24. In vertical direction, the via 70 extends at least from the second main surface 202 throughout the second semiconductor layer 22 and the active region 23 into the first semiconductor layer 21. Within the recess 24, in lateral direction, the via 70 is electrically isolated from the second semiconductor layer 22 and the active region 23 by means of the passivation layer 61 covering vertical surfaces of the recess 24.

In Figure 6, an insulating layer 6 is formed on the side of the second main surface 202 of the semiconductor layer sequence 200. By way of example, the insulating layer 6 covers the contact structure 7 completely at first. In a subsequent step, the insulating layer 6 can be planarized, so that a substantially flat, in particular a substantially planar connection surface 67 is formed. The connection surface 67 in Figure 6 is formed for instance by surfaces of the first contact area 71, the second contact area 72 and of the insulating layer 6 remote from the semiconductor layer sequence 200. In other words, after being planarized, in vertical direction, the surface of insulating layer 6 is in particular flush with the surfaces of the first contact area 71 and of the second contact area 72. At the connection surface 67, the first contact area 71 and the second contact area 72 are partially exposed. Preferably outside the recesses 24 and the regions between the subregions of the mirror layer 3, the connection surface 67 is formed as a planar connection surface. It is also possible that the insulating layer 6 fills the recesses 24 completely.

In Figure 7, an auxiliary substrate 14 is temporarily fixed to the semiconductor layer sequence 200 by means of a connecting layer 13, so that the semiconductor layer sequence 200 is arranged between the auxiliary substrate 14 and the substrate 9. The auxiliary substrate 14 may comprise a polymer or is made of a polymer. The connecting layer 13 may comprise a bonding material which can be applied onto the connection surface 67 by a spin coating method. For instance the connecting layer 13 contains a spin-on bonding material which temporarily bonds the auxiliary substrate 14 to the semiconductor layer sequence 200 and timely releases the

auxiliary substrate 14 from the semiconductor layer sequence 200. The connecting layer 13 comprises for instance a thermally decomposable spin-on bonding material having temperature-dependent adhesion. By way of example, a waferBOND® process (Brewer Science®) can be used which temporarily bonds the auxiliary substrate 14 to the semiconductor layer sequence 200 and later automatically debonds the auxiliary substrate 14 after a controllable length of time.

It is also possible to use other suitable materials for the connecting layer 13. For example, the connecting layer 13 may be formed from a photoresist material. Using a photoresist material, in particular a positive photoresist material, the connecting layer 13 may be dissolved in a simplified manner, for example by means of a photolithography process. In this case, the auxiliary substrate 14 may be formed from a radiation-transmissive material, so that the connecting layer 13 comprising the photoresist material can be exposed to radiation passing through the auxiliary substrate 14. Preferably, a protection layer 15 is formed on the side of the auxiliary substrate 14 remote from the connecting layer 13. The protection layer 15 is for example radiation-opaque and may be removed prior to the exposure of the photoresist material in the connecting layer 13. For example, the protection layer 15 is a Kapton® layer.

In Figure 8, the substrate 9 is separated from the semiconductor layer sequence 200. This can be performed for example by means of a mechanical, chemical or physical process. For example etching, in particular dry etching, grinding or a laser separation process such as a laser lift-

off process may be used. A combination of grinding and etching may also be used for removing the substrate.

In Figure 9A, the semiconductor layer sequence 200 is structured laterally into a plurality of semiconductor bodies 2. Lateral structuring means that the semiconductor layer sequence 200 is divided into a plurality of semiconductor bodies 2 being spaced laterally apart from one another. A mesa trench 20 or a plurality of trenches 20 are formed between the semiconductor bodies 2. In vertical direction, the trench 20 extends throughout the semiconductor layer sequence 200 as far as to the connecting layer 13. The trenches 20 may be formed by an etching method, for instance by a dry, wet or laser etching method, in particular in regions between the sub-regions of the mirror layer 3. The trench 20 may also be formed sideways from the semiconductor layer sequence 200. It is also possible that the step of structuring the semiconductor layer sequence 200 into a plurality of the semiconductor bodies 2 is performed prior to the process of fixing the auxiliary substrate 14 and removing the substrate 9.

In Figure 9A the first main surfaces 201 of the semiconductor bodies 2 are patterned, resulting in an optimal light extraction surface 201. It is possible that forming the trenches 20 and patterning the first main surfaces 201 are realized in a mutual process step or in two directly consecutive steps. In particular, the step of forming the trenches 20 follows the step of patterning the first main surface 201 of the semiconductor layer sequence 200.

The production step illustrated in Figure 9B corresponds substantially to the production step illustrated in Figure

9A. In contrast thereto, the substrate 9 is provided with a patterned surface 91 onto which the semiconductor layer sequence 200 has been applied. In this case, the semiconductor layer sequence 200 comprises the first main surface 201 which is patterned und in particular reproduces the patterned surface 91 of the substrate 9. After removing the substrate 9 and structuring the semiconductor layer sequence 200, each semiconductor body 2 comprises a patterned first main surface 201.

In Figure 10, the connecting layer 13 is partially removed, so that the auxiliary substrate 14 is exposed in regions of the trenches 20. The connecting layer 13 in regions of the trenches 20 may be removed for example by using a solvent, by means of an etching method or by a photolithography process. Hereby, the protection layer 15 may be removed partially or completely.

In Figure 11, an anchoring layer 8 is applied onto the semiconductor bodies 2 and onto the auxiliary substrate 14 for instance by a coating method, wherein the anchoring layer 8 covers vertical surfaces of the semiconductor bodies 2 and the trench or trenches 20 arranged sideways of the semiconductor bodies 2. The anchoring layer 8 fixes the semiconductor bodies 2 to the auxiliary substrate. Preferably, the anchoring layer 8 is in direct physical contact with the auxiliary substrate 14. As shown in Figure 11, the anchoring layer 8 may cover the vertical surfaces and/or the first main surface 201 of the semiconductor body 2 completely. It is possible that the auxiliary substrate 14 is formed to have a patterned surface facing the semiconductor bodies 2 (not shown). In this case, the anchoring layer 8 may penetrate onto the patterned auxiliary substrate 14 such that

the anchoring layer 8 is anchored to the auxiliary substrate 14 in an optimal manner, since an interface between the auxiliary substrate and the anchoring layer is enlarged due to the patterned surface, so that an adhesion area on the patterned surface is increased.

The anchoring layer 8 may be formed from dielectric material such as silicon oxide or silicon nitride or from a photoresist material. For example the anchoring layer 8 comprises substantially a photoresist material or consists of a photoresist material. It is also possible that the anchoring layer 8 is formed substantially from a low temperature (< 220 °C) dielectric or by a low temperature dielectric and a photoresist material.

After applying the anchoring layer 8, a plurality of tethers 83 are formed by structuring the anchoring layer 8 at least in regions covering the trench or trenches 20. The tethers 83 are in particular parts of the anchoring layer 8 which are arranged laterally to their associated semiconductor body 2. In top view onto the auxiliary substrate 14, the semiconductor body 2 may not have any overlaps with the tethers 83. The tethers 83 are formed to mechanically fix the semiconductor body 2 to the auxiliary substrate 14. For structuring the anchoring layer 8, a photolithography process and/or an etching process may be used.

In Figure 11A, the anchoring layer 8 comprising the tethers 83 is shown in a top view on the auxiliary substrate 14. Vertical surfaces of each of the semiconductor bodies 2 are covered by the anchoring layer 8. The anchoring layer 8 is structured into a plurality of laterally separated anchoring layers 8 associated with different semiconductor bodies 2.

Each semiconductor body 2 comprises on its lateral sides at least one or a plurality of the tethers 83. The anchoring layer 8 is structured in regions covering the trenches 20 in such a way that tethers 83 associated with different semiconductor bodies 2 are disconnected. This simplifies the process of lifting up any individual semiconductor body 2 without having influence on its neighboring semiconductor bodies 2.

In Figure 11B, anchor bars 84 as further parts of the anchoring layer 8 are formed between the semiconductor bodies 2. By way of example, the anchor bar 84 extends along a row of the semiconductor bodies 2 along a lateral direction. The tethers 83 are connected to the anchor bar 84. In this case neighboring semiconductor bodies 2 may be mechanically connected to each other by the tethers 83 and the anchor bars 84, so that a plurality of semiconductor bodies 2 may be lifted simultaneously in a simplified and safe manner.

In Figure 12, the auxiliary substrate 14 is locally detached from the semiconductor bodies 2. The semiconductor bodies 2, however, are still connected to the auxiliary substrate indirectly by means of the tethers 84. Locally detaching the auxiliary substrate 14 may be achieved by dissolving the mechanical connection between the auxiliary substrate 14 and the semiconductor bodies 2 at the connecting layer 13, for example by using timed solvent removal of the connecting layer 13 or by timely changing the adhesive effect of the connecting layer 13. In the case that the connecting layer 13 is formed from a photoresist material, the connecting layer 13 may be dissolved out by being exposed to radiation which may be transmitted through the auxiliary substrate 14. It is possible that the step of forming the tethers 84 and the step

of locally detaching the auxiliary substrate 14 are realized in a mutual process step, for example by a photolithography process.

In Figure 13, a stamp 82 is attached to the semiconductor body 2 on the side of the first main surface 201. The semiconductor body 2 having one first semiconductor layer 21, one second semiconductor layer 22 and one active region 23 together with the associated contact structure 7 having the via 70 may be selectively picked up by the stamp and lifted from the auxiliary substrate 14 such that the tethers 83 are separated from the auxiliary substrate 14. For instance, the tethers 83 are mechanically broken or released from the auxiliary substrate 14. It is possible that the tethers 83, or at least some remnants of the tethers 83, are detached from the auxiliary substrate 14, so that the anchoring layer 8 still comprises the tethers 83 or at least some remnants of the tethers 83 after the semiconductor body 2 has been completely removed from the auxiliary substrate 14. It is also possible to selectively pick up a plurality of semiconductor bodies 2 simultaneously.

In Figure 14, a main body 210 having the semiconductor body 2, the mirror layer 3, the connection layer 4, the dielectric layer 5, the insulating layer 6, the passivation 61 and the contact structure 7 is transferred by the stamp 82 and mechanically connected to a carrier 1 having a first contact pad 171 and a second contact pad 172 laterally separated from the first contact pad by an insulating pad 16. The carrier 1 comprises for example a planar bonding surface 10 which is formed by surfaces of the first contact pad 171, the second contact pad 172 and the insulating pad 16. The main body 210, at least outside the recess 24, comprises a planar connection

surface 67 which is formed by surfaces of the first contact area 71, the second contact area 72 and of the insulating layer 6. It is also possible that the recess 24 is filled with the insulating layer 6 completely. The bonding surface 10 and the connection surface 67 may be surface-finished and planarized, for example by a plasma cleaning method.

In particular the main body 210 and the carrier 1 are connected to each other by a direct-bonding method. In this case, the bonding surface 10 is in direct contact with the connection surface 67, so that a common interface between the main body 210 and the carrier 1 is formed, wherein the common interface is a planar surface and free of an adhesive material. The common interface is formed in particular by directly overlapping regions of the connection surface 67 and the bonding surface 10. The first contact area 71 and the second contact area 72 are in particular in direct electrical contact to the first contact pad 171 and the second contact pad 172, respectively. For example, the common interface is formed partially by a metal-metal-interface, an insulating-insulating-interface and a metal-insulating-interface (Figure 15). In contrast thereto, it is also possible that the main body 210 is connected to the carrier 1 by a method using an adhesive material.

In Figure 15, a semiconductor component 100 produced by a method described herein is shown. At the common interface formed by the directly overlapping regions of the connection surface 67 and the bonding surface 10, the first contact area 71 together with the first contact pad 171 and the second contact area 72 together with the second contact pad 172 in each case form a step, i.e. a jump, in the vertical direction. This provides a hint that the contact areas and

the contact pads are not formed in a single common production step but in different production steps and are connected to each other by the direct-bonding method. In Figure 15, the anchoring layer 8 is completely removed from the semiconductor component 100. In particular, an encapsulation layer may be applied on the semiconductor body 2 which comprises for instance phosphor and/or scattering particles embedded in a matrix material of the encapsulation layer. In the case that the anchoring layer 8 is formed by a radiation-transmissive or radiation-transparent material, the anchoring layer 8 may not need to be removed and can serve as the encapsulation layer of the semiconductor layer component 100.

Figure 16 schematically illustrates a further exemplary embodiment of the semiconductor component 100. This embodiment corresponds substantially to the embodiment of the semiconductor component 100 in Figure 15. In contrast thereto, in vertical direction the first contact pad 171 and the second contact pad 172 extend from the bonding surface 10 throughout the carrier 1 to a rear side 102 of the substrate. The component 100 may be electrically contacted to an external power source, for example by means of the first and the second contact pads 171 und 172 on the rear side 102. The first main surface 201 is formed as a radiation passage area 101, in particular as a radiation exit area of the component. It is also possible, that the radiation exit area is protected by a further layer.

Figures 17A to 17H illustrate some further steps of a method for producing a plurality of semiconductor components 100.

The production step illustrated in Figure 17A corresponds essentially to the production step described in Figure 1. In

contrast thereto, the semiconductor layer sequence 200 is patterned on a side remote from the substrate 9, such that a patterned second main surface 202 of the semiconductor layer sequence 200 is formed which comprises a plurality of microprisms 222. Furthermore, the connection layer 4 has a plurality of laterally separated sub-sections which in each case extend throughout the dielectric layer and are in electrical contact to the second semiconductor layer 22. Moreover, an intermediate layer 92 is formed between the substrate 9 and the semiconductor layer 2. The intermediate layer 92 may increase the quality of the epitaxially grown semiconductor body 2. In particular, the intermediate layer 92 is an electrically conductive layer having a low band-gap compared to a band-gap of the semiconductor layers of the semiconductor body 2.

In Figure 17B, the mirror layer 3 is applied on the patterned second main surface 202, such that the mirror layer 3 reproduces the patterned second main surface 201 at least in places forming the plurality of microprisms 222. The mirror layer 3 is in electrical contact with the connection layer 4. The insulating layer 6 is also patterned.

In Figure 17C, the first contact area 71 and the second contact area 72 of the contact structure 7 are formed on a side of the semiconductor layer sequence 200 remote from the substrate 9, wherein the planar connection surface 67 is formed by surfaces of the first contact area 71, the second contact area 72 and the insulating layer 6. The entire planar connection surface 67 is free of elevations or depressions.

The production steps illustrated in Figures 17D and 17E correspond essentially to the production steps described in

Figures 8 through 10. In contrast thereto, the recesses 24 and the vias 70 are formed after the substrate 9 has been removed. In vertical direction, the recess 24 extends from the first main surface 201 throughout the entire semiconductor layer sequence 200 as far as to the first contact area 71. The via 70 extends in vertical direction from the first contact area 71 to the first main surface 201 and is in particular in direct electrical contact with the first semiconductor layer 21 at the first main surface 201.

The further production steps illustrated in Figures 17F and 17G correspond essentially to the production steps described in Figures 12 and 13, wherein the main body 210 has a via 70 extending throughout the semiconductor body 2. The main body 210 may be selectively lifted from the auxiliary substrate 14 such that the tethers 83 are mechanically broken, wherein the tethers 83, or at least some remnants of the tethers 83, are detached from the auxiliary substrate 14. The anchoring layer 8 of the selectively lifted main body 210 comprises the tethers 83, or at least some remnants of the tethers 83, after being completely removed from the auxiliary substrate 14.

The production step illustrated in Figure 17H corresponds essentially to the production step described in Figure 14. In contrast thereto, the planar connection surface 67 is free of the recess 24. In this case the entire planar connection surface 67 is in particular free of elevations or depressions.

Figure 17I shows a further exemplified embodiment of a semiconductor component 100 comprising the main body 210 illustrated in Figure 17G and the carrier 1 as illustrated in

Figure 16. This semiconductor component 100 comprises the anchoring layer 8 having at least one tether 83 or remnants of the tether 83 arranged on the bonding surface 10 of the carrier 1. The anchoring layer 8 covers at least one vertical surface of the semiconductor body 2, wherein the tether 83 or remnants of the tether 83 are arranged sideways from the semiconductor body 2. The anchoring layer 8 may be partially or completely removed. In particular, the anchoring layer 8 may be formed from a material, which radiation-transmissive or transparent to radiations emitted by the active region 23. In this case, a surface of the anchoring layer 8 remote from the carrier 1 may be formed as the radiation exit area 101 of the component. In Figure 17I, the recess 24 is not completely filled by the anchoring layer 8. It is also possible that the recess 24 is completely filled by a material of the anchoring layer 8 or by another materials.

Using tethers for binding semiconductor bodies to an auxiliary substrate, wherein the tethers are formed within mesa trenches separating the semiconductor bodies, the semiconductor bodies may be held in place during and after the process of detaching the auxiliary substrate. The semiconductor bodies may then be selectively picked up and direct-bonded to a carrier, wherein no extra steps for electrical interconnection of the semiconductor body to the carrier are needed. By using the tethers, the method for producing a plurality of semiconductor components is simplified, resulting in a reduction of production costs.

The description made with reference to exemplary embodiments does not restrict the invention to these embodiments. Rather, the invention encompasses any novel feature and any combination of features, including in particular any

combination of features in the claims, even if this feature or this combination is not itself explicitly indicated in the claims or exemplary embodiments.

The present application claims the priority of the US application 62/110,365, the disclosure content of which is hereby incorporated by reference.

Claims

1. A method for producing a plurality of semiconductor components (100) each having a semiconductor body (2), comprising the following method steps:

A) applying a semiconductor layer sequence (200) having a first semiconductor layer (21), a second semiconductor layer (22) and an active region (23) being disposed between the first semiconductor layer and the second semiconductor layer on a substrate (9);

B) forming a contact structure (7) for electrically contacting the first semiconductor layer (21) and the second semiconductor layer (22);

C) structuring the semiconductor layer sequence (200) by forming at least one trench (20) separating the semiconductor bodies (2);

D) applying an auxiliary substrate (14) on the semiconductor layer sequence (200), so that the semiconductor layer sequence (200) is arranged between the auxiliary substrate (14) and the substrate (9);

E) removing the substrate (9) from the semiconductor layer sequence (200);

F) applying an anchoring layer (8) covering the trench (20) and vertical surfaces of the semiconductor bodies (2) and forming a plurality of tethers (83) by structuring the anchoring layer (8) in regions covering the trench (20);

G) locally detaching the auxiliary substrate (14) from the semiconductor bodies (20), wherein the tethers (83) remain attached to the auxiliary substrate (14); and

H) selectively picking up at least one semiconductor body (2) having one first semiconductor layer (21), one second semiconductor layer (22) and one active region (23) together with one associated contact structure (7) by separating the tethers (83) from the auxiliary substrate (14).

2. The method according to claim 1, wherein step F is carried out prior to step G and the semiconductor bodies (2) are held in place by the tethers (83) during step G.

3. The method according to claim 1, wherein the anchoring layer (8) is formed from a dielectric material and the plurality of tethers (83) are formed by etching the anchoring layer.

4. The method according to claim 1, wherein the anchoring layer (8) is formed from a photoresist material and the plurality of tethers (83) are formed by means of a photolithography process.

5. The method according to claim 1, wherein both steps of locally detaching the auxiliary substrate (14) and of forming a plurality of tethers (83) are carried out by a photolithography process.

6. The method according to claim 1, wherein during step F the anchoring layer (8) is structured, such that tethers (83) associated to different semiconductor bodies (2) are disconnected.

7. The method according to claim 1, wherein during step F an anchor bar (84) is formed between the semiconductor bodies (2) by structuring the anchoring layer (8) in regions covering the trench (20) and the semiconductor bodies (2) are connected to the anchor bar (84) by the tethers (83).

8. The method according to claim 1, wherein the substrate (9) is provided with a patterned surface (91) and the semiconductor layer sequence (200) is grown onto the patterned surface (91) of the substrate (9), such that the semiconductor layer

sequence (200) comprises a patterned first main surface (201) facing and reproducing the patterned surface (91) of the substrate (9).

9. The method according to claim 1, wherein prior to step B the semiconductor layer sequence (200) is patterned on a side remote from the substrate (9), such that a patterned second main surface (202) of the semiconductor layer sequence (200) remote from the substrate is formed which comprises microprisms (222).

10. The method according to claim 9, wherein a mirror layer (3) is applied on the patterned second main surface (202), such that the mirror layer reproduces the patterned second main surface at least in places.

11. The method according to claim 1, wherein a first contact area (71) and a second contact area (72) of the contact structure (7) and an insulating layer (6) are formed on a side of the semiconductor layer sequence (200) remote from the substrate (9), wherein a planar connection surface (67) is formed by surfaces of the first contact area (71), the second contact area (72) and the insulating layer (6), said surfaces being remote from the semiconductor layer sequence (200).

12. The method according to claim 1, wherein during step H the at least one semiconductor body (2) is selectively removed from the auxiliary substrate (14) and is connected to a carrier (1) by a direct-bonding method, which is free of using any adhesive material.

13. The method according to claim 11, in which the carrier (1) comprises a planar bonding surface (10), wherein prior to the step of direct-bonding the planar bonding surface (10) to the planar connection surface (67), the bonding surface (10) and the connection surface (67) are surface-finished by a plasma cleaning method.

14. The method according to claim 1,
- wherein the contact structure (7) is formed on a main surface (202) of the semiconductor layer sequence (200) facing away from the substrate (9), and
- wherein the contact structure (7) comprises a first contact area (71), a via (70) and a second contact area (72), said second contact area (72) being electrically connected to the second semiconductor layer (22), said via (70) being electrically connected to the first contact area (71) and extending from the main surface (202) throughout the second semiconductor layer (22) and the active region (23) into or throughout the first semiconductor layer (21).

15. A semiconductor component having a main body (210) arranged on a carrier (1), wherein
- the main body (210) comprises a semiconductor body (2) having a first main surface (201) remote from the carrier (1) and a second main surface (202) facing the carrier (1), wherein the semiconductor body (2) comprises a first semiconductor layer (21), a second semiconductor layer (22) and an active region (23) being arranged between the first semiconductor layer and the second semiconductor layer,
- the main body (210) comprises a contact structure (7) having a via (70) extending from the second main surface (202) throughout the second semiconductor layer (22) and

the active region (23) for electrically contacting the first semiconductor layer (21),

- the contact structure (7) comprises a first contact area (71) being electrically connected to the via (70) and a second contact area (72) on a side of the second main surface, wherein the first contact area (71) and the second contact area (72) are laterally separated by an insulating layer (6),
- the main body (210) comprises a planar connection surface (67) which is formed by surfaces of the first contact area (71), the second contact area (72) and the insulating layer (6),
- the carrier (1) comprises a planar bonding surface (10) which is in direct contact with the planar connection surface (67) of the main body (210), so that an common interface between the main body (210) and the carrier (1) is formed, wherein the common interface is free of any adhesive material.

16. The semiconductor component according to claim 15, in which the carrier (1) comprises a first contact pad (171) and a second contact pad (172) laterally separated from the first contact pad by an insulating pad (16), wherein

- the planar bonding surface (10) is formed by surfaces of the first contact pad, the second contact pad and the insulating pad, and
- the common interface is formed partially by a metal-metal-interface, an insulating-insulating-interface and a metal-insulating-interface.

17. The semiconductor component according to claim 15, in which the second main surface (202) is patterned and comprises a plurality of microprisms (222), wherein a mirror layer (3) is arranged between the second main surface (202) and the carrier (1) and the mirror layer

(3) reproduces the patterned second main surface (202) at least in places.

18. A device comprising a plurality of the semiconductor components (100) according to claim 15, wherein the carriers (1) of all the semiconductor components (100) are formed as a single common carrier.

FIG 1

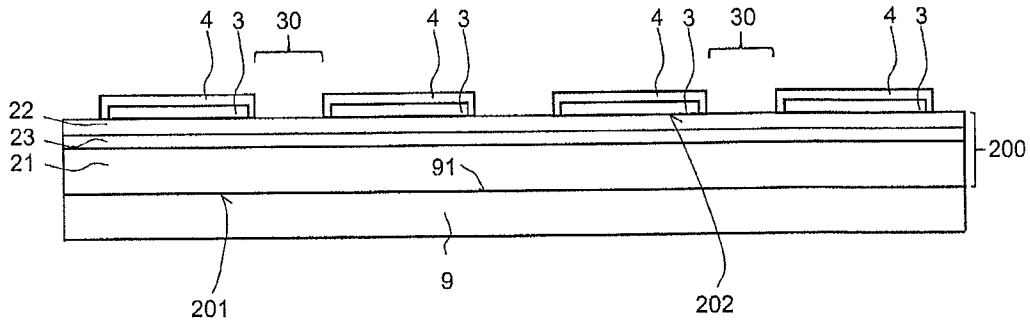


FIG 2

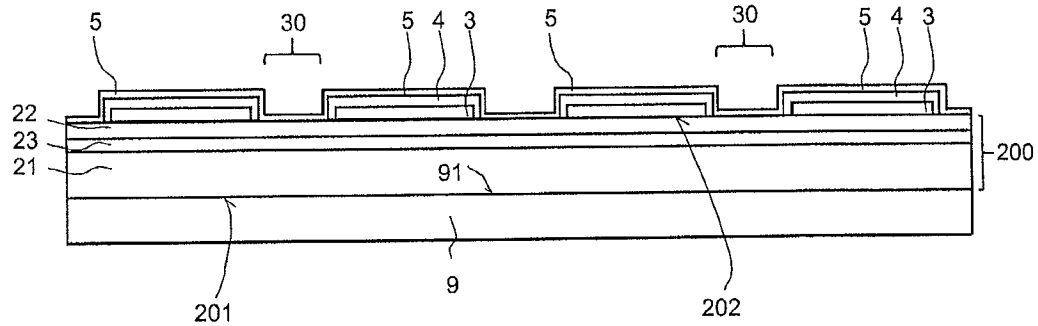


FIG 3

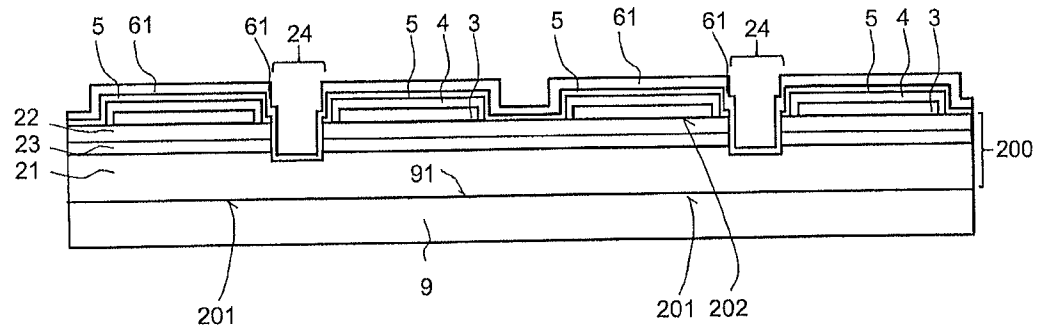


FIG 4

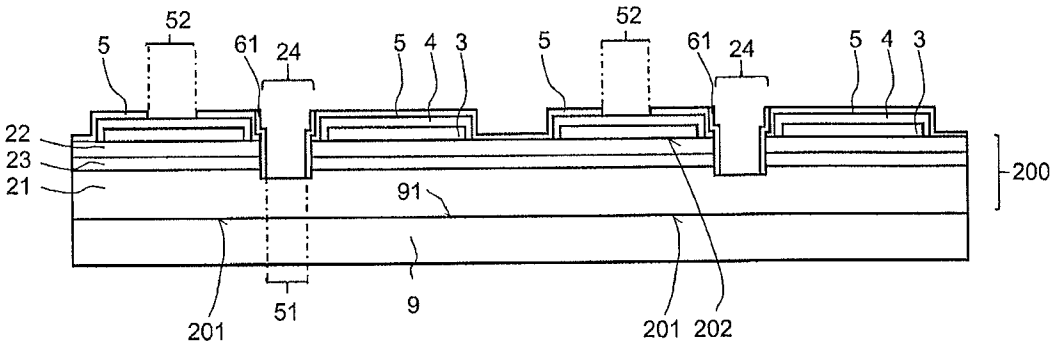

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FIG 5

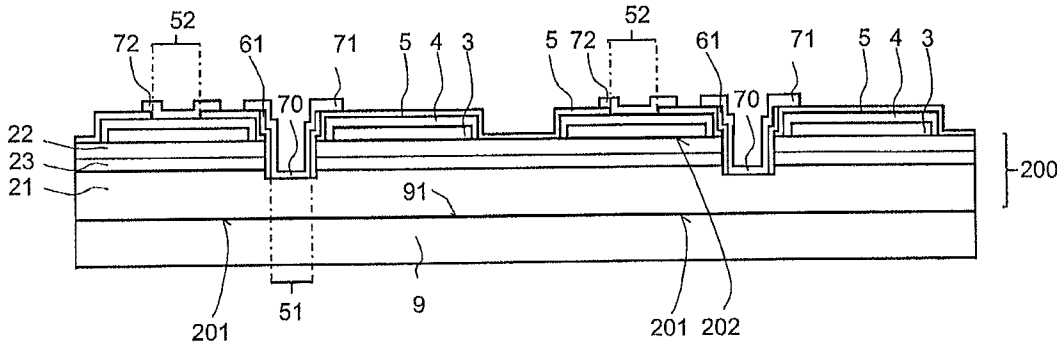

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FIG 6

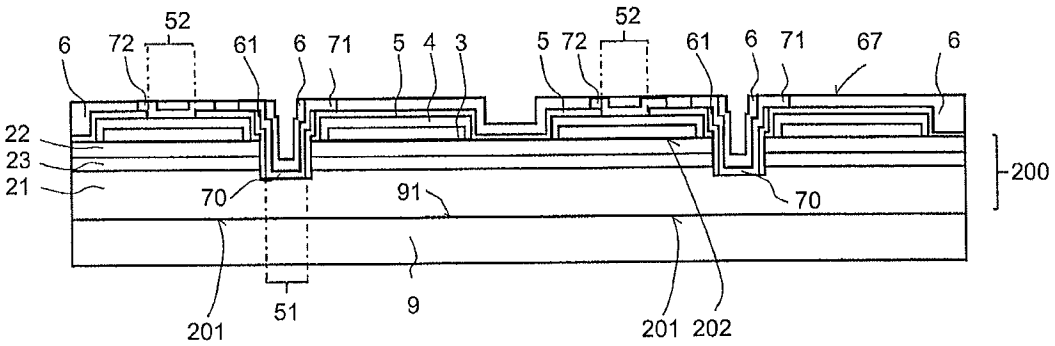

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FIG 7

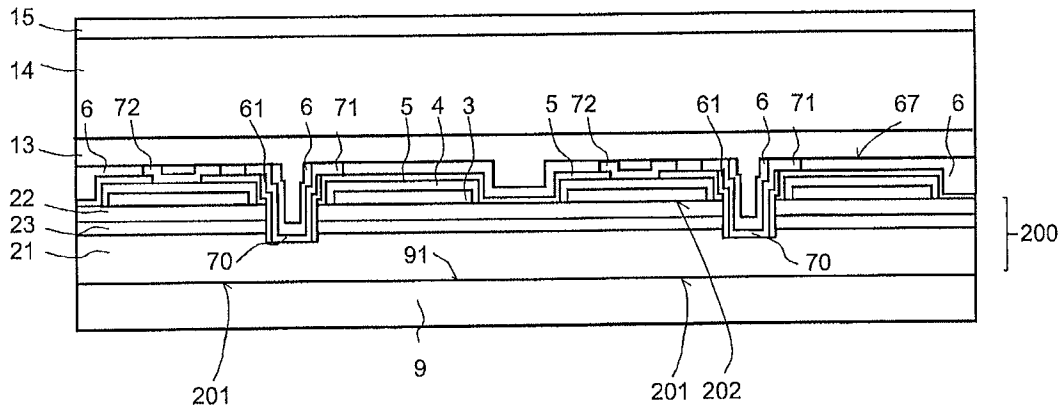

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FIG 8

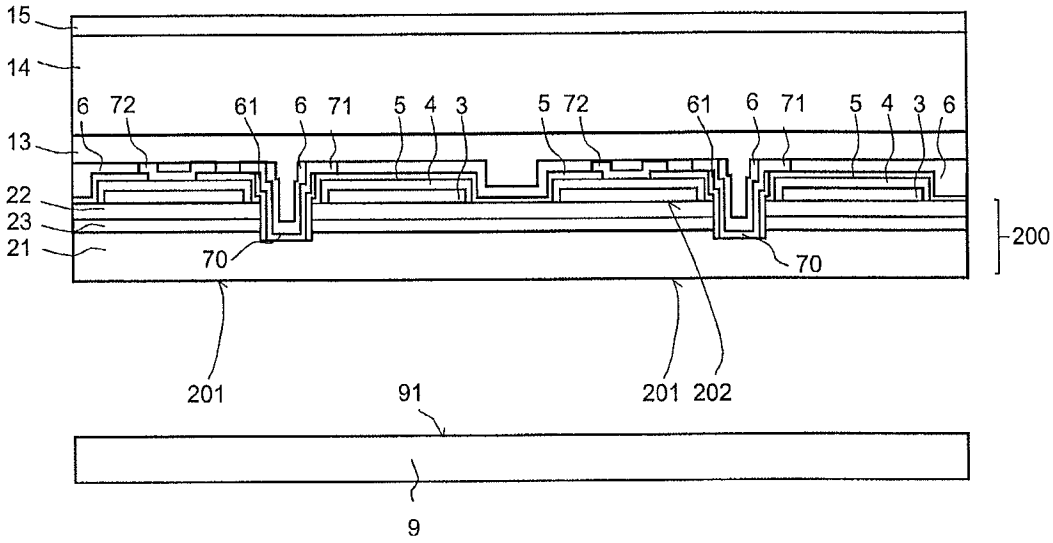

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FIG 9A

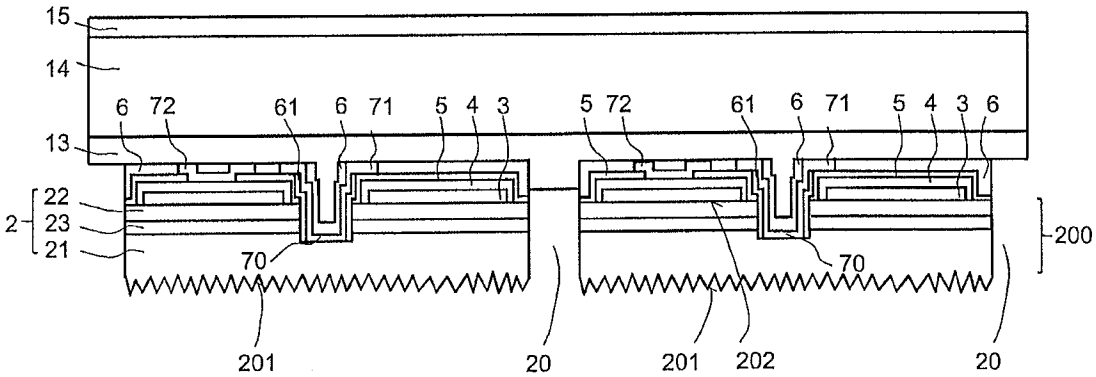

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FIG 9B

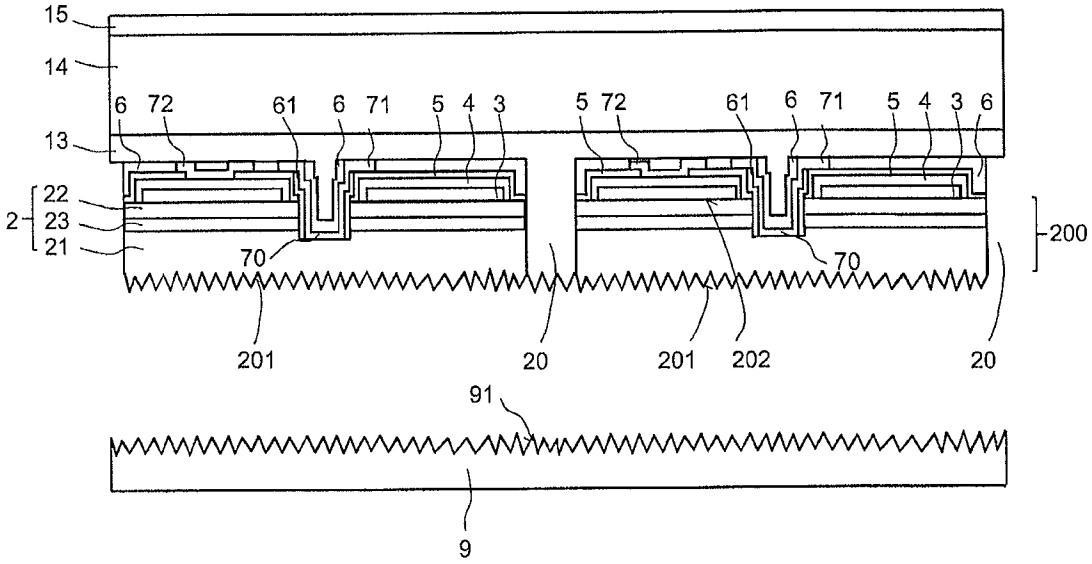

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FIG 10

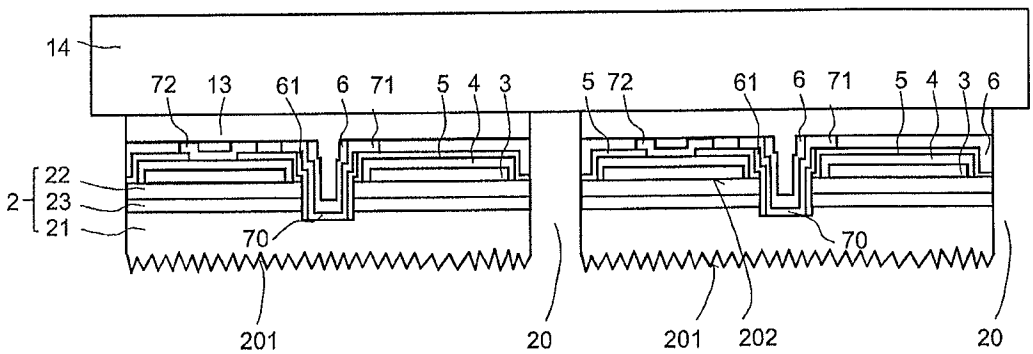

14
72 13 61 6 71 5 4 3 5 72 61 6 71 5 4 3 6
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FIG 11

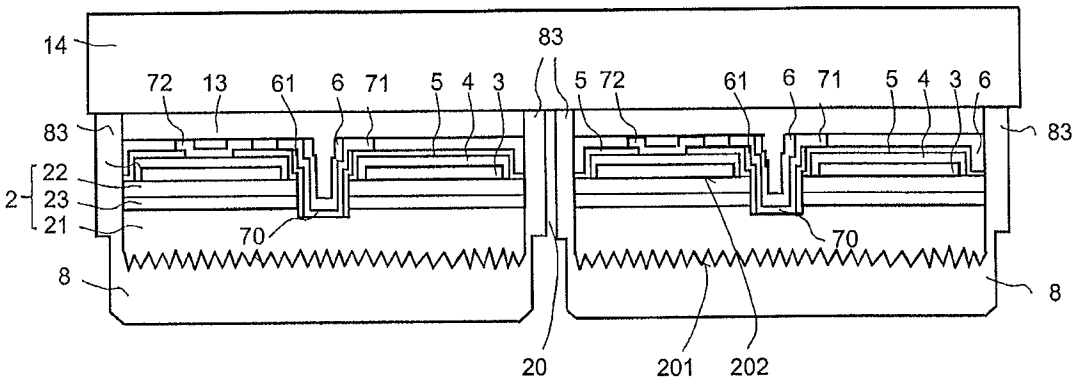


FIG 11A

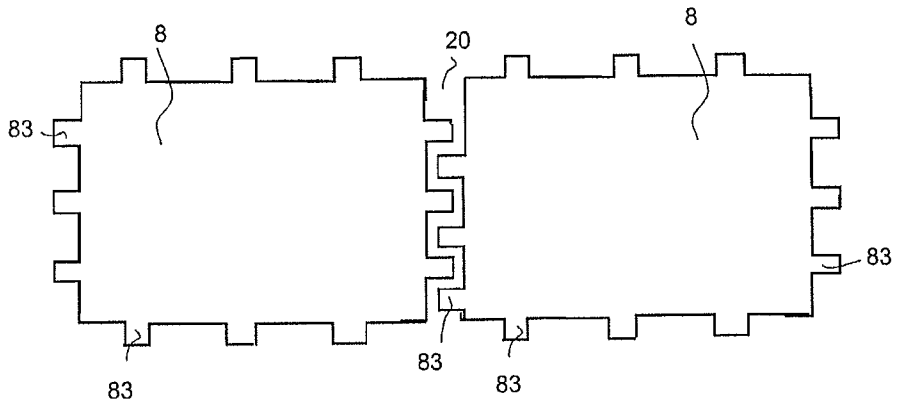


FIG 11B

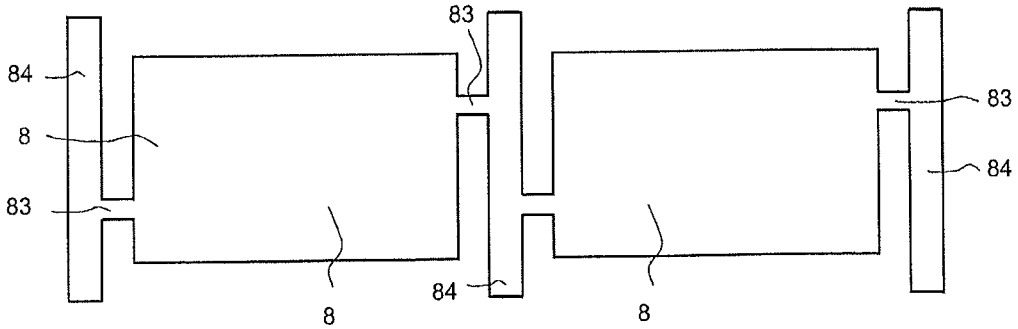


FIG 12

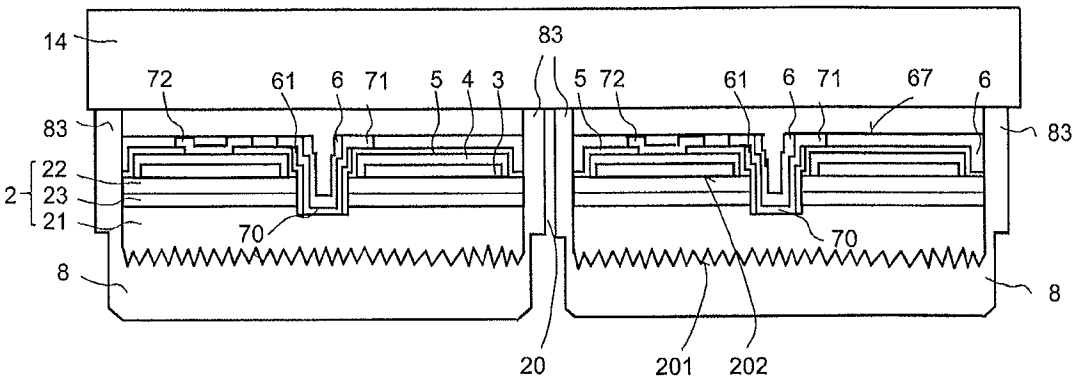

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FIG 13

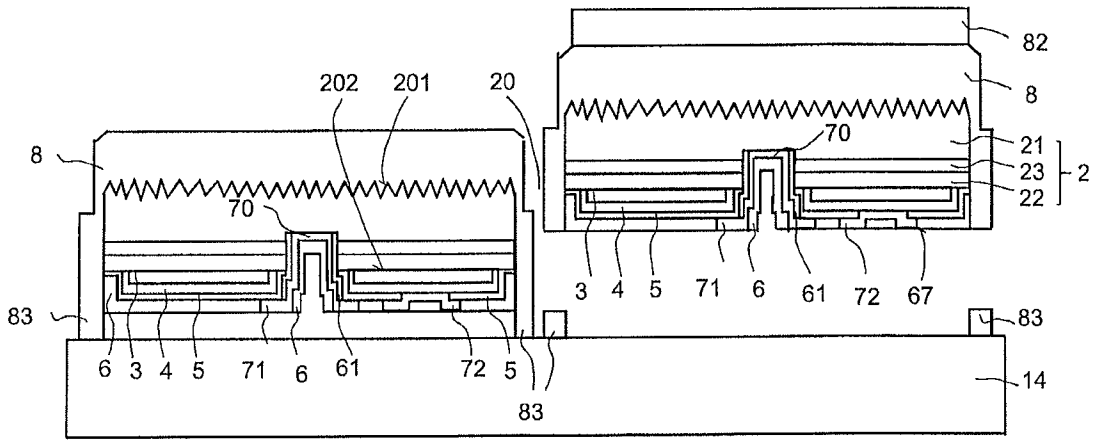

82
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FIG 14

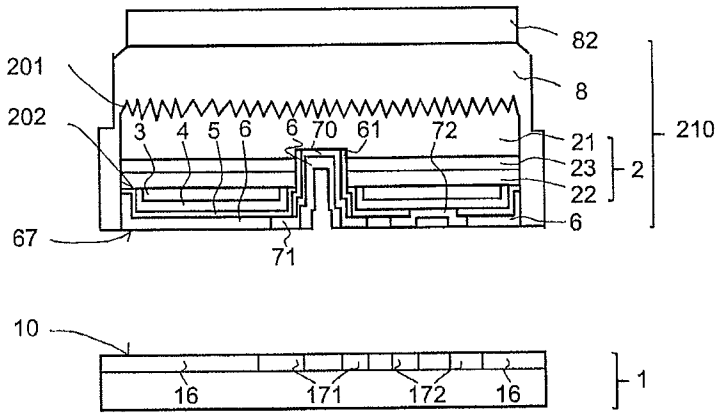


FIG 15

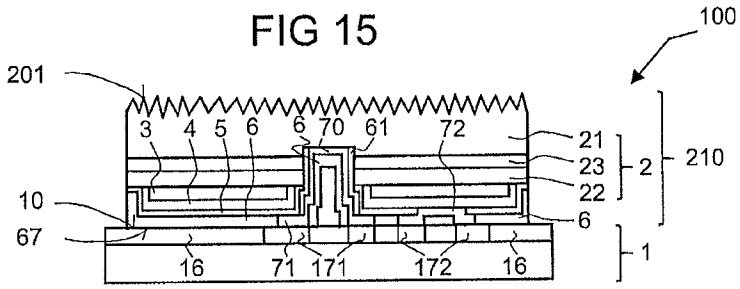


FIG 16

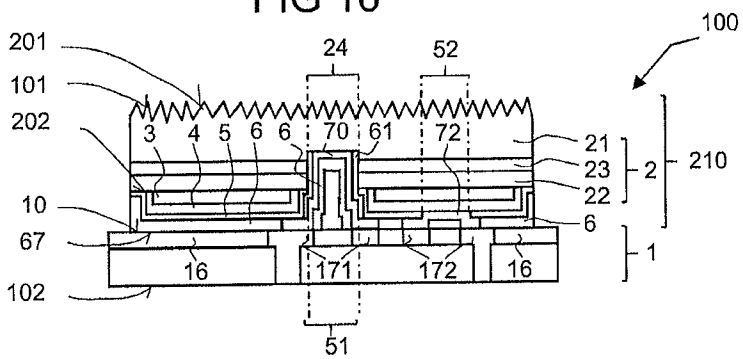


FIG 17A

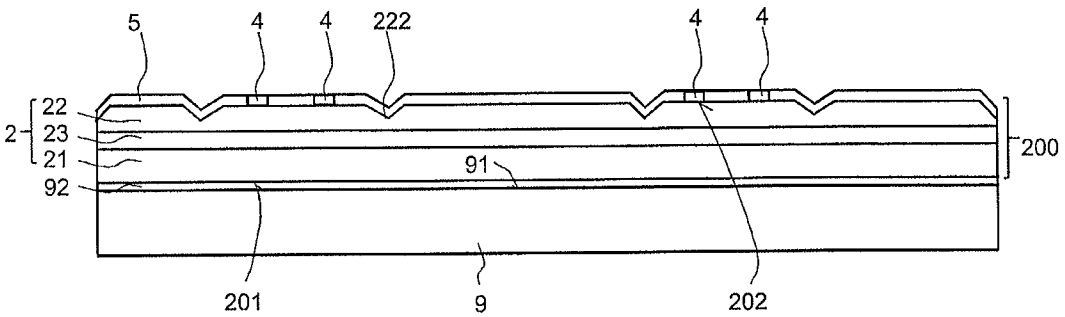


FIG 17B

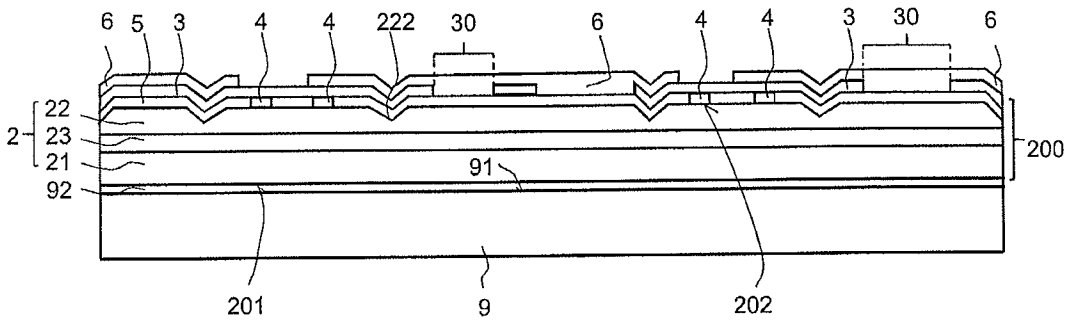


FIG 17C

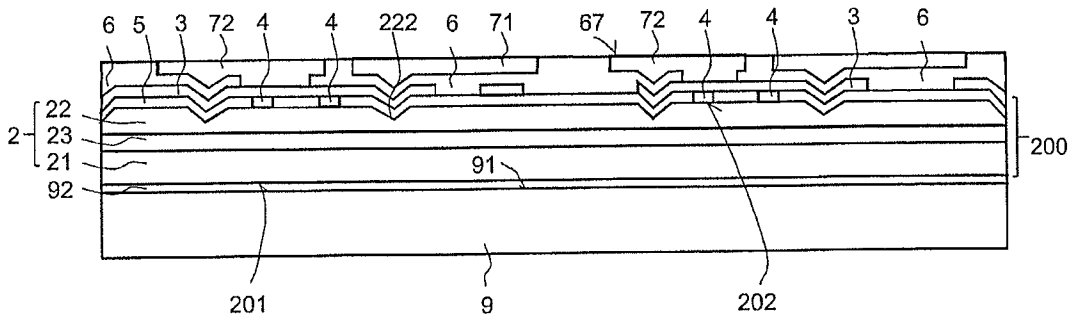


FIG 17D

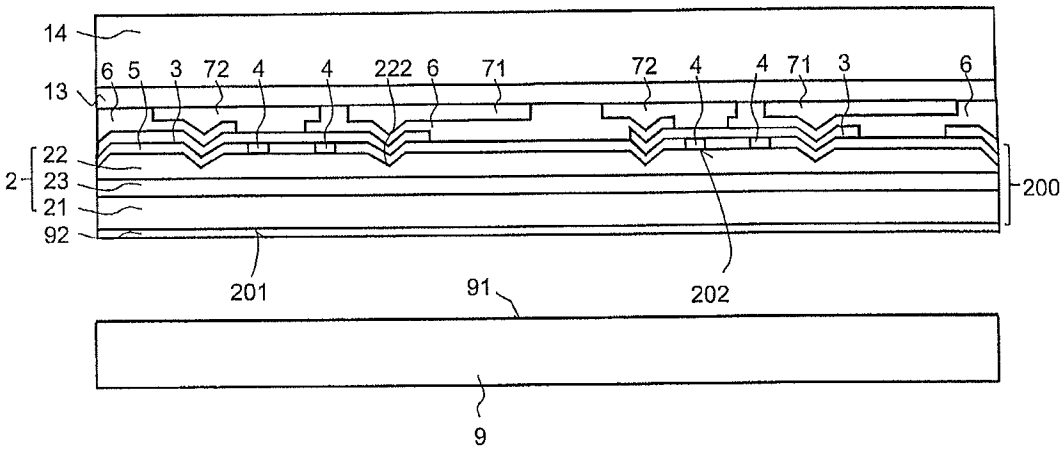


FIG 17E

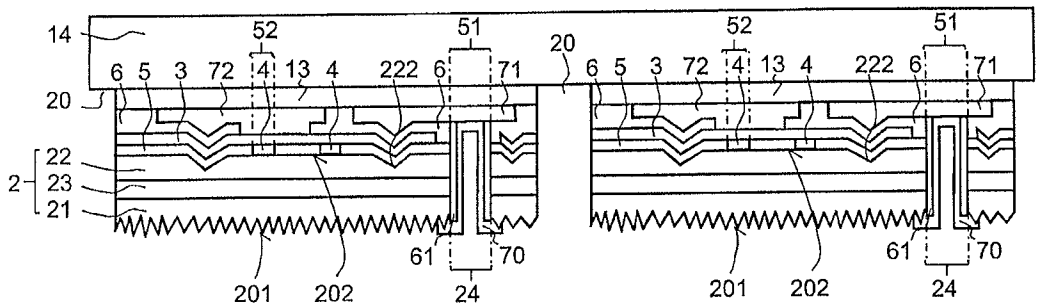


FIG 17F

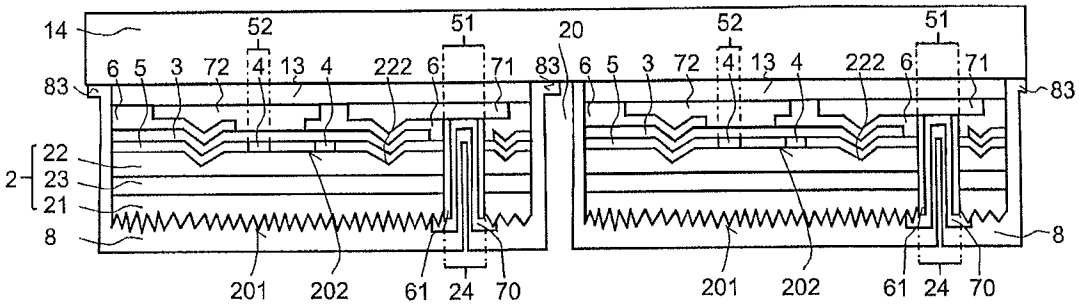


FIG 17G

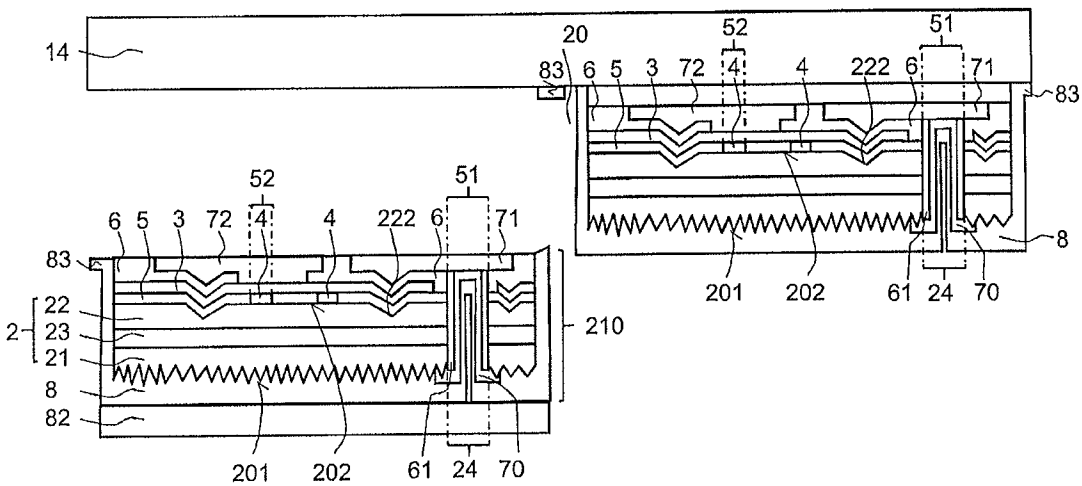


FIG 17H

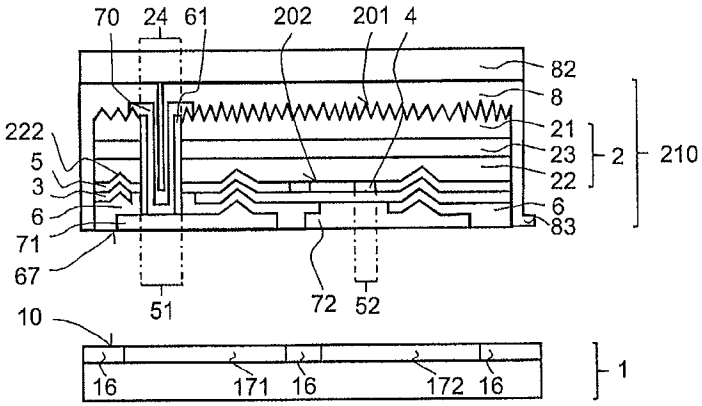
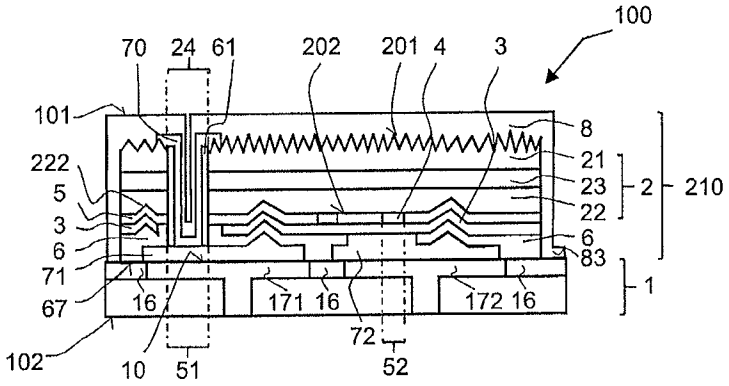


FIG 17I



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2016/051827

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L33/00 H01L33/38
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 2 757 603 A1 (TOSHIBA KK [JP]) 23 July 2014 (2014-07-23) paragraphs [0094], [0097] - [0108]; figures 8, 16	15-18
A	US 2011/136271 A1 (VON MALM NORWIN [DE]) 9 June 2011 (2011-06-09) the whole document	1-18
A	DE 10 2007 019776 A1 (OSRAM OPTO SEMICONDUCTORS GMBH [DE]) 30 October 2008 (2008-10-30) figure 7	15-18
A	US 2010/248484 A1 (BOWER CHRISTOPHER [US] ET AL) 30 September 2010 (2010-09-30) the whole document	1-18

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 May 2016	17/05/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Aichmayr, Günther

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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2016/051827

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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Information on patent family members

International application No
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