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(71) Applicant: CYPRESS SEMICONDUCTOR CORPORATION [US/US]; 198 Champion Court, San Jose, CA 95134 (US).

(72) Inventor: MIYAMAE, Toru; 1-16-1-1001 Maenami-Cho, Kasugai-Shi, Aichi 486-0903 (JP).

(74) Agent: BATEMAN, Andrew, J.; Cypress Semiconductor Corporation, 198 Champion Court, San Jose, CA 95134 (US).

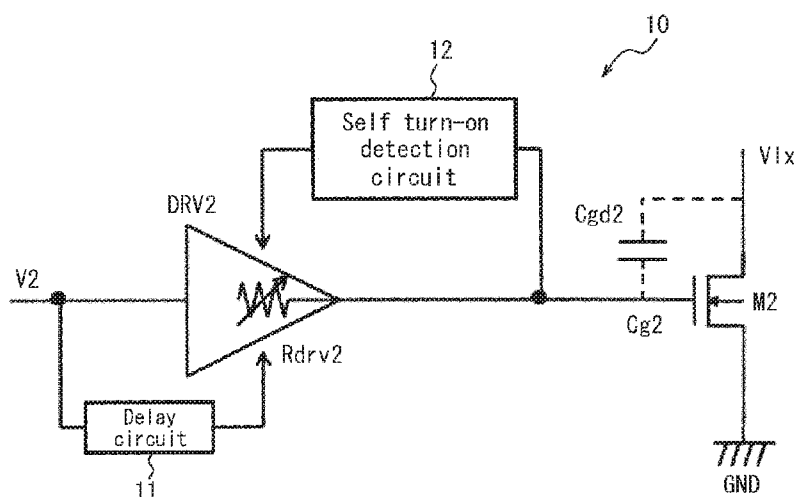
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[Continued on next page]

(54) Title: SWITCHING CIRCUIT

FIG. 3



(57) Abstract: A switching circuit includes a driver circuit DRV2 that outputs voltage for turning on and off a first transistor switch M2, positioned at a low potential side with respect to a load, among a plurality of transistor switches disposed in series between an input voltage and a ground; and a control circuit that causes the driver circuit DRV2 to output a first voltage that turns the first transistor switch M2 on upon an output voltage of the driver circuit DRV2 rising while the first transistor switch M2 is off and to cause the driver circuit DRV2 to suspend output of the first voltage upon the output voltage of the driver circuit DRV2 dropping after the driver circuit DRV2 outputs the first voltage.



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SWITCHING CIRCUIT

PRIORITY

[0001] This application is an International Application of U.S. Patent
5 Application No. 14/866,193, filed on September 25, 2015, which claims the
benefit of U.S. Provisional Application No. 62/180,524, filed on June 16,
2015, both of which are incorporated by reference herein in their entirety.

TECHNICAL FIELD

10 [0002] This disclosure relates to a switching circuit.

BACKGROUND

[0003] One type of switching circuit is a switching regulator. Switching
regulators have high conversion efficiency and are therefore widely used as
15 voltage converters in batteries for inputting voltage to a variety of control
circuits (loads). For example, switching regulators are also widely used as
on-board power supplies. In switching regulators, however, switching noise
occurs during control to switch a switching circuit (MOSFET) on and off.

[0004] To address switching noise, one conventional approach uses a noise
20 countermeasure. In greater detail, this conventional approach discloses
attenuating resonance energy by turning a plurality of auxiliary switching
elements, which each control the conduction current of high-side and low-side
switching elements, on for a predetermined time period at a timing that
matches the timing at which the switching elements are turned on. The
25 switching elements and the auxiliary switching elements are controlled by
corresponding driver circuits. One disadvantage of this conventional approach,
however, is that it slows down the switching speed of the regulator.

SUMMARY

30 [0005] This disclosure provides a switching circuit and method of control
thereof that attenuate ringing.

[0006] An exemplary switching circuit includes: a driver circuit configured to
output voltage for turning on and off a first transistor switch, positioned at a
low potential side with respect to a load, among a plurality of transistor
35 switches disposed in series between an input voltage and a ground; and a

control circuit configured to cause the driver circuit to output a first voltage that turns the first transistor switch on upon an output voltage of the driver circuit rising while the first transistor switch is off and to cause the driver circuit to suspend output of the first voltage upon the output voltage of the driver circuit dropping after the driver circuit outputs the first voltage.

[0007] In this exemplary switching circuit, the driver circuit may include a variable resistor, and resistance of the variable resistor changes in response to a signal from the control circuit.

[0008] This exemplary switching circuit may further include a delay circuit configured to delay output of the first voltage from the driver circuit to the first transistor switch based on the output voltage of the driver circuit.

[0009] In this exemplary switching circuit, when the first transistor switch is on, the driver circuit may decrease the resistance of the variable resistor until the output voltage falls below the first voltage and increase the resistance of the variable resistor upon the output voltage becoming equal to or less than the first voltage.

[0010] In this exemplary switching circuit, the first transistor switch may be a MOSFET controlled by voltage supplied to a gate thereof.

[0011] The switching circuit according to the following embodiments can attenuate ringing.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] In the accompanying drawings:

FIG. 1 is a waveform diagram illustrating the relationship between a switching voltage waveform and a control signal that controls an auxiliary switch in an example of a switching regulator;

FIG. 2 is a waveform diagram illustrating a change in the switching voltage waveform due to a change in the input voltage;

FIG. 3 is a functional block diagram schematically illustrating a switching circuit according to Embodiment 1;

FIG. 4 is a circuit diagram illustrating the principle of self turn-on;

FIG. 5 is a waveform diagram illustrating the relationship between voltages in the circuit in FIG. 4;

FIG. 6 illustrates an example of the structure of a switching circuit according to Embodiment 1;

FIG. 7 is a waveform diagram illustrating the relationship between voltages in the circuit in FIG. 6;

FIG. 8 illustrates attenuation of ringing when using the circuit in FIG. 6;

5 FIG. 9 illustrates an example of the structure of a switching circuit according to Embodiment 2;

FIGS. 10A to 10C illustrate adjustment of delay time in the circuit in FIG. 9;

10 FIGS. 11A and 11B illustrate attenuation of ringing when using the circuit in FIG. 9; and

FIG. 12 illustrates a modification to Embodiment 2.

DETAILED DESCRIPTION

15 [0013] Even if the switching frequency in a switching regulator is, for example, several hundred kHz, ringing corresponding to the switching frequency occurs due to the sudden change in current when switching between on and off. Due to ringing, the wiring and the like of the switching regulator becomes an antenna and radiates noise. As a countermeasure against such noise, the switching frequency in the switching regulator may be lowered to
20 slow down the speed of switching, thereby suppressing the peak of ringing. In this case, however, since the speed of switching is slower, the energy conversion efficiency of the switching regulator may be reduced. Furthermore, if the speed of switching slows down, it becomes impossible in some cases to perform switching at the required switching frequency, for example even
25 when a predetermined speed of switching (such as 2 MHz or more) is required to avoid generation of AM band noise.

30 [0014] In one conventional approach, if a sufficiently long time for the resonance energy to attenuate is set as the time period during which the corresponding auxiliary switching element is turned on in order to limit the conduction current of the low-side switching element when the high-side switching element is turned on, then the current corresponding to this time is wasted. Therefore, as the length of time during which the auxiliary switching element is on grows longer, the efficiency of the switching regulator grows worse. Accordingly, this length of time is preferably short. Shortening this
35 length of time, however, makes it difficult to turn on the auxiliary switching

element at a timing matching the timing of ringing.

[0015] In the waveform of ringing, the initial peak is the highest, and the ringing gradually attenuates thereafter, as illustrated by the waveform of the switching voltage V_m in FIG. 1. Therefore, if the initial peak of ringing can be
5 attenuated, the subsequent ringing will also be attenuated. Accordingly, the auxiliary switching element in the aforementioned conventional approach is ideally turned on during a time period Δt_2 that matches the initial peak of ringing illustrated in FIG. 1. It is difficult, however, to turn the auxiliary switching element on during this appropriate time period Δt_2 .

10 [0016] Even if the auxiliary switching element can be set to turn on during this predetermined time period Δt_2 , the time period Δt_1 from the start of ringing until the auxiliary switching element should be turned on varies, for example when the input voltage varies as illustrated in FIG. 2. Hence, it is difficult to turn the auxiliary switching element on at the preferred timing.

15 Furthermore, when attempting to turn the auxiliary switching element on via control by a driver circuit after detecting a change in the switching voltage V_m , it is difficult to turn the switching element on at an appropriate timing due to the delay from detection of the change in the switching voltage V_m until the auxiliary switching element turns on.

20 [0017] Embodiments for taking a countermeasure against noise without reducing the speed of switching are described below with reference to the drawings.

[0018] Embodiment 1

FIG. 3 is a block diagram of a switching circuit according to
25 Embodiment 1. This switching circuit is, for example, used in a DC-DC converter that temporally divides input voltage by controlling high-side and low-side transistor switches with respect to a load, smooths the temporally divided input voltage, and outputs the result. A switching circuit 10 is provided with a driver circuit DRV2, a delay circuit 11, and a self turn-on
30 detection circuit 12. The driver circuit DRV2 includes an output resistor R_{drv2} that is a variable resistor. A low-side transistor switch M2 is controlled to be on or off by output of the driver circuit DRV2. Via self turn-on, the switching circuit 10 causes the timing at which ringing occurs and the timing at which current flows to the ground (GND) to match.

35 [0019] With reference to FIG. 4, the principle of self turn-on in the switching

circuit of FIG. 3 is now described. In FIG. 4, structural elements that are the same as the structural elements in the circuit in FIG. 3 are labeled with the same reference signs. The circuit in FIG. 4 includes driver circuits DRV1 and DRV2 and transistor switches M1 and M2 that, for example, are MOSFETs or the like. Input voltage V_{in} is supplied to the drain of the transistor switch M1. The source of the transistor switch M1 is connected to the source of the transistor switch M2. The drain of the transistor switch M2 is connected to the ground GND. The outputs of the driver circuit DRV1 and the driver circuit DRV2 are respectively provided to the gate terminals of the transistor switch M1 and the transistor switch M2. The driver circuit DRV2 is also connected to the ground GND.

[0020] The driver circuit DRV1 outputs a driver output voltage V_{g1} upon input of an input voltage V_1 . The driver circuit DRV2 outputs a driver output voltage V_{g2} upon input of an input voltage V_2 . Here, the transistor switches M1 and M2 are respectively high-side and low-side switches. The voltage V_{lx} is an output voltage provided to a non-illustrated load.

[0021] The driver circuit DRV2 includes an output resistor R_{drv2} . The driver circuit DRV2 corresponds to the driver circuit DRV2 illustrated in FIG. 3. As the resistance of the output resistor R_{drv2} is larger, a parasitic capacitance C_{gd2} occurs between the drain and the gate of the transistor M2.

[0022] FIG. 5 is a waveform diagram illustrating the relationship between the voltages V_1 , V_2 , V_{g1} , V_{g2} , and V_{lx} in the circuit in FIG. 4. At time t_1 illustrated in FIG. 5, the transistor switch M1 changes from off to on and begins to conduct, at which point the voltage V_{lx} rises. At this time, if the resistance of the output resistor R_{drv2} in the driver circuit DRV2 has a certain value, then due to the increase in the voltage V_{lx} , the voltage V_{g2} increases through the parasitic capacitance C_{gd2} . As a result, the transistor switch M2 turns on regardless of the output of the driver circuit DRV2, and current flows to the ground. This phenomenon by which the transistor switch M2 turns on based on a change in the voltage V_{lx} is referred to as self turn-on. The switching circuit 10 of this embodiment uses this self turn-on to cause the timing at which ringing occurs and the timing at which current flows to the ground (GND) to match.

[0023] FIG. 3 further illustrates how the same input voltage V_2 as the voltage that is input into the driver circuit DRV2 is also input into the delay circuit 11.

The delay circuit 11 then outputs the input voltage V2 as output voltage after delaying a predetermined length of time. The output voltage output by the delay circuit 11 is provided to the driver circuit DRV2. The self turn-on detection circuit 12 detects whether, at the output side of the driver circuit
5 DRV2, self turn-on has occurred in the transistor switch M2. The self turn-on detection circuit 12 corresponds to the "control circuit" in this embodiment. In greater detail, the self turn-on detection circuit 12 detects whether self turn-on has occurred in the transistor switch M2 due to a change in the signal at the gate of the transistor switch M2.

10 [0024] FIG. 6 illustrates an example of a switching circuit according to Embodiment 1.

[0025] The driver circuit DRV2 includes NOR circuits 31 and 32, a NOT circuit 33, transistor switches M3, M4, and M5, and a resistor R1. In this embodiment, the transistor switch M3 is a p-type MOSFET, and the transistor
15 switches M4 and M5 are n-type MOSFETs.

[0026] Voltage V3 output by the delay circuit 11 and voltage V4 output by the self turn-on detection circuit 12 are provided to the NOR circuit 31. The NOR circuit 31 inverts the logical sum of the signals indicated by the input voltages V3 and V4 and outputs the result.

20 [0027] The voltage output by the NOR circuit 31 and the voltage V2 that is input into the driver circuit DRV2 are provided to the NOR circuit 32. The NOR circuit 32 inverts the logical sum of the signals indicated by the input voltages and outputs the result (voltage V5).

[0028] The voltage V2 input into the driver circuit DRV2 is inverted at the
25 NOT circuit 33 and provided to the gate of the transistor switch M3. The source of the transistor switch M3 is connected to a power source VDD. The drain of the transistor switch M3 is connected to the drain of the transistor switch M4 and to the drain of the transistor switch M5.

[0029] The voltage V2 input into the driver circuit DRV2 is inverted at the
30 NOT circuit 33 and provided to the gate of the transistor switch M4. The source of the transistor switch M4 is connected to the ground GND via the resistor R1.

[0030] The voltage V5 output by the NOR circuit 32 is input into the gate of the transistor switch M5. The source of the transistor switch M5 is connected
35 to the ground GND.

[0031] In the driver circuit DRV2 with the above-described structure, the output resistor Rdrv2 is subjected to variable control by controlling the transistor switches M3, M4, and M5 to turn on or off. In other words, the magnitude of voltage drop due to the resistor R1 with respect to the output voltage in the node N is changed between a state in which the transistor switches M3, M4, and M5 are all conducting and a state in which the transistor switches M3 and M4 are conducting while the transistor switch M5 is not conducting. When the resistance of the output resistor Rdrv2 is less than a certain value, then self turn-on does not occur, whereas when the resistance of the output resistor Rdrv2 is at least a certain value, self turn-on does occur. The state in which self turn-on occurs is referred to below as a self turn-on state, and the state in which self turn-on does not occur is referred to as a non-self turn-on state. Whether or not self turn-on occurs in the driver circuit DRV2 is described below.

[0032] As illustrated in FIG. 6, the delay circuit 11 is configured with a plurality of NOT circuits connected in series.

[0033] The self turn-on detection circuit 12 includes a transistor switch M6, a resistor R2, a NOT circuit 21, and a latch circuit 22. The voltage of the node N between the driver circuit DRV2 and the transistor switch M2 is input into the gate of the transistor switch M6. The drain of the transistor switch M6 is connected to a power source VDD via the resistor R2, and the drain is connected to the ground GND.

[0034] The NOT circuit 21 is connected to the power source VDD via the resistor R2. The NOT circuit 21 outputs a signal (voltage V6) that is the inversion of the signal indicated by the power source voltage.

[0035] The latch circuit 22 is a so-called SR latch circuit. The voltage V6 output by the NOT circuit 21 is input into the S input port of the latch circuit 22. The same input voltage V2 as the voltage that is input into the driver circuit DRV2 is input into the input port R of the latch circuit 22. The latch circuit 22 outputs a signal (voltage V4) from the output port Q. The voltage V4 that is output is then input into the NOR circuit 31 of the driver circuit DRV2.

[0036] FIG. 7 is a waveform diagram illustrating the relationship between the voltages V2, V3, V4, V5, V6, Vg2, and Vlx in the circuit in FIG. 6. With reference to FIG. 7, the following provides a detailed description of operations

in the driver circuit DRV2 to switch between the non-self turn-on state and the self turn-on state and of the occurrence of self turn-on.

[0037] At the start point of the waveform diagram in FIG. 7, the driver circuit DRV2 is in the non-self turn-on state. Once the voltage V2 changes from High to Low at time t2, the voltage Vg2 output by the driver circuit DRV2 also lowers over a predetermined delay time due to the delay circuit 11. The predetermined delay time that it takes for the voltage Vg2 to change from High to Low is also referred to below as a "transition period". The transition period is, for example, 0.5 ns. Once the transition period elapses after time t2, the voltage V5 output by the NOR circuit 32 changes from High to Low at time t3. As a result, the value of the output resistor Rdrv2 of the driver circuit DRV2 increases. In other words, at this time, the driver circuit DRV2 switches from the non-self turn-on state to the self turn-on state.

[0038] In this state, once the voltage Vlx suddenly rises at time t4, the voltage Vg2 temporarily rises as per the principle described with reference to FIGS. 4 and 5. When the voltage Vg2 rises in this way, self turn-on occurs. When self turn-on occurs, the voltage Vg2 exceeds a predetermined threshold vth. By self turn-on, the noise of the voltage Vlx can be attenuated.

[0039] The voltage Vg2 that started to rise at time t4 is input into the self turn-on detection circuit 12. In the self turn-on detection circuit 12, the transistor switch M6 is configured to conduct upon input into the gate of a voltage Vg2 exceeding the predetermined threshold vth. The transistor switch M6 enters a conducting state when the voltage Vg2 is the threshold vth or more and a non-conducting state when the voltage Vg2 is less than the threshold vth. By conduction of the transistor switch M6, the self turn-on detection circuit 12 detects the self turn-on state. Conversely, by non-conduction of the transistor switch M6, the self turn-on detection circuit 12 detects the non-self turn-on state. Once the non-self turn-on state is entered, the voltage V6 input into the latch circuit 22 changes from Low to High. As a result, the voltage V4 output by the latch circuit 22 changes from Low to High.

[0040] Once the voltage V4 that has changed to High is input into the NOR circuit 31, the voltage V5 output by the NOR circuit 32 changes from Low to High. By the voltage V5 that has become High being input into the gate of the transistor switch M5, the transistor switch M5 turns on. As a result, the value

of the output resistor R_{drv2} of the driver circuit DRV2 lowers. Hence, the driver circuit DRV2 switches from the self turn-on state to the non-self turn-on state.

[0041] The time Δt_3 that self turn-on continues is determined by the delay in the circuit that detects the self turn-on. The time Δt_3 that self turn-on continues is, for example, 3 ns. Once the time Δt_3 elapses and the voltage V_{g2} falls below the threshold v_{th} , the transistor switch M6 enters a non-conducting state.

[0042] FIG. 8 illustrates attenuation of ringing when using the circuit in FIG. 6. The graph in the upper tier of FIG. 8 illustrates the change in switching voltage when not using the switching circuit 10 according to this embodiment, and the graph in the lower tier of FIG. 8 illustrates the change in switching voltage when using the switching circuit 10 according to this embodiment. The graphs in FIG. 8 illustrate the experimental results for an input voltage V_{in} of 12 V. As illustrated in FIG. 8, when using the switching circuit 10 according to this embodiment, ringing is attenuated as compared to when not using the switching circuit 10.

[0043] Embodiment 2

FIG. 9 illustrates an example of a switching circuit according to Embodiment 2. As compared to the switching circuit 10 according to Embodiment 1, a switching circuit 40 according to Embodiment 2 can cause the timing at which self turn-on occurs to match the timing of ringing with even higher accuracy. A description of portions of the switching circuit 40 according to Embodiment 2 that are the same as the switching circuit 10 according to Embodiment 1 is omitted, so as to focus on the differences. In the switching circuit 40 according to Embodiment 2, structural elements that are the same as those of the switching circuit 10 according to Embodiment 1 are labeled with the same reference signs.

[0044] The switching circuit 40 according to Embodiment 2 differs from the switching circuit 10 according to Embodiment 1 by not including the delay circuit 11 and by including an Up/Down counter 41 and a variable delay circuit 42.

[0045] The input voltage V_2 is input into the variable delay circuit 42, and the variable delay circuit 42 delays the input voltage by a predetermined length of time and outputs the result as output voltage V_3 . The output voltage

V3 that is output by the variable delay circuit 42 is provided to the NOR circuit 31 of the driver circuit DRV2. The predetermined length of time (delay time) by which the variable delay circuit 42 delays the input voltage V2 is determined based on a control signal provided by the Up/Down counter 41.

5 The variable delay circuit 42 for example determines the delay time to be within a range of 1.2 ns to 6.0 ns, in increments of 0.3 ns.

[0046] The input voltage V2 and the voltage V4 output by the latch circuit 22 of the self turn-on detection circuit 12 are input into the Up/Down counter 41. Based on the input voltages V2 and V4, the Up/Down counter 41 transmits, to
10 the variable delay circuit 42, a control signal for adjusting (changing) the delay time in the variable delay circuit 42. For example, when the self turn-on detection circuit 12 detects self turn-on, the signal indicated by the voltage V4 becomes High, since the transistor switch M6 is in a conducting state. At this time, the Up/Down counter 41 outputs a control signal for delaying the
15 variable delay circuit 42 by one step to the variable delay circuit 42. Conversely, when the self turn-on detection circuit 12 detects non-self turn-on, the signal indicated by the voltage V4 becomes Low, since the transistor switch M6 is in a non-conducting state. At this time, the Up/Down counter 41 outputs a control signal for accelerating the variable delay circuit 42 by one
20 step to the variable delay circuit 42.

[0047] Based on the signal V3 provided by the variable delay circuit 42, the driver circuit DRV2 controls the timing at which self turn-on is produced in the transistor switch M2.

[0048] With reference to FIGS. 10A to 10C, adjustment of the delay time by
25 the Up/Down counter 41 and the variable delay circuit 42 and the timing of when self turn-on occurs are now described. FIGS. 10A to 10C illustrate the relationship between the voltages V2, V3, V4, V5, V6, Vg2, and Vlx in the circuit in FIG. 9. If the delay time is too short, then as illustrated in FIG. 10A, self turn-on occurs earlier than the timing of the initial peak of ringing. Hence,
30 ringing cannot be sufficiently attenuated. Therefore, in order to match the timing of self turn-on with the timing of ringing, when the self turn-on detection circuit 12 detects self turn-on (self turn-on state), the variable delay circuit 42 increases the delay time by one step (i.e. 0.3 ns) based on the control signal provided by the Up/Down counter 41. In other words, when self
35 turn-on occurs in the transistor switch M2, the variable delay circuit 42

extends the delay time by 0.3 ns. The timing at which self turn-on occurs can thus be delayed.

[0049] Conversely, when the delay time is too long, then as illustrated in FIG. 10B, self turn-on does not occur (non-self turn-on state) even though ringing is occurring. Therefore, in order to match the timing of self turn-on with the timing of ringing, when the self turn-on detection circuit 12 does not detect self turn-on of the transistor switch M2, the variable delay circuit 42 decreases the delay time by one step (i.e. 0.3 ns) based on the control signal provided by the Up/Down counter 41. In other words, when self turn-on does not occur in the transistor switch M2, the variable delay circuit 42 shortens the delay time by 0.3 ns. The timing at which self turn-on occurs can thus be accelerated.

[0050] As illustrated in FIG. 10C, by repeating the above control, the variable delay circuit 42 adjusts the timing at which self turn-on occurs so as to match the timing of the initial peak of ringing. Hence, the switching circuit 40 according to Embodiment 2 can cause the timing at which self turn-on occurs to match the timing of ringing with even higher accuracy.

[0051] FIGS. 11A and 11B illustrate attenuation of ringing when using the circuit in FIG. 9. The graphs in the upper tiers of FIGS. 11A and 11B illustrate the change in switching voltage when not using the switching circuit 40 according to this embodiment, and the graphs in the lower tiers of FIGS. 11A and 11B illustrate the change in switching voltage when using the switching circuit 40 according to this embodiment. The graphs in FIG. 11A illustrate the experimental results for an input voltage V_{in} of 12 V, and the graphs in FIG. 11B illustrate the experimental results for an input voltage V_{in} of 24 V. As illustrated in FIG. 11A, when using the switching circuit 40 according to this embodiment, ringing is attenuated as compared to when not using the switching circuit 40. Furthermore, as illustrated in FIG. 11B, ringing is attenuated even if the input voltage changes and the timing of ringing changes, since self turn-on occurs in conjunction with the timing of ringing by using the switching circuit 40 according to this embodiment.

[0052] FIG. 12 illustrates a modification to this embodiment. To the structure in FIG. 9, this modification adds an auxiliary switch M2-2 for the transistor switch M2 and an auxiliary driver circuit DRV2-2 that performs on/off control of the auxiliary switch M2-2. In this modification, while the transistor switch

M2 is in a non-conducting state, the input voltage to the driver circuit DRV2 is Low, and therefore the auxiliary switch M2-2 is also in a non-conducting state. Accordingly, for example a comparison with a structure that includes an auxiliary switch such as PTL 1 shows that although it is difficult with only an
5 auxiliary switch to maintain a good conversion efficiency while suppressing ringing, it is possible to suppress ringing at an appropriate timing by combining a structure that includes an auxiliary switch with the structure of this embodiment.

[0053] Although exemplary embodiments have been described with reference
10 to the accompanying drawings, it is to be noted that various changes and modifications will be apparent to those skilled in the art based on this disclosure. Therefore, such changes and modifications are to be understood as included within the scope of this disclosure. For example, the functions and the like included in each component may be reordered in any logically
15 consistent way. Furthermore, structural components and the like may be combined into one or divided.

CLAIMS

1. A switching circuit comprising:
a driver circuit configured to output voltage for turning on and off a
5 first transistor switch, positioned at a low potential side with respect to a load,
among a plurality of transistor switches disposed in series between an input
voltage and a ground; and
a control circuit configured to cause the driver circuit to output a first
voltage that turns the first transistor switch on upon an output voltage of the
10 driver circuit rising while the first transistor switch is off and to cause the
driver circuit to suspend output of the first voltage upon the output voltage of
the driver circuit dropping after the driver circuit outputs the first voltage.
2. The switching circuit of claim 1, wherein the driver circuit
15 includes a variable resistor, and resistance of the variable resistor changes in
response to a signal from the control circuit.
3. The switching circuit of Claim 1, further comprising a delay
circuit configured to delay output of the first voltage, from the driver circuit
20 to the first transistor switch, based on the output voltage of the driver circuit.
4. The switching circuit of Claim 2, wherein when the first
transistor switch is on, the driver circuit decreases the resistance of the
variable resistor until the output voltage falls below the first voltage and
25 increases the resistance of the variable resistor upon the output voltage
becoming equal to or less than the first voltage.
5. The switching circuit of Claim 1, wherein the first transistor
switch is a metal-oxide-semiconductor field-effect transistor (MOSFET)
30 controlled by voltage supplied to a gate thereof.
6. The switching circuit of Claim 1, further comprising an
up/down counter and a variable delay circuit, wherein an output of the
up/down counter is coupled to an input of the variable delay circuit, and an
35 output of the variable delay circuit is coupled to an input of the driver circuit.

7. The switching circuit of Claim 6, further comprising:
an auxiliary switch coupled in parallel with the first transistor switch at the
low potential side with respect to the load; and an auxiliary driver circuit
configured to output voltage for turning on and off the auxiliary switch.

5 8. The switching circuit of Claim 1, further comprising:
a second transistor switch, positioned at a high potential side with respect to
the load, among the plurality of transistor switches disposed in series between
the input voltage and the ground; and a high-side driver circuit configured to
output voltage for turning on and off the second transistor switch.

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9. The switching circuit of Claim 8, further comprising an output
node between the second transistor switch and the first transistor switch,
wherein an output load voltage at the output node is provided to the load.

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10. The switching circuit of Claim 1, wherein an output load
voltage of the switching circuit is coupled to the load in a switching regulator.

20

11. A method of attenuating ringing in a switching circuit, the
method comprising: causing a driver circuit, of the switching circuit, to output
a first voltage that turns a first transistor switch on upon an output voltage of
the driver circuit rising while the first transistor switch is off; wherein the
first transistor switch, among a plurality of transistor switches disposed in
series between an input voltage and a ground, is positioned at a low potential
side with respect to a load; and causing the driver circuit to suspend output of
the first voltage upon the output voltage of the driver circuit dropping after
25 the driver circuit outputs the first voltage.

25

12. The method of Claim 11, further comprising:
detecting a self turn-on state and a non-self turn-on state of the driver circuit;
and changing resistance of a variable resistor of the driver circuit in response
to detecting the self turn-on state or the non-self turn state.

30

13. The method of Claim 12, further comprising increasing the resistance of the variable resistor in response to the driver circuit switching from the non-self turn-on state to the self turn-on state.

5 14. The method of Claim 12, further comprising decreasing the resistance of the variable resistor in response to the driver circuit switching from the self turn-on state to the non-self turn-on state.

10 15. The method of Claim 11, further comprising matching a timing at which ringing occurs in the switching circuit with a timing at which current flows to the ground.

15 16. The method of Claim 11, further comprising delaying output of the first voltage, from the driver circuit to the first transistor switch, based on the output voltage of the driver circuit.

17. The method of Claim 16, wherein delaying output of the first voltage comprises one of: using a plurality of NOT-circuits connected in series to delay output of the first voltage; and using an up/down counter coupled to a variable delay circuit to delay output
20 of the first voltage.

18. An apparatus comprising:
a load; and

a switching regulator coupled to provide voltage to the load, the switching regulator comprising:

25 a driver circuit configured to output voltage for turning on and off a first transistor switch, positioned at a low potential side with respect to the load, among a plurality of transistor switches disposed in series between an input voltage and a ground; and

30 a control circuit configured to cause the driver circuit to output a first voltage that turns the first transistor switch on upon an output voltage of the driver circuit rising while the first transistor switch is off and to cause the driver circuit to suspend output of the first voltage upon the output voltage of the driver circuit dropping after the driver circuit outputs the first voltage.

19. The apparatus of Claim 18, wherein the load is a control circuit.

5 20. The apparatus of Claim 18, wherein the switching regulator is configured as an on-board power supply.

FIG. 1

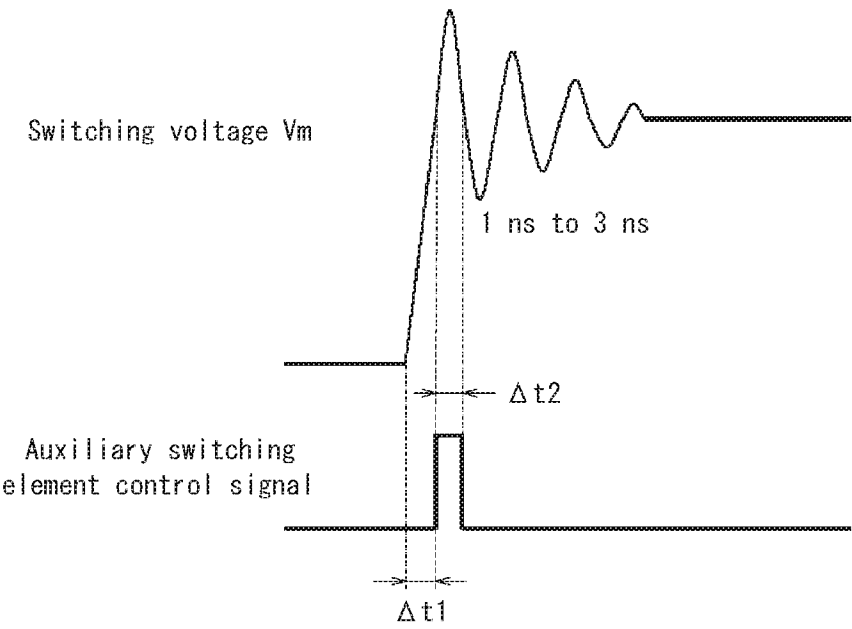


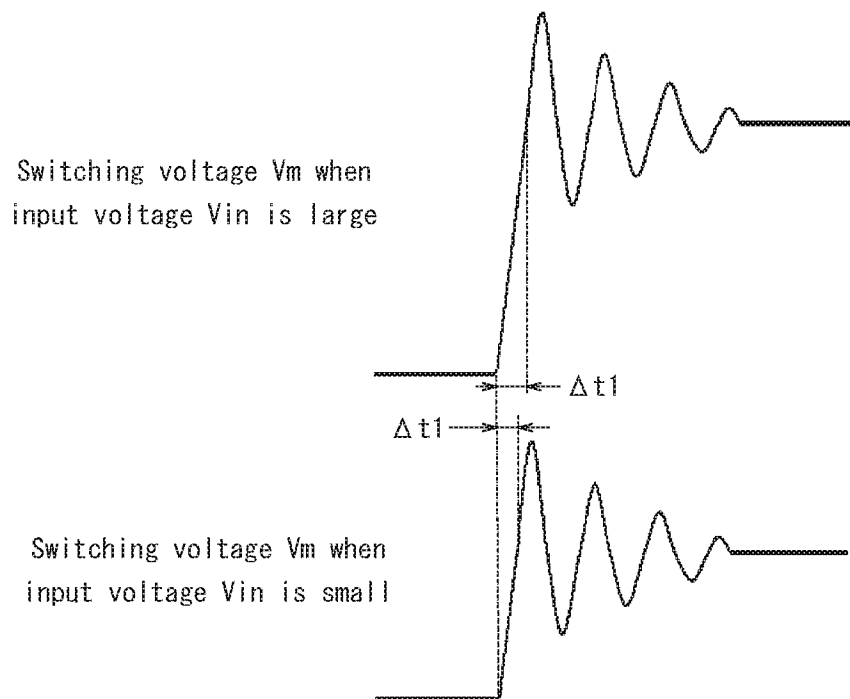
FIG. 2

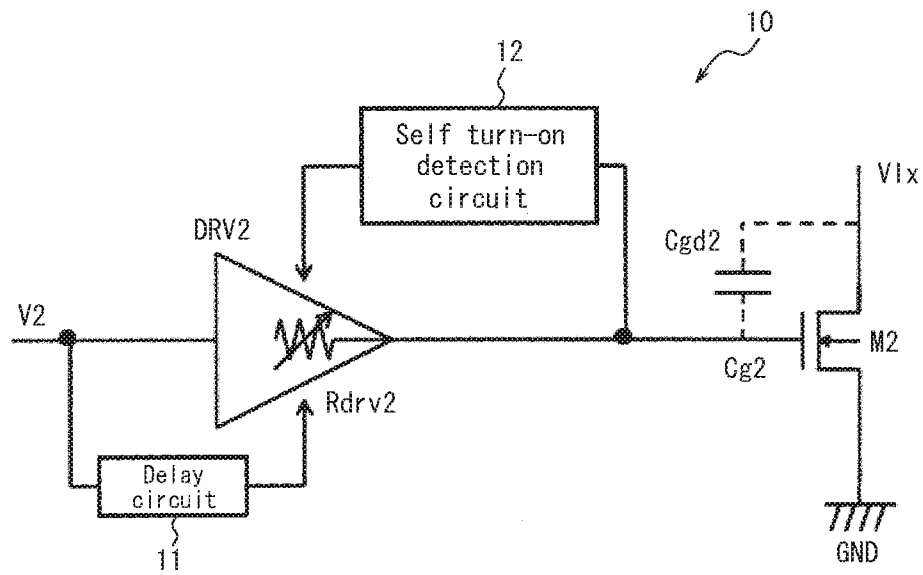
FIG. 3

FIG. 4

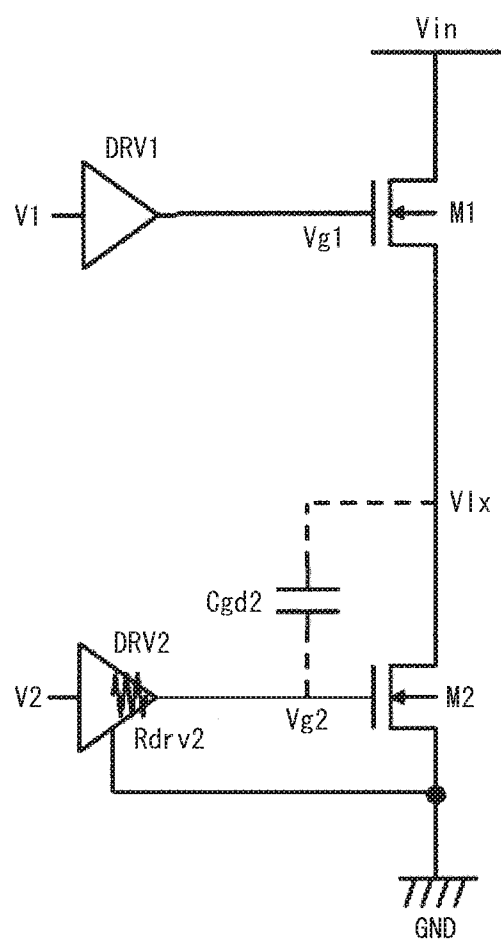


FIG. 5

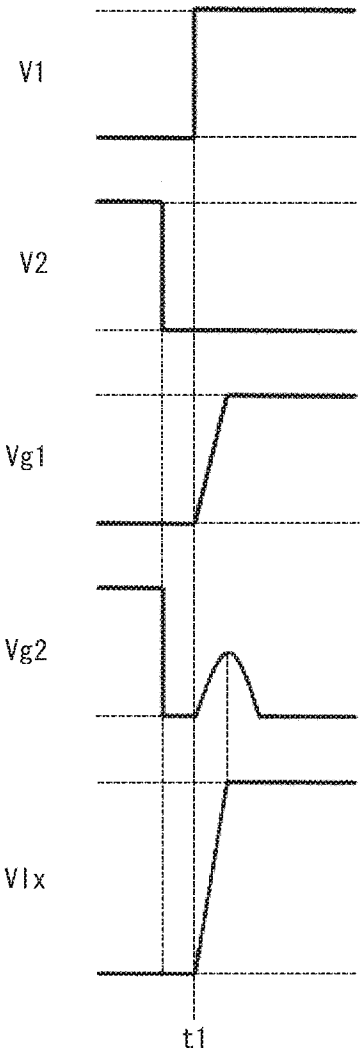


FIG. 6

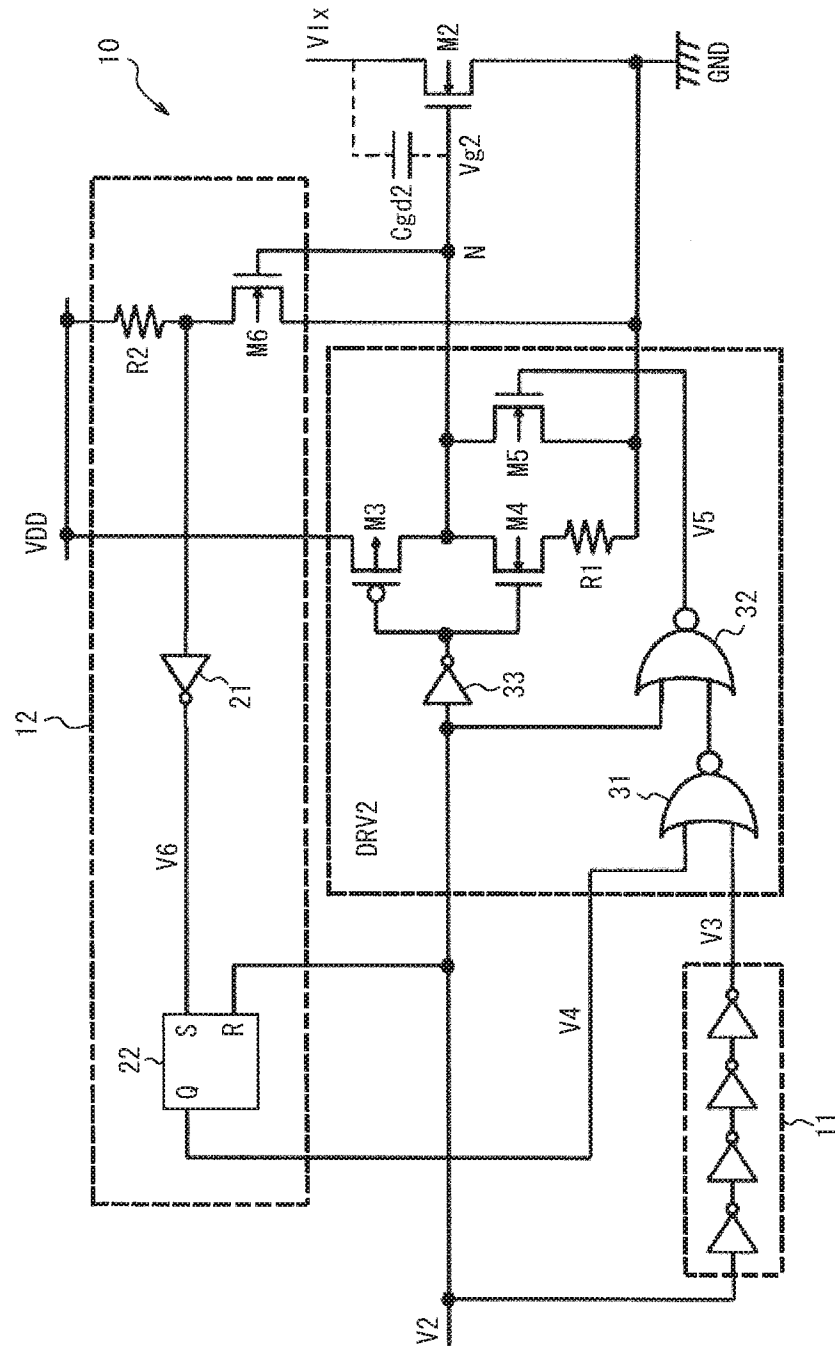


FIG. 7

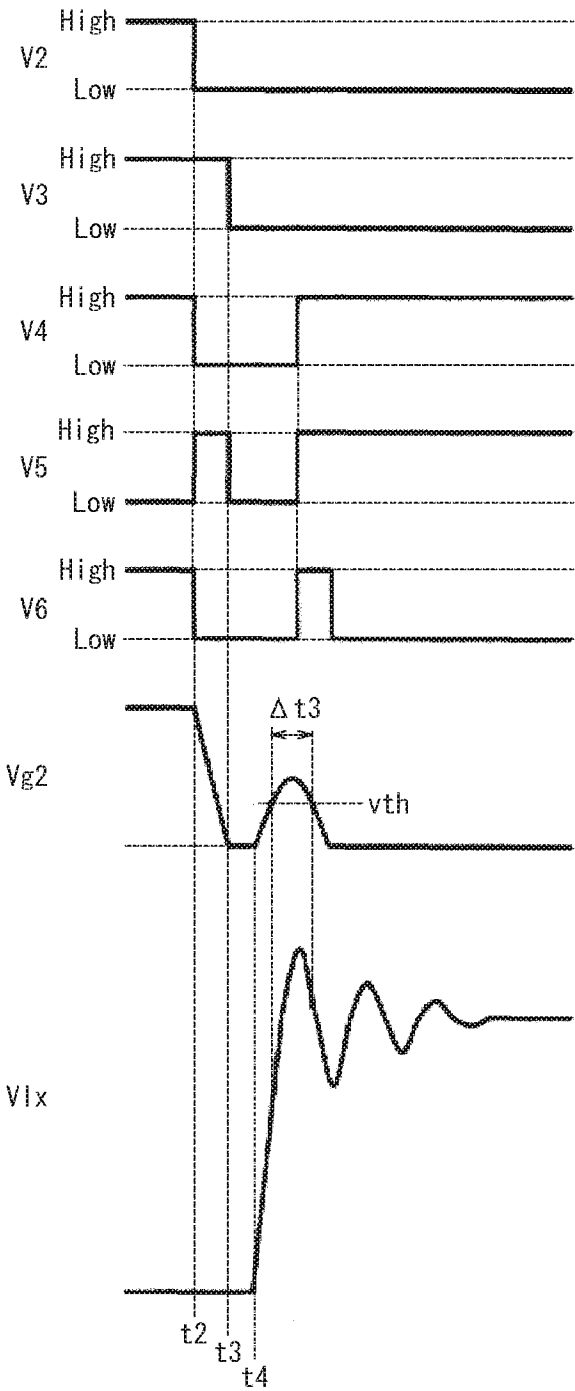


FIG. 8

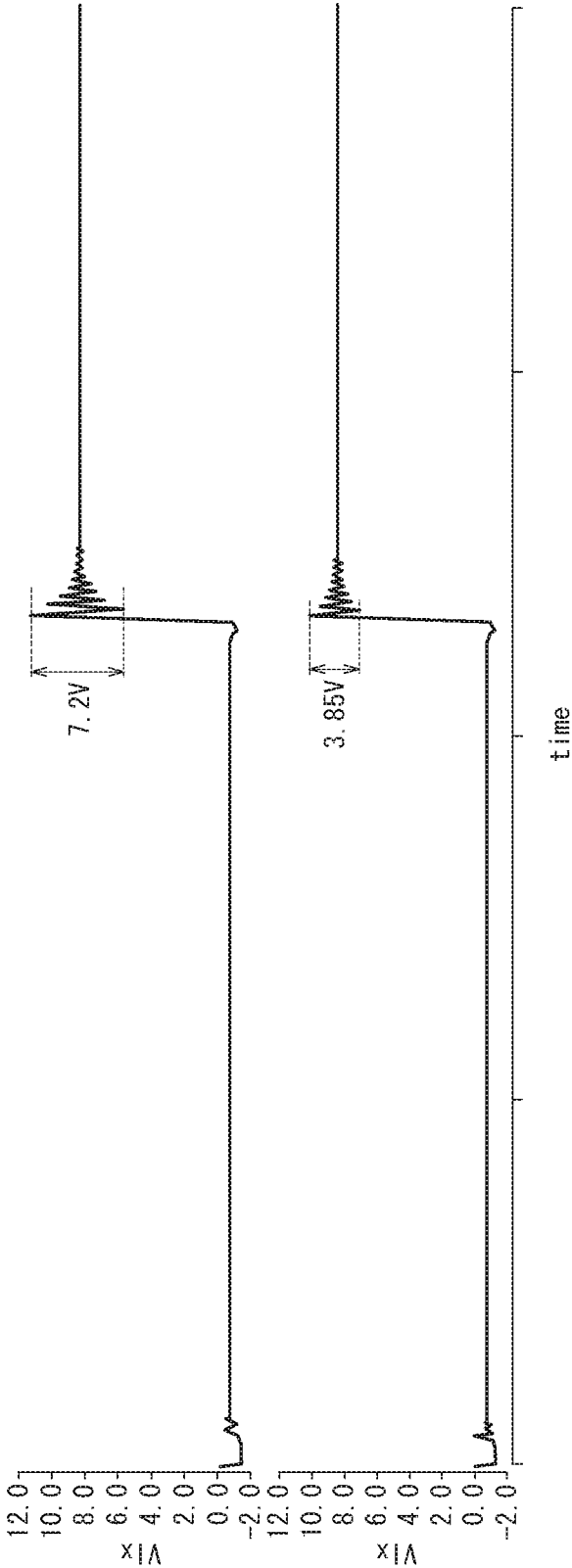


FIG. 9

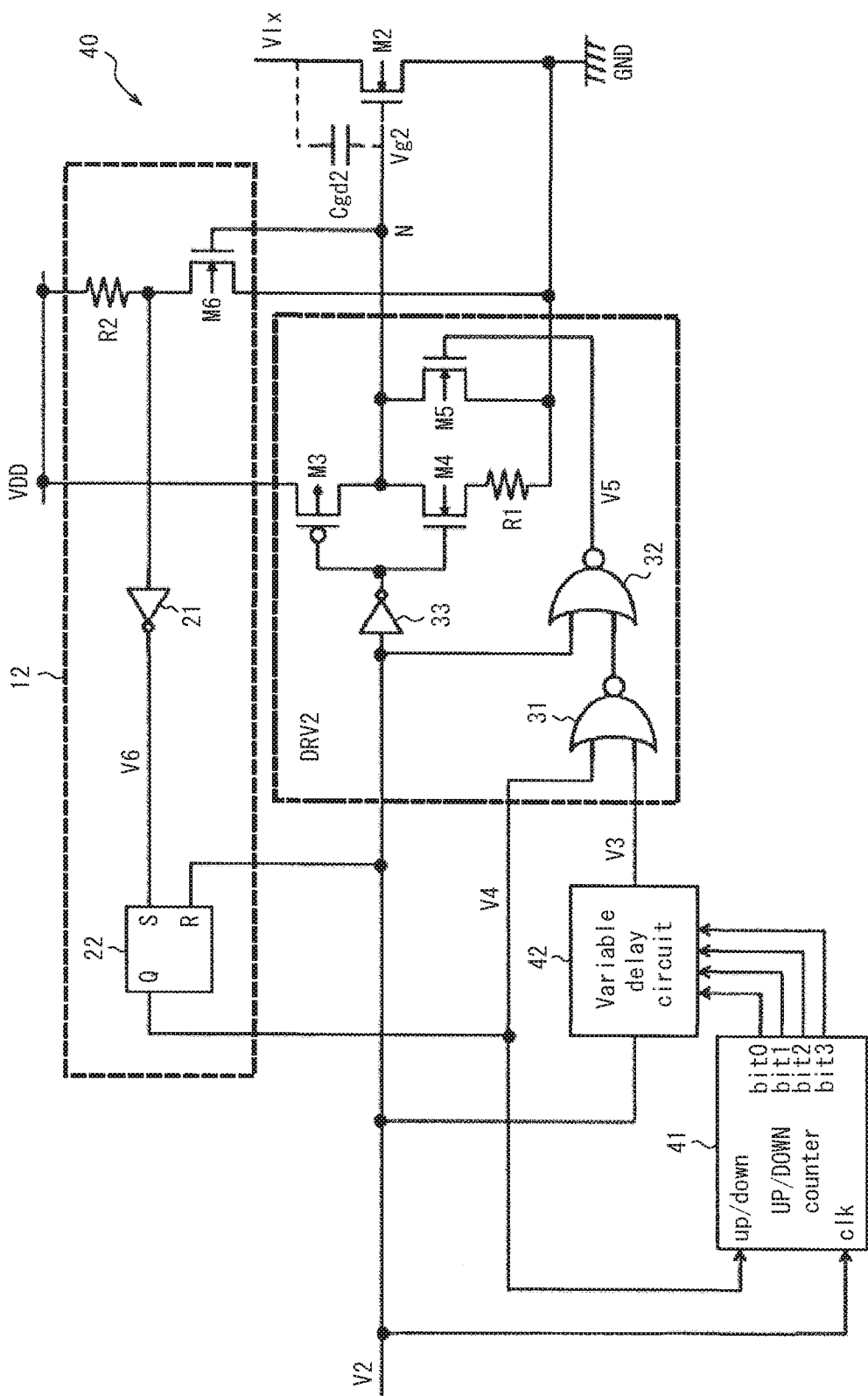


FIG. 10A

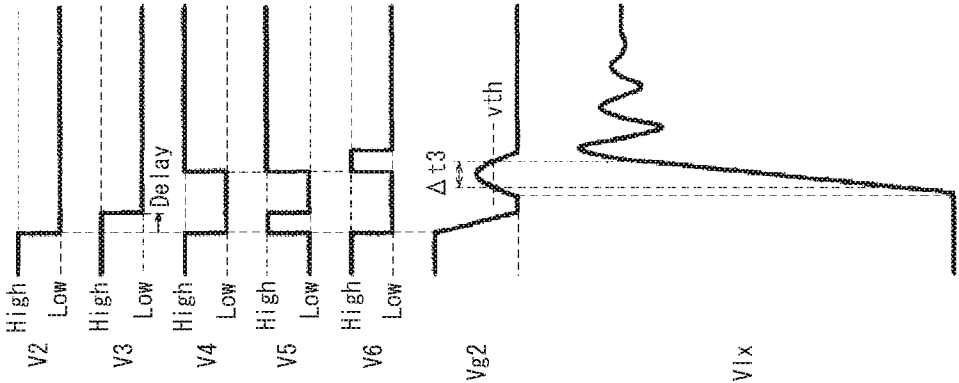


FIG. 10B

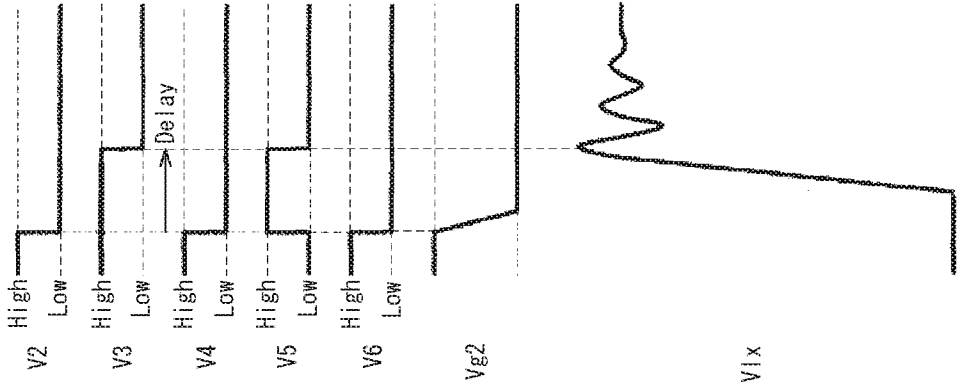


FIG. 10C

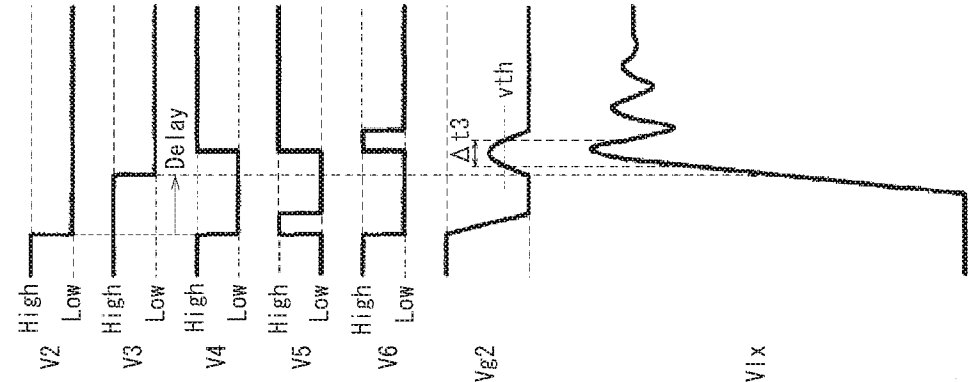


FIG. 11A

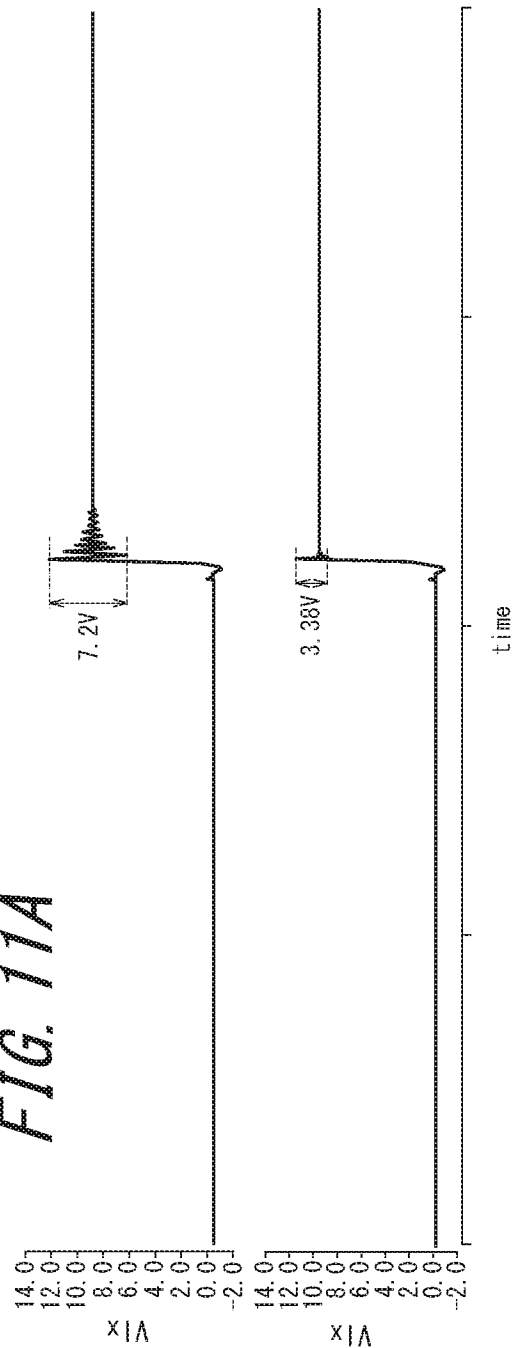
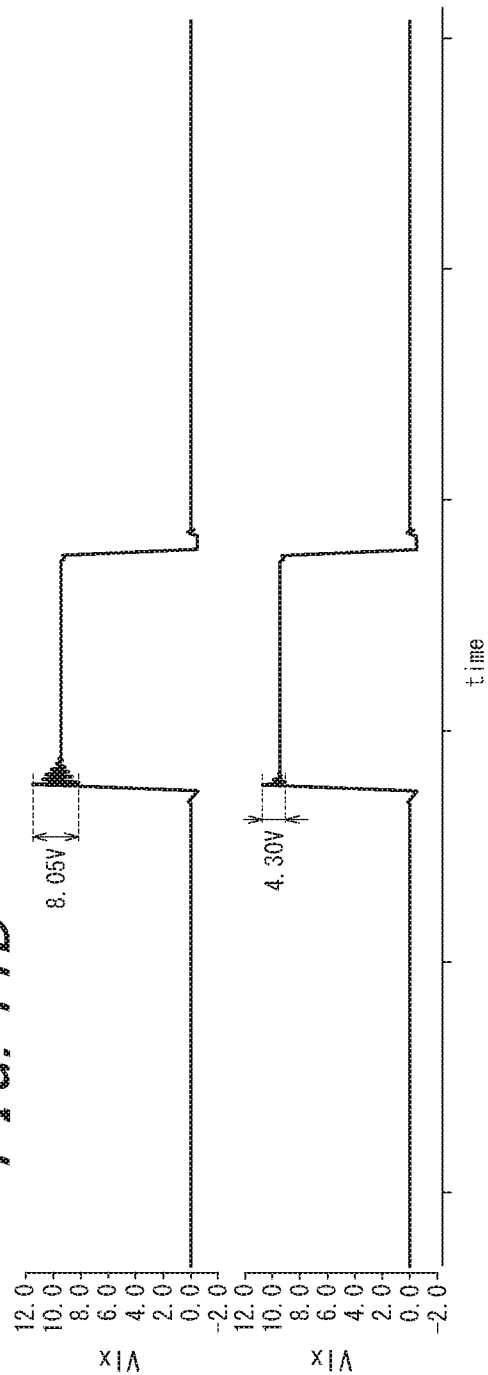


FIG. 11B



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2016/020449

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G05F 1/00, G05F 1/10, G05F 1/46, G05F 1/56, G05F 1/595; H02M 3/156, H02M 3/157 (2016.01)

CPC - G05F 1/00, G05F 1/10, G05F 1/46, G05F 1/56, G05F 1/595; H02M 3/156, H02M 3/1563 (2016.02)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - G05F 1/00, G05F 1/10, G05F 1/46, G05F 1/56, G05F 1/595; H02M 3/156, H02M 3/157 (2016.01)

CPC - G05F 1/00, G05F 1/10, G05F 1/46, G05F 1/56, G05F 1/595; H02M 3/156, H02M 3/1563 (2016.02)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC - 323/all, 271, 282-285 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Orbit, Google Patents, Google Scholar

Search terms used: switch, circuit, regulator, ringing, noise, low-side, transistor, MOSFET, variable resistor, ground, drive, feedback, voltage

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 8,773,099 B2 (GRANGER) 08 July 2014 (08.07.2014) entire document	1-20
A	US 2012/0062190 A1 (HAIPLIK et al) 15 March 2012 (15.03.2012) entire document	1-20
A	US 7,495,871 B2 (HAVANUR) 24 February 2009 (24.02.2009) entire document	1-20
A	US 7,696,731 B2 (HUANG et al) 13 April 2010 (13.04.2010) entire document	1-20
A	US 2013/0193937 A1 (KABUSHIKI KAISHA TOSHIBA et al) 01 August 2013 (01.08.2013) entire document	1-20
A	US 2008/0048631 A1 (KIM) 28 February 2008 (28.02.2008) entire document	1-20
A	US 8,278,897 B2 (SCHIFF et al) 02 October 2012 (02.10.2012) entire document	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

02 May 2016

Date of mailing of the international search report

17 MAY 2016

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