Fig. 1
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The present disclosure generally relates to the field of electronics. More particularly, an embodiment of the invention relates to priority based intelligent platform passive thermal management.

BACKGROUND

As integrated circuit (IC) fabrication technology improves, manufacturers are able to integrate additional functionality onto a single silicon substrate. As the number of these functionalities increases, however, so does the number of components on a single IC chip. Additional components add additional signal switching, in turn, generating more heat. The additional heat may damage an IC chip by, for example, thermal expansion. Also, the additional heat may limit usage locations and/or usage applications of a computing device that includes such chips.

For example, a portable computing device may solely rely on battery power for its operations. Hence, as additional functionality is integrated into portable computing devices, the need to reduce power consumption becomes increasingly important, for example, to maintain battery power for an extended period of time. Non-portable computing systems also face cooling and power consumption issues as their IC components use more power and generate more heat.

BRIEF DESCRIPTION OF THE DRAWINGS

The detailed description is provided with reference to the accompanying figures. In the figures, the left-most digit(s) of a reference number identifies the figure in which the reference number first appears. The use of the same reference numbers in different figures indicates similar or identical items.

Figs. 1 and 4-6 illustrate block diagrams of embodiments of computing systems, which may be utilized to implement various embodiments discussed herein.
Fig. 2 illustrates a block diagram of portions of a processor core and other components of a computing system, according to an embodiment.

Fig. 3 illustrates a flow diagram of a method in accordance with an embodiment.

DETAILED DESCRIPTION

In the following description, numerous specific details are set forth in order to provide a thorough understanding of various embodiments. However, various embodiments of the invention may be practiced without the specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to obscure the particular embodiments of the invention. Further, various aspects of embodiments of the invention may be performed using various means, such as integrated semiconductor circuits ("hardware"), computer-readable instructions organized into one or more programs ("software"), or some combination of hardware and software. For the purposes of this disclosure reference to "logic" shall mean either hardware, software, firmware, or some combination thereof. Also, the use of "instruction" and "micro-operation" (uop) is interchangeable as discussed herein.

Power management is crucial for mobile devices (such as phones, tablets, UMPC (Ultra Mobile Personal Computer), laptop computers such as ultrabooks, etc.) and hence it is critical that such platforms are highly optimized from a power/thermal and performance point of view. In computing systems, the Advanced Configuration and Power Interface (ACPI) specification provides an open standard for device configuration and power management by the Operating System (OS). In some embodiments, at least some of the power consumption states and/or techniques discussed herein may be in accordance with or similar to those defined under ACPI specification, Revision 3.0, September 2004, which extends the thermal model beyond the previous processor centric support. This extended thermal model incorporated into ACPI 3.0 specification addresses a growing need for an intelligent and better holistic platform level thermal management of mobile platforms. The need arose, in part, because there are now more components on the system that are heat generators than just the processor as was the case several years ago when the previous version of the thermal model was defined (e.g., in revision 1.0).

Moreover, the implementation of ACPI 3.0 thermal model is also known as Dynamic Power Performance Management technology (DPPM). This new platform thermal management model involves the platform determining the relationship between different power consuming
and heat generating components on the system and various hotspots on the system as measured by (e.g., dedicated) platform level thermal sensor(s). Then, the platform can expose these determined relationship information in the form of a Thermal Relationship Table (TRT). However, determining and generating the TRT values may be a cumbersome and time consuming process prone to errors and involves a lot of engineering effort. This has made ACPI 3.0 less feasible to incorporate into systems and hence may have resulted in hindrance for broad DPPM adoption.

To this end, some embodiments modify the TRT definition and use it as a priority table instead of a pure scientific thermal relationship table, e.g., providing the ease of understanding and ease of implementation benefits.

Such techniques may be implemented in any platform, e.g., in an embedded controller implementation of thermal management and/or in OS power/thermal management. As such, some embodiments may be provided in various computing devices, e.g., including phones, UMPCs, tablets, laptops like ultrabooks, desktop computer, computer servers, System on Chip (SoC) device(s), etc. (such as those discussed herein with reference to Figs. 1 and 4-6).

Furthermore, the techniques discussed herein may be used in any type of computing system and/or processors discussed with reference to Figs. 1 and 4-6. More particularly, Fig. 1 illustrates a block diagram of a computing system 100, according to an embodiment of the invention. The system 100 may include one or more processors 102-1 through 102-N (generally referred to herein as "processors 102" or "processor 102"). The processors 102 may communicate via an interconnection network or bus 104. Each processor may include various components some of which are only discussed with reference to processor 102-1 for clarity. Accordingly, each of the remaining processors 102-2 through 102-N may include the same or similar components discussed with reference to the processor 102-1.

In an embodiment, the processor 102-1 may include one or more processor cores 106-1 through 106-M (referred to herein as "cores 106" or more generally as "core 106"), a shared cache 108, a router 110, and/or a processor control logic or unit 120. The processor cores 106 may be implemented on a single integrated circuit (IC) chip. Moreover, the chip may include one or more shared and/or private caches (such as cache 108), buses or interconnections (such as a bus or interconnection network 112), memory controllers (such as those discussed with reference to Figs. 4-6), or other components.
In one embodiment, the router 110 may be used to communicate between various components of the processor 102-1 and/or system 100. Moreover, the processor 102-1 may include more than one router 110. Furthermore, the multitude of routers 110 may be in communication to enable data routing between various components inside or outside of the processor 102-1.

The shared cache 108 may store data (e.g., including instructions) that are utilized by one or more components of the processor 102-1, such as the cores 106. For example, the shared cache 108 may locally cache data stored in a memory 114 for faster access by components of the processor 102. In an embodiment, the cache 108 may include a mid-level cache (such as a level 2 (L2), a level 3 (L3), a level 4 (L4), or other levels of cache), a last level cache (LLC), and/or combinations thereof. Moreover, various components of the processor 102-1 may communicate with the shared cache 108 directly, through a bus (e.g., the bus 112), and/or a memory controller or hub. As shown in Fig. 1, in some embodiments, one or more of the cores 106 may include a level 1 (L1) cache 116-1 (generally referred to herein as "L1 cache 116").

In one embodiment, the control unit/logic 120 causes modification to the TRT definition (i.e., relative to ACPI 3.0) and utilizes the modified TRT as a priority table instead of a pure scientific thermal relationship table. In some embodiments, logic 120 may operate based, at least in part, on input from OS software and/or software application(s) (e.g., that may be stored in the memory 114). Moreover, the ability to control the level of power/thermal setting(s) may be used to optimize platform power consumption and/or thermal behavior in response to various determinations such as based on the workload, scenario, usage, temperature, electric current, power consumption, etc. (e.g., based on input from one or more sensors 150 in some embodiments). As illustrated in Fig. 1, sensor(s) 150 may be thermally coupled or otherwise proximate to one or more components that are thermally influenced 151 (also referred to herein as target(s)) to detect variations in temperature that are caused by one or more heat generating components 152 (also referred to herein as source(s)). Furthermore, at least some OS operations discussed herein may be interchangeably performed by software applications, firmware, etc.

Fig. 2 illustrates a block diagram of portions of a processor core 106 and other components of a computing system, according to an embodiment of the invention. In one embodiment, the arrows shown in Fig. 2 illustrate the flow direction of instructions through the core 106. One or more processor cores (such as the processor core 106) may be implemented on a single integrated circuit chip (or die) such as discussed with reference to Fig. 1. Moreover, the chip may
include one or more shared and/or private caches (e.g., cache 108 of Fig. 1), interconnections (e.g., interconnections 104 and/or 112 of Fig. 1), control units, memory controllers, or other components.

As illustrated in Fig. 2, the processor core 106 may include a fetch unit 202 to fetch instructions (including instructions with conditional branches) for execution by the core 106. The instructions may be fetched from any storage devices such as the memory 114 and/or the memory devices discussed with reference to Figs. 4-6. The core 106 may also include a decode unit 204 to decode the fetched instruction. For instance, the decode unit 204 may decode the fetched instruction into a plurality of uops (micro-operations).

Additionally, the core 106 may include a schedule unit 206. The schedule unit 206 may perform various operations associated with storing decoded instructions (e.g., received from the decode unit 204) until the instructions are ready for dispatch, e.g., until all source values of a decoded instruction become available. In one embodiment, the schedule unit 206 may schedule and/or issue (or dispatch) decoded instructions to an execution unit 208 for execution. The execution unit 208 may execute the dispatched instructions after they are decoded (e.g., by the decode unit 204) and dispatched (e.g., by the schedule unit 206). In an embodiment, the execution unit 208 may include more than one execution unit. The execution unit 208 may also perform various arithmetic operations such as addition, subtraction, multiplication, and/or division, and may include one or more arithmetic logic units (ALUs). In an embodiment, a co-processor (not shown) may perform various arithmetic operations in conjunction with the execution unit 208.

Further, the execution unit 208 may execute instructions out-of-order. Hence, the processor core 106 may be an out-of-order processor core in one embodiment. The core 106 may also include a retirement unit 210. The retirement unit 210 may retire executed instructions after they are committed. In an embodiment, retirement of the executed instructions may result in processor state being committed from the execution of the instructions, physical registers used by the instructions being de-allocated, etc.

The core 106 may also include a bus unit 214 to enable communication between components of the processor core 106 and other components (such as the components discussed with reference to Fig. 1) via one or more buses (e.g., buses 104 and/or 112). The core 106 may also include one or more registers 216 to store data accessed by various components of the core 106 (such as values related to power consumption state settings).
Furthermore, even though Fig. 1 illustrates the control unit 120 to be coupled to the core 106 via interconnect 112, in various embodiments the control unit 120 may be located elsewhere such as inside the core 106, coupled to the core via bus 104, etc.

Table 1 below shows the fields in the Thermal Relationship Table (TRT) as defined in the ACPI 3.0 specification.

<table>
<thead>
<tr>
<th>FIELD</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source</td>
<td>Reference to the device that is thermally influencing the target device</td>
</tr>
<tr>
<td>Target</td>
<td>Reference to the device that is being thermally influenced by the source device</td>
</tr>
<tr>
<td>Influence</td>
<td>Thermal influence of source device on the target device, represented as tenths of degrees Kelvin that the source device raises the temperature of the target device per Watt of the thermal load that the source device generates</td>
</tr>
<tr>
<td>Sampling Period</td>
<td>The minimum period of time in tenths of seconds that OSPM (OS directed configuration and Power Management) should wait after applying a passive control to the device indicated by Source Device to determine its impact on the device indicated by Target Device.</td>
</tr>
</tbody>
</table>

Table 1

Some embodiments modify the definition of the "Influence" field in Table 1 to instead be a priority value such that the thermal engineer can intuitively apply a policy to determine the order and priority of various sources. The modified field definitions are as defined in Table 2 below.

<table>
<thead>
<tr>
<th>FIELD</th>
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</thead>
<tbody>
<tr>
<td>Source</td>
<td>Reference to the device that is thermally influencing the target device</td>
</tr>
<tr>
<td>Target</td>
<td>Reference to the device that is being thermally influenced by the</td>
</tr>
<tr>
<td>Priority</td>
<td>Arbitrary number representing the influence priority of the source device on the target device. For example, the higher the value, the more influence the source has on the target (or type of priority, such as the reverse of the aforementioned priority, depending on the implementation). If two entries with same target device reference have the same priority value, then both the sources have equal influence on the target.</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>Sampling Period</td>
<td>The minimum period of time in tenths of seconds that OSPM should wait after applying a passive control to the device indicated by Source Device to determine its impact on the device indicated by Target Device.</td>
</tr>
</tbody>
</table>

Table 2

Fig. 3 illustrates a flow chart of a method 300 used to perform passive thermal control using priority values of a TRT, according to an embodiment. One or more components of Figs. 1-2 or 4-6 (e.g., logic 120) may be used to perform one or more operations discussed with reference to Fig. 3 in various embodiments. Furthermore, operations 308 and 322 in Fig. 3 may be interchanged with other priority policies such as ascending order, descending order, no particular sort order, etc. in some embodiments (e.g., to provide more flexibility for customization).

Referring to Figs. 1-3, at an operation 302, thermal monitoring is started (e.g., using sensor(s) 150 that feed detected temperature values/information to logic 120). At an operation 304, method 300 waits for reaching a threshold value (such as a _PSV (Passive Thermal Trip Point as defined in ACPI specification) value). If the detected temperature exceeds the threshold at operation 306, operation 308 gathers a list of sources for the target device in descending order of priority (e.g., based on the priority field of the TRT). At an operation 310, it is determined whether the highest priority sources limited (e.g., completely) in power/performance. If so, the source or sources are limited with the next highest priority in the list at operation 312; otherwise, source or sources are limited with the highest priority in the list at operation 314.

At operation 306, if the temperature has not exceeded the threshold, an operation 320 determines whether passive policy action is active on any sources. If not, method 300 continues waiting at operation 304; otherwise, an operation 322 gathers a list of (e.g., all) sources for the
target device that are currently passively controlled in ascending order of priority. At an operation 324, (e.g., all) passively controlled source(s) are reduced (or unlimited) by one power/power level. An operation 326 determines whether (e.g., all) passively controlled source(s) are completely unlimited. If so, method 300 resumes with operation 304; otherwise an operation 316 waits for a sampling period of time (e.g., in accordance with the corresponding value stored in the TRT). As shown in Fig. 3, method 300 performs operation 316 after operations 312, 314, and 326.

Using the priority value instead of the original influence value as defined in the TRT object allows a thermal engineer to quickly come up with a relationship table based on the platform component placements and quick analysis of thermal behavior of various targets under various workloads. This may save a significant amount of time in thermal determination and system design. Since the passive control algorithm implementation seeks an appropriate control point using the sampling period information and (e.g., constantly) adjusts performance/power to meet the thermal targets, having a reasonable enough priority value is sufficient and it is not required to have a more accurate influence value in some embodiments. Also, since the priority value can be an arbitrary pre-defined integer value, the resulting passive limiting action and the performance determination is repeatable and predictable over several runs.

In accordance with an embodiment, by making it easier to implement a holistic platform level thermal management solution, thermal behavior of the platform is improved and hence may indirectly help with the resilience avoiding any thermally induced malicious attacks (e.g., running severe workloads, causing unexpected operating conditions to trigger thermal conditions/management etc.).

Fig. 4 illustrates a block diagram of a computing system 400 in accordance with an embodiment of the invention. The computing system 400 may include one or more central processing unit(s) (CPUs) 402 or processors that communicate via an interconnection network (or bus) 404. The processors 402 may include a general purpose processor, a network processor (that processes data communicated over a computer network 403), or other types of a processor (including a reduced instruction set computer (RISC) processor or a complex instruction set computer (CISC)). Moreover, the processors 402 may have a single or multiple core design. The processors 402 with a multiple core design may integrate different types of processor cores on the same integrated circuit (IC) die. Also, the processors 402 with a multiple core design may be implemented as symmetrical or asymmetrical multiprocessors. In an embodiment, one or more
of the processors 402 may be the same or similar to the processors 102 of Fig. 1. For example, one or more of the processors 402 may include the control unit 120 discussed with reference to Figs. 1-3. Also, the operations discussed with reference to Figs. 1-3 may be performed by one or more components of the system 400.

A chipset 406 may also communicate with the interconnection network 404. The chipset 406 may include a memory control hub (MCH) 408. The MCH 408 may include a memory controller 410 that communicates with a memory 412 (which may be the same or similar to the memory 114 of Fig. 1). The memory 412 may store data, including sequences of instructions, that may be executed by the CPU 402, or any other device included in the computing system 400. In one embodiment of the invention, the memory 412 may include one or more volatile storage (or memory) devices such as random access memory (RAM), dynamic RAM (DRAM), synchronous DRAM (SDRAM), static RAM (SRAM), or other types of storage devices. Nonvolatile memory may also be utilized such as a hard disk. Additional devices may communicate via the interconnection network 404, such as multiple CPUs and/or multiple system memories.

The MCH 408 may also include a graphics interface 414 that communicates with a display device 416. In one embodiment of the invention, the graphics interface 414 may communicate with the display device 416 via an accelerated graphics port (AGP). In an embodiment of the invention, the display 416 (such as a flat panel display) may communicate with the graphics interface 414 through, for example, a signal converter that translates a digital representation of an image stored in a storage device such as video memory or system memory into display signals that are interpreted and displayed by the display 416. The display signals produced by the display device may pass through various control devices before being interpreted by and subsequently displayed on the display 416.

A hub interface 418 may allow the MCH 408 and an input/output control hub (ICH) 420 to communicate. The ICH 420 may provide an interface to I/O device(s) that communicate with the computing system 400. The ICH 420 may communicate with a bus 422 through a peripheral bridge (or controller) 424, such as a peripheral component interconnect (PCI) bridge, a universal serial bus (USB) controller, or other types of peripheral bridges or controllers. The bridge 424 may provide a data path between the CPU 402 and peripheral devices. Other types of topologies may be utilized. Also, multiple buses may communicate with the ICH 420, e.g., through multiple bridges or controllers. Moreover, other peripherals in communication with the ICH 420 may
include, in various embodiments of the invention, integrated drive electronics (IDE) or small computer system interface (SCSI) hard drive(s), USB port(s), a keyboard, a mouse, parallel port(s), serial port(s), floppy disk drive(s), digital output support (e.g., digital video interface (DVI)), or other devices.

The bus 422 may communicate with an audio device 426, one or more disk drive(s) 428, and a network interface device 430 (which is in communication with the computer network 403). Other devices may communicate via the bus 422. Also, various components (such as the network interface device 430) may communicate with the MCH 408 in some embodiments of the invention. In addition, the processor 402 and one or more other components discussed herein may be combined to form a single chip (e.g., to provide a System on Chip (SOC)). Furthermore, the graphics accelerator 416 may be included within the MCH 408 in other embodiments of the invention.

Furthermore, the computing system 400 may include volatile and/or nonvolatile memory (or storage). For example, nonvolatile memory may include one or more of the following: read-only memory (ROM), programmable ROM (PROM), erasable PROM (EPROM), electrically EPROM (EEPROM), a disk drive (e.g., 428), a floppy disk, a compact disk ROM (CD-ROM), a digital versatile disk (DVD), flash memory, a magneto-optical disk, or other types of nonvolatile machine-readable media that are capable of storing electronic data (e.g., including instructions).

Fig. 5 illustrates a computing system 500 that is arranged in a point-to-point (PtP) configuration, according to an embodiment of the invention. In particular, Fig. 5 shows a system where processors, memory, and input/output devices are interconnected by a number of point-to-point interfaces. The operations discussed with reference to Figs. 1-4 may be performed by one or more components of the system 500.

As illustrated in Fig. 5, the system 500 may include several processors, of which only two, processors 502 and 504 are shown for clarity. The processors 502 and 504 may each include a local memory controller hub (MCH) 506 and 508 to enable communication with memories 510 and 512. The memories 510 and/or 512 may store various data such as those discussed with reference to the memory 412 of Fig. 4.

In an embodiment, the processors 502 and 504 may be one of the processors 402 discussed with reference to Fig. 4. The processors 502 and 504 may exchange data via a point-to-point (PtP) interface 514 using PtP interface circuits 516 and 518, respectively. Also, the processors...
502 and 504 may each exchange data with a chipset 520 via individual PtP interfaces 522 and 524 using point-to-point interface circuits 526, 528, 530, and 532. The chipset 520 may further exchange data with a graphics circuit 534 via a graphics interface 536, e.g., using a PtP interface circuit 537.

At least one embodiment of the invention may be provided within the processors 502 and 504. For example, the control unit 120 of Figs. 1-4 may be located within the processors 502 and 504. Other embodiments of the invention, however, may exist in other circuits, logic units, or devices within the system 500 of Fig. 5. Furthermore, other embodiments of the invention may be distributed throughout several circuits, logic units, or devices illustrated in Fig. 5.

The chipset 520 may communicate with a bus 540 using a PtP interface circuit 541. The bus 540 may communicate with one or more devices, such as a bus bridge 542 and I/O devices 543. Via a bus 544, the bus bridge 542 may communicate with other devices such as a keyboard/mouse 545, communication devices 546 (such as modems, network interface devices, or other communication devices that may communicate with the computer network 403), audio I/O device 547, and/or a data storage device 548. The data storage device 548 may store code 549 that may be executed by the processors 502 and/or 504.

In some embodiments, one or more of the components discussed herein can be embodied as a System On Chip (SOC) device. Fig. 6 illustrates a block diagram of an SOC package in accordance with an embodiment. As illustrated in Fig. 6, SOC 602 includes one or more Central Processing Unit (CPU) cores 620, one or more Graphics Processor Unit (GPU) cores 630, an Input/Output (I/O) interface 640, and a memory controller 642. Various components of the SOC package 602 may be coupled to an interconnect or bus such as discussed herein with reference to the other figures. Also, the SOC package 602 may include more or less components, such as those discussed herein with reference to the other figures. Further, each component of the SOC package 602 may include one or more other components, e.g., as discussed with reference to the other figures herein. In one embodiment, SOC package 602 (and its components) is provided on one or more Integrated Circuit (IC) die, e.g., which are packaged into a single semiconductor device.

As illustrated in Fig. 6, SOC package 602 is coupled to a memory 660 (which may be similar to or the same as memory discussed herein with reference to the other figures) via the memory controller 642. In an embodiment, the memory 660 (or a portion of it) can be integrated on the SOC package 602.
The I/O interface 640 may be coupled to one or more I/O devices 670, e.g., via an interconnect and/or bus such as discussed herein with reference to other figures. I/O device(s) 670 may include one or more of a keyboard, a mouse, a touchpad, a display, an image/video capture device (such as a camera or camcorder/video recorder), a touch screen, a speaker, or the like. Furthermore, SOC package 602 may include/integrate the logic 120 in an embodiment. Alternatively, the logic 120 may be provided outside of the SOC package 602 (i.e., as a discrete logic).

In various embodiments of the invention, the operations discussed herein, e.g., with reference to Figs. 1-6, may be implemented as hardware (e.g., logic circuitry), software, firmware, or combinations thereof, which may be provided as a computer program product, e.g., including (e.g., a non-transitory) machine-readable or computer-readable medium having stored thereon instructions (or software procedures) used to program a computer to perform a process discussed herein. The machine-readable medium may include a storage device such as those discussed with respect to Figs. 1-6.

Additionally, such computer-readable media may be downloaded as a computer program product, wherein the program may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals embodied in a carrier wave or other propagation medium via a communication link (e.g., a bus, a modem, or a network connection).

Reference in the specification to "one embodiment," "an embodiment," or "some embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiment(s) may be included in at least an implementation. The appearances of the phrase "in one embodiment" in various places in the specification may or may not be all referring to the same embodiment.

Also, in the description and claims, the terms "coupled" and "connected," along with their derivatives, may be used. In some embodiments of the invention, "connected" may be used to indicate that two or more elements are in direct physical or electrical contact with each other. "Coupled" may mean that two or more elements are in direct physical or electrical contact. However, "coupled" may also mean that two or more elements may not be in direct contact with each other, but may still cooperate or interact with each other.

Thus, although embodiments of the invention have been described in language specific to structural features and/or methodological acts, it is to be understood that claimed subject matter
may not be limited to the specific features or acts described. Rather, the specific features and acts are disclosed as sample forms of implementing the claimed subject matter.
CLAIMS

1. An apparatus comprising:
   control logic, the control logic at least partially comprising hardware logic, to
   cause modification to a power consumption limit of one or more components of a platform based
   on one or more thermal relationships between one or more power consuming components of the
   platform and one or more heat generating components of the platform,
   wherein a first relationship of the one or more thermal relationships is to indicate
   an influence priority of a source component of the platform on a target component of the
   platform.

2. The apparatus of claim 1, wherein the one or more heat generating components is to
   comprise the source component.

3. The apparatus of claim 1, wherein the one or more power consuming components is to
   comprise the target component.

4. The apparatus of claim 1, further comprising logic to determine an impact of the
   modification to the power consumption limit after a sampling period of time lapses.

5. The apparatus of claim 1, further comprising memory to store data corresponding to the
   one or more thermal relationships.

6. The apparatus of claim 1, further comprising logic to determine the one or more thermal
   relationships based on input from one or more sensors that are proximate to the one or more
   components of the platform.

7. The apparatus of claim 1, wherein the one or more thermal relationships are to be stored
   in a thermal relationship table at least partially in accordance with Advanced Configuration and
   Power Interface (ACPI) specification.

8. The apparatus of claim 1, wherein the first relationship is to replace a second relationship
   that is to indicate a temperature value corresponding to a thermal influence of the source
   component on the target component.
9. The apparatus of claim 1, further comprising memory to store an operating system software, wherein the operating system software is to trigger the modification to the power limit.

10. The apparatus of claim 1, further comprising memory to store an application software, wherein the application software is to trigger the modification to the power limit.

11. The apparatus of claim 1, wherein the one or more components are to comprise a processor having one or more processor cores.

12. The apparatus of claim 1, wherein one or more of the logic and the one or more components are on a same integrated circuit die.

13. A method comprising:

   causing modification to a power consumption limit of one or more components of a platform based on one or more thermal relationships between one or more power consuming components of the platform and one or more heat generating components of the platform, wherein a first relationship of the one or more thermal relationships indicates an influence priority of a source component of the platform on a target component of the platform.

14. The method of claim 13, further comprising determining an impact of the modification to the power consumption limit after a sampling period of time lapses.

15. The method of claim 13, further comprising storing the one or more thermal relationships in memory.

16. The method of claim 13, further comprising determining the one or more thermal relationships based on input from one or more sensors.

17. A computing system comprising:

   memory to store data corresponding to one or more thermal relationships; a processor coupled to the memory; and control logic, the control logic at least partially comprising hardware logic, to cause modification to a power consumption limit of one or more components of the system based on the one or more thermal relationships between one or more power consuming components of the platform and one or more heat generating components of the platform, wherein a first relationship of the one or more thermal relationships is to indicate
an influence priority of a source component of the platform on a target component of the
platform.

18. The system of claim 17, wherein the one or more heat generating components is to
comprise the source component.

19. The system of claim 17, wherein the one or more power consuming components is to
comprise the target component.

20. The system of claim 17, further comprising logic to determine an impact of the
modification to the power consumption limit after a sampling period of time lapses.

21. The system of claim 17, further comprising logic to determine the one or more thermal
relationships based on input from one or more sensors that are proximate to the one or more
components of the platform.

22. The system of claim 17, wherein the one or more thermal relationships are to be stored in
a thermal relationship table at least partially in accordance with Advanced Configuration and
Power Interface (ACPI) specification.

23. The system of claim 17, wherein the first relationship is to replace a second relationship
that is to indicate a temperature value corresponding to a thermal influence of the source
component on the target component.

24. The system of claim 17, wherein the one or more components are to comprise one or
more processor cores of the processor.

25. The system of claim 17, wherein one or more of the logic and the one or more
components are on a same integrated circuit die.

26. A computer-readable medium to store instructions that when executed by a processor
cause the processor to:

cause modification to a power consumption limit of one or more components of a
platform based on one or more thermal relationships between one or more power consuming
components of the platform and one or more heat generating components of the platform,
wherein a first relationship of the one or more thermal relationships indicates an
influence priority of a source component of the platform on a target component of the platform.
27. The computer-readable medium of claim 26, wherein the instructions are to cause the processor to determine an impact of the modification to the power consumption limit after a sampling period of time lapses.

28. The computer-readable medium of claim 26, wherein the instructions are to cause the processor to store the one or more thermal relationships in memory.

29. The computer-readable medium of claim 26, wherein the instructions are to cause the processor to determine the one or more thermal relationships based on input from one or more sensors.

30. The computer-readable medium of claim 26, wherein the instructions are to cause the processor to replace a second relationship, indicative of a temperature value corresponding to a thermal influence of the source component on the target component, with the first relationship.
FIG. 1

SUBSTITUTE SHEET (RULE 26)
**Fig. 2**

**SUBSTITUTE SHEET (RULE 26)**
FIG. 4
FIG. 6
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

G06F 1/26 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/26; G06F 1/28; G05B 11/01; G06F 1/20; G06F 9/46; G05D 23/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: power consumption limit, priority, thermal management, thermal relationship table, heat, source, target

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<tr>
<th>Category</th>
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<td>A</td>
<td>US 8315746 B2 (KEITH COX et al.) 20 November 2012 See paragraphs [0011], [0015H0016], [0023H0026], [0028H0029], [0033], [0061]-[0062]; claims 1-2, 8-9; and figures 2B-2C, 4.</td>
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<td>US 2012-0173037 AI (GUY M. THERIEN et al.) 05 July 2012 See paragraphs [0002], [0012], [0016]-[0018], [0027]-[0039], [0042], [0046]-[0047]; claims 8, 10-11; and figures 2, 4-5, 7.</td>
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<td>A</td>
<td>KEP 10-2011-0041570 A (INTEL CORPORATION) 21 April 2011 See paragraphs [0001], [0012H0017], [0037 H0039]; claim 1; and figures 1, 3-5.</td>
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</tr>
<tr>
<td>A</td>
<td>EP 1965288 A2 (COOLIT SYSTEMS INC.) 03 Sept ember 2008 See paragraphs [0001], [0004H0005], [0037H0039]; and figures 2-4.</td>
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</tr>
<tr>
<td>A</td>
<td>US 2012-0216065 AI (DENILSON NASTACIO) 23 August 2012 See paragraphs [0003], [0008], [0032]-[0041], [0051]-[0080]; and figures 1, 3-4.</td>
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Further documents are listed in the continuation of Box C. See patent family annex.

Date of the actual completion of the international search: 08 October 2013 (08. 10.2013)

Date of mailing of the international search report: 09 October 2013 (09.10.2013)

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<th>Publication date</th>
<th>Patent family member(s)</th>
<th>Publication date</th>
</tr>
</thead>
<tbody>
<tr>
<td>US 8315746 B2</td>
<td>20/11/2012</td>
<td>CN 102099761 A</td>
<td>15/06/2011</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EP 2294497 A</td>
<td>16/03/2011</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 2009-0299543 Al</td>
<td>03/12/2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 2013-041513 Al</td>
<td>14/02/2013</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 2009-148710 Al</td>
<td>10/12/2009</td>
</tr>
<tr>
<td>US 2012-0173037 Al</td>
<td>05/07/2012</td>
<td>CN 100429605 C</td>
<td>29/10/2008</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CN 1957317 A</td>
<td>02/05/2007</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EP 1763723 A2</td>
<td>21/03/2007</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 1292689 B</td>
<td>11/01/2008</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 2005-288886 Al</td>
<td>29/12/2005</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 2009-099807 Al</td>
<td>16/04/2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 7467059 B2</td>
<td>16/12/2008</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 8135559 B2</td>
<td>13/03/2012</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 2006-011992 A2</td>
<td>02/02/2006</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 2009-535722 A</td>
<td>01/10/2009</td>
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<tr>
<td></td>
<td></td>
<td>US 2008-0011467 Al</td>
<td>17/01/2008</td>
</tr>
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<td>EP 1965288 A2</td>
<td>03/09/2008</td>
<td>CA 2573941 Al</td>
<td>15/07/2008</td>
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<tr>
<td></td>
<td></td>
<td>EP 1965288 A3</td>
<td>30/09/2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 2008-0186670 Al</td>
<td>07/08/2008</td>
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<td></td>
<td></td>
<td>US 7991515 B2</td>
<td>02/08/2011</td>
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<tr>
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<td></td>
<td>US 8457807 B2</td>
<td>04/06/2013</td>
</tr>
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