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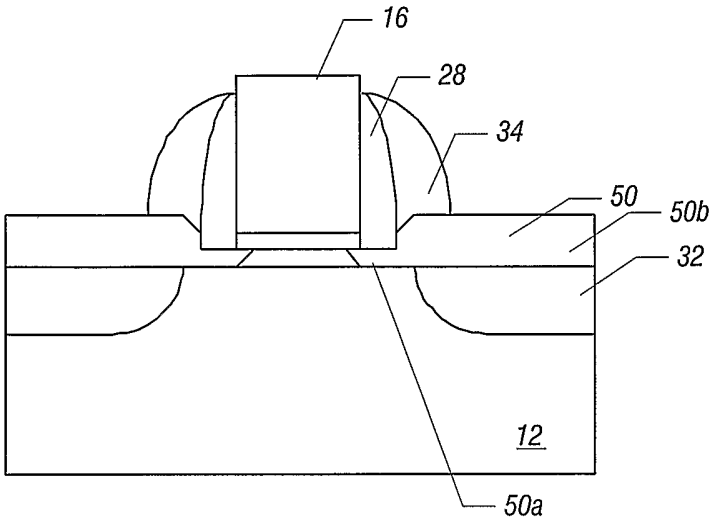
(54) Title: EPITAXIALLY DEPOSITED SOURCE/DRAIN



(57) Abstract: An epitaxially deposited source/drain extension may be formed for a metal oxide semiconductor field effect transistor. A sacrificial layer may be formed and etched away to undercut under the gate electrode. Then a source/drain extension of epitaxial silicon may be deposited to extend under the edges of the gate electrode. As a result, the extent by which the source/drain extension extends under the gate may be controlled by controlling the etching of the sacrificial material. Its thickness and depth may be controlled by controlling the deposition process. Moreover, the characteristics of the source/drain, extension may be controlled independently of those of the subsequently formed deep or heavily doped source/drain junction.

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EPITAXIALLY DEPOSITED SOURCE/DRAIN

Background

This invention relates generally to metal oxide semiconductor field effect transistors.

Metal oxide semiconductor field effect transistors include a gate that is self-aligned with a source/drain. The source/drain may include a deeper or heavily doped region and a shallower and lightly doped region, sometimes called a tip or source/drain extension.

Gate underlap is the amount by which the source/drain material diffuses under the gate after ion implantation and subsequent heat processing. After implantation, the material that is implanted is exposed to heat which causes the material to move downwardly into the substrate and, to a lesser extent, laterally under the gate. Thus, in a system using an ion implanted source/drain extension, the amount of underdiffusion is determined as a function of junction depth.

It is desirable to have relatively shallow junction depth for the source/drain extension to support smaller transistor dimensions. Usually, in source/drain extension implantation techniques, the minimum tip junction depths are determined by the necessary gate underlap.

The shallower the source/drain extension, generally the shorter the gate lengths that may be utilized without increasing off-state leakage currents. Extension doping under the gate edge is needed to ensure a low resistance path between the inversion layer under the gate and the highly doped source/drain extension region. The low resistance is needed for a high drive currents, which are critical for high circuit switching speeds.

Thus, there is a need for better ways to make source/drain junctions of field effect transistors.

Brief Description of the Drawings

Figure 1 is a greatly enlarged, cross-sectional view at one stage of manufacture;

Figure 2 is an enlarged, cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

Figure 3 is an enlarged, cross-sectional view at still a subsequent stage of manufacture in accordance with one embodiment of the present invention;

Figure 4 is an enlarged, cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention; and

Figure 5 is an enlarged, cross-sectional view at still a subsequent stage of manufacture in accordance with one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a heavily doped semiconductor substrate 12 may be covered by a sacrificial, undoped, or lightly doped epitaxial silicon layer 18. The layer 18 may be less than 500 Angstroms thick in one embodiment. A gate electrode structure including a gate 16 formed over a gate dielectric 14 may be defined on the epitaxial silicon layer 18.

The selective deposition of the sacrificial epitaxial silicon layer 18 may be carried out, for example, using dichlorosilane-based chemistry in a single wafer chemical vapor deposition reactor, such as an Epsilon 3000 epitaxial reactor, available from ASM International NV, Bilthoven, Netherlands. The film may be deposited with gas flows of 150-200sccm of dichlorosilane, 100-150sccm of HCl, 20slm of H_2 at 825°C in a processed pressure of 20Torr. Under these processing conditions, a deposition rate of 10-15 nanometers per minute may be achieved for silicon on exposed substrate

while achieving selectivity to spacer and oxide regions. Other deposition techniques may also be used.

The arrangement shown in Figure 1 is sometimes called a delta doped transistor. Because there is relatively high doping below the epitaxial layer 18, a large delta or change in concentration occurs at the interface between the substrate 12 and the epitaxial silicon layer 18.

The structure shown in Figure 1 may be covered by a spacer material and then anisotropically etched to form the sidewall spacers 28 shown in Figure 2. Some limited etching of the epitaxial silicon 18 may occur at the same time depending on the selectivity of the spacer etch.

After spacer formation, a selective wet etch may remove the exposed portions of the epitaxial silicon layer 18 and may continue etching under the gate 16 to achieve the undercut structure shown in Figure 3. The extent of gate 16 undercut can be controlled by adjusting the etch time.

The epitaxial silicon layer 18 may be selectively etched with a variety of hydroxide-based solutions, for example. However, for high selectivity of the undoped or lightly doped layer 18 to the heavily doped substrate 12, relatively mild processing conditions may be employed.

In one embodiment, an aqueous ammonium hydroxide solution in the concentration range of 2 to 10 percent by volume at 20°C may be used together with sonication. The sonication may be provided by a transducer that dissipates ultra or megasonic energy with a power of .5 to 5 watts per cm^2 in one embodiment of the present invention. Since the delta doped transistor has a heavily doped region below the undoped region, it may serve as an etch stop layer for the wet etch.

After the wet etch undercut, a doped selective epitaxial silicon layer 50 may be grown. A shallow, highly

doped source/drain extension 50a laterally extends the desired distance under the gate 16 edge and the sidewall spacer 28, as shown in Figure 4. A thicker source/drain region 50b is aligned with the edge of the spacer 28 and extends away from the spacer 28. The spacer 28 enables the length of the extension 50a to be tailored and allows the thickness of the layer 50 to expand without shorting to the gate 16. The thicker region 50b reduces resistance of the region 50 and brings the lower resistance region close to the edge of the gate 16.

In forming the P-type MOS (PMOS) transistor, the source/drain extension 50a and raised source/drain 50b may be formed by selectively depositing epitaxial boron doped silicon or silicon germanium with a germanium concentration of up to 30 percent, as one example. Under the processing conditions of 100sccm of dichlorosilane, 20slm H_2, 750-800°C, 20Torr, 150-200sccm HCl, diborane flow of 150-200sccm and GeH_4 flow of 150-200sccm, a highly doped silicon germanium film with a deposition rate of 20 nanometers per minute, a boron concentration of 1E20 cm^{-3}, and a germanium concentration of 20 percent may be achieved in one embodiment. A low resistivity of 0.7-0.9 mOhm-cm results from the high boron concentration of the film.

Low resistivity provide the benefit of high conductivity in the extension and source/drain regions in some embodiments. This lowered resistivity may reduce the external resistance. The larger unit cell of the silicon germanium present in source/drain regions 50b may exert compressive strain on the channel, which in turn may result in enhanced mobility and transistor performance in some embodiments.

In the N-type transistor (NMOS), the source/drain 50b and source/drain extension 50a may be formed using *in situ*

phosphorus doped silicon deposited in one embodiment. The silicon may be deposited selectively under processing conditions of 100sccm of dichlorosilane, 25-50sccm HCl, 200-300sccm of 1 percent PH_3 with a H_2 gas carrier flow of 20slm at 750°C and 20Torr. A phosphorous concentration of 2E20 cm^{-3} with a resistivity of 0.4-0.6 mOhm-cm may be achieved in the deposited film in one embodiment.

Thereafter, a second thin spacer 34 may be formed using conventional techniques as shown in Figure 5. A deep source/drain 32 may be formed by ion implantation using the spacers 28 and 34 and the gate 16 as a mask. The annealing of the deep source/drain 32 may be done in a way that reduces or minimizes the dopant diffusion including the dopant in the layer 50.

The characteristics of the shallow source/drain extensions 50a and the degree by which they underlap the gate 16 may be independent of the characteristics of the deep source/drain junction 32. The extent of extension underlap of the gate 16 of the source/drain extension 50a may be controlled as desired.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. A method comprising:

forming a metal oxide semiconductor field effect transistor having an epitaxially deposited source/drain that extends under the edges of a gate electrode.

2. The method of claim 1 including forming a source/drain extension that extends under the edges of a gate electrode.

3. The method of claim 1 including forming a sacrificial epitaxially deposited material over a substrate and forming a gate electrode over said epitaxially deposited layer.

4. The method of claim 3 wherein forming a sacrificial epitaxially deposited material includes epitaxially depositing a silicon material.

5. The method of claim 3 including selectively etching said epitaxially deposited material.

6. The method of claim 5 including using sonication to selectively etch said material.

7. The method of claim 3 including forming a sidewall spacer on said gate electrode and etching under said sidewall spacer.

8. The method of claim 5 including selectively etching said epitaxially deposited material so as to undercut said gate electrode.

9. The method of claim 8 including depositing an epitaxial material on said substrate and extending under said gate electrode.

10. The method of claim 9 including forming a doped epitaxial material.

11. The method of claim 8 including forming said epitaxial material to be thinner near the gate electrode and thicker spaced from said gate electrode.

12. The method of claim 1 including forming a delta doped transistor.

13. A field effect transistor comprising:

a substrate;

a doped epitaxial semiconductor material formed over said substrate; and

a gate electrode formed over said doped epitaxial semiconductor material, said doped epitaxial semiconductor material extending under said gate electrode.

14. The transistor of claim 13 including a source/drain having a source/drain extension, said source/drain extension being formed of said doped epitaxial semiconductor material and extends under the edges of the gate electrode.

15. The transistor of claim 14 wherein said material has a first thickness near said gate electrode and a second thickness spaced from said gate electrode, said second thickness being greater than said first thickness.

16. The transistor of claim 15 including a sidewall spacer, said material extending under said sidewall spacer.

17. The transistor of claim 16 wherein said second thickness is aligned with said sidewall spacer.

18. The transistor of claim 13 wherein said transistor is a delta doped transistor.

19. The transistor of claim 13 including an ion implanted source/drain under said doped epitaxial semiconductor material.

20. A method comprising:

forming a epitaxial semiconductor layer over a semiconductor substrate wherein the epitaxial semiconductor layer has a lower doping concentration than the substrate;

forming a gate structure including a gate electrode and a sidewall spacer over said epitaxial semiconductor layer; and

selectively etching the exposed portion of said epitaxial semiconductor layer as well as a portion of said epitaxial semiconductor layer under said gate electrode.

21. The method of claim 20 including epitaxially depositing a doped semiconductor material over said substrate to fill the region under said gate electrode and under said sidewall spacer.

22. The method of claim 21 wherein said epitaxial semiconductor layer has a first thickness under said gate electrode and a second thickness spaced from said gate electrode.

23. The method of claim 22 including forming said second thickness in alignment with said spacer.

24. The method of claim 20 including forming a deep source/drain region by ion implantation.

25. The method of claim 20 including forming said epitaxial semiconductor layer extending under said gate electrode and having a greater thickness outbound of said gate electrode and a lesser thickness under said gate electrode.

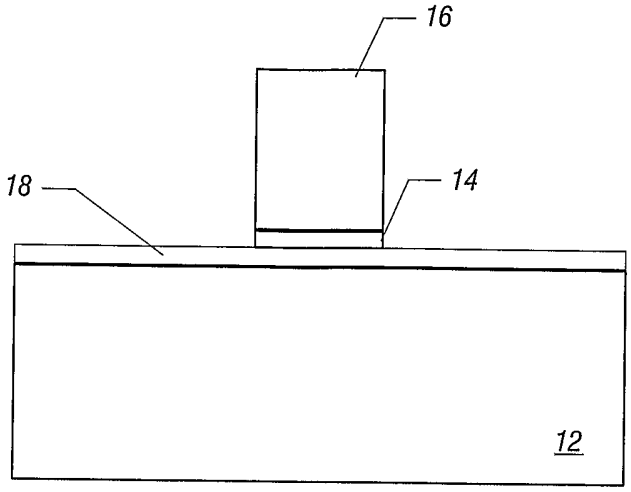

FIG. 1

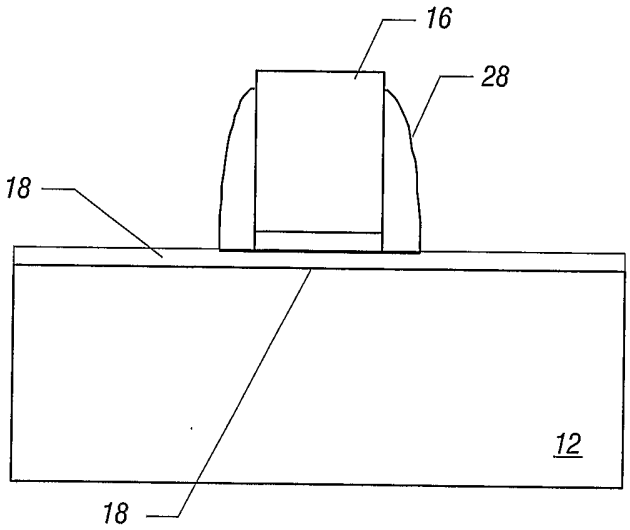

FIG. 2

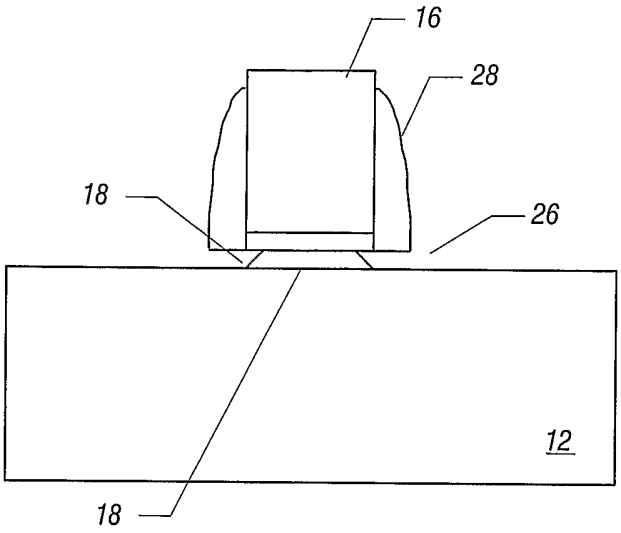

FIG. 3

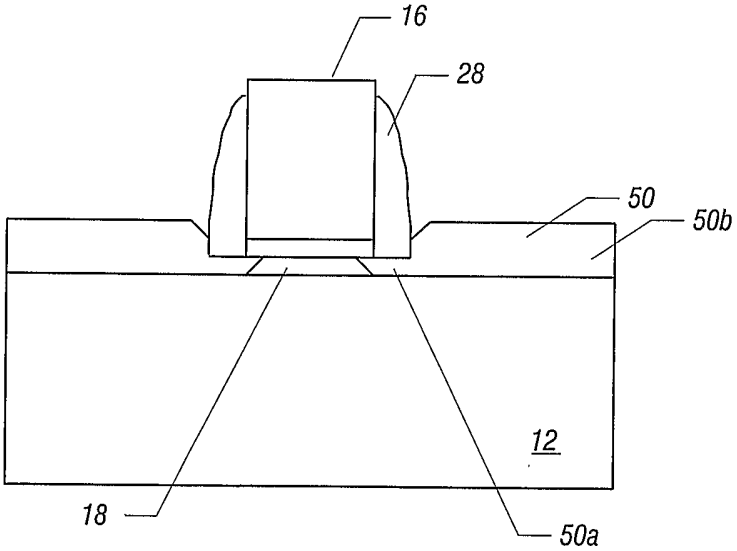

FIG. 4

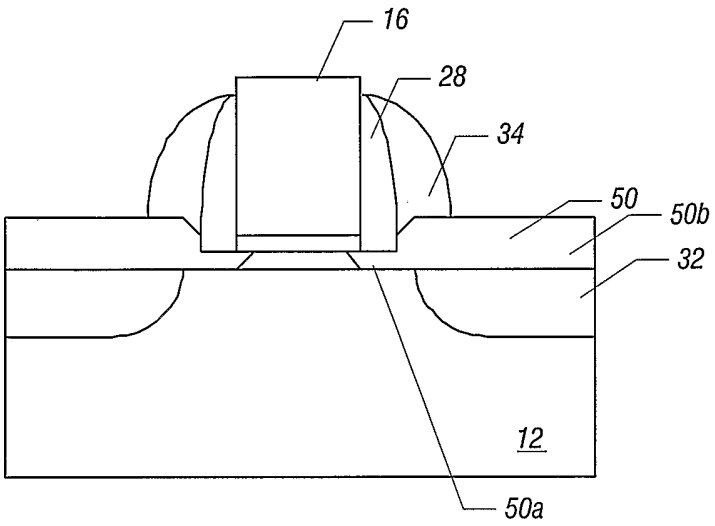

FIG. 5

INTERNATIONAL SEARCH REPORT

International Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
X A	US 6 214 679 B1 (MURTHY ANAND ET AL) 10 April 2001 (2001-04-10) column 3, line 34 - column 9, line 20	1-11, 13-17,19 20-23,25
X	WO 00/30169 A (INTEL CORPORATION; MURTHY, ANAND, S; CHAU, ROBERT, S; MORROW, PATRICK;) 25 May 2000 (2000-05-25) pages 6-14	1,2, 13-17
X A	US 6 605 498 B1 (MURTHY ANAND S ET AL) 12 August 2003 (2003-08-12) figures 5,6	1,2,13, 14 20,21
X	US 6 342 421 B1 (MITANI YUICHIRO ET AL) 29 January 2002 (2002-01-29) figure 21	1,2, 13-17

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[X] Further documents are listed in the continuation of box C

[X] Patent family members are listed in annex

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Date of the actual completion of the international search	Date of mailing of the international search report
30 March 2005	06/04/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P B 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Gélébart, J

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/035204

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
X	PATENT ABSTRACTS OF JAPAN vol. 012, no. 217 (E-624), 21 June 1988 (1988-06-21) & JP 63 013379 A (NIPPON TELEGR & TELEPH CORP <NTT>), 20 January 1988 (1988-01-20) abstract	1,2, 13-17
X	GANNAVARAM S ET AL: "LOW TEMPERATURE (800oC) RECESSED JUNCTION SELECTIVE SILICON-GERMANIUM SOURCE/DRAIN TECHNOLOGY FOR SUB-70 NM CMOS" INTERNATIONAL ELECTRON DEVICES MEETING 2000. IEDM. TECHNICAL DIGEST. SAN FRANCISCO, CA, DEC. 10 - 13, 2000, NEW YORK, NY : IEEE, US, 10 December 2000 (2000-12-10), pages 437-440, XP000988876 ISBN: 0-7803-6439-2 the whole document	1,2, 13-17

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US2004/035204

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6214679 B1	10-04-2001	NONE	
WO 0030169 A	25-05-2000	AU 1470200 A	05-06-2000
		EP 1147552 A1	24-10-2001
		JP 2002530864 T	17-09-2002
		WO 0030169 A1	25-05-2000
		US 2005012146 A1	20-01-2005
US 6605498 B1	12-08-2003	NONE	
US 6342421 B1	29-01-2002	JP 8153688 A	11-06-1996
		US 5864161 A	26-01-1999
JP 63013379 A	20-01-1988	NONE	