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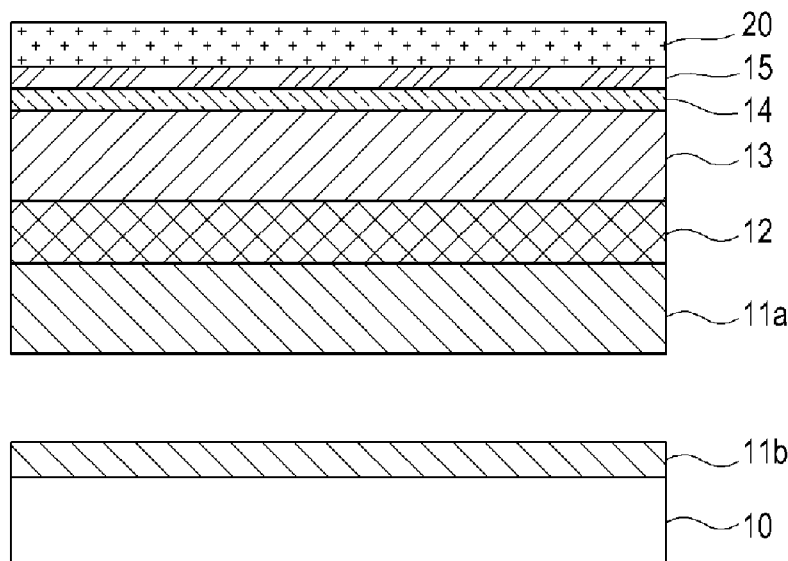
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[Continued on next page]

(54) Title: LIGHT EMITTING DEVICE WITH SUBSTRATE SEPARATION BY ION IMPLANTATION

[Fig. 4]

(57) Abstract: Embodiments of a method
for forming a light emitting device are dis-
closed. This method includes forming a
stacked structure including a substrate, a
lower semiconductor layer of a first conduc-
tivity type, an active layer, and an upper
semiconductor layer of a second conduc-
tivity type, wherein the stacked structure in-
cludes a separation layer formed below the
active layer by ion implantation, and per-
forming a thermal process upon the stacked
structure to divide the separation layer later-
ally such that the stacked structure is sepa-
rated into an upper part and a lower part.
The light emitting device may be fabricated
with substrate separation by ion implanta-
tion to prevent cracking and enable fabrica-
tion of a large size light emitting device
having high efficiency at low costs.

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Description

LIGHT EMITTING DEVICE WITH SUBSTRATE SEPARATION BY ION IMPLANTATION

Technical Field

- [1] The present disclosure relates to a light emitting device, more particularly, to a method of forming a light emitting device using substrate separation by ion implantation.

Background Art

- [2] A light emitting diode (LED), as a representative example of a light emitting device, is formed with compound semiconductor materials suitable for emitting green, blue or ultraviolet light. In order to form the LED, a semiconductor layer of a first conductivity type, an active layer, and a semiconductor layer of a second conductivity type are formed one after another on a substrate. An electrode of the first conductivity type (a first electrode) and another electrode of the second conductivity type (a second electrode) are formed. If the substrate is a dielectric, the semiconductor layer of the second conductivity type and the active layer are selectively etched to expose a part of the semiconductor layer of the first conductivity type. The first and second electrodes are respectively formed on the exposed part of the semiconductor layer of the first conductivity type and the semiconductor layer of the second conductivity type. In this fashion, the conventional horizontal structure LED may be formed.
- [3] In the horizontal structure LED, the area of the first electrode that does not emit light causes loss in effective light emitting areas. When a large current is applied to the device, the effect of current crowding appears around the first electrode, which generates excessive heat. The heat cannot be sufficiently emitted due to the low thermal conductivity of the dielectric substrate, notably degrading the performance of the device. Furthermore, defects are generated in the semiconductor layer of the first conductivity type due to the difference in lattice constants of the substrate and the semiconductor layer of the first conductivity type. Thus, a thick buffer layer is required on the substrate to reduce the defects. The difference in the coefficients of thermal expansion between the substrate and the first semiconductor layer causes the substrate to bend. Thus, it is difficult to process a large size wafer having a diameter of more than 2 inches.
- [4] To prevent the loss in effective light emitting area, which is caused in the horizontal structure of the LED, a vertical structure LED has been proposed using a conductive SiC substrate, where two electrodes are vertically located on opposite sides of the substrate. However, the LED using the conductive SiC substrate fails to provide

solutions to the fundamental problems such as the generation of defects in the semiconductor layer formed on the substrate and bending of the wafer.

- [5] Further, in the conventional fabrication process for forming the vertical structure LED, a metal reflecting layer may be formed over the grown epilayers. A conductive bonding layer may be formed on the metal reflecting layer to bond a conductive substrate to the metal reflecting layer, and the substrate may be lifted off by laser irradiation (Laser Lift Off, LLO). The vertical structure LED formed with the LLO method has improved luminous efficiency, radiation property and electrostatic tolerance.
- [6] The vertical structure LED also has a smaller chip area, compared to the horizontal structure LED. Nevertheless, the vertical structure LED fabricated by LLO process is still confronted with the same problems as associated with the horizontal structure, such as the defects due to the lattice mismatch, a thick buffer layer, difficulty in using a large size substrate, and so on. In addition, physical impact may be imposed to the interface between the substrate and the semiconductor layer during the LLO process. This physical impact causes cracks in the semiconductor layer, and the performance and reliability of the device may be degraded.

Disclosure of Invention

Technical Solution

- [7] A method of forming a light emitting device using substrate separation by ion implantation is provided. Embodiments forming a light emitting device are disclosed herein. In one embodiment, by way of a non-limiting example, a method of forming a light emitting device includes forming a stacked structure including a substrate, a lower semiconductor layer of a first conductivity type, an active layer, and an upper semiconductor layer of a second conductivity type, wherein the stacked structure includes a separation layer formed below the active layer; and performing a thermal process upon the stacked structure to divide the separation layer laterally such that the stack structure is separated into an upper part and a lower part.
- [8] In another embodiment, the forming of the stacked structure includes forming the lower semiconductor layer of the first conductivity type on a substrate, forming the active layer on the lower semiconductor layer, forming the upper semiconductor layer of the second conductivity type on the active layer; and forming the separation layer by implanting ions into the substrate or the lower semiconductor layer.
- [9] In another embodiment, forming the stacked structure includes forming the separation layer by implanting ions into the substrate; and sequentially forming the lower semiconductor layer of the first conductivity type, the active layer and the upper semiconductor layer of the second conductivity type on the substrate having the

separation layer formed therein. The forming of the separation layer further includes forming an ion implantation mask covering an edge of the substrate; forming the separation layer by implanting the ions on portions of the substrate not covered by the mask and wherein ions are not implanted in portions of the substrate covered by the mask; and removing the ion implantation mask after the ion implantation. A cutting process or etching along a base line extended from a border between the separation layer and the non-implantation area is performed after separating the stacked structure into the upper part and the lower part through the thermal process.

Advantageous Effects

- [10] A vertical structure light emitting device can be formed without using conventional laser lift off (LLO) processes, so that no mechanical impact may be imposed, thus making no cracks, increasing device yields, and improving reliability. A semiconductor substrate may be reused, and the fabrication cost may be drastically reduced.

Brief Description of Drawings

- [11] Figs. 1 to 5 are cross sectional views showing a process of forming a vertical structure light emitting device in accordance with a first embodiment.
- [12] Figs. 6 to 11 are cross sectional views showing a process of forming a vertical structure light emitting device in accordance with a second embodiment.

Best Mode for Carrying out the Invention

- [13] One aspect of the present invention relates to a method of forming a vertical structure light emitting device. In the method, a lower semiconductor layer of a first conductivity type, an active layer, and an upper semiconductor layer of a second conductivity type may be stacked on a substrate to form a stacked structure. A separation layer may be formed in an area beneath the active layer. A thermal process may be performed to divide the separation layer SL1 laterally such that the stacked structure is separated into an upper part and a lower part.
- [14] In another aspect of the present invention, a separation layer may be formed in a substrate by implanting ions at a predetermined depth before epilayer growth. The substrate including the separation layer may constitute a stacked structure together with semiconductor layers laminated on the growth substrate by crystal growth processes. A thermal process may be performed to divide the stacked structure so that it is separated laterally into an upper part and a lower part. A thermal process for forming Ohmic contact may unintentionally induce such separation.

Mode for the Invention

- [15] A detailed description is provided below with reference to the accompanying drawings. One of ordinary skill in the art may realize that the following description is illustrative only and is not in any way limiting. Other embodiments of the present

invention may readily suggest themselves to such skilled persons having the benefit of this disclosure.

[16]

[17] First Embodiment

[18] Layers of thin films constituting a light emitting device may be formed on a substrate to configure a stacked structure. An ion implantation process may be performed to implant ions at a depth where a separation layer is to be formed. A conductive layer may be formed on the top of the stacked structure for reflection and/or Ohmic contact. A thermal process may be further performed to cause lateral separation in the layer to which the ions have been implanted, i.e., in the separation layer to separate the stacked structure into an upper part and a lower part. A fundamental light emitting device structure may be formed with the separated upper part of the stacked structure. A process of forming electrodes for applying currents to the fundamental light emitting device structure may also be performed.

[19] Hereinafter, a first embodiment will be described in more detail with reference to Figs. 1 to 5.

[20] As shown in Fig. 1, a lower semiconductor layer 11 of a first conductivity type, an active layer 12, and an upper semiconductor layer 13 of a second conductivity type may be sequentially grown on a substrate 10. The lower semiconductor layer 11, the active layer 12, and the upper semiconductor layer 13 may constitute the basic structure of the light emitting device. In one embodiment of the invention, the growth substrate 10 may be selected from the group consisting essentially of a sapphire substrate, a SiC substrate, a sapphire substrate having a GaN-based semiconductor layer laminated thereon, a SiC substrate having a GaN-based semiconductor layer laminated thereon, and a GaN substrate. If the substrate having the GaN-based semiconductor layer is adopted as the substrate 10, the lower semiconductor layer 11 and the upper semiconductor layer 13 may be formed with the GaN-based semiconductor layers to prevent generation of defects due to a difference in the lattice constants. In the event that the lower semiconductor 11 is an n-type semiconductor, the upper semiconductor 13 may be a p-type semiconductor, while in the event that the lower semiconductor 11 is a p-type semiconductor, the upper semiconductor 13 may be an n-type semiconductor. The "GaN-based" semiconductor may be represented as $\text{Al}_x\text{Ga}_y\text{In}_{(1-x-y)}\text{N}$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$ and $0 \leq x+y \leq 1$), and may include compound semiconductor materials suitable for emitting green, blue or ultraviolet light.

[21] Next, as shown in Fig. 2, a separation layer SL1 may be formed by accelerating and implanting ions at a desired depth from the surface of the upper semiconductor layer 13. While Fig. 2 illustrates an example of forming the separation layer SL1 within the lower semiconductor layer 11, the separation layer SL1 may be formed within the

growth substrate 10 in accordance with another embodiment. In the ion implantation process, acceleration energy of the ions may be determined by the depth from the surface of the upper semiconductor 13 to the position where the separation layer SL1 is to be formed, and the type of ions used. In this embodiment, ions of light chemical elements, whose atomic numbers are 54 or less, are implanted with an acceleration energy ranging from 100 KeV to 10 MeV, thereby forming separation layer SL1 within the lower semiconductor layer 11 or the growth substrate 10.

[22] The stack structure formed in accordance with the processes of Figs. 1 and 2 may include growth substrate 10, lower semiconductor layer 11, active layer 12, and upper semiconductor layer 13, which are formed on growth substrate 10. The stacked structure also may include separation layer SL1 formed in the lower area (lower semiconductor layer 11 or growth layer 10) which is lower than active layer 12.

[23] With reference to Fig. 3, an Ohmic contact layer 14 and a metal layer 15 for reflecting light are formed on the upper semiconductor layer 13, and a conductive substrate 20 may be joined to the metal layer 15. In this embodiment, the metal layer 15 may be at least one film of one metal selected from the group consisting essentially of Cu, Al, Au, Pd, Ti, In, Ni and Pt or an alloy film of at least two metals selected from the above-mentioned group. Conductive substrate 20 may be made of a low-priced semiconductor or metal substrate having a high heat transmission coefficient, such as Si, Cu and Al, or an alloy substrate whose composition can be adjusted to have the same thermal expansion coefficient as the GaN semiconductor layer. A conductive transparent electrode of Indium Tin Oxide (ITO) may be used as the Ohmic contact layer 14. However, the Ohmic contact layer 14 may be omitted in some embodiments if metal layer 15 has sufficient Ohmic contact characteristics.

[24] The stacked structure formed in accordance with the processes of Figs. 1 to 2 may include growth substrate 10, lower semiconductor layer 11, active layer 12, upper semiconductor layer 13 and separation layer SL1 which is formed in the lower area (lower semiconductor layer 11 or growth layer 10), which is lower than active layer 12. According to Fig. 3, the stacked structure may further include Ohmic contact layer 14, metal layer 15 and conductive layer 20.

[25] A thermal process may be applied to the stacked structure in accordance with the processes illustrated in Figs. 1 and 2 or in accordance with the processes illustrated in Figs. 1 to 3, in order to divide the separation layer SL1 laterally such that the stack structure is separated into an upper part and a lower part. The thermal process includes a heating process or a process involving heating. The heating process may be applied to the stacked structure at a temperature ranging from 100°C to 1000°C, so that the lower semiconductor layer 11 may be separated along the separation layer SL1 into a first lower semiconductor layer 11a and a second lower semiconductor 11b, as shown

in Fig. 4.

[26] Meanwhile, the separation along the separation layer SL1 may be accomplished by the heating process for the Ohmic contact only if the heating process can supply sufficient heat for separation.

[27] Referring to Fig. 5, an electrical contact pad 16 may be formed on a surface of the first lower semiconductor layer 11a, which is exposed by the separation process. A transparent electrode (not illustrated) may be formed on the surface of the first lower semiconductor layer 11a. In this case, the electrical contact pad 16 may be formed on the transparent electrode. Further, in order to improve light emission efficiency, a roughening process may be performed upon the surface of the first lower semiconductor layer 11a before forming the transparent electrode or the electrical contact pad 16. The stacked layers from the first lower semiconductor layer 11a to the electrical contact pad 16 are diced into the individual chips and packaged into a lamp or SMD (surface mount device) form.

[28] In the semiconductor light emitting device formed in accordance with the aforementioned embodiment, the conductive substrate 20 and the transparent electrode (or the electrical contact pad 16) function as an n (or p)- type electrode and a p (or n)-type electrode, respectively. Light may be generated in the active layer 12 by the combination of the electrons and the holes when a voltage is applied to each end of the electrodes. The generated light may be emitted in the direction of all solid angle. The light emitted from the active layer 12 in the direction of the conductive layer 20 may be reflected toward and emitted through the surface of the first lower semiconductor layer 11a, with the result that optical power output may increase.

[29] The growth substrate 10 and the second lower semiconductor layer 11b remaining thereon may be reused as a growth substrate to form another vertical semiconductor light emitting device. The loss of the growth substrates can be prevented when fabricating the light emitting devices. Especially when using high-priced growth substrates such as a GaN substrate, the manufacturing costs can be remarkably reduced owing to the reuse of the growth substrate 10.

[30] Furthermore, when subsequently manufacturing a vertical structure light emitting device, the same kind of thin film having no defects can be grown on the second lower semiconductor layer 11b, which enables repeated manufacture of the vertical structure light emitting devices with high efficiency at lower costs. In this case, if the second lower semiconductor 11b has a rough surface, polishing may be performed upon the second lower semiconductor layer 11b before reuse.

[31]

[32] Second Embodiment

[33] Hereinafter, a second embodiment will be described with reference to Figs. 6 to 11.

- [34] As shown in Fig. 6, a separation layer SL2 may be formed by implanting ions into a growth substrate 30. Ion implanting energy may be adjusted to be approximately in the range of 1 keV to 10 MeV so that separation layer SL2 may be formed at the depth ranging from about 10 nm to 10,000 nm from the surface of the growth substrate 30. The growth substrate 30 may be selected from the group consisting essentially of a sapphire substrate, a SiC substrate, a sapphire substrate having a GaN-based semiconductor layer laminated thereon, a SiC substrate having a GaN-based semiconductor layer laminated thereon and a GaN substrate. The implanted ions may be at least one kind of light chemical element, whose atomic numbers are 54 or less. To prevent the upper part of the separation layer SL2 from being separated during the subsequent crystal growing process, implanting ions at the edge of growth substrate 30 may not be necessary. For example, as illustrated in Fig. 6, the edge area A of the growth substrate 30 may be covered with an ion implantation mask M. The mask M may be removed after finishing the ion implantation. A device such as a chuck for holding the growth substrate 30 may function as the ion implantation mask M while implanting ions.
- [35] Subsequently, as shown in Fig. 7, in one embodiment a lower semiconductor layer 31 of a first conductivity type, an active layer 32 and an upper semiconductor layer 33 of a second conductivity type may be sequentially formed on the growth substrate 30 in which the separation layer SL2 has been formed. If the lower semiconductor layer 31 is an n-type, the upper semiconductor layer 33 is a p-type. Or, if the lower semiconductor layer 31 is a p-type, the upper semiconductor layer 33 is an n-type. If the substrate having the GaN-based semiconductor layer is adopted as the growth substrate 30, a lower semiconductor layer 31 and an upper semiconductor layer 33 may be formed with the GaN-based semiconductor layers to thereby prevent generation of the defects due to a difference in the lattice constants. The "GaN-based" semiconductor may be represented as $Al_xGa_yIn_{(1-x-y)}N$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq x+y \leq 1$), and may include compound semiconductor materials suitable for emitting light in green, blue or ultraviolet light.
- [36] The stacked structure formed according to the processes of Figs. 6 and 7 may include the growth substrate 30, the lower semiconductor layer 31, the active layer 32 and the upper semiconductor layer 33, which are formed one after another on the growth substrate 30 in which the separation layer SL2 is formed. The separation layer SL2 may exist in the lower area (the growth substrate 30), which is lower than the active layer 32 similar to the first embodiment.
- [37] Referring to Fig. 8, an Ohmic contact layer 34 and a metal layer 35 for reflecting light are formed on top of the upper semiconductor layer 33. The metal layer 35 in one embodiment may be formed of at least one film of one metal selected from the group consisting essentially of Cu, Al, Au, Pd, Ti, In, Ni and Pt or an alloy film of at least

two metals selected from the above-mentioned group. An ITO type conductive transparent electrode may be used as the Ohmic contact layer 34, which however may be omitted if the metal layer 35 has sufficient Ohmic contact characteristics. A conductive substrate 40 may be joined to the metal layer 35, as shown in Fig. 9. A low-priced semiconductor or metal substrate having a high heat transmission rate, such as Si, Cu and Al, or an alloy substrate whose composition can be adjusted to have the same thermal expansion coefficient as the GaN semiconductor layer, may be employed as the conductive substrate 40. An end portion of the conductive substrate 40 may be positioned at lines B extended from the border between the separation layer SL2 and the edge area A to which ions have not been implanted.

[38] The stacked structure formed according to the processes of Figs. 6 to 9 may include the growth substrate 30, the lower semiconductor layer 31, the active layer 32, the upper semiconductor layer 33, the Ohmic contact layer 34, the metal layer 35, the conductive substrate 40 joined to the metal layer 35, and the separation layer SL2 formed below active layer 32, i.e., in the growth substrate 30.

[39] During the formation process such as a crystal growing process, the stacked structure may be separated into an upper part and a lower part. However, the stacked structure including the lower semiconductor layer 31, the active layer 32, the upper semiconductor layer 33, the Ohmic contact layer 34 and the conductive layer 40 may still be attached to the growth substrate 30 without being detached from the growth substrate 30. This is accomplished during the ion implantation stage by ensuring ions are not implanted in edge area A through the use of an ion implantation mask. In some embodiments, it is possible that some ions may be implanted in some portions that are covered by the mask, but ions for the most part will not be implanted in portions covered by the mask.

[40] Subsequently, as shown in Fig. 10, a cutting process may be performed by using a laser, a scribe or a diamond saw to cut the metal layer 35, the Ohmic contact layer 34, the upper semiconductor layer 33, the active layer 32, the lower semiconductor layer 31 and a part of the growth substrate 30, along the lines B to which the ends of the conductive substrate 40 are aligned. By this cutting process, the growth substrate 30, the lower semiconductor layer 31, the active layer 32, the upper semiconductor layer 33 and the Ohmic contact layer 34 are respectively divided into a first growth substrate 30a and a second growth substrate 30b, a first lower semiconductor layer 31a and a second lower semiconductor layer 31b, a first active layer 32a and a second active layer 32b, a first upper semiconductor layer 33a and a second upper semiconductor 33b, a first Ohmic contact layer 34a, a second Ohmic contact layer 34b and the first metal layer 35a and the second metal layer 35b. The second growth substrate 30b may include the edge of the growth substrate 30 and a lower part of the separation layer

SL2. The second lower semiconductor layer 31b, the second active layer 32b, the second upper semiconductor 33b, the second Ohmic contact layer 34b and the second metal layer 35b may be left on the edge of the growth substrate 30.

- [41] Instead of cutting along the lines B using a laser, a scribe or a diamond saw, a dry etching or wet chemical etching process may be applied to remove the second metal layer 35b, a second Ohmic contact layer 34b, a second upper semiconductor 33b, a second active layer 32b, a second lower semiconductor layer 31b, and upper portion of the substrate down to separation layer SL2.
- [42] The stack structure of the first growth substrate 30a, the first lower semiconductor layer 31a, the first active layer 32a, the first upper semiconductor layer 33a, the first Ohmic contact layer 34a, the first metal layer 35a and the conductive substrate 40 may constitute the light emitting device. An etching process and a polishing process may be performed to remove the second lower semiconductor 31b, the second active layer 32b, the second upper semiconductor layer 33b, the second Ohmic contact layer 34b and the second metal layer 35b, which have been left on the edge of the second growth substrate 30b, so that only the second growth substrate 30b may remain. The remaining second growth substrate 30b may be reused as the growth substrate 30 shown in Fig. 6, after going through a surface smoothing process such as polishing.
- [43] If the first growth substrate 30a is a conductive substrate, the first growth substrate 30a may be part of the first lower semiconductor layer 31a. If first growth substrate 30a is a dielectric, the first growth substrate 30a may be removed to expose the surface of the first lower semiconductor layer 31a, and a transparent electrode (not illustrated) may be formed on the exposed surface of the first lower semiconductor 31a. An electrical contact pad 36 may be formed on the transparent electrode, as shown in Fig. 11. An electrical contact pad 36 may be formed directly on the first lower semiconductor layer 31a if transparent electrode is not needed. Further, in order to improve light emission efficiency, a roughening process may be performed upon the surface of the first lower semiconductor layer 31a before forming the transparent electrode or the electrical pad 36. A dicing process to form individual chips and packaging into a lamp or SMD (surface mount device) form may also be performed in some embodiments.
- [44] In the vertical structure semiconductor light emitting device formed in accordance with the second embodiment, the currents may flow vertically from the p-type electrode to the n-type electrode of the light emitting device. Light may be generated in the first active layer 32a by the combination of electrons and holes, and the generated light may be emitted in the direction of all solid angle. The light emitted in the direction of the conductive substrate 40 may be reflected toward and emitted through the surface of the first lower semiconductor layer 31a, resulting in an increased optical power output.

- [45] In the aforementioned first and second embodiments, if the growth substrates 10 and 30 are conductive substrates, an edge emitting laser may be manufactured by additionally performing a cleavage process on the first lower semiconductors 11a and 31a, the active layers 12 and 32a, and the first upper semiconductor layers 13 and 33a.
- [46] As mentioned above, a light emitting device may be formed using separation by ion implantation to prevent cracking, and it may enable fabrication of a large size light emitting device having high efficiency at a low costs. Further, by preventing or minimizing damage on the growth substrate, the unit price of a device may not increase despite the use of a high-priced substrate. Therefore, a high-priced substrate with high performance can be used at a minimum cost. Light emitting devices formed using methods in accordance with the described embodiments may enable mass production of a GaN-based LEDs having high quality, high brightness, high yield and improved reliability at low costs.
- [47] Further, the light emitting device forming methods in accordance with the described embodiments do not need to utilize conventional laser lift off (LLO) processes, so that no mechanical impact may be imposed, thus making no cracks, increasing performance and improving reliability.
- [48] Furthermore, since the semiconductor growth substrate may be reused, the fabrication cost may be drastically reduced. Further, the size of a substrate (wafer) may not be limited to 2 inches which a large size substrate producible with a wafer fabricating technique may be limited to.
- [49] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure. More particularly, numerous variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

Industrial Applicability

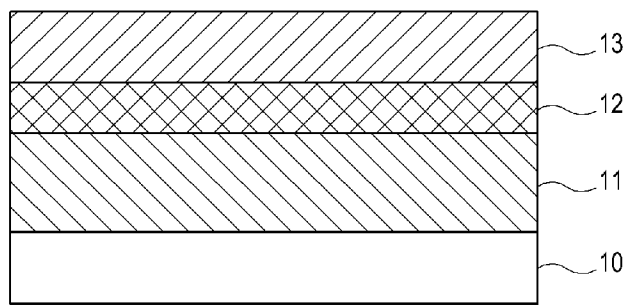
- [50] A light emitting device may be formed using substrate separation by ion implantation.

Claims

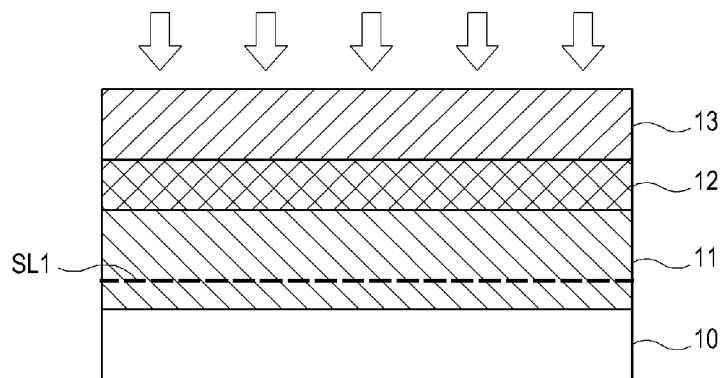
- [1] A method of forming a light emitting device, the method comprising:
forming a stacked structure including a substrate, a lower semiconductor layer of a first conductivity type, an active layer, and an upper semiconductor layer of a second conductivity type, wherein the stack structure includes a separation layer formed below the active layer; and
performing a thermal process upon the stacked structure to divide the separation layer laterally such that the stacked structure is separated into an upper part and a lower part.
- [2] The method of Claim 1, wherein the forming of the stacked structure comprises:
forming the lower semiconductor layer of the first conductivity type on the substrate;
forming the active layer on the lower semiconductor layer;
forming the upper semiconductor layer of the second conductivity type on the active layer; and
forming the separation layer by implanting ions into the substrate or the lower semiconductor layer.
- [3] The method of Claim 1, wherein the forming of the stacked structure comprises:
forming the separation layer by implanting ions into the substrate; and
sequentially forming the lower semiconductor layer of the first conductivity type on the substrate, the active layer on the lower semiconductor layer, and the upper semiconductor layer of the second conductivity type on the active layer.
- [4] The method of Claim 3, wherein the forming of the separation layer further comprises:
forming an ion implantation mask covering at least one edge of the substrate;
forming the separation layer by implanting the ions on portions of the substrate not covered by the mask and wherein ions are not implanted in portions of the substrate covered by the mask; and
removing the ion implantation mask after the ion implantation.
- [5] The method of Claim 4, further comprising:
performing a cutting process or an etching process along base lines extended from borders between the separation layer and the non-implantation area after performing the thermal process to separate the stacked structure into the upper part and the lower part.
- [6] The method of Claim 1, further comprising:
forming an Ohmic contact layer on the upper semiconductor layer after forming the stacked structure, wherein the Ohmic contact layer is formed with a thermal

- process for Ohmic contact;
forming a metal layer on the Ohmic contact layer; and
joining a conductive substrate to the metal layer.
- [7] The method of Claim 6, wherein the thermal process for separating the stacked structure into the upper part and the lower part is performed after joining the conductive substrate to the metal layer.
- [8] The method of Claim 6, wherein the thermal process for separating the stacked structure into the upper part and the lower part is a thermal process for forming the Ohmic contact layer.
- [9] The method of Claim 6, wherein the metal layer is formed of at least one metal selected from the group consisting essentially of Cu, Al, Au, Pd, Ti, In, Ni and Pt or an alloy of at least two metals selected from the above-mentioned group.
- [10] The method of Claim 2, wherein the separation layer is formed by implanting ions of at least one kind of atom, wherein the atomic number of the atom is 54 or less.
- [11] The method of Claim 7, further comprising:
exposing a surface of the lower semiconductor layer after separating the stacked structure into the upper and lower parts of the separation layer by the thermal processing; and
forming an electrical contact pad on the exposed surface.
- [12] The method of Claim 11, wherein exposing the surface of the lower semiconductor layer includes removing the substrate left on the lower surface of the lower semiconductor layer if the substrate left is non-conducting material.
- [13] The method of Claim 11, further comprising:
forming a transparent electrode on the exposed surface before forming the electrical contact pad.
- [14] The method of Claim 11, further comprising:
performing a roughness process on the surface of the lower semiconductor layer before forming the transparent electrode.
- [15] The method of Claim 6, further comprising:
cleaving side surfaces of the lower semiconductor layer, the active layer and the upper semiconductor layer to form a light emitting laser diode after separating the stacked structure into the upper and lower parts of the separation layer.

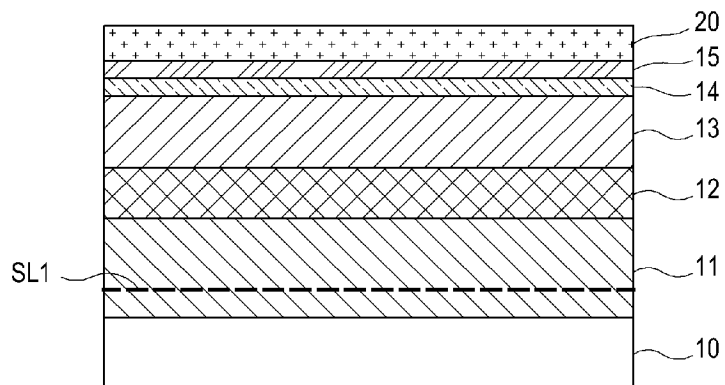
[Fig. 1]



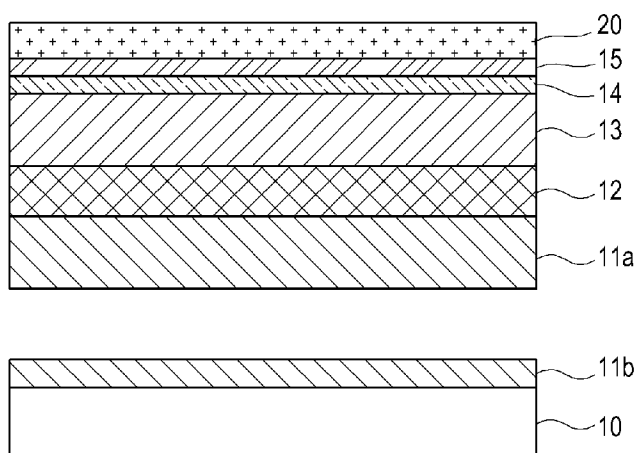
[Fig. 2]



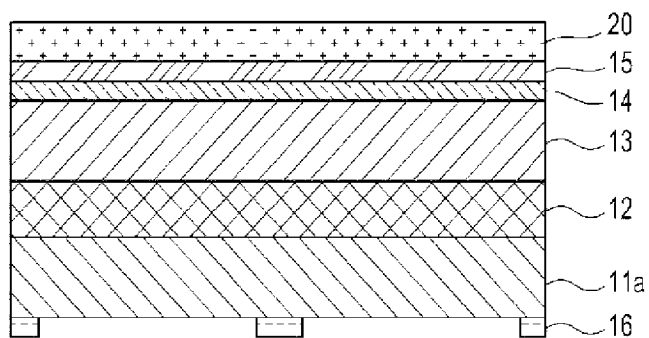
[Fig. 3]



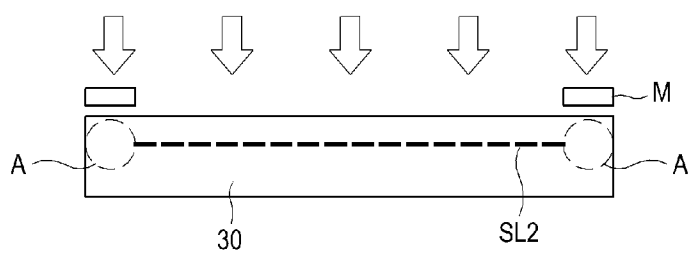
[Fig. 4]



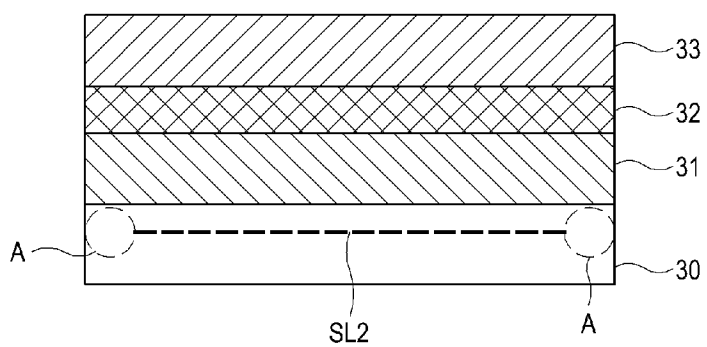
[Fig. 5]



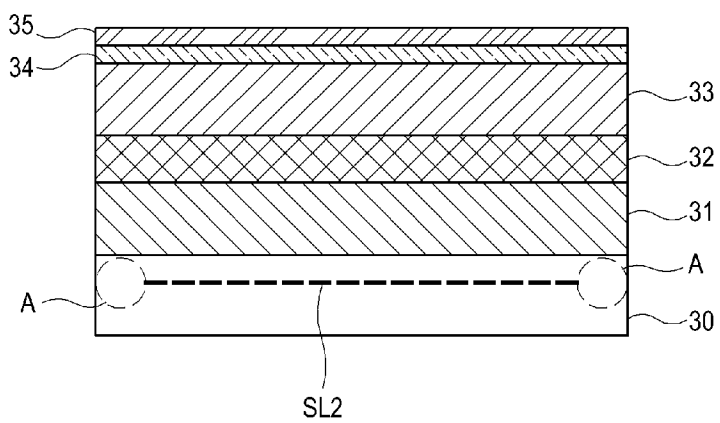
[Fig. 6]



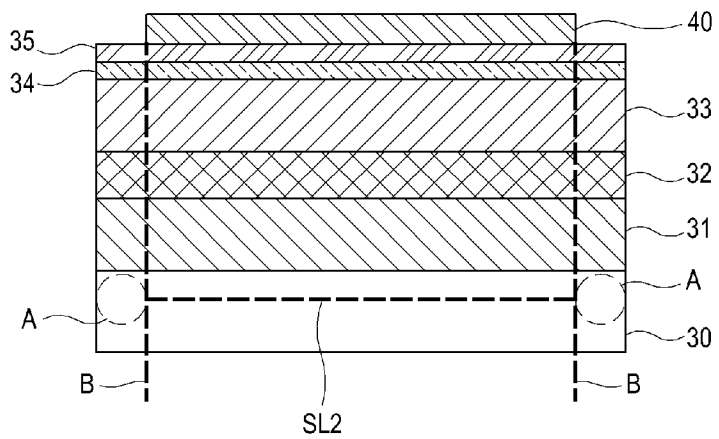
[Fig. 7]



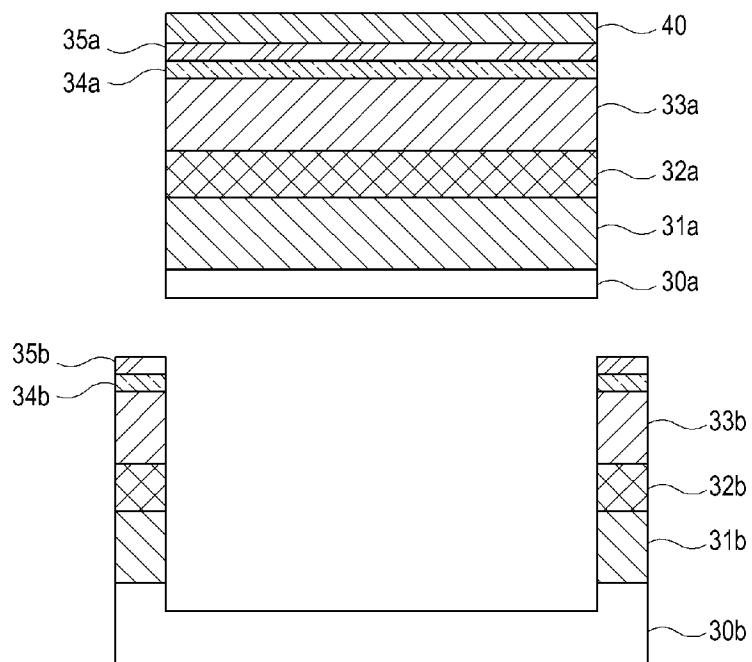
[Fig. 8]



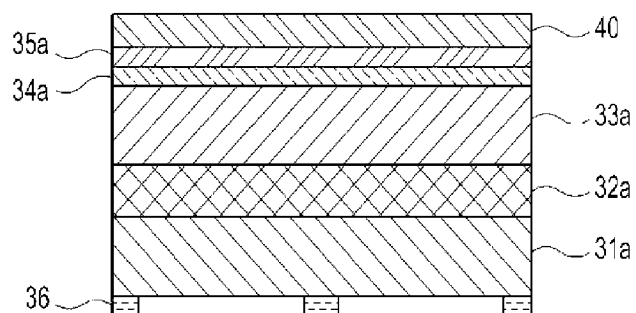
[Fig. 9]



[Fig. 10]



[Fig. 11]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2009/004510**A. CLASSIFICATION OF SUBJECT MATTER*****H01L 33/12(2010.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 33/12; C30B 33/00; H01L 21/20; H01L 27/15; H01L 33/00;

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

(Chinese Patents and application for patent)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: vertical, thermal, LLO, free stand

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	KR 10-0835076 B1 (SAMSUNG ELECTRO-MECHANICS CO., LTD) 03 June 2008 See Claims 1,2, Paragraph [0046]-[0063] and Figures 9,10	1-15
Y	KR 10-2008-0078679A(S.O.I TEC SILICON ON INSULATOR TECHNOLOGIES)27August2008 See Claims 7,12, Paragraph [0037]-[0049] and Figures 1,2	1-15
A	US 2003-0189212 A1 (MYUNG CHEOL YOO) 09 October 2003 See Claims 23,43, Paragraph [0042]-[0043] and Figures 9,10	1-15

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search

08 APRIL 2010 (08.04.2010)

Date of mailing of the international search report

09 APRIL 2010 (09.04.2010)

Name and mailing address of the ISA/KR

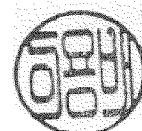
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Information on patent family members

International application No.

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