

(10) International Publication Number
WO 2014/182129 A1(43) International Publication Date
13 November 2014 (13.11.2014)

- (51) **International Patent Classification:**
B82B 3/00 (2006.01) **C01G 9/02** (2006.01)
- (21) **International Application Number:**
PCT/KR20 14/004 170
- (22) **International Filing Date:**
9 May 2014 (09.05.2014)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
10-2013-0053 164 10 May 2013 (10.05.2013) KR
- (71) **Applicants:** POSTECH ACADEMY-INDUSTRY
FOUNDATION [KR/KR]; 77, Cheongam-ro, Nam-gu,
Pohang-si, Gyeongsangbuk-do 790-784 (KR). SEOUL VI-

OSYS CO., LTD. [KR/KR]; 1B-36, 65-16, Sandan-ro
163beon-gil, Danwon-gu, Ansan-si, Gyeonggi-do 425-85 1
(KR).

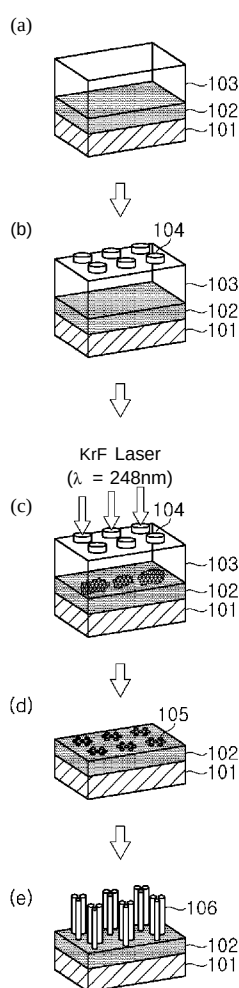
(72) **Inventors:** LEE, Jong Lam; Gyosu Apt. E-1403, 155,
Jigok-ro, Nam-gu, Pohang-si, Gyeongsangbuk-do 790-75 1
(KR). KIM, Sung Joo; Byucksan Apt.106-502, 105-21,
Hakgam-daero, Sasang-gu, Busan 617-771 (KR). KIM,
Buem Joon; Hyundai Milat C-1402, 19, Gyeongui-ro, Ils-
andong-gu, Goyang-si, Gyeonggi-do 410-360 (KR).

(74) **Agent:** AIP PATENT & LAW FIRM; 30-1, Teheran-ro
14-gil, Gangnam-gu, Seoul 135-935 (KR).

(81) **Designated States** (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,

[Continued on nextpage]

(54) **Title:** MANUFACTURING METHOD OF ZINC OXIDE NANOROD ARRAYS AND NANOROD ARRAYS MADE BY
THE SAME AND SEMICONDUCTOR DEVICE USING THE SAME



(57) **Abstract:** Disclosed are a method of manufacturing zinc oxide nanorod arrays grown in a certain pattern in a predetermined region of a nitride semiconductor, and zinc oxide nanorod arrays manufactured by the same. The method includes: preparing a growth substrate having a first surface and a second surface; growing a nitride semiconductor layer on the first surface of the growth substrate; placing a support substrate on the nitride semiconductor layer; forming a mask pattern on the second surface of the growth substrate; and removing the growth substrate from the nitride semiconductor layer by providing a laser beam through the second surface of the growth substrate having the mask pattern.

DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,

TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

Description

Title of Invention: MANUFACTURING METHOD OF ZINC OXIDE NANOROD ARRAYS AND NANOROD ARRAYS MADE BY THE SAME AND SEMICONDUCTOR DEVICE USING THE SAME

Technical Field

- [1] Exemplary embodiments of the present invention relate to a method of manufacturing zinc oxide nanorod arrays, nanorod arrays manufactured by the same, and a semiconductor device using the nanorod arrays, and more particularly, to a method of manufacturing zinc oxide nanorod arrays growing in a certain pattern in a predetermined region of a nitride semiconductor, nanorod arrays manufactured by the same, and a semiconductor device using the nanorod arrays.

Background Art

- [2] One-dimensional and nano-scale materials have recently been extensively studied due to optical and electrical properties thereof and potential utilization in electronics and optoelectronics. Recently, zinc oxide (ZnO) nanorods have been spotlighted since the zinc oxide nanorods have not only a band-gap energy of about 3.37 eV and a high exciton binding energy of 60 meV, but also direct band-gap properties. In addition, the zinc oxide nanorods have high piezoelectric properties and chemical sensing properties, and thus can be used for nano-scale mechanical devices or sensors. Accordingly, various studies have been actively made for development of a method of manufacturing zinc oxide nanorods.
- [3] Zinc oxide can be formed into nanorods through various methods, such as metal organic chemical vapor deposition (MOCVD), hydrothermal synthesis, etc. In MOCVD, zinc oxide nanorods are grown at high temperature. Thus, MOCVD has a limit to the kind of substrate used for growing the zinc oxide nanorods. On the other hand, in hydrothermal synthesis, the zinc oxide nanorods are grown at low temperature. Thus, hydrothermal synthesis has no strict limit to the kind of substrate, and requires relatively low cost and a simple growth process.
- [4] Zinc oxide nanorod arrays may be formed by methods using e-beam lithography and nanostructures. E-beam lithography has an advantage of much higher resolution than general photo-processes, but has disadvantages of high costs and low productivity. The method using nanostructures has advantages of relatively low costs and a simple process, but has a disadvantage of difficulty in providing good reproducibility in a large area.

- [5] The above information disclosed in this Background section is only for enhancement of understanding of the background of the invention and, therefore, it may contain information that does not constitute prior art.

Disclosure of Invention

Technical Problem

- [6] Exemplary embodiments of the present invention provide a method of manufacturing zinc oxide nanorod arrays, nanorod arrays manufactured by the same and a semiconductor device using the nanorod arrays, in which the zinc oxide nanorod arrays are selectively grown at low temperature.
- [7] Exemplary embodiments of the present invention provide a method of manufacturing zinc oxide nanorod arrays at low cost using a simple process to provide good reproducibility in a large area, nanorod arrays manufactured by the same, and a semiconductor device using the nanorod arrays.
- [8] Additional features of the invention will be set forth in the description which follows, and in part will become apparent from the description, or may be learned from practice

Solution to Problem

- [9] An exemplary embodiment of the present invention discloses a method of manufacturing zinc oxide nanorod arrays including: preparing a growth substrate having a first surface and a second surface; growing a nitride semiconductor layer on the first surface of the growth substrate; placing a support substrate on the nitride semiconductor layer; forming a mask pattern on the second surface of the growth substrate; and removing the growth substrate from the nitride semiconductor layer by providing a laser beam through the second surface of the growth substrate having the mask pattern.
- [10] The mask pattern is used to form a transfer pattern on the nitride semiconductor layer and the transfer pattern may be used as a seed for forming zinc oxide nanorod arrays.
- [11] The method may further include growing zinc oxide nanorod arrays by applying hydrothermal synthesis to the nitride semiconductor layer from which the growth substrate is removed. With hydrothermal synthesis, it is possible to grow the zinc oxide nanorod arrays at low temperature and low cost.
- [12] The hydrothermal synthesis may employ a mixed solution of zinc salt and hexamethylenetetramine.
- [13] The mixed solution may have a molarity of 0.0001M to 1M.
- [14] The mask pattern may be formed by a lift-off process.
- [15] The mask pattern may be formed of one of oxide, nitride, organic and polymer materials.
- [16] The lift-off process may include forming a mask layer on a photoresist pattern and removing the photoresist pattern, and the mask layer may be formed by thermal de-

position, electron-beam evaporation, or sputtering.

- [17] The oxide may include Al_2O_3 , MgO, ZnO, NiO, ITO or SiO_2 .
- [18] The nitride semiconductor layer may comprise a p-type semiconductor doped with p-type impurities, an n-type semiconductor doped with n-type impurities, or an undoped semiconductor.
- [19] The support substrate may include Si, Cu, Ni, polydimethylsiloxane (PDMS), polyethylene terephthalate (PET), or polyurethane acrylate (PUA).
- [20] The growth substrate may include a sapphire substrate, and the sapphire substrate may have a thickness of 100 μm to 1000 μm .
- [21] The mask pattern may include masking elements separated from each other, each of the masking elements may have a width of 2 μm to 100 μm , and a distance between the masking elements may range from 2 μm to 100 μm .
- [22] The masking elements may have a thickness from 100 nm to 1000 nm.
- [23] The laser beam may have a wavelength of 248 nm and an energy of 400 mJ to 700 mJ.
- [24] The growth substrate may include a sapphire substrate, a nitride substrate, or a SiC substrate.
- [25] The method may further include applying surface treatment to a surface of the nitride semiconductor layer, from which the growth substrate is removed, with ultraviolet/ozone (UVO), oxygen plasma, nitrogen plasma or argon plasma. Surface treatment of the nitride semiconductor layer can increase nucleation site density on the surface of the nitride semiconductor layer.
- [26] Surface treatment using UVO may be performed for 1 minute to 60 minutes.
- [27] Nanorod arrays may be manufactured by one of the foregoing methods. By the foregoing methods, the nanorod arrays may be easily manufactured at low cost.
- [28] A semiconductor device includes a substrate; and nanorod arrays each comprising unit arrays arranged on the substrate, wherein nanorods within the unit array are arranged in a ring or plate shape.
- [29] The nanorods may include zinc oxide.
- [30] The nanorods within the unit array may be irregularly arranged in a ring or plate shape.
- [31] The semiconductor device may further include a nitride semiconductor layer placed on the substrate, wherein the nanorod arrays are placed on the nitride semiconductor layer.

Advantageous Effects of Invention

- [32] Embodiments of the present invention may provide a method of manufacturing zinc oxide nanorod arrays, nanorod arrays manufactured by the same, and a semiconductor

device using the nanorod arrays, in which the zinc oxide nanorod arrays are selectively grown at low temperature. In addition, there may be provided a method of manufacturing zinc oxide nanorod arrays at low cost using a simple process to provide good reproducibility in a large area, nanorod arrays manufactured by the same, and a semiconductor device using the nanorod arrays.

[33] Further, the manufacturing method according to the invention allows the zinc oxide nanorod arrays to be grown to have a pattern in a predetermined region, and can be easily incorporated into an existing semiconductor process, thereby providing high connectivity with the existing process.

[34] Furthermore, nanorod arrays manufactured by the manufacturing method according to the invention are excellent in vertical alignment and measured value reproducibility. Furthermore, a semiconductor device using the zinc oxide nanorod arrays manufactured according to the present invention has excellent reliability.

Brief Description of Drawings

[35] Fig. 1 is perspective views showing a method of manufacturing zinc oxide nanorod arrays according to an exemplary embodiment of the present invention.

[36] Fig. 2 is a diagram showing a process of separating a growth substrate in the manufacturing method according to an exemplary embodiment of the present invention.

[37] Fig. 3 shows an optical photograph and scanning electron micrographs (SEM) of a transfer pattern formed on a surface of a nitride semiconductor layer according to an exemplary embodiment of the present invention.

[38] Fig. 4 shows atomic force micrographs (AFM) of the transfer pattern formed on the surface of the nitride semiconductor layer according to an exemplary embodiment of the present invention.

[39] Fig. 5 shows photographs and graphs of scanning photoemission microscopy (SPEM) and X-ray photoemission spectroscopy (XPS) analysis results of the surface of the nitride semiconductor layer having the transfer pattern according to an exemplary embodiment of the present invention.

[40] Fig. 6 shows SEM photographs of zinc oxide nanorods grown on a transfer pattern according to an exemplary embodiment of the present invention.

Mode for the Invention

[41] The invention is described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure is thorough, and will fully convey the scope of the invention to those skilled in the art.

- [42] Fig. 1 is perspective views showing a method of manufacturing zinc oxide nanorod arrays according to an exemplary embodiment of the present invention. In Fig. 1, (a), (b), (c), (d) and (e) show respective operations of the manufacturing method according to the embodiment of the present invention.
- [43] Referring to Fig. 1(a), first, a nitride semiconductor layer 102 is grown on a first surface of a growth substrate 103, and the grown nitride semiconductor layer 102 is placed on a support substrate 101. The growth substrate 103 is a substrate capable of growing a nitride semiconductor layer thereon, and is not particularly limited so long as the substrate is a transparent substrate allowing a laser beam to pass therethrough. For example, the growth substrate 103 may include a sapphire substrate, a nitride substrate, or a SiC substrate.
- [44] The growth substrate 103 may have any thickness so long as the growth substrate allows growth of the nitride semiconductor layer thereon. For example, the growth substrate 103 may have a thickness from about 100 μm to about 1000 μm . If the thickness of the growth substrate 103 is less than 100 μm , the growth substrate is likely to be bent or broken, thereby making it difficult to perform the process. Conversely, if the thickness of the growth substrate 103 is greater than 1000 μm , the laser beam is wastefully absorbed into the growth substrate upon laser lift-off. The growth substrate 103 may have a thickness from 300 μm to 500 μm .
- [45] The nitride semiconductor layer 102 may be a p-type semiconductor doped with p-type impurities, an n-type semiconductor doped with n-type impurities, or an undoped semiconductor. The support substrate 101 may include Si, Cu, Ni, polydimethylsiloxane (PDMS), polyethylene terephthalate (PET), or polyurethane acrylate (PUA).
- [46] Referring to Fig. 1(b), a mask pattern 104 is formed on a second surface of the growth substrate 103. The second surface refers to a rear surface of the surface on which the nitride semiconductor layer 102 is grown. The mask pattern 104 may be formed by a lift-off technique. That is, the mask pattern 104 may be formed by photolithography and deposition. For example, a mask layer is formed on a photoresist pattern on the growth substrate 103, and the photoresist pattern is then removed to form the mask pattern.
- [47] The mask pattern 104 may have an island pattern, and each masking element may have various shapes. Each masking element of the mask pattern 104 may have various shapes, sizes and pitches according to purposes of use. For example, each masking element may have a disk shape having a diameter of about 2 μm to 100 μm . In addition, a distance between the elements of the mask pattern 104 may range from about 2 μm to 100 μm . However, the diameter or distance of the masking elements of the mask pattern 104 is selected to form a transfer pattern having a sufficient size on the surface of the nitride semiconductor layer 102. The transfer pattern refers to a region formed on the

surface of the nitride semiconductor layer 102 and having higher roughness than other regions.

[48] While forming the mask pattern 104, deposition may refer to a process based on thermal deposition, electron-beam evaporation, or sputtering. The mask pattern 104 may be formed of a publicly known material capable of partially blocking the energy of a laser beam. The mask pattern 104 may be formed of an oxide, nitride, organic or polymer material. The oxide may include Al_2O_3 , MgO , ZnO , NiO , ITO , or SiO_2 . The thickness of the mask pattern 104 is determined to partially block or scatter the energy of the laser beam. For example, the mask pattern 104 may have a thickness from about 100 nm to 1000 nm. If the thickness of the mask pattern 104 is smaller than 100 nm, it can be difficult to sufficiently decrease energy of an incident laser beam. Conversely, if the thickness of the mask pattern 104 is greater than 1000 nm, most energy of the incident laser beam is absorbed into the mask pattern 104, thereby making it difficult to separate the growth substrate 103 beneath the mask pattern 104 from the nitride semiconductor layer 102. The transfer pattern formed by transmission of the laser beam and separation of the growth substrate 103 will be described below.

[49] Referring to Fig. 1(c), the laser beam is emitted to pass through the second surface of the growth substrate 103 having the mask pattern 104 formed thereon. The laser may be a KrF laser. The KrF laser is advantageous since it can minimize thermal effects around a processing region. The laser beam may have a wavelength of 248 nm. The laser beam may have an energy of 400 mJ to 700 mJ. The energy of the laser beam may be suitably adjusted according to the thickness of the growth substrate, and the substances and sizes of the support substrate and the mask pattern. If the energy of the laser beam entering an interface between the growth substrate and the nitride semiconductor layer is insufficient, GaN of the nitride semiconductor layer can be unevenly decomposed. As a result, during laser lift-off, a GaN surface of the nitride semiconductor layer can be partially chipped off. On the other hand, if the energy of the laser entering the interface between the growth substrate and the nitride semiconductor layer is excessively high, crystallinity of GaN is broken by the laser beam to a deep portion of the nitride semiconductor layer. Therefore, it is difficult to achieve normal growth of zinc oxide nanorods on the surface of the nitride semiconductor layer.

[50] The laser beam partially or completely passes through the mask pattern 104 and the growth substrate 103 and is absorbed at the interface between the growth substrate 103 and the nitride semiconductor layer 102. As a result, GaN can be decomposed by Formula 1.

[51] $2 \text{ GaN} \rightarrow 2 \text{ Ga} + \text{N}_2$ (KrF laser at 248 nm) — (1)

[52] In Formula 1, GaN on the surface of the nitride semiconductor layer 102 can be decomposed into Ga and N_2 . In Formula 1, a KrF laser beam having a wavelength of 248

nm is used. GaN has a band-gap energy of 3.4 eV, and if the KrF laser beam enters GaN at 5 eV, the energy of the laser beam is absorbed into GaN. Accordingly, GaN is decomposed, and N₂ gas is generated and Ga is melted at the interface. As a result, the growth substrate 103 is separated from the nitride semiconductor layer 102. The mask pattern 104 is placed in an incident direction of the laser beam. Therefore, the energy of the laser beam can be partially blocked or absorbed into the mask pattern 104, so that the energy level of the laser beam reaching the interface differs depending on the location of the interface.

- [53] Referring to Fig. 1(d), the growth substrate 103 is separated from the nitride semiconductor layer 102. As described above with reference to Fig. 1(c), since the energy of the laser beam absorbed into the surface of the nitride semiconductor layer 102 is varied, the transfer pattern 105 can be formed on the nitride semiconductor layer 102. The transfer pattern 105 is formed corresponding to the mask pattern 105. That is, relatively rough transfer elements formed on the surface of the mask pattern 105 correspond to the masking elements, and a region between the transfer elements is relatively flat.
- [54] After the nitride semiconductor layer 102 and the growth substrate 103 are separated, the surface of the nitride semiconductor layer 102 may be subjected to inductively coupled plasma (ICP) etching. ICP etching can improve crystallinity of GaN on the surface of the nitride semiconductor layer 102 and remove damage due to the laser beam.
- [55] Referring to Fig. 1(e), nanorods are formed on the nitride semiconductor layer having the transfer pattern 105. That is, as described above, the nitride semiconductor layer 102 formed on the support substrate 101 includes the transfer pattern 105, and the nanorods 106 may be grown using the transfer pattern 105.
- [56] The nanorods 106 may be grown by hydrothermal synthesis. In general, the surface of high roughness has high surface energy and thus easy adsorption with outer atoms to lower the surface energy. Therefore, if the nitride semiconductor having the transfer pattern 105 formed on the surface thereof is dipped in an aqueous solution containing Zn and O ions, the Zn and O ions are adsorbed to a portion in which the transfer pattern is formed, thereby proceeding nucleation and growth. That is, the transfer pattern of the nitride semiconductor may serve as a seed for growing the zinc oxide nanorods.
- [57] First, before growing the nanorods 106, the surface of the nitride semiconductor layer 102 formed with the transfer pattern may be subjected to surface treatment using ultraviolet/ozone (UVO). Through UVO treatment, the surface of the nitride semiconductor layer 102 can be cleaned and damage of the surface due to the laser beam can be recovered. UVO treatment is efficient in decontamination of hydrocarbon-

containing substances. In addition, UVO treatment has an effect of increasing nucleation site density on the surface of the nitride semiconductor layer 102. Zinc oxide and gallium nitride are structurally identical in that both have a Wurtzite crystal structure. Zinc oxide has lattice constants of $a=3.250 \text{ \AA}$ and $c=5.207 \text{ \AA}$ which are very similar to those of gallium nitride having lattice constants of $a=3.189 \text{ \AA}$ and $c=5.185 \text{ \AA}$. Thus, if zinc oxide is formed on the surface of gallium nitride, it is possible to form a nanostructure having a greater vertical-orientation. Therefore, it is possible to form a highly dense array of zinc oxide nanorods by increasing the nucleation site density on the surface of the nitride semiconductor layer 102. In addition, UVO treatment can increase the density and diameter of the zinc oxide nanorods 106 growing on the surface of the nitride semiconductor layer 102. Although UVO treatment is preferable, the present invention is not limited thereto. Alternatively, surface treatment using oxygen plasma, nitrogen plasma and argon plasma may also be used.

[58] Surface treatment using UVO may be performed for 1 minute to 60 minutes. If surface treatment is performed for less than 1 minute, it is impossible to obtain a desired cleaning effect. Conversely, surface treatment for longer than 60 minutes is not efficient due to little improvement in the cleaning effect.

[59] Thereafter, the support substrate 101 including the nitride semiconductor layer 102 is secured by a holder to have the treated surface facing downward, and then dipped in a mixed solution within an autoclave, thereby forming the zinc oxide nanorods through hydrothermal synthesis. During hydrothermal synthesis, the shape, diameter and length of the nanorods may be adjusted through change in conditions, such as temperature, time, the amount of aqueous solution, molar ratio, pH, etc. The autoclave used in hydrothermal synthesis refers to a container for chemical treatment under conditions of high temperature and high pressure, which is used to provide stable growth conditions. Typically, the autoclave is maintained at $60 \sim 600 \text{ }^{\circ}\text{C}$ and $250 \sim 1200 \text{ atm}$. According to embodiments of the invention, the autoclave is maintained at $90 \text{ }^{\circ}\text{C}$ during hydrothermal synthesis.

[60] In addition, the aqueous solution for hydrothermal synthesis contains deionized water, zinc salt, and hexamethylenetetramine. Here, a molar ratio of zinc salt to hexamethylenetetramine is maintained in the range from 2:1 to 1:2 in order to form normal nanorods.

[61] In addition, in the aqueous solution for hydrothermal synthesis, the aqueous solution of zinc salt and hexamethylenetetramine has a molarity of $0.0001\text{M} \sim 1\text{M}$. If the molarity is less than 0.0001M , it is difficult to control the content of zinc salt and the zinc oxide nanostructure cannot be easily formed. On the other hand, if the molarity is more than 1M , the amount of sources consumed for growing the zinc oxide nanostructure is so large, thereby making it difficult to control the shape and size of the

nanostructure. The zinc salt may be zinc nitrate hexahydrate.

- [62] Fig. 2 is a diagram of a process of separating a growth substrate in the method of manufacturing zinc oxide nanorod arrays according to an exemplary embodiment of the present invention. In Fig. 2, (a) schematically shows intensity E_a of energy absorbed at the interface between the growth substrate 103 and the support substrate 102, and (b) schematically shows the nitride semiconductor layer including the transfer pattern 105.
- [63] Referring to Fig. 2(a), a KrF laser beam enters the second surface of the growth substrate 103 including the mask pattern 104 for laser blocking. As shown in the intensity E_a of energy absorbed at the interface, the interface under the respective masking elements of the mask pattern 104 absorbs less energy than other regions of the interface. That is, at the interface between the growth substrate 103 and the support substrate 102, the intensity of absorbed energy differs depending on the location of the mask pattern 104.
- [64] Referring to Fig. 2(b), since the intensity of laser energy entering the surface of the nitride semiconductor layer 102 differs, the degree of decomposition differs depending on the location of the mask pattern on the surface of the nitride semiconductor layer 102 as described in Formula 1. Specifically, when KrF laser beams enter the surface of the nitride semiconductor layer 102, Ga is more melted and N_2 gas is more generated in a portion to which relatively high energy is applied. On the contrary, Ga is less melted in a portion to which relatively low energy is applied. Thus, the surface of the nitride semiconductor layer 102 may have different roughness depending on the locations thereof. That is, if there is no mask pattern 104 on the top of the nitride semiconductor layer, GaN is sufficiently decomposed to form a relatively flat surface. On the contrary, if the mask pattern 104 is present thereon, GaN is less decomposed to form a relatively rough surface.
- [65] Fig. 3 shows an optical photograph and scanning electron micrographs (SEM) of a transfer pattern formed on a surface of a nitride semiconductor layer according to an exemplary embodiment of the present invention. In Fig. 3, (a) shows an optical photograph of the substrate surface taken from a right upper box, and (b), (c), and (d) are SEM photographs of the transfer pattern. Fig. 3 shows the surface of the nitride semiconductor layer subjected to inductively coupled plasma (ICP) etching after removing the growth substrate by the laser beams. Here, the laser may have an energy of about 600 mJ.
- [66] Fig. 4 shows atomic force micrographs (AFM) of the transfer pattern formed on the surface of the nitride semiconductor layer according to an exemplary embodiment of the present invention, which is taken from a white dotted-line box of Fig. 3 (d). In Fig. 4, (a) shows a two-dimensional photograph of the transfer pattern, and (b) shows a

three-dimensional photograph of the transfer pattern.

- [67] Referring to Figs. 3 and 4, nano-scale dots are arranged in a portion on the surface of the nitride semiconductor layer 102 in which transfer elements of the transfer pattern 104 are formed, thereby providing high roughness to the surface thereof. On the contrary, a portion of the transfer pattern 104 in which the transfer elements are not formed has relatively low roughness. According to measurement results obtained from AFM, line (1) passing through the transfer elements of the transfer pattern 104 has an average roughness of 24.8 nm, and line (2) passing through a region in which the transfer elements of the transfer pattern 104 are not formed has an average roughness of 3.7 nm.
- [68] According to the thicknesses of the mask pattern 104 and the growth substrate 103 and the intensity of incident laser beams, the dots are arranged in a ring form at the edges of the transfer elements, or in a plate form (not shown) throughout the entire region of the transfer elements.
- [69] Fig. 5 shows photographs and graphs of scanning photoemission microscopy (SPEM) and X-ray photoemission spectroscopy (XPS) analysis results of the surface of the nitride semiconductor layer having the transfer pattern according to an exemplary embodiment of the present invention. SPEM and XPS analysis provides information about chemical components in a local point on the surface of the nitride semiconductor.
- [70] Fig. 5(a) is an SPEM analysis photograph with regard to a peak of Ga 3d within a region of 60 μm x 60 μm . Referring to Fig. 5(a), it can be seen that the peak of Ga 3d in Region (1) is higher than that in Region (2) according to the area and roughness of the transfer pattern. Fig. 5(b) is an XPS analysis graph with regard to Regions (1) and (2). Referring to Fig. 5(b), it can be seen that Region (1) has high intensity in analysis of Regions (1) and (2) at a core level of Ga 3d.
- [71] Fig. 5(c) is an SPEM analysis photograph with regard to a peak of N 1s within a region of 60 μm x 60 μm . Referring to Fig. 5(c), it can be seen the peak of N 1s in Region (1) is similar to that in Region of (2) regardless of the area and roughness of the transfer pattern. Fig. 5(d) is an XPS analysis graph with regard to Regions (1) and (2). Referring to Fig. 5(d), it can be seen that Regions (1) and (2) have substantially the same intensity in analysis of Regions (1) and (2) at a core level of N 1s.
- [72] Through this analysis, it can be seen that the concentration of Ga is relatively high on the surface of the nitride semiconductor having the transfer pattern and high surface roughness. In other words, since the mask elements are formed on the transfer element region of the transfer pattern before separating the growth substrate, laser beams having relatively low energy enter the surface so that relatively less decomposition occurs, thereby causing Ga to have a relatively high concentration.

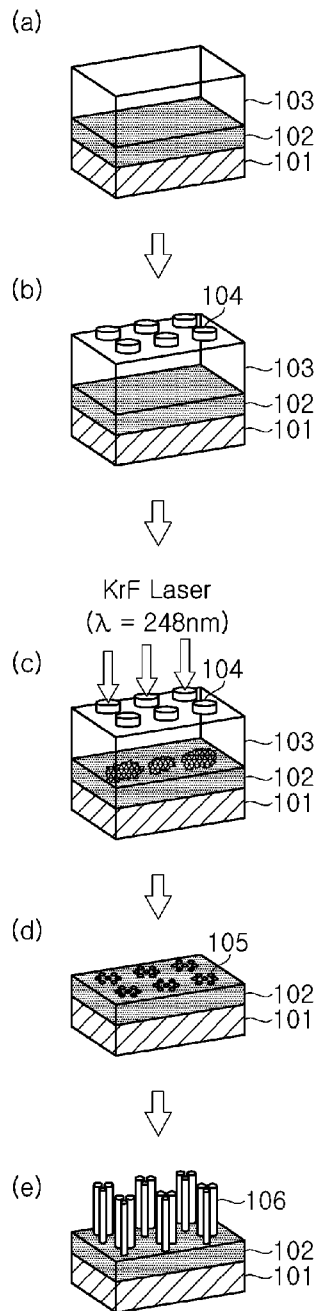
- [73] Fig. 6 shows scanning electron micrographs (SEM) of zinc oxide nanorods grown on a transfer pattern according to an exemplary embodiment of the present invention. A sapphire substrate having a thickness of 380 μm was used as a growth substrate, and aluminum oxide (Al_2O_3) having a thickness of 500 nm was used as a mask pattern. In addition, laser beams were emitted at about 600 mJ for laser lift-off. Zinc oxide nanorod arrays were grown through hydrothermal synthesis under conditions of a growing temperature of 90 °C and a molarity of 25 mM.
- [74] Referring to Fig. 6, it can be seen that the zinc oxide nanorods 106 are selectively grown to form arrays in a region having the transfer pattern 105 formed thereon. In addition, the zinc oxide nanorods 106 are formed to have a ring shape corresponding to the respective transfer elements of the transfer pattern 105. Thus, it can be confirmed that the transfer pattern 105 serves as a seed for growing the zinc oxide nanorods 106. On the other hand, the arrays of the zinc oxide nanorods 106 may be applied to various semiconductor devices, for example, pressure or gas sensors, nano generators, and, in particular, to nano devices. Further, in the method of manufacturing nanorod arrays according to the present invention, as shown in Fig. 6, the nanorod arrays may include at least one unit array, which may include nanorods arranged in a ring shape. The nanorods may be irregularly arranged in a ring shape. The nanorods may be formed of various materials in accordance with purposes of use. In particular, the nanorods may include zinc oxide.
- [75] The method of manufacturing zinc oxide nanorod arrays according to the embodiments of the present invention can be easily incorporated into a typical semiconductor process. In addition, the manufacturing method employs photolithography and laser processes, thereby providing high reproducibility. Further, since the zinc oxide nanorods are grown at low temperature through hydrothermal synthesis, the method according to the present invention has economic feasibility and is applicable to a large area process.
- [76] Although some embodiments have been disclosed herein, it should be understood by those skilled in the art that these embodiments are given by way of illustration only, and that various modifications, variations, and alterations can be made without departing from the spirit and scope of the present invention. Thus, the embodiments and the accompanying drawings disclosed herein are not to limit the present invention, but to illustrate the present invention. That is, the scope of the present invention is not limited by the embodiments and the accompanying drawings. Therefore, the scope of the present invention should be limited only by the accompanying claims and equivalents thereof.

Claims

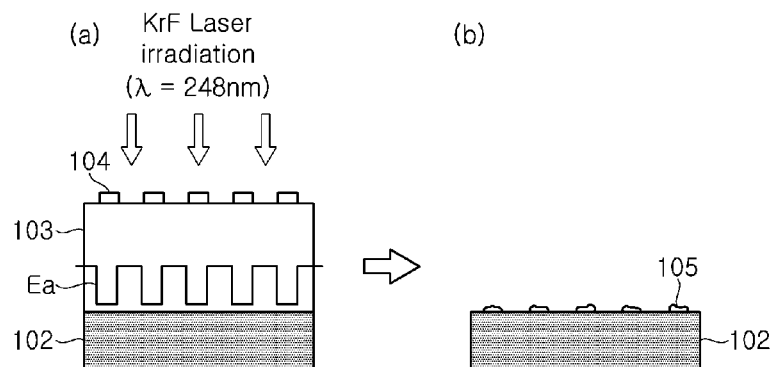
- [Claim 1] A method of manufacturing zinc oxide nanorod arrays, comprising:
preparing a growth substrate having a first surface and a second surface;
growing a nitride semiconductor layer on the first surface of the growth substrate;
placing a support substrate on the nitride semiconductor layer;
forming a mask pattern on the second surface of the growth substrate;
and
removing the growth substrate from the nitride semiconductor layer by providing a laser beam through the second surface of the growth substrate having the mask pattern.
- [Claim 2] The method of claim 1, further comprising:
growing zinc oxide nanorod arrays by applying hydrothermal synthesis to the nitride semiconductor layer from which the growth substrate is removed.
- [Claim 3] The method of claim 2, wherein the hydrothermal synthesis employs a mixed solution of zinc salt and hexamethylenetetramine.
- [Claim 4] The method of claim 3, wherein the mixed solution has a molarity of 0.0001M to 1M.
- [Claim 5] The method of claim 1, wherein the mask pattern is formed by a lift-off process.
- [Claim 6] The method of claim 5, wherein the mask pattern comprises one of oxide, nitride, organic and polymer materials.
- [Claim 7] The method of claim 5, wherein the lift-off process comprises forming a mask layer on a photoresist pattern and removing the photoresist pattern, the mask layer being formed by thermal deposition, electron-beam evaporation, or sputtering.
- [Claim 8] The method of claim 6, wherein the oxide comprises Al_2O_3 , MgO , ZnO , NiO , ITO or SiO_2 .
- [Claim 9] The method of claim 1, wherein the nitride semiconductor layer comprises a p-type semiconductor doped with p-type impurities, an n-type semiconductor doped with n-type impurities, or an undoped semiconductor.
- [Claim 10] The method of claim 1, wherein the support substrate comprises Si, Cu, Ni, polydimethylsiloxane (PDMS), polyethylene terephthalate (PET), or polyurethane acrylate (PUA).

- [Claim 11] The method of claim 1, wherein the growth substrate comprises a sapphire substrate, the sapphire substrate having a thickness of 100 μm to 1000 μm .
- [Claim 12] The method of claim 1, wherein the mask pattern comprises masking elements separated from each other, the masking elements having a width of 2 μm to 100 μm , a distance between the masking elements ranging from 2 μm to 100 μm .
- [Claim 13] The method of claim 12, wherein the masking elements have a thickness from 100 nm to 1000 nm.
- [Claim 14] The method of claim 1, wherein the laser beam has a wavelength of 248 nm and an energy of 400 mJ to 700 mJ.
- [Claim 15] The method of claim 1, wherein the growth substrate comprises a sapphire substrate, a nitride substrate, or a SiC substrate.
- [Claim 16] The method of claim 1, further comprising:
applying surface treatment to a surface of the nitride semiconductor layer, from which the growth substrate is removed, with ultraviolet/ozone (UVO), oxygen plasma, nitrogen plasma, or argon plasma.
- [Claim 17] The method of claim 16, wherein the surface treatment using UVO is performed for 1 minute to 60 minutes.
- [Claim 18] Nanorod arrays manufactured by the method according to any one of claims 1 to 17.
- [Claim 19] A semiconductor device comprising:
a substrate; and
nanorod arrays comprising unit arrays arranged on the substrate, wherein nanorods within the unit array are arranged in a ring or plate shape.
- [Claim 20] The semiconductor device of claim 19, wherein the nanorods comprise zinc oxide.
- [Claim 21] The semiconductor device of claim 19, wherein the nanorods within the unit array are irregularly arranged in a ring or plate shape.
- [Claim 22] The semiconductor device of claim 19, further comprising:
a nitride semiconductor layer placed on the substrate, wherein the nanorod arrays are placed on the nitride semiconductor layer.

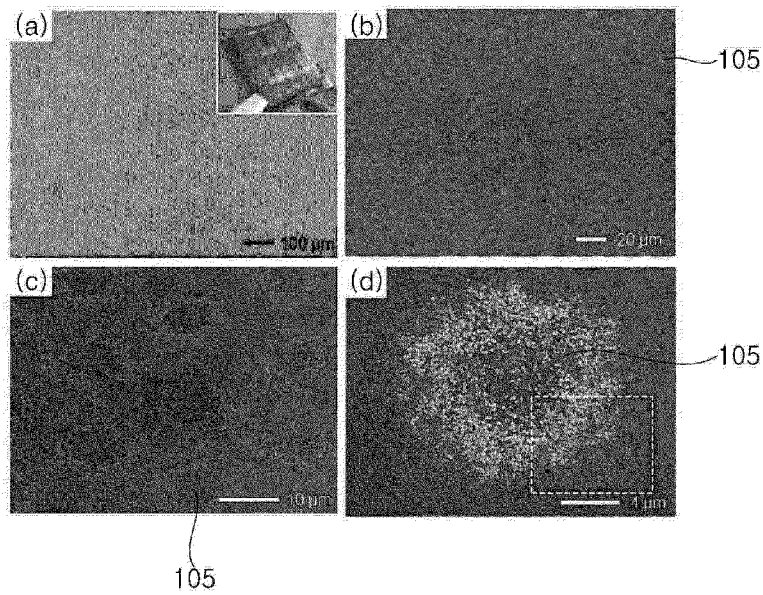
[Fig. 1]



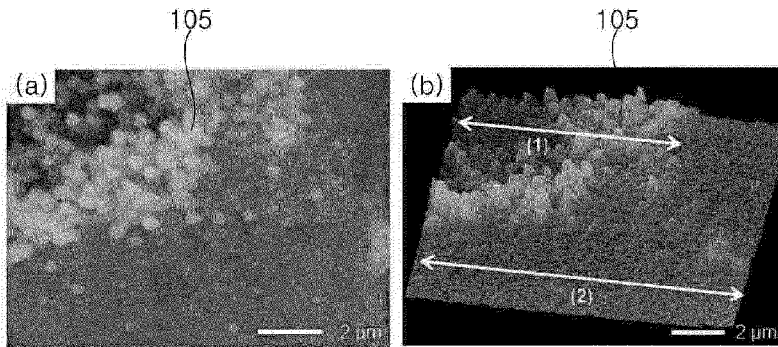
[Fig. 2]



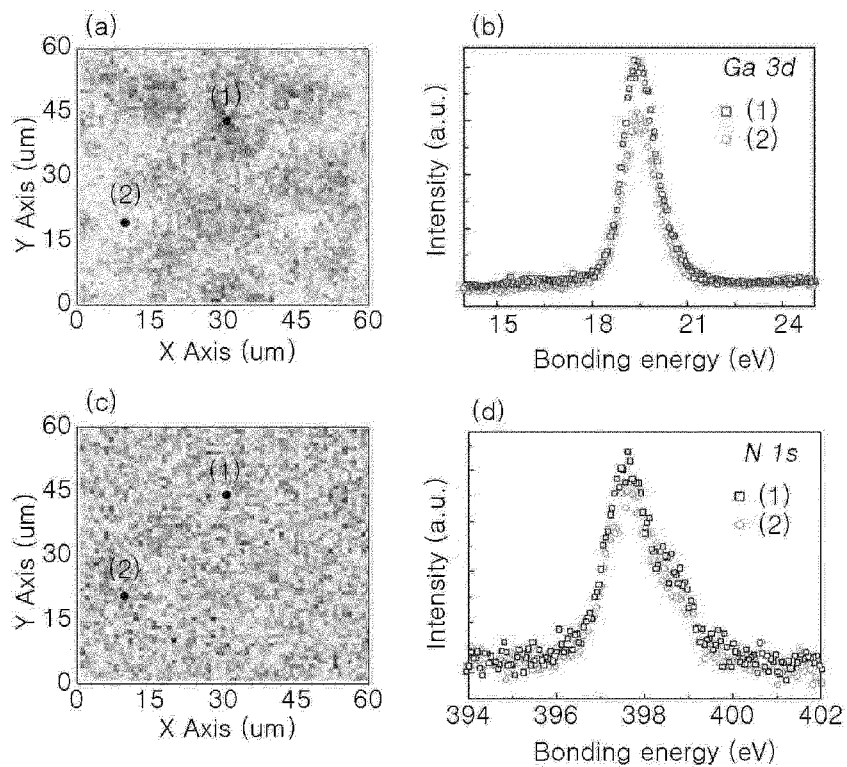
[Fig. 3]



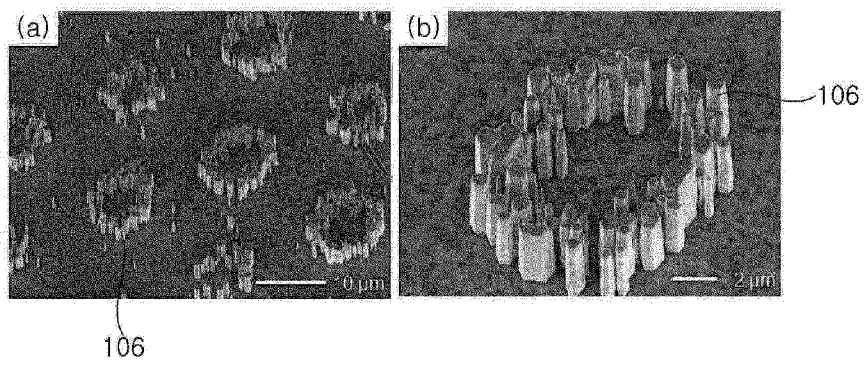
[Fig. 4]



[Fig. 5]



[Fig. 6]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2014/004170**A. CLASSIFICATION OF SUBJECT MATTER****B82B 3/00(2006.01)i, C01G 9/02(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

B82B 3/00; H01L 33/28; B32B 3/10; C30B 25/00; H01L 21/00; C01G 9/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: zinc oxide, nanorod array, nitride semiconductor, laser beam, mask pattern, hydrothermal synthesis

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CHIU, C. H. et al. "Enhancement of Light Output Intensity by Integrating ZnO Nanorod Arrays on GaN-Based LED Vertical LEDs", Electrochemical and Solid-State Letters, 11 (4) pages H84-H87, 2008 See abstract; figure v, Device Fabrication of page H84.	1, 5-15, 18-22
Y		2-4, 16, 17
Y	KR 10-2012-0077596 A (POSTECH ACADEMY-INDUSTRY FOUNDATION et al.) 10 July 2012 See abstract; claims 1-3 and 8; paragraph [0038].	2-4, 16, 17
A		1, 5-15, 18-22
A	US 8110417 B2 (YANG, JONG IN et al.) 7 February 2012 See abstract; claims 1-9.	1-22
A	US 2008-0107876 A1 (YI, GYN-CHUL et al.) 8 May 2008 See abstract; claims 1-24.	1-22
A	ZANG, KE YAN et al., "A New Method for Lift-off of Ill-Ni tride Semiconductors for Heterogeneous Integration", Nanoscale Res Lett, 2010, 5 pages 1051-1056. See abstract.	1-22

II Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

03 September 2014 (03.09.2014)

Date of mailing of the international search report

03 September 2014 (03.09.2014)

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan City, 302-701,
Republic of Korea

Facsimile No. +82-42-472-7140

Authorized officer

HONG, Sung Ran

Telephone No. +82-42-481-5405



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2014/004170

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-2012-0077596 A	10/07/2012	None	
US 8110417 B2	07/02/2012	DE 102009020819 AI JP 2010-098288 A JP 5130435 B2 KR 10-1018179 B1 KR 10-2010-0042438 A US 2010-0099212 AI us 2011-0008924 AI us 7816284 B2	22/04/2010 30/04/2010 30/01/2013 28/02/2011 26/04/2010 22/04/2010 13/01/2011 19/10/2010
us 2008-0107876 AI	08/05/2008	KR 10-0767284 B1 KR 10-20070096607 A	17/10/2007 02/10/2007