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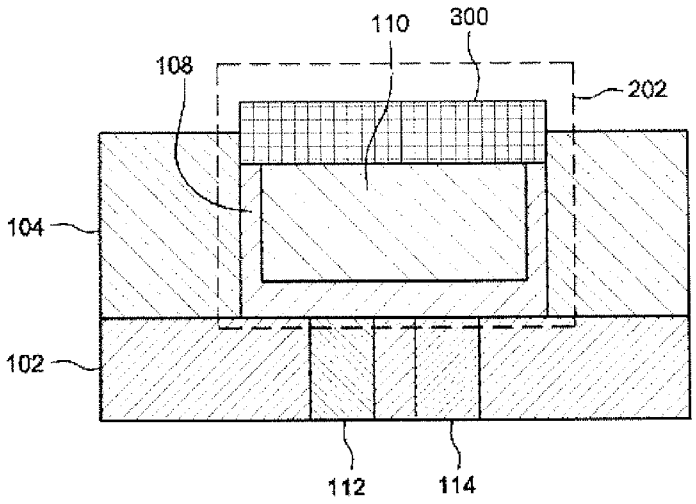
(54) **Title**: METHOD FOR FORMING A METAL CAP IN A SEMICONDUCTOR MEMORY DEVICE

[Fig. 3]



(57) **Abstract**: Exemplary embodiments of the present invention are directed towards a method for fabricating a semiconductor memory device comprising selectively depositing a material to form a cap (300) above a recessed cell structure (202) in order to prevent degradation of components inside the cell structure in oxidative or corrosive environments.

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Description

Title of Invention: METHOD FOR FORMING A METAL CAP IN A SEMICONDUCTOR MEMORY DEVICE

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of US Priority Patent Application US14/283539 filed May 21, 2014, the entire contents of each which are incorporated herein by reference.

Technical Field

[0002] Certain embodiments of the disclosure relate to forming a semiconductor device. More specifically, embodiments of the disclosure relate to a method for forming a metal cap in a semiconductor memory device.

Background Art

[0003] Recently, the requirements on nonvolatile memory chips' storage capacity and power consumption have been advancing rapidly. Development of miniaturized and high-speed semiconductor elements is progressing at a similar pace. Resistance varying memory device are being used more often to replace flash memory devices. A resistance varying memory device employs a variable resistance element as a storage element. The resistance varying memory device includes, but is not limited to, ReRAM (Resistive RAM), CBRAM (Conductive Bridging Random Access Memory), phase change RAM (PCRAM), and the like. In a typical resistive memory device, cell material is deposited on a substrate using a conventional method, such as CVD, PVD, or plating. The cell material can be homogenous or non-homogeneous, e.g., consisting of multiple layers. The substrate, including bottom electrodes, can be homogenous or nonhomogeneous, e.g., a combination of metal contacts and a dielectric. A conductive metal layer is deposited on the cell material, acting as the top electrode. Generally, the cell material resistance is changed, for example, from a high-resistance state to a low-resistance state, when a certain voltage is applied to the top electrode.

Summary

[0004] However, it is difficult to make such a memory cell structure using photoresist masking and plasma etching, because the cell material tends to be complex and may, for example, consist of multiple transitional metal elements. Thus, these advanced cell materials cannot be patterned easily by commercially available dry etching methods. Accordingly, a damascene process is generally used to fabricate the cell structures, where a thick layer (acting as a template layer) is deposited on a substrate and patterned with open trenches where cell material will be deposited. A thick coating of the cell material is then deposited that significantly overfills the trenches in the

template layer. The excess cell material above the template layer (referred to as overburden) is removed through chemical-mechanical planarization (CMP), and the template layer is exposed. The template layer is selectively removed or exhumed via a chemical method, a wet strip or a dry strip, and isolated cell structures are fabricated.

[0005] However, during the exhumation, the top of the cell materials is impacted or damaged through oxidization or corrosion because of the dry/wet chemical reactions. This degrades the top electrode conductivity and the cell material performance.

[0006] Therefore there is a need in the art for a method for forming a semiconductor memory device without degradation of the cell material in accordance with exemplary embodiments of the present invention.

[0007] A method for forming a metal cap in a semiconductor memory device is provided substantially as shown in and/or described in connection with at least one of the figures, as set forth more completely in the claims.

[0008] These and other features and advantages of the present disclosure may be appreciated from a review of the following detailed description of the present disclosure, along with the accompanying figures in which like reference numerals refer to like parts throughout.

Brief Description of Drawings

[0009] [fig.1]Fig. 1 depicts a first step in a fabrication process in accordance with exemplary embodiments of the present invention.

[fig.2]Fig. 2 depicts a second step in the fabrication process in accordance with exemplary embodiments of the present invention.

[fig.3]Fig. 3 depicts a third step in the fabrication process in accordance with exemplary embodiments of the present invention.

[fig.4]Fig. 4 depicts a fourth step in the fabrication process in accordance with exemplary embodiments of the present invention.

Description of Embodiments

[0010] Certain implementations may be found in a selectively formed metal cap in a memory cell structure. According to one embodiment, a memory cell can be formed with a damascene process. Namely, a template layer is patterned and etched to form trenches, active cell material and a first metal layer are deposited forming structures in the trenches, and then the structures in the trenches are isolated by a chemical-mechanical planarization (CMP). The exposed first metal surface is cleaned and selectively covered with a cap which comprises a second metal. The second metal has some resistance to oxidation and/or corrosion. The template layer is selectively removed by plasma enhanced oxidation, known as exhumation, or by chemical dissolving. The top surface of the active cell material and the top electrode are

protected by the cap layer during template layer removal. The memory cell may be resistive RAM (ReRAM), conductive-bridge RAM (CB-RAM) cell, phase change memory (PCRAM), or the like.

[0011] Figs. 1-4 depict a method for forming a metal cap in a semiconductor memory device 100 in accordance with exemplary embodiments of the present invention.

[0012] Fig. 1 depicts a first step in a fabrication process of the device 100. The result of a damascene process is the structure shown in Fig. 1, where a substrate 102 has a first contact 112 and a second contact 114 (bottom electrode contacts - BEC). Those of ordinary skill in the art will recognize that the substrate 102 may contain a single contact, or a plurality of contacts, depending on the usage of the resulting device 100 and the present invention does not limit the device 100 to having merely two contacts. The metal contacts 112 and 114 are electrically conductive, acting as bottom electrodes, and are fabricated through a substrate layer 102 which contains dielectric material such as silicon oxide, silicon nitride, or the like. This dielectric layer 102 separates the active cell material 108 from an active semiconductor base material (not shown in Fig. 1, but well known to those of ordinary skill in the art). The active semiconductor base material can be a terminal, for example, a gate terminal, of a transistor. In some embodiments such a transistor is a metal-oxide-semiconductor field-effect transistor (MOSFET) for amplifying or switching electronic signals. A template layer 104 sits atop the substrate 102. A trench 105 is formed in the template layer 104 during the damascene process. Cell material 108 is deposited on and lines the trench 105. A first metal layer 110 is formed above the cell material 108 to fill the trench 105. The first metal layer 110 will form the top electrode. In some embodiments, copper is chosen as the first metal layer 110 to achieve a low resistance cell metal line. In other embodiments, the metal layer 110 may be Cu, Au, Ta, Ru, Pt, W, Ti, Poly, or the like. The template layer 104 may be comprised of Carbon, PolySilicon, Silicon oxide, or the like.

[0013] Fig. 2 depicts a second step in the fabrication process in accordance with exemplary embodiments of the present invention. Chemical-mechanical planarization (CMP) is performed to remove the bulk of the first metal layer 110 and a portion of the cell material 108. The planarized first metal layer 110 and the cell material 108 form the cell structure 202, which is recessed from the plane of the template layer 104. According to one embodiment, the CMP process uses traditional CMP abrasives such as colloidal silica, fumed silica, or colloidal alumina. The first metal layer 110 and the cell material 108 are removed by mechanical actions and/or chemical modification during the CMP. When the template layer 104 is exposed by CMP, the friction between the wafer surface and the polishing pad might change significantly, and a friction-based endpointed process control method becomes feasible. Similarly, wafer

surface optical reflection strength might change significantly when the template layer 104 is exposed by CMP and this makes an optical friction-based end-pointed process control method feasible. After the change in process traces (such as friction trace or optical reflection trace) is captured, over-polishing begins. Over-polishing results in the cell material 108 receding beneath the plane of the template layer 104, leaving a recess 200. The depth of the recess 200 is mostly determined by the over-polish time. Over polishing also fully exposes the surface of the template layer 104 so that it will be consumed later with an exhumation method. After the CMP, a wet clean process is performed to remove any oxidized surface metal and to expose a fresh surface of the first metal layer 110 in the trench 105. The fresh surface aids in the selective deposition the cap material in recess 200 at a later stage described in Fig. 3. In some embodiments, the cap material to be deposited in recess 200 is W or Ti, both of which have stronger resistance to corrosion than copper (namely, the first metal layer 110) or the active cell material 108. The cell structure 202 is more stable when a wet clean process is applied onto the wafer after the template layer 104 is exhumed, in order to remove various polymer residuals generated during plasma enhanced exhumation. According to some embodiments, a plasma-based dry etch method selectively removes the template layer 104 while the cell material 108 remains. In some cases, highly active chemical species may be generated when the template layer 104 is exhumed, producing solid byproducts over the surface of the cell structure 202. According to one embodiment, these by-products are selectively removed by a wet clean method using some acidic or basic aqueous solution. This process is generally referred to as the post-etch clean, well known to those of ordinary skill in the art. Copper is sensitive to this clean. W and Ti are immune to such wet clean.

[0014] Fig. 3 depicts a third step in the fabrication process in accordance with exemplary embodiments of the present invention. A material is selectively deposited as a cap 300 in the recess 200 on the fresh surface of the first metal layer 110, to protect the cell structure 202, and specifically to protect the first metal layer 110 from any chemical reaction that may be caused when the template layer 104 is selectively removed. The cap 300 is only deposited in the recess 200 and is not deposited on the template layer 104. The template layer 104 is still exposed after cap 300 formation. In some embodiments, the cap 300 may be formed using W, Ti, Co, or the like, able to be selectively deposited over the first metal layer 110. As an example, according to one embodiment, the selective depositing of the elemental tungsten is by chemical vapor deposition within a deposition chamber using gaseous WF_6 and SiH_4 as deposition precursors which are fed to the chamber during the deposition. Inert and/or other gases may be fed to the chamber during the deposition. In this embodiment during the deposition, substrate temperature is from approximately 250°C to 350°C, chamber

pressure is from approximately 1 mTorr to 100 mTorr, WF_6 flow rate to the chamber is from approximately 10 sccm to 1,000 sccm, and SiH_4 flow rate to the chamber is from approximately 5 sccm to 50 sccm. An example inert gas flow rate (e.g., Ar) is approximately 0 sccm to 1,000 sccm. Those of ordinary skill in the art will recognize that these ranges are not specifically required and other ranges may be used in the implementation of the present invention.

[0015] A W Cap or Ti Cap has resistance to corrosion during a wet clean, which further prevents corrosion of the first metal layer 110 (e.g., a Cu layer). In some embodiments, the cap 300 is a selective dielectric cap using materials such as SiN, SiOx, and high-k dielectrics such as HfOx, AlOx, ZrOx, and the like. According to exemplary embodiments, the selective metal or selective dielectric is deposited by one of chemical vapor deposition (CVD), atomic layer deposition (ALD), selective electroless plating or the like. In some embodiments, the cap 300 can be sacrificial, i.e., the cap 300 can be selectively removed by dry etch technology after template layer 104 exhumation.

[0016] Fig. 4 depicts a fourth step in the fabrication process in accordance with exemplary embodiments of the present invention. The template layer 104 is selectively removed via a dry process or a wet process. According to exemplary embodiments, if the template layer 104 is carbon, oxygen-containing plasma is used for the exhume process. If the template layer is polysilicon, exhumation can be performed using F-containing plasma dry etch. In another embodiment where the template layer 104 is comprised of silicon oxide, an HF containing aqueous solution is used for the exhumation process. Those of ordinary skill in the art will recognize that the exhumation process will conform to the material used to form the template layer 104. Due to the formation of the cap 300 above the first metal layer 110, the top surface of the metal layer 110 in the cell structure 202 is prevented from oxidation or corrosion during exhumation and is well preserved as compared to exhume processes where the copper layer is not protected. However, part of the side wall of the active cell material 108 might be oxidized or chemically modified, shown as the sidewall film 400 in Fig. 4. The sidewall film 400 becomes a barrier to isolate the inner cell structures 108 and 110 from various chemical reactions outside. While the present disclosure has been described with reference to certain embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted without departing from the scope of the present disclosure. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the present disclosure without departing from its scope. Therefore, it is intended that the present disclosure not be limited to the particular embodiment disclosed, but that the present disclosure will include all embodiments falling within the scope of the appended claims.

Claims

[Claim 1] A method for fabricating a semiconductor memory device comprising:
selectively depositing a material to form a cap above a recessed cell structure in order to prevent degradation of components inside the cell structure in oxidative or corrosive environments.

[Claim 2] The method of claim 1, wherein selectively depositing the cap material further comprises:
using one of chemical vapor deposition, atomic layer deposition or selective electroless plating for deposition.

[Claim 3] The method of claim 1, further comprising removing the cap using a dry etch method.

[Claim 4] The method of claim 1 further comprising:
performing the selective depositing after a chemical-mechanical planarization is performed on the material used to form the recessed cell structure.

[Claim 5] The method of claim 4 wherein the recessed cell structure comprises a low resistance top electrode and active cell material, and the cell structure is formed in a trench in a template layer.

[Claim 6] The method of claim 5 wherein the selective cap is a metal cap formed using one of W, Ti, or Co.

[Claim 7] The method of claim 5 further comprising:
performing a chemical-mechanical planarization (CMP) process to form the recessed cell structure prior to selectively depositing the material forming the cap.

[Claim 8] The method of claim 7, wherein the cap is a metal cap formed of one of W, TiN, TaN, Ta or TiW.

[Claim 9] The method of claim 7, wherein the cap is a dielectric cap formed of one of SiN, SiOx, HfOx, AlOx or ZrOx.

[Claim 10] A device comprising:
a recessed cell structure formed in a trench atop a substrate, the trench created by a damascene process; and
a cap formed above the recessed cell structure to protect the recessed cell structure from degradation.

[Claim 11] The device of claim 10 wherein the cap is formed by a selective deposition.

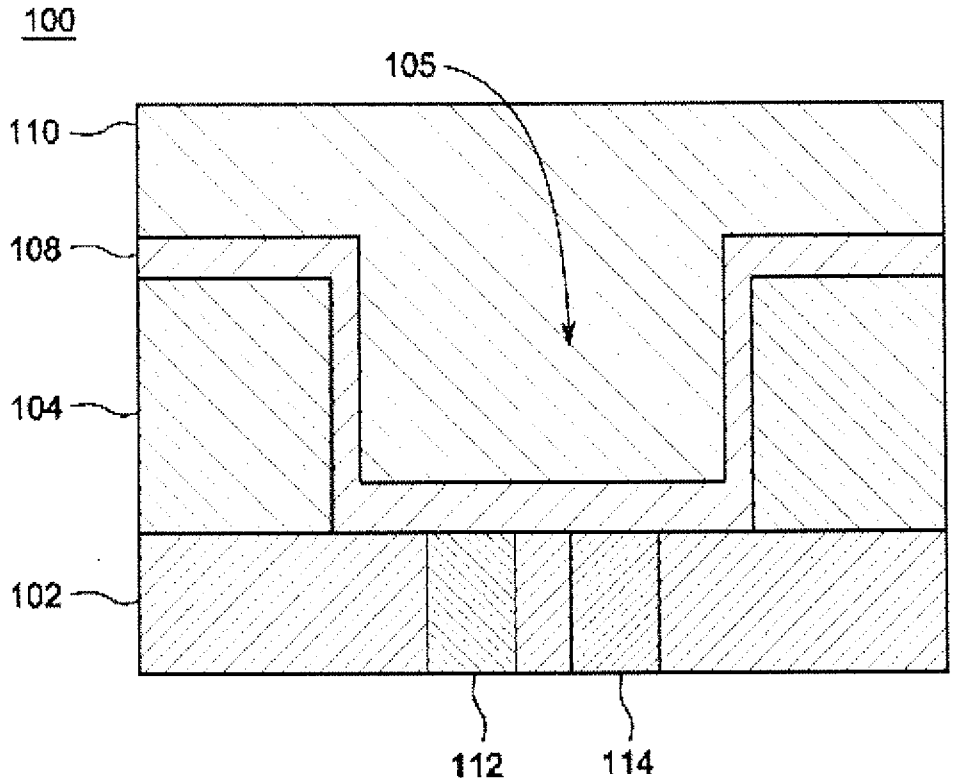
[Claim 12] The device of claim 11 forming a memory cell, wherein the memory cell is a resistive RAM (ReRAM) cell, conductive-bridge RAM

(CB-RAM) cell, or a phase change memory (PCRAM) cell.

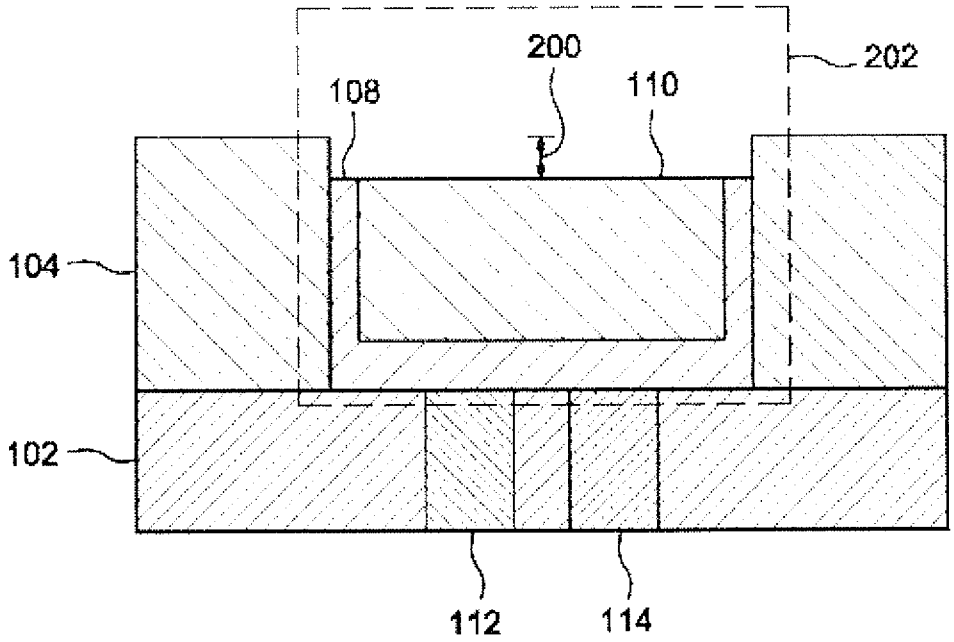
[Claim 13] The device of claim 11 wherein the cap is a dielectric cap or a metal cap.

[Claim 14] The device of claim 13, wherein the metal cap is formed using one of W, TiN, TaN, Ta or TiW, and the dielectric cap is formed using one of SiN, SiOx, or a high-k dielectric.

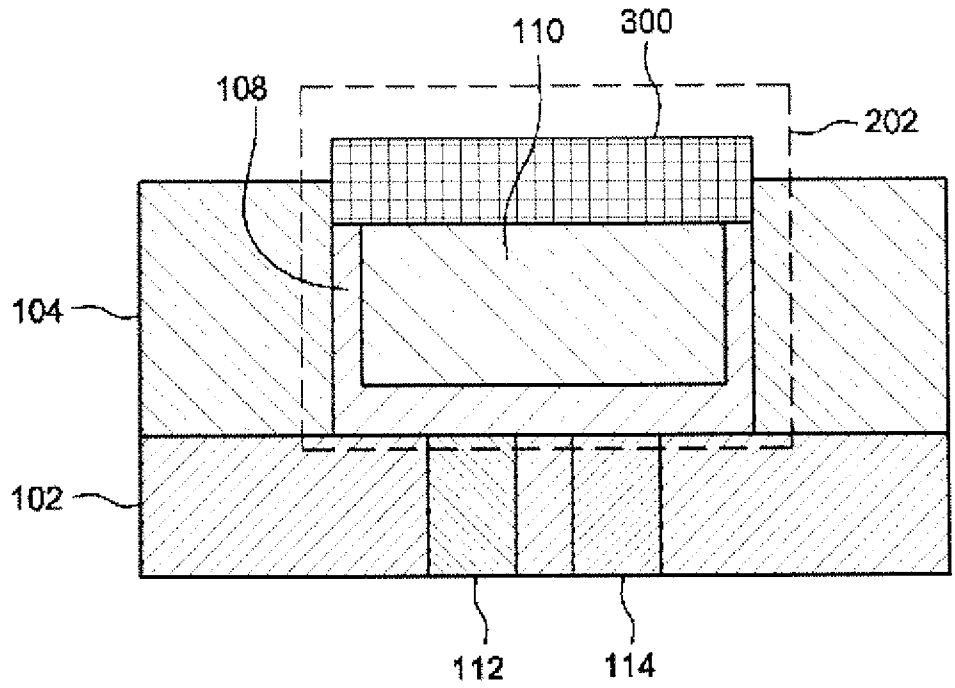
[Fig. 1]



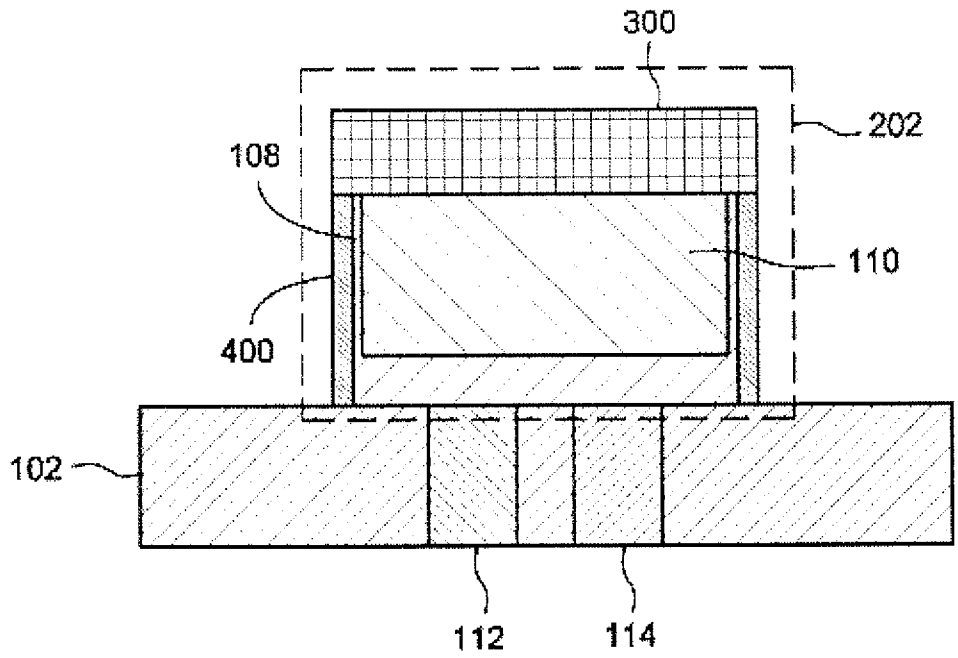
[Fig. 2]



[Fig. 3]



[Fig. 4]



INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2015/002281

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L45/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, COMPENDEX, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X Y	US 2006/094236 A1 (ELKINS ET AL) 4 May 2006 (2006-05-04) paragraphs [0034] - [0038] figure 8	1,2,4, 10-14 3,5-9
Y	US 2014/124726 A1 (OH) 8 May 2014 (2014-05-08) paragraphs [0106], [0108] figure 3N+P	1-14
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
29 July 2015	05/08/2015

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No
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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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