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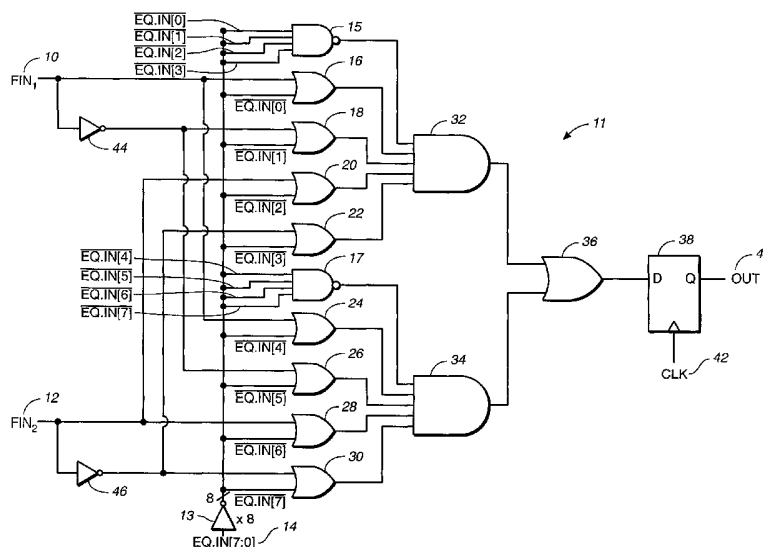
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(54) Title: SPARE CELL ARCHITECTURE FOR FIXING DESIGN ERRORS IN MANUFACTURED INTEGRATED CIRCUITS



(57) Abstract: A fully self-sufficient configurable spare gate cell (11) has two types of inputs: a functional input bus (FIN; 10,12; 68; 76) and an equation input bus (EQ.IN; 70; 78), whereby the spare gate cell can be transformed into any sum of product operator by the assertion of certain signals to the equation input bus. The spare cell may also include a D flip-flop (38; 84). In a spare state, the functional input buses are connected to an area of pre-defined logic (64) where the need for bug fixes are high. Thus, the spare cell would be automatically placed close to the bug-fix area during the place-and-route phase of chip design, thereby reducing the need to look for routing channels.



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Description

SPARE CELL ARCHITECTURE FOR FIXING DESIGN
ERRORS IN MANUFACTURED INTEGRATED CIRCUITS

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TECHNICAL FIELD

The present invention relates to a method and apparatus for the repair of integrated circuits. In particular, the present invention relates to spare cell architecture and the placement and the connection thereof in integrated logic circuits.

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BACKGROUND ART

Although a variety of tools and techniques are available to check and verify a new integrated circuit (IC) design before it is submitted to the manufacturing line for production, there are design errors that cannot be detected until the design has been fully implemented, fabricated and tested at wafer and/or module level. In memory and logic circuits, redundancy can be built into the design so that spare cells are available for repair purposes. Once a design defect has been identified, it has to be isolated and replaced, or connected in a different manner or way. The isolation is typically performed by a focused ion beam (FIB), which cuts off connections to the defective cell by ion sputtering. With the addition of reactive gases and adjustments to operating parameters, ion-induced deposition of conductive material can be performed as well. This provides chip designers with the ability to evaluate the result of a fix before committing to a design change by metal layer change that is cost effective, as the designers could use a FIB machine to validate the fix before generating a new metal layer.

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Replacement comes in the form of spare cells that are typically scattered around the IC. A traditional way to repair such design defects in logic circuits is to scatter redundant logic gates, such as AND gates and OR gates, around the circuit to be used as replacements. This method is acceptable so long as the defective circuit elements being replaced are also simple AND or OR gates. Complications arise when a replacement cell is needed for a more complicated logic function. For instance, to replace an XOR function, one would need to connect together two AND gates and one OR gate. However, since the simple logic gates are typically individually scattered around the circuit, the wiring that is required to string them together can get quite convoluted. Furthermore, as more and more components are being packed into smaller and smaller chip spaces, it is becoming more difficult to find routing paths to wire the simple replacement gates together to form a more advanced gate and to redirect the inputs and outputs of the defective logic. An alternative would be to scatter a complete library of logic functions throughout the circuit. However, this is not a cost effective solution because only a few of the functions in the library will be used and a lot of them will sit idle.

A more versatile solution calls for the use of configurable logic blocks. For instant, U.S. Patent No. 6,255,845 to Wong et al. teaches the combination of one or more inverters with a configurable logic building block, like a multiplexer, to form a spare cell that can be configured to perform a plurality of different logic-gate functions. Initially, the inputs and outputs of the inverters and the configurable logic block are not connected together in any particular manner. In their spare state, the inputs of all circuits within the spare cell are tied to a reference voltage, e.g. Vcc or Vss,

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available on the IC. To use the spare cell, one or more input connections to the reference voltage are cut, and the inputs and outputs are selectively interconnected to each other and/or to signals and elements of the pre-defined logic circuit on the chip. The teachings of Wong et al. help reduce the number of spare cells needed, as well as the number of connection needed to form advanced gates. However, in some cases, routing paths may need to be found to bridge the inverters to the reconfigurable logic block, and, if necessary, from the reconfigurable logic block to a flip-flop. Since the dense circuitry used in most IC chips causes it to be difficult to find routing paths and since making electrical connections with FIB is a slow process, one objective of the present invention is to provide a spare cell structure that does not require as many internal connections to activate. The spare cell logic described in the Wong et al. patent does not take into account the path routings for any logic equation that can be implemented by the spare cells.

Another critical problem confronting IC layout designers is the need to have a balanced clock tree in order to maintain synchronous logic. However, the need to connect clock pins of the flip-flops through routing paths of unpredictable distances to the existing clock trees can easily disrupt a delicately balanced clock tree. Therefore, it is another objective of the present invention to provide a spare cell structure that does not upset a predefined balanced clock tree.

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SUMMARY OF THE INVENTION

The above objectives have been achieved by spare cells in the form of configurable combinatorial networks (CCN) that are placed strategically throughout a custom IC as spare cells. The spare cells can be

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configured to perform a variety of Sum of Product (e.g. XOR, NOR, or more complex logical functions) logic functions, without the need for additional inverters, by connecting either a power supply or ground to specific locations using metal layer modification. There are two input buses feeding into a CCN: a functional input bus and an equation input bus; each of these buses having different functions. The output of the CCN can be connected to a D flip-flop (DFF) having its clock pin connected to a predefined clock tree. The functional input bus carries data for the CCN, while the equation input bus carries the configuration control signals that specify the function of the CCN.

To facilitate efficient FIB repairs, the spare cell CCN, and DFFs are placed (during the integrated circuit's design phase) near a logic area where a need for defective cell replacement is determined to be highly probable. Connection paths between a spare cell and the nearby logic area are defined in such a way that automatic placement routing is guaranteed to be present near the desired logic area, so that the activation of the CCN would not upset the delicately balanced clock tree.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a logic circuit diagram of a preferred embodiment of a spare cell of the present invention, which is in the form of a configurable combinatorial network (CCN) and associated D flip-flop (DFF).

Fig. 2 is a block diagram showing a way to connect a spare cell to a pre-defined logic area without a DFF.

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Fig. 3 is a block diagram showing another way to connect a spare cell to a pre-defined logic area with a DFF.

5 BEST MODE FOR CARRYING OUT THE INVENTION

In the preferred embodiment of the present invention, as shown in Figure 1, the spare cell 11 is made up of a plurality of OR gates having a first and second inputs, acting as input gates for a first and second functional input terminals FIN1 10 and FIN2 12 and an equation input bus terminal EqIN 14 that carries a first equation input signal line EQIN[0], a second equation input signal line EQIN[1], a third equation input signal line EQIN[2], a fourth equation input line EQIN[3], a fifth equation input line EQIN[4], a sixth equation input line EQIN[5], a seventh equation input line EQIN[6] and an eighth equation input signal line EQIN[7]. The equation input lines EQIN[7:0] are negated by a first bank of eight inverters 13, one for each equation input line. The first functional input terminal 10 is connected to the first inputs of first and second OR gates 16 and 24 and the input of a second inverter 44. The output of the second inverter 44 is connected to the first inputs of a third and fourth OR gates 18 and 26. The second functional input terminal 12 is connected to the first inputs of fifth and sixth OR gates 20 and 28, and to an input of a third inverter 46. The output of the third inverter is connected to the first input of seventh and eighth OR gates 22 and 30. The first equation input signal line EQIN[0] connects to the second input of the first OR gate 16. The second equation input signal line EQIN[1] connects to the second input of the third OR gate 18. The third equation input signal line EQIN[2] connects to the second input of the fifth OR gate 20. The fourth equation input signal line EQIN[3] connects to

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the second input of the seventh OR gate 22. The fifth equation input signal line EQIN[4] connects to the second input of the second OR gate 24. The sixth equation input signal line EQIN[5] connects to the second input of the fourth OR gate 26. The seventh equation input signal line EQIN[6] connects to the second input of the sixth OR gate 28. The eighth equation input signal line EQIN[7] connects to the second input of the eighth OR gate 30. The first four equation input signal lines EQIN[3:0] also connect to a first 4-input NAND gate 15 while the last four equation input signal lines EQIN[7:4] connect to a second 4-input NAND gate 17. The outputs of the first, third, fifth and seventh 2-input OR gates 16, 18, 20, 22 and the output of the first 4-input NAND gate 15 are connected to the inputs of a first 5-input AND gate 32. The outputs of the second, fourth, sixth and eighth OR gates 24, 26, 28, 30 and the output of the second 4-input NAND gate 17 are connected to the inputs of a second 5-input AND gate 34. The outputs of the first and second 5-input AND gates 32 and 34 are connected to inputs of a ninth 2-input OR gate 36. For applications where the output requires a D flip-flop (DFF), the output of the ninth 2-input OR gate 36 would be connected to the input of a DFF 38. The clock pin of the DFF 38 is connected to an existing clock tree in the predefined logic area where the need for a bug fix is probable. The scan data input pin of the DFF 38 can be connected to the logic scan chain of the predefined logic.

One of the strengths of the present invention lies in the fact that the CNN obeys a given formula as it is illustrated by the following example, wherein the replacement calls for an exclusive OR (XOR) gate. The logic equation for XOR gate can be expressed as follows:

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$$OUT = (FIN_1 \overline{FIN_2}) + (\overline{FIN_1} FIN_2)$$

The equation above may be mapped onto the CCN formula as shown below:

$$\begin{aligned} OUT[0] = & (\overline{FIN_2} + \overline{EQIN[7]}) \cdot (FIN_2 + \overline{EQIN[6]}) \cdot (\overline{FIN_1} + \overline{EQIN[5]}) \cdot \\ & (FIN_1 + \overline{EQIN[4]}) \cdot (EQIN[7] + EQIN[6] + EQIN[5] + EQIN[4]) \\ 5 \quad & + (\overline{FIN_1} + \overline{EQIN[3]}) \cdot (FIN_2 + \overline{EQIN[2]}) \cdot \\ & (\overline{FIN_1} + \overline{EQIN[1]}) \cdot (FIN_1 + \overline{EQIN[0]}) \cdot \\ & (EQIN[3] + EQIN[2] + EQIN[1] + EQIN[0]) \end{aligned}$$

This dictates that the output of the first and second 5-input AND gates 32 and 34 have to be $FIN_1 \overline{FIN_2}$ and $\overline{FIN_1} FIN_2$ respectively. In order to produce such outputs, the inputs to the first 5-input AND gate 32 should have a FIN_1 and a $\overline{FIN_2}$ and three 1s, while the inputs to the second 5-input AND gate 34 should have a $\overline{FIN_1}$ and a FIN_2 and three 1s. In order to present a FIN_1 and not $\overline{FIN_1}$ to the input of the first 5-input AND gate 32, the equation input $\overline{EQIN[0]}$ to the first 2-input OR gate 16 must be a "0" and the equation input $\overline{EQIN[1]}$ to the third 2-input OR gate 18 must be a "1". By the same token, in order to present a $\overline{FIN_2}$ but not a FIN_2 at the input of the first 5-input AND gate 32, the equation input $\overline{EQIN[2]}$ to the fifth 2-input OR gate 20 must be a 1 and the equation input the seventh 2-input OR gate $\overline{EQIN[3]}$ must be a "0". Since at least one of the four equation input signal lines is a 1, the output of the first 4-input NAND gate 15 must be a 1 as well. To provide a $\overline{FIN_1} FIN_2$ at the output of the second 5-input AND gate 34, the inputs must consist of a $\overline{FIN_1}$, a FIN_2 , and three 1s. This can be accomplished by sending a "1" to the equation input

$\overline{EQIN}[4]$ of the second 2-input OR gate 24, a "0" to the equation input $\overline{EQIN}[5]$ of the fourth OR gate 26, a "0" to the equation input $\overline{EQIN}[6]$ of the sixth OR gate 28, and a "1" to the equation input of the eighth OR gate 30

5 $\overline{EQIN}[7]$. Since at least one of the four equation input signal lines is a 1, the output of the second 4-input NAND gate 17 must be a 1 as well. So, in summary, in order to configure the CCN into an XOR gate, and taking into account the first inverter 13, the signals appearing
10 at the equation inputs of the eight 2-input OR gates $\overline{EQIN}[7:0]$ should have the following sequence: 0110 1001.

The first and second 4-input NAND gate 15, 17 are useful for generating simple function like AND and OR. For instance, to turn the CCN into a simple AND
15 gate, the formula to implement is:

$$OUT = FIN_1 \cdot FIN_2$$

The resulting signal at the equation input signal line
20 $\overline{EQIN}[7:0]$ would be 00000101. The four 1s in $\overline{EQIN}[7:4]$ ensure a 0 output from the second 4-input NAND gate 17, which in turn ensure a 0 output from the second 5-input AND gate 34.

These equation input signals 14 for the
25 equation input can be generated during defective cell replacement by connecting the second, third, fifth and eighth wires in the bus to the power supply using the FIB system and by leaving the remaining wires connected to the ground. To further minimize FIB repair or metal
30 layer reprocessing, one may connect the input bus to a special function register of the predefined logic that can be loaded with a specific eight digit binary number

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through any serial or parallel means such as SCAN, JTAG, and software user interface.

In today's highly modulized integrated circuits, a typical microcontroller might include a processor core, a memory module, an external bus interface, module, and internal bus, a plurality of timer modules, and various serial and parallel peripheral interface module, such as modules for universal synchronous asynchronous receiver transmitter (USART), universal serial bus (USB), and parallel bus. These modules are typically at various stages of development. Some of these module designs have been used repeatedly in various circuits and thus the need for defective cell replacement are low, while other circuits may have just been implemented for the first time and, thus, the chance for requiring bug fixes is high. Therefore, strategically placing spare cells near modules of the latter type would significantly reduce the routing distances and improve defect repair efficiency. However, current place-and-route tools tend to place unconnected spare cells randomly, with all of the inputs connected to ground. A place-and-route engineer will have to find routing paths in case of metal fix repair. The unique separation of inputs in the present invention enables a designer to connect the functional inputs of the spare cells to an area where the needs for defective cell replacement are highly probable without modifying the predefined functionality, while keeping the equation inputs connected to ground. This way, the spare cells would be automatically placed by the place-and-route tools near areas where defective cell replacement is most likely.

In Figure 2, an integrated circuit chip 60 with a plurality of peripheral functional modules such as a Universal Synchronous Asynchronous Receiver Transmitter

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(USART) 62, Universal Serial Bus (USB) 64 and Serial Peripheral Interface (SPI) 66 is shown. In the case where it has been determined that the USB 64 is the module with a high probability for requiring defective cell replacement, then during the design phase, the functional inputs 68 of the spare cells are connected to the existing functional signals (sequential or combinational gate outputs) of the USB 64 logic area where the need for defective cell replacement is most probable. As a result, not only will there be pre-existing routing paths for the functional inputs 68 that can be used for defective cell replacement, but also the place-and-route tool would automatically place the CCN 72 close to the USB 64 module, thereby reducing the distance of the routing paths for the output of the CCN 72.

For defective cell replacement that call for an output with a D flip-flop, an alternative connection, shown in Figure 3, is possible. In Fig. 3, the clock pin 74 of the DFF 84 in the spare gate cell 80 could be connected to a branch of a clock tree 82 in the USB 64 in its spare state, thereby eliminating the need of connecting the clock pin when defective cell replacement is needed, potentially inducing clock tree imbalance. Furthermore, since the clock pin connection 74 would force the place-and-route tool to place the DFF 84 close to the area of the chip where the need for defective cell replacement is high, and since the output of the CCN 86 is connected to the DFF 84, the functional inputs 76 would be located near defective cell replacement area, thereby reducing the potential routing distance of functional inputs 76.

Although only one embodiment of the configurable combinational logic has been shown in the proceeding paragraphs, one skill in the art will, after seeing the disclosed invention, quickly recognize that

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there are other ways to realize a sum of product logical function using simple combination logic cells. It is also possible that multi CCN could be connected together to form a single spare gate cell.

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Claims

1. In an integrated circuit having a plurality of
5 interconnected logic cells, potentially including at least one defective logic cell, a plurality of spare cells dispersed within the integrated circuit for the replacement of any said defective logic cells, each spare cell comprising:
- 10 a configurable combinatorial network (CCN) implementing any of a plurality of sum of product logical functions, said CCN having a plurality of equation input terminals that receive control signals which configure the CCN to perform one or more specified logical
15 functions, a plurality of functional input terminals and one or more output terminals selectively connectable to the integrated circuit in place of a defective logic cell, so as to receive variable data signals from the integrated circuit at said functional input terminals and
20 to output to the integrated circuit a result of the specified logical function performed upon the data signals.
2. The spare gate cell of claim 1, each spare cell
25 further comprising a D flip-flop, wherein an output terminal of the CCN is connected to an input of said D flip-flop, an output of said D flip-flop being selectively connectable to the integrated circuit.
- 30 3. The spare gate cell of claim 2, wherein a clock pin of the D flip-flop is selectively connectable to a preexisting clock tree in an area of the integrated circuit where it has been determined that a need for defective cell replacement is highly probable.

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4. The spare gate cell of claim 2, wherein a scan data input pin of the D flip-flop is selectively connectable to a pre-existing clock tree in an area of the integrated circuit where it has been determined that a need for defective cell replacement is highly probable.

5. The spare gate cell of claim 1, wherein at least one of the plurality of functional input terminals is connected in its spare state to an area of the integrated circuit in which a need for defective cell replacement has been determined to be highly probable.

6. The spare cell of claim 5, wherein a D flip-flop of the spare cell is connected to a clock tree in the same area of the integrated circuit as said functional input terminals.

7. The spare gate cell of claim 1, wherein the equation input terminals are connected arbitrarily to either power terminals or power ground terminals when the CCN is in a spare state, and wherein the equation input terminals are selectively connected to power supply terminals through metal layer modifications when the CCN is an active state, thereby transforming the CCN into a specific combinational network.

8. The spare gate cell of claim 1, wherein the equation input terminals are connected to a register, the logical function of the CCN being determined by a value that is stored in the register that can be accessed through any serial and parallel means.

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9. The spare gate cell of claim 1, wherein the CCN is comprised of a first, second, third, fourth, fifth, sixth, seventh, and eighth 2-input OR gates, each having a first and a second input and an output, and a first and second 4-input NAND gate, each having four inputs and one output, the first input of the first OR gate being connected to a first functional input terminal, the first input of the second OR gate being connected to a complement of said first functional input, the first input of the third OR gate being connected to a second functional input terminal, the first input of the fourth OR gate being connected to a complement of said second functional input, the first input of the fifth OR gate being connected to said first functional input terminal, the first input of the sixth OR gate being connected to a complement of said first functional input, the first input the seventh OR gate being connected to said second functional input terminal, the first input of the eighth OR gate being connected to a complement of said second functional input, wherein the second inputs of the first, second, third, fourth, fifth, sixth, seventh, and eighth OR gates being connected to a first, second, third, fourth, fifth, sixth, seventh, and eighth equation input signal lines, each of which is connected to one of the equation input terminals through an inverter, the first, second, third and fourth equation input signal lines being connected to inputs of the first 4-input NAND gate and the fifth, sixth, seventh and eighth equation input signal lines being connected to inputs of the second 4-input NAND gate, wherein the outputs of the first, second, third and fourth 2-input OR gates and the output of the first 4-input OR gate being connected to a first 5-input AND gate and the outputs of the fifth, sixth, seventh, and eighth OR gates and the output of the 4-input OR gate being connected to a second 5-input AND

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gate, each of the first and second 5-input AND gates having five inputs and a single output, wherein the output of the first and second 5-input AND gates being connected to a ninth 2-input OR gate having two inputs and an output, said output of the ninth OR gate being connected to the output terminal of the CCN, whereby the CCN performs a specific sum-of-product combinational logical operation on the functional inputs, as determined by the connections of selected equation inputs to power supply, and output the result at the output terminal of the CCN.

10. In an integrated circuit, a method for replacing a defective logic cell comprising:

identifying at least one area of an integrated circuit where defective cell replacement is likely to be required;

placing a spare cell having a configurable combinatorial network in each area of the integrated circuit where defective cell replacement is likely to be required;

connecting any functional inputs of the configurable combinatorial network to any existing functional signals of the logic area where defective cell replacement is likely to be required; and

configuring and activating the spare cell whenever defective cell replacement is required.

11. The method of claim 10, further including deactivating a defective cell.

12. The method of claim 10, wherein the activation step is accomplished through metal layer modification.

13. The method of claim 11, wherein the deactivation

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step is accomplished through metal layer modification.

14. The method of claim 10, wherein the spare gate cell further includes a D flip-flop.

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15. The method of claim 14, further including connecting the D flip-flop clock pin to an existing clock tree in the area where defective cell replacement may be necessary, said connection occurring when the D flip-flop is in a spare state.

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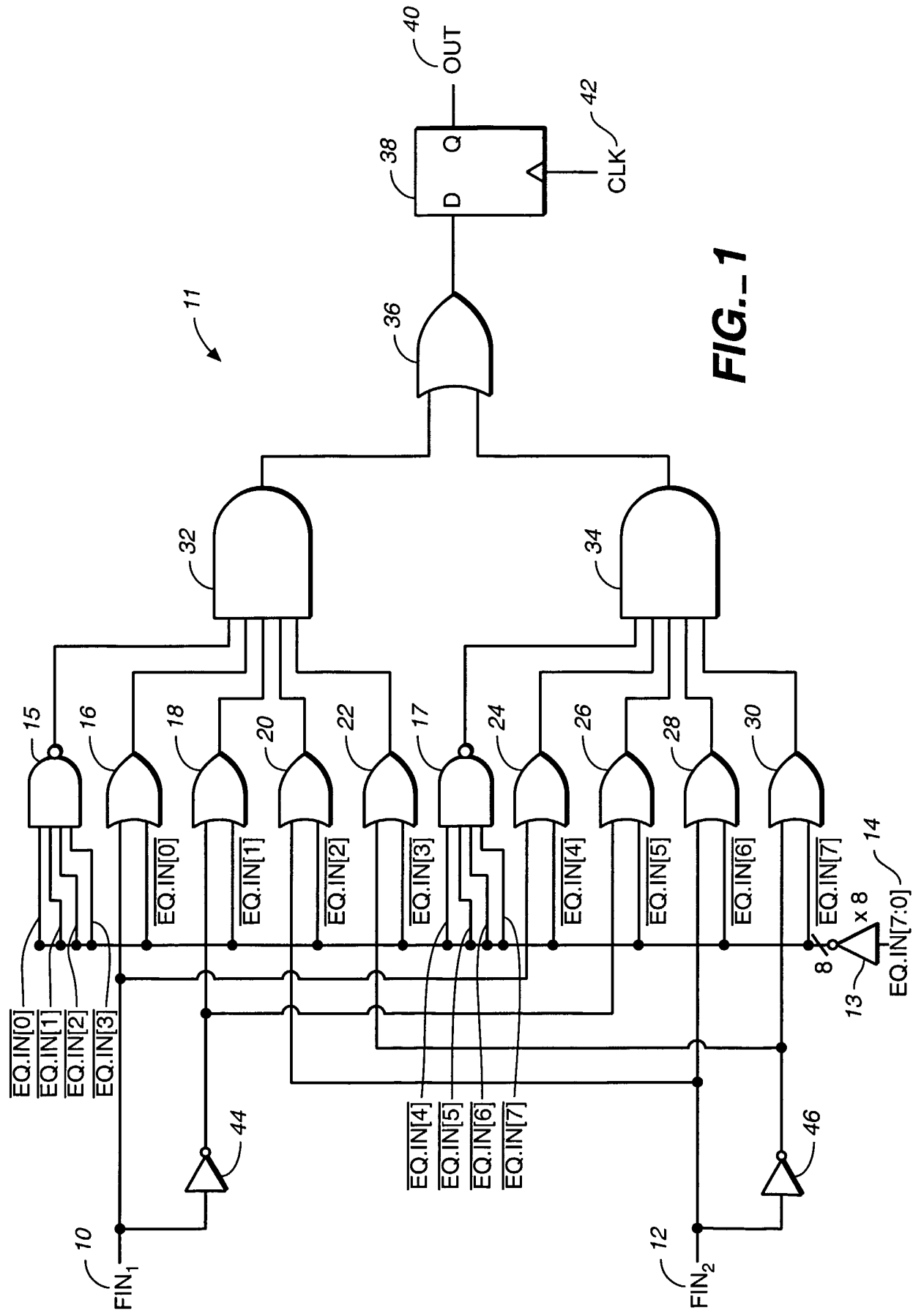
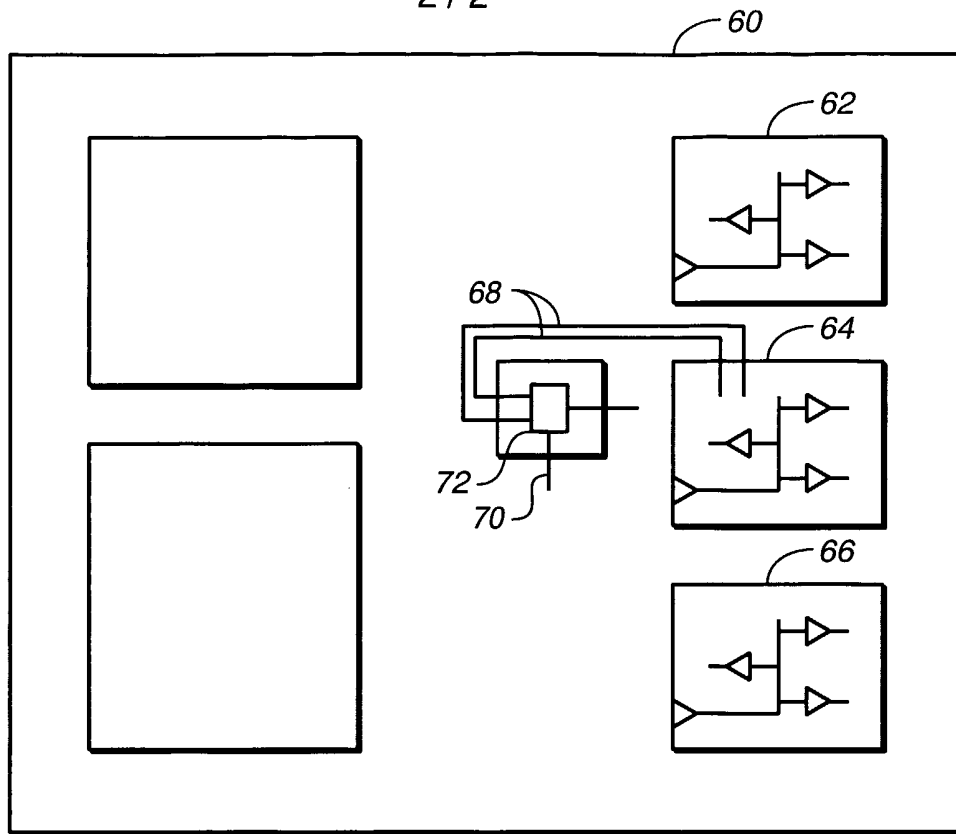
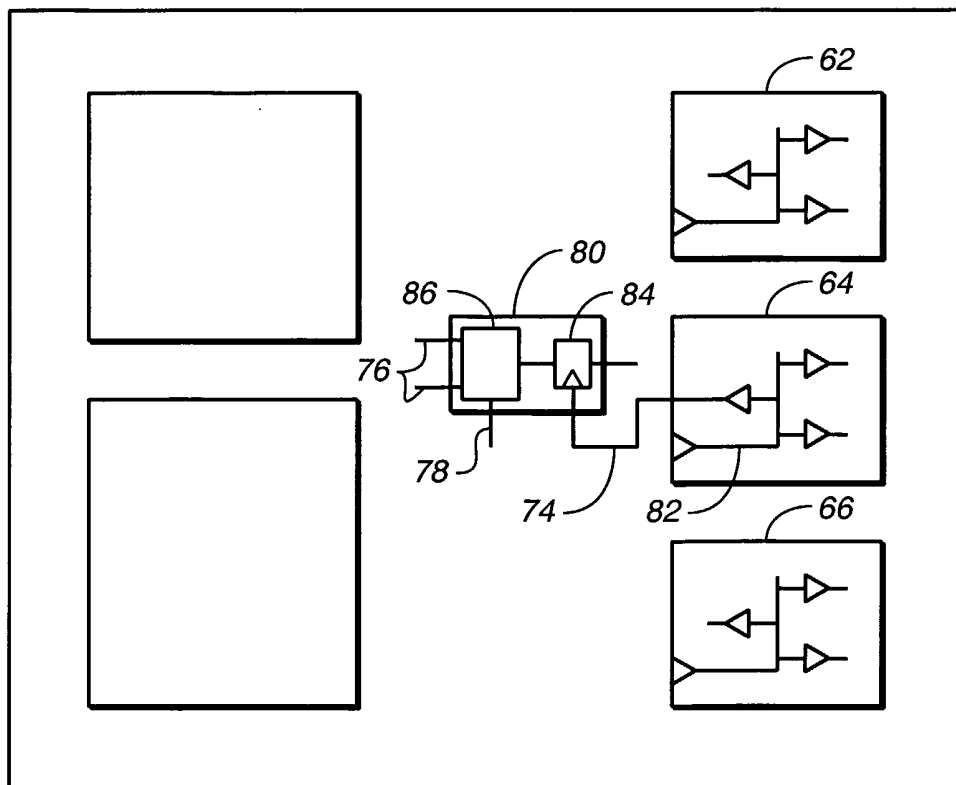


FIG. 1

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**FIG. 2****FIG. 3**

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER

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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 326/9, 10, 12, 38, 39, 40, 41

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPAT EAST

search terms: redundance, spare, programmable

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,107,820 A (JEFFERSON et al) 22 August 2000 (22.08.2000), see figures 2 & 6.	1-15
A	US 6,166,559 A (MCCLINTOCK et al) 26 December 2000 (26.12.2000), see figures 1 & 15.	1-15

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