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(54) A power converter apparatus

(57) The apparatus includes a gate control circuit (GC), a gate amplifier (GA) and a full wave bridge circuit comprising gate turn-off thyristors (GTOU1–GTOW1) and thyristors (U2–W2). The gate control circuit includes a phase shift signal generator (PS), a chopper signal generator (CSG) and a gate pulse generator (PC). The A.C. to D.C. power conversion is obtained by connecting the gate turn-off elements (GTOU1–GTOW1) to the positive arms of a three-phase full wave bridge circuit and by repeating the mode of supplying power to a load (L) from an A.C. power supply Ea by controlling the gate turn-off elements, and the mode of making the current flowing to the load free wheel at the time of interruption of the power supply mode. When the power supply mode and the free wheel mode are switched over, overvoltage at the time of the switching is suppressed by simultaneously causing the power supply and freewheel currents to flow.

FIG. 1

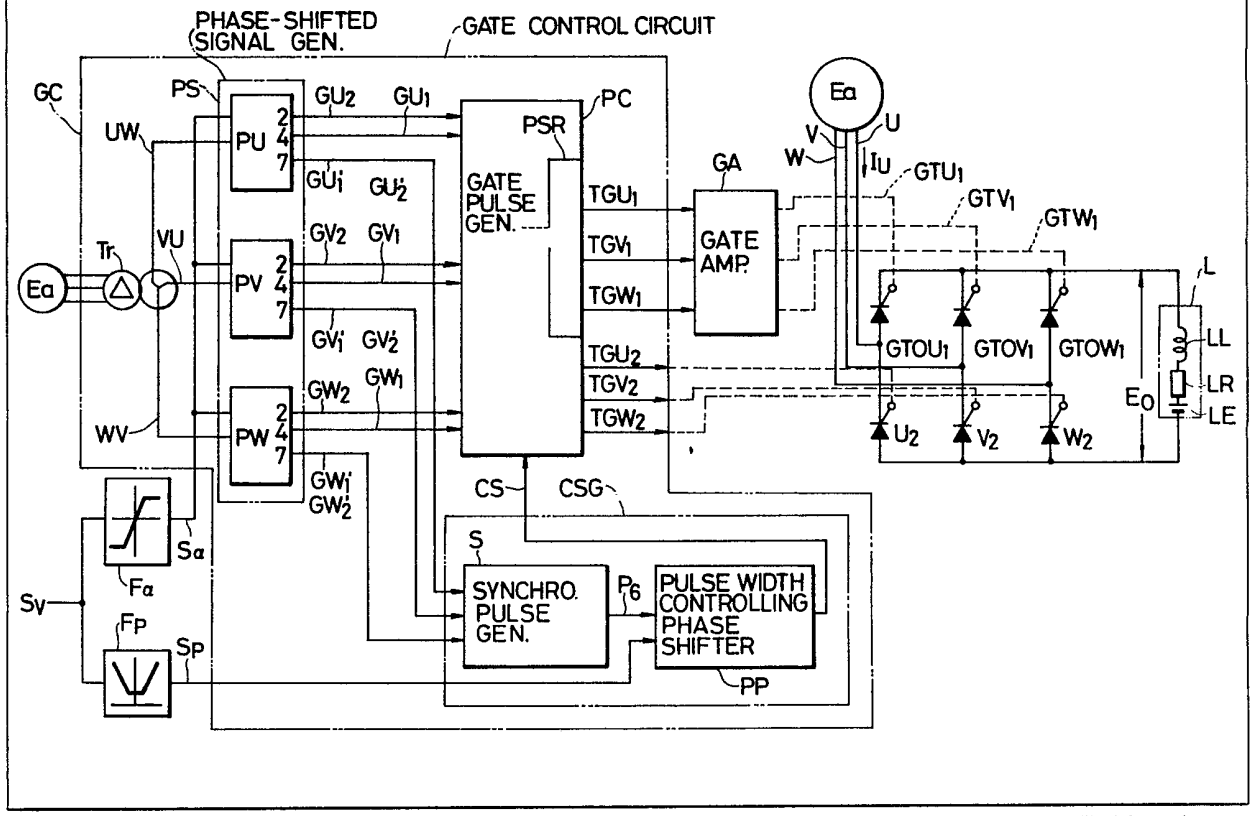

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FIG. 1

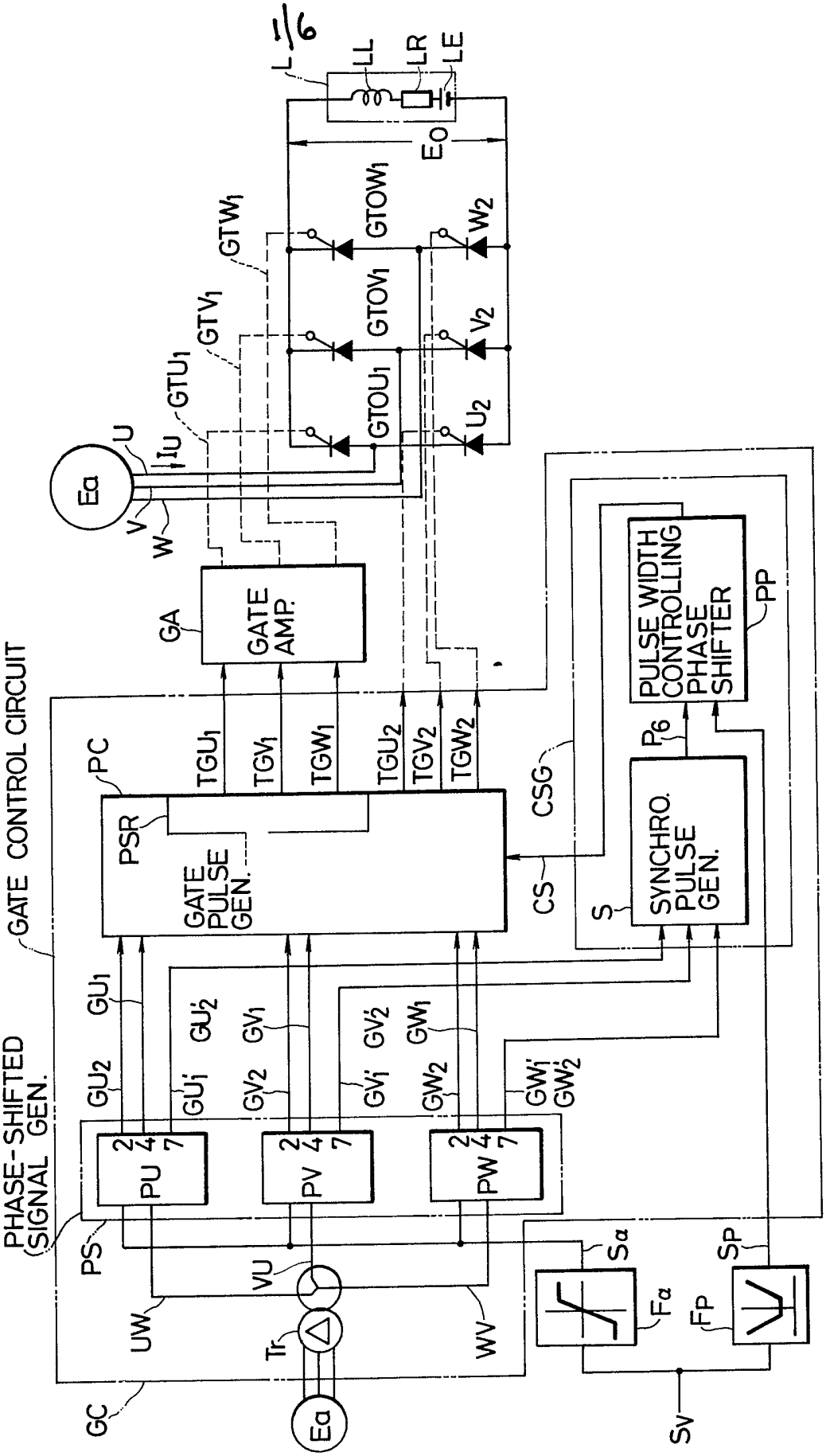

L
LL
LR
LE
Eo
GTW1
GTOW1
W2
GTV1
GTOV1
V2
GTU1
GTOU1
U2
U
Iu
V
W
Ea
GA
GATE AMP.
PC
PSR
GATE PULSE GEN.
TGU1
TGV1
TGW1
TGU2
TGV2
TGW2
CSG
CS
S
SYNCHRO. PULSE GEN.
P6
PULSE WIDTH CONTROLLING PHASE SHIFTER
PP
GATE CONTROL CIRCUIT
PHASE-SHIFTED (SIGNAL GEN.
GU1
GU2
GU'1
GU'2
GV1
GV2
GV'1
GV'2
GW1
GW2
GW'1
GW'2
2 4 7
PU
PV
PW
PS
VU
UW
WV
Tr
Ea
GC
Sα
Fα
SP
FP
Sv

FIG. 2

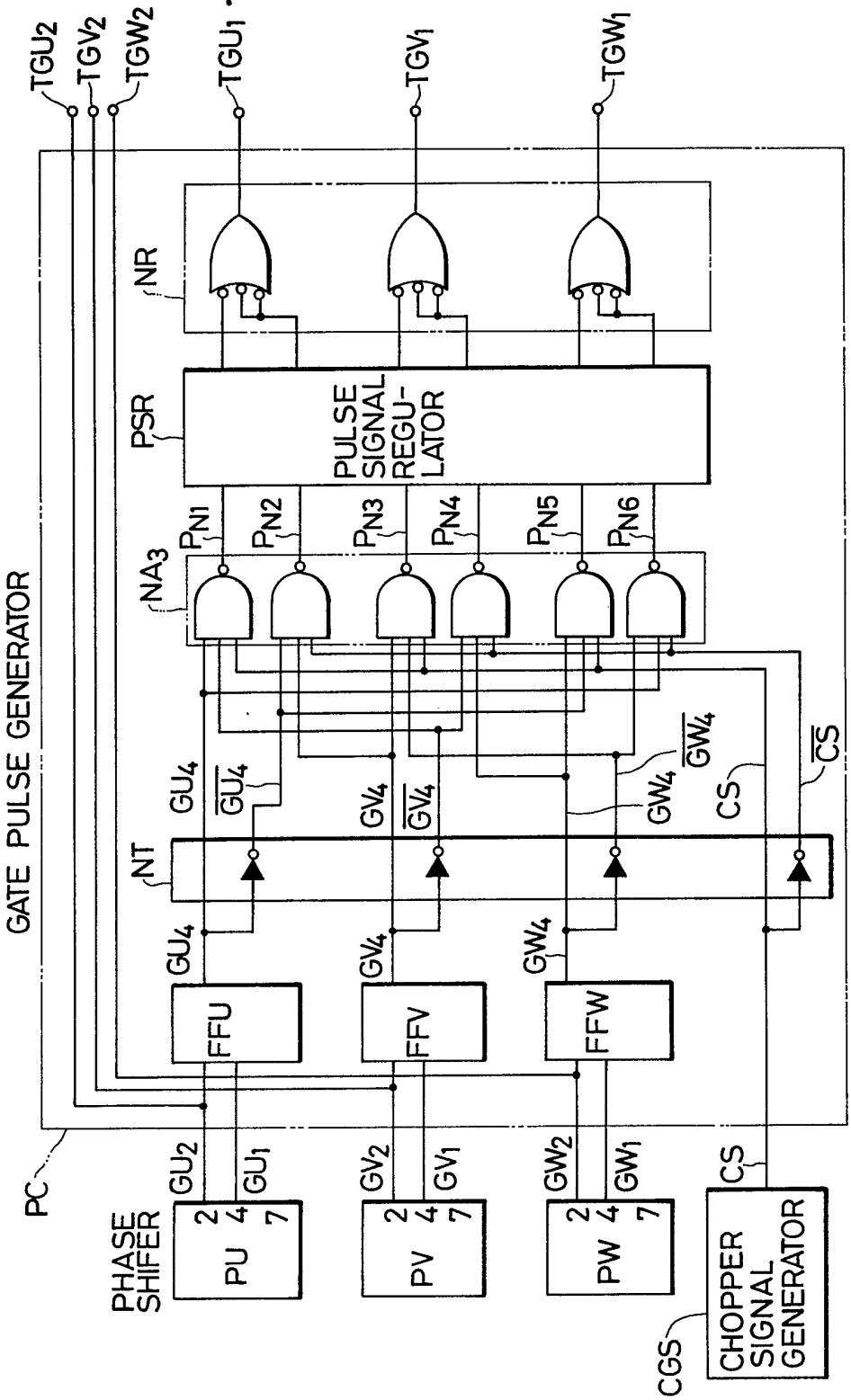

GATE PULSE GENERATOR
TGU2
TGV2
TGW2
TGU1
TGV1
TGW1
NR
PSR
PULSE SIGNAL REGU-LATOR
PN1
PN2
PN3
PN4
PN5
PN6
NA3
GU4
GV4
GW4
CS
NT
FFU
FFV
FFW
PC
GU2
GU1
GV2
GV1
GW2
GW1
PHASE SHIFER
2 4 7
PU
PV
PW
CGS
CHOPPER SIGNAL GENERATOR

FIG. 3

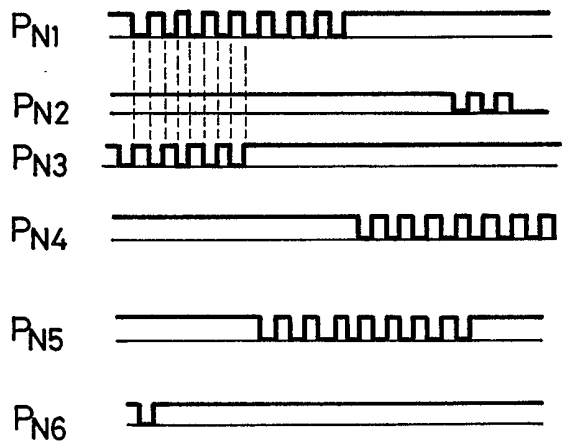

P_{N1}
P_{N2}
P_{N3}
P_{N4}
P_{N5}
P_{N6}

FIG. 4

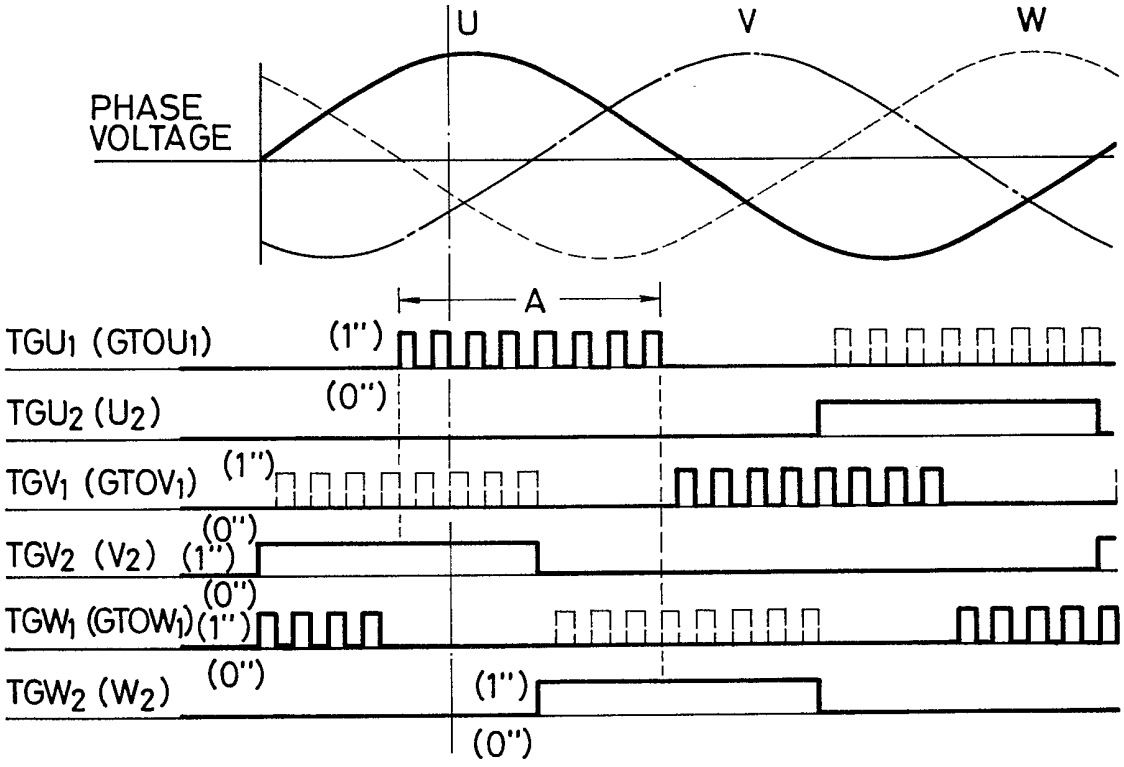

U
V
W
PHASE VOLTAGE
A
TGU1 (GTOU1)
(1")
(0")
TGU2 (U2)
TGV1 (GTOV1)
(1")
(0")
TGV2 (V2)
(1")
(0")
TGW1 (GTOW1)
(1")
(0")
TGW2 (W2)
(1")
(0")

FIG. 5(A)

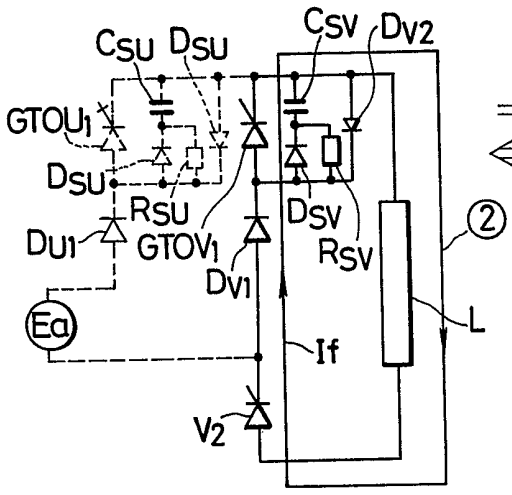


FIG. 5(B)

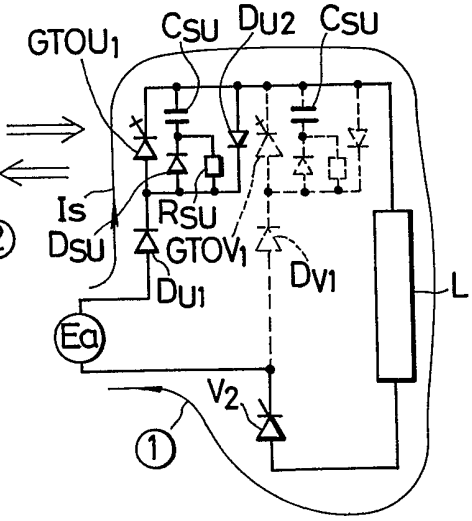
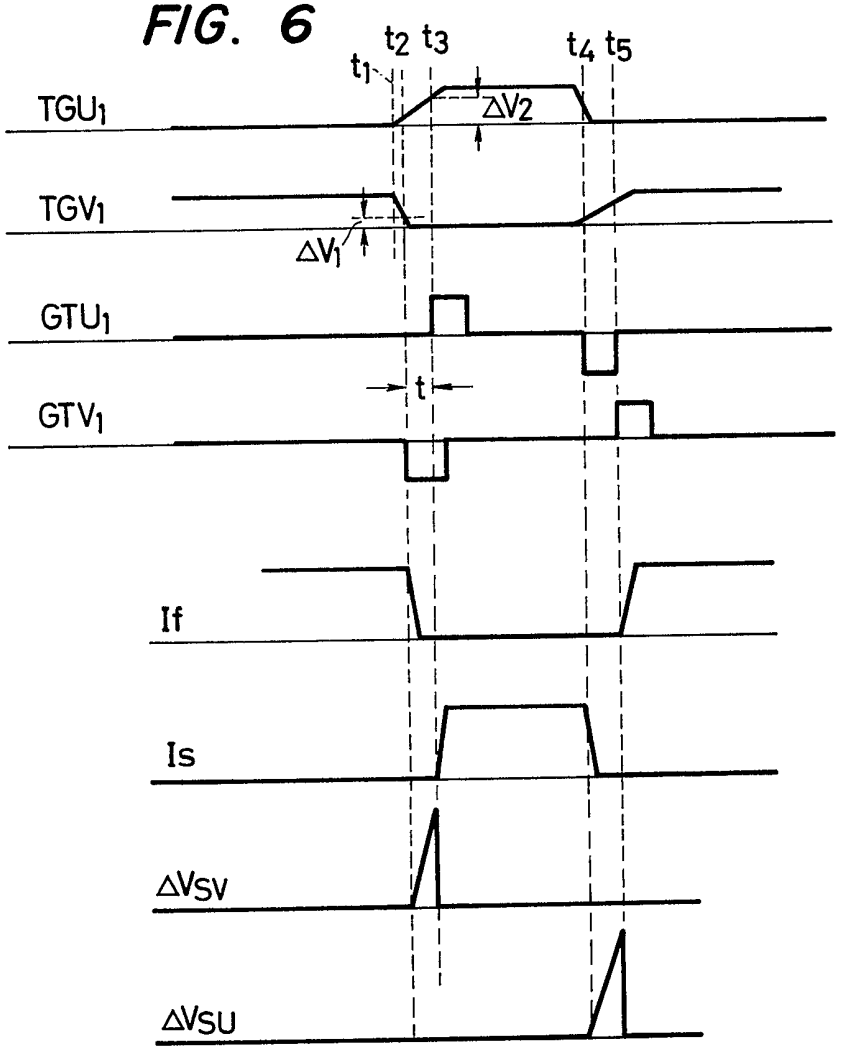


FIG. 6



5/6

FIG. 7

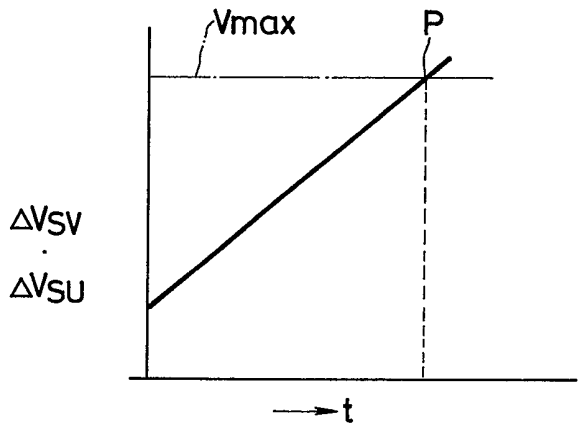

Vmax
P
ΔVSV
ΔVSU
t

FIG. 9

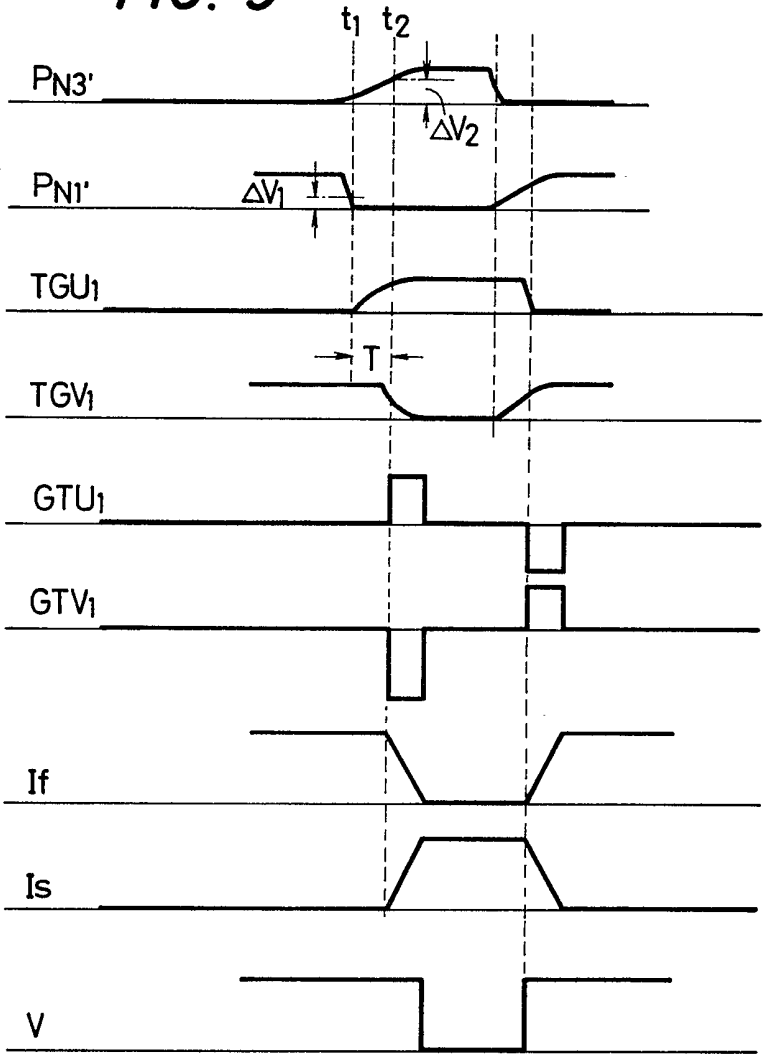

t1
t2
PN3'
ΔV2
PN1'
ΔV1
TGU1
T
TGV1
GTU1
GTV1
If
Is
V

FIG. 8(A)

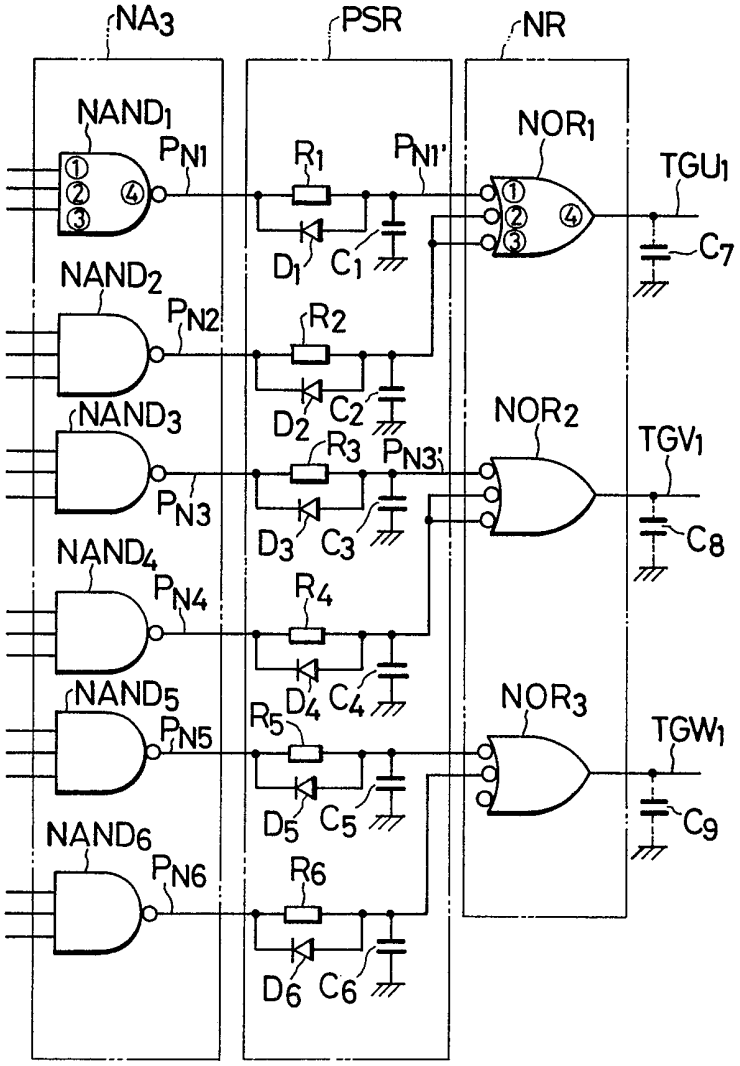
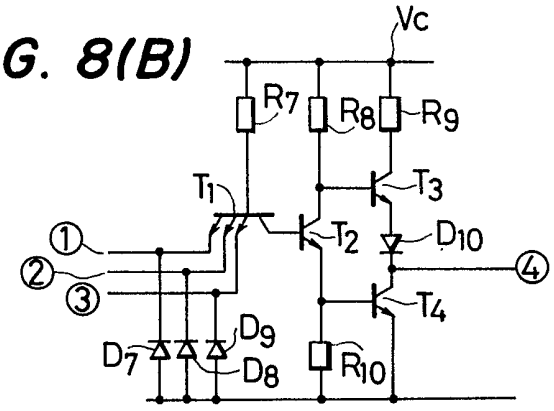

NA3
PSR
NR
NAND1
PN1
R1
PN1'
NOR1
TGU1
C7
D1
C1
NAND2
PN2
R2
D2
C2
NAND3
R3
PN3'
NOR2
TGV1
PN3
D3
C3
C8
NAND4
PN4
R4
D4
C4
NAND5
NOR3
TGW1
R5
PN5
D5
C5
C9
NAND6
PN6
R6
D6
C6

FIG. 8(B)


Vc
R7
R8
R9
T1
T3
T2
D10
T4
D9
D7
D8
R10

SPECIFICATION

A power converter apparatus

The present invention relates to an A.C. to D.C. power converter apparatus.

Previously, various proposals have been made in relation to apparatus employing full wave bridge circuits for obtaining variable D.C. power from A.C. power sources or for converting D.C. to A.C. power and they have been put to practical use. Moreover, single-phase or polyphase A.C. is employed according to the use; although apparatus which utilizes polyphase A.C. is more complicated technically than apparatus which utilizes single-phase A.C. However there are many problems which are common to both single phase and polyphase systems. A description of a three-phase A.C. apparatus will now be given in greater detail. Based on the above description, a system which utilizes single-phase A.C. will be readily appreciated by those skilled in the art.

A full wave bridge circuit is generally made up of thyristors, wherein the ignition phase angles of a group of thyristors connected to the positive arm of the circuit and another group of thyristors connected to its negative arm are made equal, the circuit being used to control output voltage by making the phase angle variable.

However, the disadvantage of this method is that the power-factor is reduced, whilst the ripple component is increased, in regions where the D.C. output voltage is low.

As a way of improving the disadvantage occurring in the low output voltage region, a system has been previously disclosed in United States Patent Specification No. 4,245,293. In the method shown in the above Specification, the ignition phase angles of the groups of thyristors on the positive and negative sides in the low output voltage region are made different in order to improve the operation by causing a short-circuiting mode to occur between both the groups of thyristors.

However, as further improvements in the power-factor have been desired the following methods have also been proposed and disclosed in the following:

(a) "A Pulsewidth Controlled A.C. to D.C. Converter to Improve Power Factor and Waveform of A.C. Line Current" (IEEE TRANSACTION ON INDUSTRY APPLICATIONS, VOL. IA–15, No. 6, NOVEMBER/DECEMBER, 1979).

(b) British Patent Specification No. 2,076,233.

In either case, the mode of supplying power to an A.C. load by connecting controllable switching means with the function of breaking current to the positive arm of a full wave bridge circuit to control the switching means and by rectifying an A.C. power source, and the mode of causing the current flowing through the D.C. load to flow back at the time of breaking current in the power supplying mode are repeated and A.C. to D.C. power conversion may be carried out.

In this method, it is possible to make the output voltage variable by varying the period (chopping pulsewidth) of the above supplying mode and, because the relation between the A.C. supply source voltage and current is maintained roughly in the same phase, the power-factor is allowed to be close to unity. Due to the development of elements having large capacitance recently such as gate turn-off thyristors (hereinafter referred to as "GTO elements") and transistors, this method is attracting attention.

However, it has been made clear that, because the power supplying mode and flowback mode are repeated by forcing the current being supplied to be cut off using the controllable means with the function of breaking the current in this method, the switching means may be destroyed resulting in uncontrollable operation.

It is an object of the present invention to provide a highly reliable power converter apparatus with the greater power-factor by preventing controllable switching means having a current-breaking function from being destroyed at the time of carrying out A.C. to D.C. power conversion.

According to the present invention there is provided a power converter apparatus including: an A.C. power supply; a D.C. load; controllable switching means connected across said A.C. power supply and said D.C. load and provided with a current-breaking function for alternately repeating the mode of rectifying said A.C. power supply and supplying power to said D.C. load and the mode of making the current flowing to said D.C. load flow back; and gate control means for controlling said switching means in such a manner that, at the time of said power-supply-to-flow-back-mode switching, said power supply current and said flow-back current are allowed to simultaneously flow.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:–

Figure 1 is a block circuit diagram of a preferred form of a power converter apparatus;

Figure 2 is a circuit diagram of the gate pulse generator circuit PC shown in Fig. 1;

Figure 3 is an output pulse waveform diagram of the NAND circuit NA3 shown in Fig. 2;

Figure 4 is a waveform diagram illustrating the relation between phase voltage and the output pulse of the gate pulse generator circuit;

Figures 5A and 5B are circuit diagrams illustrating flow-back and power supply modes in operation;

Figure 6 is a waveform diagram of a signal in each portion when a pulse signal regulator circuit PSR is not provided;

Figure 7 is a graph illustrating the characteristics of overvoltage;

Figure 8 (A) is a detailed circuit of one example of the pulse signal regulator circuit PSR;

Figure 8 (B) is a circuit diagram showing the internal configuration of NAND and NOR elements; and

Figure 9 is a waveform diagram of a signal in each portion when the pulse signal regulator circuit PSR is provided.

Although the description will be given with reference to power conversion between a three-phase power supply and A.C. when a GTO element is employed as a controllable switching means with a current-breaking function, it will be readily understood that the present invention can be utilized even when other switching means such as single-phase A.C. supplies or transistors, chopper apparatus and the like are used.

The example given in Fig. 1 is one which has been constructed by applying the present invention to the power converter apparatus disclosed in British Patent Specification No. 2,076,233. Reference should be made to the above British Patent Specification for the construction and operation of this power converter apparatus in detail and the description of the portion which relates to the present invention is now given in detail.

In Fig. 1, there is shown a full wave bridge circuit comprising GTO elements GTOU1, GTOV1 and GTOW1 connected to each of its positive arms and thyristors U2; V2 and W2 connected to its negative arms. A three-phase A.C. supply Ea is connected to an A.C. terminal of the full wave bridge circuit. Moreover, the D.C. output voltage Eo of the full wave bridge circuit is applied to a load L including resistance RL, inductance LL, and a D.C. voltage source EL. At this time, the time constant LL/RL of the load L is assumed to be sufficiently longer than the period of the A.C. supply and the D.C. voltage source LE has a value lower than the output voltage Eo. For instance, a condition like this is established when an armature circuit as the load L is connected to control a D.C. motor by means of the full wave bridge circuit.

In the apparatus shown in Fig. 1, a gate control circuit GC controls the D.C. output voltage Eo by controlling the GTO elements GTOU1–GTOW1 and thyristors U2–W2 according to a voltage command signal Sv.

This gate control circuit GC comprises a phase-shift signal generator PS, a chopping signal generator CSG and a gate pulse generator PC.

The details of this gate control circuit GC are identical to those disclosed in British Patent Specification No. 2,076,233.

A transformer Tr converts the three-phase supply Ea to line voltages UW, VU, WV having a neutral point and inputs the voltages to phase shifters PU, PV, PW. The input of a phase command signal $S\alpha$ is also given to the phase shifters PU, PV, PW. The command signal $S\alpha$ is generated by a function generator $F\alpha$ having such an output (shown) that the control angle of lag α becomes zero within a large range of voltage command signals Sv, or a large range of output voltage. Therefore, the phase shifters PU, PV, PW generate a phase pulse corresponding to the phase command signal $S\alpha$ and inputs the pulse to the gate pulse generator circuit PC and chopping signal generator circuit CGS. At this time, the positive half wave of the supply Ea and the negative half wave of the supply Ea are generated from pins No. 4 and 2 of the phase shifters PU, PV, PW, respectively. Moreover, pin No. 7 generates pulses GU'1–GW'1, GU'2–GW'2 of the positive and negative half waves of the supply Ea.

This pin No. 7 inputs the phase-shifting pulse signals GU'1,–GW'1, GU'2–GW'2 of the positive and negative half waves generated to a synchronizing pulse generator circuit S. This synchronizing pulse generator circuit S comprises a pulse generator and a flip-flop and drives the pulse generator in synchronism with the phase shifting pulse signals GU'1–GW'2 while generating a synchronizing pulse P6 with frequencies higher than those of the A.C. supply Ea.

This synchronizing pulse P6 is used as a chopping reference pulse of the pulsewidth control phase shifter Pp of the GTO element.

A pulsewidth command signal S_p is applied to the GTO pulsewidth control phase shifter PP. This GTO pulsewidth command signal S is obtained from a function generator F_P generating such a signal (the characteristics of which are shown) as is provided with small and constant pulsewidth within a small range of voltage command signals Sv, or small range of output voltage, and with large pulsewidth within a large range of voltage command Sv, or a large range of output voltage. The GTO pulsewidth control phase shifter PP generates a chopping signal CS corresponding to the pulsewidth command signal S_P with the frequency of the synchronizing pulse P6 and inputs the signal to the gate pulse generator circuit PC.

The gate pulse generator circuit PC generates pulse signals TGU1–TGW1 for the GTO elements GTOU1–GTOW1 and gate signals TGU2–TGW2 for the thyristors U2–W2 based on the above-mentioned input signals as described hereinafter.

The pulse signals TGU1–TGW1 are supplied to a gate signal amplifier GA. The gate

signal amplifier GA generates gate pulses GTU1–GTW1 which are supplied to the GTO elements GTOU1–GTOW1.

In the above described apparatus, the pulse signal regulator circuit PSR is provided in the pulse generator circuit PC so as to regulate the pulse signals TGU1–TGW1 in such a manner that the power supply and flow-back modes of the full wave bridge circuit are overlapped.

The details of the pulse generator circuit PC are shown in Fig. 2. In Fig. 2, except for the fact that the pulse signal regulator circuit PSR is provided, the pulse generator circuit is substantially the same as that disclosed in British Patent Specification No. 2,076,233.

In other words, the pulses GU2–GW2 obtained from the terminals of the three phase phase shifter PU–PW are used as the gate signals TGU2–TGW2 for the thyristors U2–W2. Fig. 4 illustrates the waveforms of the gate signals TGU2–TGW2.

On the other hand, a group of pulses GU1–GW2 obtained from the terminals 2 and 4 of the three phase phase shifters PU–PW are supplied to flip flop circuits FFU–FFW and the chopping signal CS from the chopper signal generator CGS are applied to a NOT circuit NT so that pulses $\overline{GR4}$–$\overline{GW4}$ with inverted codes and $\overline{CS}$ can be obtained.

Based on the above pulses, a NAND circuit NA3 outputs pulses PN1–PN6 shown in Fig. 3. These pulses PN1–PN6 are supplied to a NOR circuit NR through the pulse signal regulator circuit PSR as described later and the NOR circuit NR outputs the pulses GU1–TGW1 shown in Fig. 4. The pulses TGU1–TGW1 indicate a period during which each of the GTO elements GTOU1–GTOW1 are conducting.

Fig. 4 illustrates the waveforms of the phase voltages U, V, W of the three phase A.C. supply Ea, pulse signals TGV1–TGW1 and gate signals TGV2–TGW2. The pulse signals TGV1–TGW1 are converted to those which turn on the GTO element at the time of its rising by means of the gate signal amplifier GA and turn off the element at the time of its decaying, and become the gate signals GTU1–GTW1 for the GTO elements. As a result, the pulse signals TGV1–TGW1 indicate a period during which the GTO elements GTOU1–GTOW1 are conducting when they are "1", whereas a period during which the GTO elements GTOU1–GTOW1 are not conducting when they are "O".

Accordingly, the operation during a period A in Fig. 4 is such that, because the pulse signal TGU1 and gate signal TGV2 are "1" at first, the GTO elememt GTOU1 and thyristor V2 conducts, forming the mode in which power is supplied from the supply Ea to the load L. In other words, a circuit shown by an actual line in Fig. 5B is formed and supply current Is from the supply Ea is allowed to flow along a loop (1).

Subsequently, when the pulse signals TGU1 and TGV1 become "0" and "1", respectively, the GTO elememt GTOU1 is cut off, whereas the GTO element GTOV1 conducts. Therefore, the supply current Is breaks, forming the flow-back mode in which load current up to that time flows through the thyristor V2 and GTO element GTOV1; that is, a circuit shown by an actual line in Fig. 5A is formed, causing flow-back current If to flow in the route along a loop (2).

When the pulse signals TGU1 and TGV1 become "1" and "0" again, the circuit in Fig. 5B is formed and power is supplied from the supply Ea to the load L again.

In the first half of the period (a), the on-off operations of the above GTOU1 and GTOV1 form a pair and cause the power supply and flow-back modes to be alternately repeated so as to supply D.C. power to the load L.

In the second half of the period (a), as clearly shown in the waveforms in Fig. 4, the on-off operations of the GTO elements GTOU1 and GTOW1 cause the power supply and flow-back modes to be alternately repeated so as to supply D.C. power to the load L.

Although the operations during the period (A) have been described up to now, corresponding GTO elements GTOU1–GTOW1 are controlled during another period according to the relation illustrated in Fig. 4.

Therefore, if the pulse signals TGU1–TGW1 during the period "1" are controlled, the D.C. output voltage Eo will be also controlled.

A capacitor C_{SU}, diode D_{SU} and resistor R_{SU} added to Fig. 5 constitute a known snubber circuit for absorbing overvoltage generated when the GTO element GTOU1 is interrupted. Moreover, diodes D_{U1}, D_{U2} are provided to protect the GTO element GTOU1 from reverse voltage. These snubber circuit and diodes D_{U1}, D_{U2} are provided in each of the other GTO elements GTOV1, GTOW2.

The conventional pulse signal TFU1–TGW1 as shown in Fig. 6 has its rise time delayed and its decay time to be quickened. This is due to the connected capacitor for improving noise resistance and the floating capacitance of a signal line and is the phenomenon necessarily resulting because of the circuit configuration.

Although each one of the pulse signals GU1 and TGV1 is shown in Fig. 6, the same is applied to other pulse signals.

In Fig. 6, the pulse signal TGV1 sharply decays at time t1, whereas the pulse signal TGU1 slowly rises. The pulse signals TFV1 and TGU1 are applied to the gate signal amplifier GA and converted to the gate signals GTV1 and GTU1. The gate signal amplifier GA generates a gate signal when the off voltage becomes less than $\Delta V1$ and an on gate signal when the on voltage exceeds $\Delta V2$.

Consequently, the on gate signal is gener-

ated in the gate signal GTV1 by means of the gate amplifier GA at the time T2 when the pulse signal TGV1 becomes less than $\Delta V1$. However, because the rise of the pulse signal TGU1 is slow, the off gate signal is generated in the gate signal GTU1 by means of the gate amplifier GA at time t3; that is, the time difference between the off gate of the gate signal GTV1 and the on gate of the gate signal GTU1 occurs.

For this reason, a time difference occurs after interrupting the flow-back current If using the GT0 element GT0V1 and before making the GT0 element GT0U1 conduct.

The constant-current operation of the inductance component LL of the load L causes the flow-back current to flow into the capacitor C_{SV} connected to GT0V1 element in parallel during the time difference *t*. The charge voltage ΔV_{SV} of the capacitor C_{SV} at this time becomes $\Delta V_{SV} = If \cdot T/C_{SV}$ and this voltage is applied to the GT0 element GT0V1.

For the same reason, after the off gate is generated in the gate signal GTU1 at the time t4, the on gate is generated in the gate signal GTV1 at the time t5. Therefore, the constant-current operation of the inductance component LL of the load L in this case causes the current to flow into the capacitor C_{SU} connected to the GT0 element GT0U1 in parallel. The charge voltage ΔV_{SU} of the capacitor C_{SU} in this case becomes much greater because the supply voltage Ea is added.

If the above time difference *t* is long, the charge voltages ΔV_{SU}, ΔV_{SV} will exceed, as shown in Fig. 7, the threshold voltage Vmax allowable for the GT0 elements GT0U1–GT0W1, causing the breakdown of the GT0 elements.

On the contrary, since this example is equipped with the pulse signal regulator circuit PS for regulating the pulse signals TGU1–TGW1, such a phenomenon will not occur.

Fig. 8 shows the configuration of the pulse signal regulator circuit PSR. The circuit comprises resistors R1–R6, diodes D1–D6 and capacitors C1–C6.

This circuit utilizes ordinary elements shown in Fig. 8B for both NAND elements NAND1–NAND6 forming the NAND circuit NA3 and for NOR elements NOR1–NOR3 forming the NOR circuit NR. Since these elements are well known, further detailed description of them will be omitted. It is sufficient to note that the element itself comprises transistors T1–T4, diodes D7–D10, resistors R7–R10 and power supply Vc. Accordingly, if the signal "0" is applied to either of the terminals (1)–(3), the transistors T1 and T3 will be turned on, whereas the transistors T2 and T4 will be turned off; thus "1" appears at the output terminal (4) because of the supply Vc. Only when the input signals of the input terminals (1)–(3) all become "1", the above operation is inverted and the transistor T4 is turned on, so that the output terminal (4) becomes "0" because of short-circuiting.

The pulse signal regulator circuit PSR inputs the output pulse signals P_{N1}–P_{N6} of the NAND circuit NA3 shown in Fig. 3 and regulates the circuit in such a manner that overlapping occurs when the pulse signals TGU1–TGW1 rise and decay. For this reason, it has been so arranged that the above overvoltage generated in the full wave bridge circuit may be suppressed.

The operation of the circuit is as follows:

As has already been described, the time difference shown in Fig. 6 occurs in the conventional pulse signals TGU1–TGW1. This is due to the capacitor connected for absorbing surge and the floating capacitance of a signal line; this is equivalently shown in Fig. 8A by means of capacitors C7–C9.

The pulse signals TGU1–TGW1 are prepared by the NOR circuit NR based on the pulse signals P_{N1}–P_{N6} shown in Fig. 3.

Taking the operation of the above pulse signals TGU1 and TGV1 in the form of a pair as an example, when the pulse signals P_{N2} and P_{N4} are in the state of "1", the operation is conducted by the pulse signals P_{N1}–P_{N3}. In other words, when the pulse signal P_{N1} is in the state of "1", the pulse signal P_{N3} is in the state of "0" and the pulse signals TGU1 and TGV1 are in such a state that their codes are inverted.

In this case, because the elements shown in Fig. 8B are used for the NAND elements NAND1, NAND3 and their outputs are connected to the pulse signal regulator circit PSR, the relation between the pulse signals P_{N1}, P_{N3} and TGU1, TGV1 changes in the manner illustrated in Fig. 9.

In other words, the pulse signal P_{N1} rises with the time constant consisting of the internal resistance R9 of the NAND element NAND 1, resistance R1 and capacitor C1. On the other hand, when the signal P_{N1} decays, the charge of the capacitor C1 sharply decays through the diode D1 and the internal transistors T4 of the NAND element NAND1. Therefore, input signal P_{N1} of the NOR element NOR1 has a pulse which is slow to rise and quick to decay.

This is also applicable to the input signal P_{N3}, of the NOR element NOR2.

Accordingly, in connection with the outputs of the NOR elements NOR1 and NOR2 to which pulse signals $P_{N1'}$ and $P_{N3'}$, as shown in Fig. 9, the pulse signal TGU1 rises at the time t1, whereas the pulse signal TGV1 decays at the time t2; that is, an overlap T is available.

The pulse signals TGU1 and TGV1, based on the relation between the NOR elements NOR1, NOR2 and the capacitor for absorbing surge and floating capacitance have waveforms which are slow to rise and quick to decay.

However, due to the above overlapping time T, no time difference occurs in the gates signals GTU1 and GTV1 as the outputs of the gate signal amplifier GA. In other words, it becomes possible to give the on gate signal GTU1 to the GTO element GTOU1 and simultaneously the off gate signal to the GTO element GTOV1, and vice versa.

Accordingly, the power supply mode of the GTO element GTOU1, load L, thyristor V2, and supply Ea occurs on the instant that the operating of interrupting the current If flowing in the flow-back of the GTO element GTOV1, load L and thyristor V2; that is, as shown in Fig. 9, the flow-back current If is decreasing, whilst the power supply current Is is increasing.

In this case, the GTO element GTOV1 conducts the so-called operation of rectifying the supply, or turning-off as the GTO element GTOU1 operates, so that no overvoltage will occur because of the presence of the inductance LL of the load L.

The above operation is also applicable to a case in which the GTO element GTOV1 is made to conduct by interrupting the GTO element GTOU1, that is, the power supply mode is switched over to the flow-back one, and the overvoltage can be suppressed.

As mentioned above, because when the power supply mode is changed to the flow-back mode, the period during which both modes simultaneously occurs is provided, the generation of the overvoltage as the reason for the breakdown of the switching means can be suppressed and the reliability of a power converter apparatus may be improved.

In the examples described above, reference has been made to the case of employing the pulse signal regulator PSR but the present invention is not limited to such a case. In other words, it is readily realizable to overlap the pulse signals P_{N1}–P_{N6} by means of a computer and to overlap the pulse signals TGU1–TGW1 and further the gate signals GTU1–GTW1 by means of a timing factor or a computer.

In addition, switching means having a current-breaking function are not limited to GTO elements and, as previously mentioned, known transistors, chopper apparatus and the like may also be employed.

CLAIMS

1. A power converter apparatus including: an A.C. power supply; a D.C. load; controllable switching means connected across said A.C. power supply and said D.C. load and provided with a current-breaking function for alternately repeating the mode of rectifying said A.C. power supply and supplying power to said D.C. load and the mode of making the current flowing to said D.C. load flow back; and gate control means for controlling said switching means in such a manner that, at the time of said power-supply-to-flow-back-mode switching, said power supply current and said flow-back current are allowed to simultaneously flow.

2. A power converter apparatus according to Claim 1, wherein said gate control means controls said switching means in such a way that said flow-back current is made to rise during a period of time that said power supply current is decreasing.

3. A power converter apparatus according to Claim 1, wherein said gate control means controls said switching means in such a manner that said power supply current is allowed to rise during a period of time that said flow-back current is decreasing.

4. A power converter apparatus according to Claim 1, wherein said gate control means is so arranged that said control means causes said switching means forming said flow-back mode to hold an on state whilst said switching means forming said power supply mode is holding an off state.

5. A power converter apparatus according to Claim 4, wherein said gate control means is so arranged that said control means simultaneously generates a gate off signal and a gate on signal for said switching means forming said power supply mode and said flow-back mode, respectively.

6. A power converter apparatus according to Claim 1, wherein said gate control means is so arranged that said control means causes said switching means forming said power supply mode to hold an on state while said switching means forming said flow-back mode is holding an off state.

7. A power converter apparatus according to Claim 6, wherein said gate control means is so arranged that said control means simultaneously generates a gate off signal and a gate on signal for said switching means forming said flow-back mode and said power supply mode, respectively.

8. A power converter apparatus according to Claim 1, wherein a full wave bridge circuit is connected across said A.C. power supply and said D.C. load, said switching means being connected to each of a plurality of arms of said full wave bridge circuit.

9. A power converter apparatus according to Claim 8, wherein said switching means is connected to the positive arm of said full wave bridge circuit, whereas thyristors are connected to its negative arms.

10. A power converter apparatus according to Claim 8, wherein said power supply mode is formed by making any of said switching means of said full wave bridge circuit conduct, whereas said flow-back mode is formed by making switching means connected to the arms forming a closed loop with said D.C. load.

11. A power converter apparatus according to Claim 10, wherein said gate control

means operates to overlap a terminating point of a period during which said switching means forming said power supply mode is conducting and a starting point of a period during which said switching means forming said flow-back mode is conducting.

12. A power converter apparatus according to Claim 10, wherein said gate control means operates to overlap a terminating point of a period during which said switching means forming said flow-back mode is conducting and a starting point of a period during which said switching means forming said power supply mode is conducting.

13. A power converter apparatus constructed and arranged to operate substantially as herein described with reference to and as illustrated in the accompanying drawings.

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