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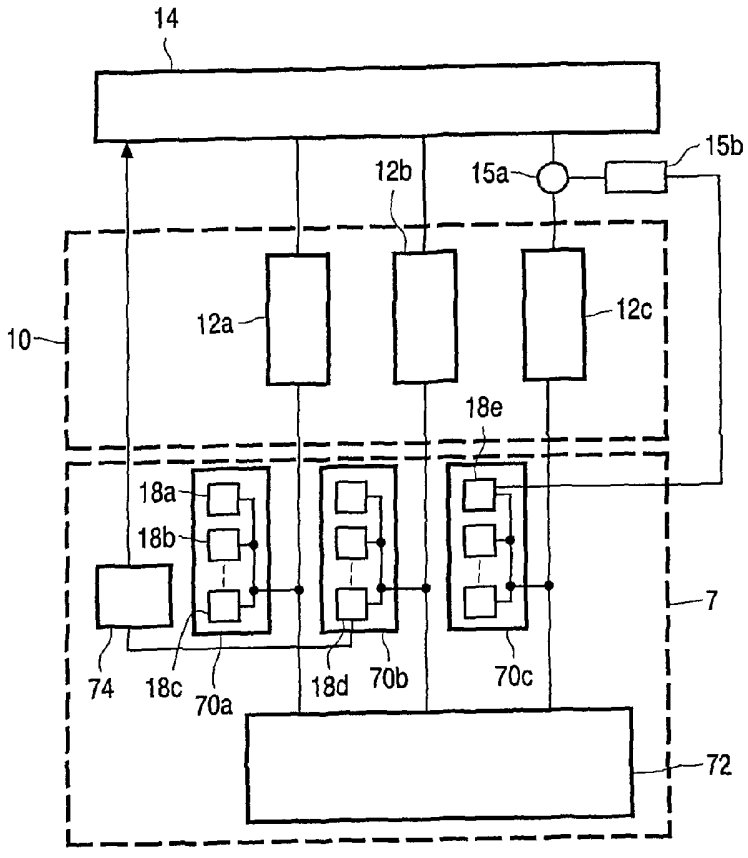
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(54) Title: VLIW PROCESSOR WITH INSTRUCTION ADDRESS MODIFICATION



(57) Abstract: A program of instruction words is executed with a VLIW data processing apparatus. The apparatus comprises a plurality of functional units capable of executing a plurality of instructions from each instruction word in parallel. The instructions from each of at least some of the instruction words are fetched from respective memory units in parallel, addressed with an instruction address that is common for the functional units. Translation of the instruction address into a physical address can be modified for one or more particular ones of the memory units. Modification is controlled by modification update instructions in the program. Thus, it can be selected dependent on program execution which instructions from the memory units will be combined into the instruction word in response to the instruction address.

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MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

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INTERNATIONAL SEARCH REPORT

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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 473 420 A (HITACHI LTD) 4 March 1992 (1992-03-04) page 6, line 58 - page 7, line 19; figure 5	1,11
A	EP 1 176 505 A (ST MICROELECTRONICS SA) 30 January 2002 (2002-01-30) abstract paragraph '0054! - paragraph '0061!	1,11
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A	US 6 026 479 A (RAJE PRASAD A ET AL) 15 February 2000 (2000-02-15)	

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☒ Patent family members are listed in annex.

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