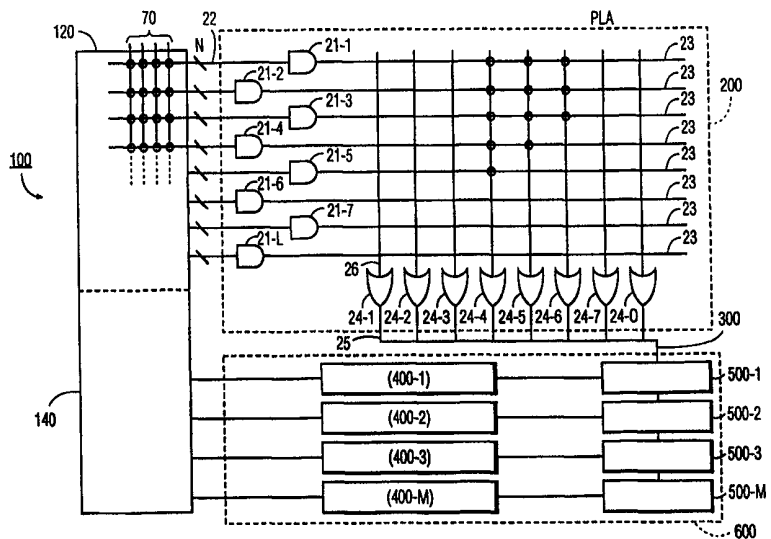




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(54) Title: A PROGRAMMABLE LOGIC DEVICE WITH MACROCELL CONTROLLED BY A PLA



(57) Abstract

A programmable logic device (PLD) includes a macrocell which controls the output path of the logic signals output by one or more logic arrays implementing user logic functions. Complex control terms are implemented and provided to the macrocell by a programmable logic array (PLA), which includes at least one (and typically a plurality) of Sum terms (OR gates) electrically programmably coupled to a plurality of Product terms (AND gates) receiving input logic signals. In a favorable embodiment, the PLD includes a plurality of macrocells coupled via a communication channel to the PLA which generates the control terms. The PLA has the advantage of improving density and flexibility, so that complex control terms may be implemented without the need to implement multiple paths through the user logic arrays, thereby avoiding decreases in speed and poaching of capacity from the user logic arrays.

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A programmable logic device with macrocell controlled by a PLA.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to programmable logic devices (PLD's), and more particularly, to an improvement in the generation of control terms for macrocells within PLD's.

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2. Description of the Prior Art

PLD's are well known and widely used in the field of semiconductor integrated circuits. PLD's typically have logic structure which is available to implement a user's boolean arithmetic. Such structure is in the form of multiple arrays of AND and OR gates

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interconnected in various combinations. The AND gates implement the boolean logic "AND" function to provide the product of selected inputs and the OR gates implement the boolean logic "OR" function to provide the sum of selected inputs. An OR gate whose inputs are the outputs of a plurality of AND gates implements the boolean "SUM OF PRODUCTS" function.

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Given enough products, often referred to for convenience as "p-terms", the sum of the products can express all boolean transfer functions.

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PLD's also include macrocells, which are the destination of the user logic. A macrocell is circuitry which controls where and how the output of one or more logic arrays is directed within the PLD, such as directly to an output pin or to another logic array. Macrocells may also determine, for example: whether the user logic is combinatorial or registered; whether the output of the user logic is inverted or non-inverted; whether a register is clocked by a logic element or a global synchronous clock; whether the output of the user logic is fed back into itself; and/or whether the output is driven continuously, driven under control of a logic output or external pin control, or left three-state.

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Known techniques for controlling these macrocell features use dedicated or multiplexed functionality pins to control dynamic macrocell features. By dynamic is meant features that change during normal operation, such as an output buffer that is turned on and off by some logic, in contrast to a feature set by a programmable element and left unchanged during normal operation. Dynamic features include: direct control of the macrocell feature by an external pin; control by a single product term (AND equation) that has the same inputs

available to it as are available in the user logic (simple control term); and control by a single SUM term (OR equation) that has the same inputs available to it as are available in the user logic (simple control term).

An example of control by a single product term is known from a relatively
5 simple PLD, the 16V8 available from Philips Semiconductors. Each macrocell has a simple array with a plurality of AND gates feeding a single OR gate. The output of the OR gate feeds the data input of a D-type flip flop of the macrocell. Of interest is that the output of one of the AND gates may be steered away from the Sum term (OR gate) to control the output buffer. Figure 1 illustrates a more complex PLD, known from Philips Semiconductors' model XPLA2
10 PLD. This device has numerous macrocells (5-1, 5-2, ...) which receive control term signals (CT1, CT2 ... - CT-8) via a common bus 4. These control term signals are generated via input signals input via a programmable input array 1 to an AND array consisting of a plurality of eight AND gates (2-1, 2-2, ... 2-8) each of which feeds a multiplexor (3-1, ... 3-8) that can provide either the inverted or non-inverted output of the respective product terms. Every
15 signal input to the input array 1 has both the true and complement. In coordination with the multiplexors, the AND array can appear either as Sum terms or as Product terms (but not both). Thus, in the above-described devices, the generated control term is limited to a simple AND equation, or to simple OR equations.

It is an object of the invention to provide a PLD with improved architecture for
20 controlling macrocells within a PLD.

SUMMARY OF THE INVENTION

Generally speaking, according to the invention, a programmable logic device includes a plurality of input lines for carrying a plurality of input signals, and a first array of
25 logic gates coupled to the input lines and implementing a logic function. A macrocell is coupled to the first array and implements a control function on the logic output of the first array in response to control terms received at control inputs of the macrocell. A control term programmable logic array (PLA) generates the control terms for the macrocell and includes (i) a plurality of programmable AND gates, each AND gate having a respective AND output and
30 a plurality of inputs each coupled by a programmable connection to associated ones of the plurality of input lines, for receiving input signals and (ii) a programmable OR gate having an OR output, and a plurality of inputs each coupled by a programmable connection to each of the AND outputs of the plurality of AND gates. Favorably, the control term PLA includes a plurality of additional programmable OR gates, each having an OR output coupled to the

macrocell and a plurality of inputs coupled by a programmable connection to each AND output of the plurality of AND gates.

The invention is based on the recognition that it is often desirable to control one or more macrocells within a PLD with "complex control terms," that is, control terms
5 generated with boolean equations having more than a single product term or sum term. The known prior art devices are only efficient at generating simple control terms. While complex control terms could be generated with these devices, it would require two or more passes, using the user logic and at least one macrocell. The first pass would implement a simple control term with the control term logic structure existing for that purpose. The output of the
10 first pass would use one macrocell and then be fed back as a new input to the user logic. The output of this second pass would be used as "as is" or combined with other inputs to create the complex control term. This feedback approach wastes a macrocell to create an internal signal that would otherwise be available for additional logic to be implemented by the user. Two passes requires more time (nanoseconds) to implement than is taken for single pass, simple control terms. Thus, generating complex terms in the previously described conventional
15 devices decreases the speed of the PLD and poaches on the capacity of the existing user logic.

By contrast, in the present invention, the PLA is efficient at generating complex control terms for the macrocells, so multiple passes are not needed to generate complex control terms. Within the PLA, every product term (AND gate) is available to every OR gate.
20 Thus, the PLA provides inherent flexibility to create complex Sum-of-Product equations. Additionally, the ability to use a single Product term in more than one Sum term increase effective density. Furthermore, Sum-of-Product Asynchronous clock signals can be generated with the control term PLA, which was not possible with the prior art devices described herein. Such Asynchronous clock signals are desirable because they permit great flexibility in
25 controlling the macrocells, due to their programmability, as compared to synchronous clock signals which are not user modifiable.

Favorably, in a complex PLD, a plurality of macrocells are coupled to a plurality of user logic arrays in a common logic block. The control terms for each of the macrocells in the logic block are generated by one PLA and distributed to the macrocells via a
30 communication channel, such as a bus.

These and other object, features and advantages of the invention will become apparent with reference to the following detailed description and the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a prior art PLD, illustrating generation of simple control terms for a plurality of macrocells;

Figure 2 shows a PLD according to the invention with a PLA which generates
5 complex control terms for each of a plurality of macrocells;

Figure 3 illustrates an embodiment for a logic array 300 of Fig. 2 including a portion of the programmable input array 100; and

Figure 4 illustrates an exemplary macrocell 400.

10 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 2 illustrates a PLD according to the invention which includes an input array 100, a plurality M of logic arrays (400-1, 400-2, ... 400-M) and a plurality M of macrocells (500-1, 500-2, 500-M). The plurality of logic arrays 400 and their associated macrocells 500 form a logic block 600. A control term PLA 200 provides control term logic
15 and outputs control terms on the communication channel 300 which connects the outputs of the PLA 200 to each of the macrocells 500. A PLD device may have a plurality of these logic blocks 600 and associated PLA's 200.

The input array 100 includes a first portion 120 for control term input signals for the PLA 200 and a second portion 140 for receiving logic inputs for the user logic arrays
20 400. Physically, the input array 100 is a single programmable input array having a plurality of input lines 70. A single logic input signal may be input to one or both of (i) the control term PLA 200 and (ii) any of the user logic arrays 400. Alternatively, however, it is also possible to have different, mutually exclusive sets of input lines for the portions 120, 140, although this would be less flexible than with common input lines.

25 The array 200 is known in the art as a PLA, for "programmable logic array". The array 200 has an AND array including a plurality (L) of AND gates 21 (21-1, 21-2 ... 21-L). Each of the AND gates 21 has a plurality of AND inputs (N) represented by the slashed single line 22 and a respective AND output feeding output lines 23. The array 200 also includes an array of a plurality (O) of OR gates 24 (24-1 ... 24-O)

30 Each of the AND inputs (collectively represented by line 22) of each AND gate 21 has a programmable connection with each of a plurality N of input lines 70 of the input array 100. Each of the programmable connections is represented by a circle at the intersection of the input lines 70 and the lines 22, only a few of which are shown for the sake of clarity. Similarly, each of the OR gates 24 has a plurality (L) of OR inputs (collectively represented by

lines 26) each having a programmable connection with each of the AND output lines 23 so as to selectively receive the logical output of any of the AND gates 21-1 ... 21-L. The programmable connection of each of the multiple inputs of the OR gates 24 to the output lines 23 is represented by the single lines 26 and the circled intersections with the lines 23 (only
5 some of which are shown for purposes of clarity). Each of the OR gates 24 has a respective logical OR output provided on output lines 25.

As used herein, the term "programmable connection" means any device which is capable of being programmed to electrically close or open a circuit connection between two circuit elements which it functionally connects. Accordingly, this term includes, but is not
10 limited to, fuses, antifuses, electrically-erasable floating gate memory elements and SRAM memory elements.

Within the logic block 600, each of the logic arrays 400 may be any of the type conventionally used in the art. For example, the logic array 400-1 may be a PAL array as illustrated in Fig. 3. The PAL array 400-1 implements a Sum of Products function and
15 includes a plurality (P) of AND gates 31 (31-1 31-P) each of which has a plurality of inputs (collectively represented by lines 32) which can be programmed to receive any of the N input signals. Each AND gate has an AND output 33 which has a non-programmable, or fixed, connection to a respective input of the OR gate 34. This OR gate has an output 35 which is the Sum of Products of the signals provided on inputs 32.

Fig. 3 also illustrates a typical architecture for connecting the signal input lines to the AND gates of the PAL array 400-1 and the PLA 200. The input lines 70 are each connected in series with an inverter 71 whose respective outputs provide opposite polarity (high and low; "1" or "0") signals of the signal input at a respective input 70 on lines 71(a). The non-inverted signal is available on line 71(b). Each dual line 71(a), 71(b) may be
25 connected by a programmable connection to the multiple N inputs of each of the AND gates 31-1...31-P and 21-1...21-L of the PAL and PLA arrays 400-1, 200. This connectability is represented by the circle at each intersection of the lines. Thus, for example, where the AND gates 31 have eighty (80) inputs each, the input array would have (40) forty inputs, each AND gate then being capable of receiving forty signals and forty inverted signals. Fig. 3 also
30 illustrates the implementation of one type of boolean logic which a user may desire to implement, in this case an XOR function $A * \text{XOR} * B * \text{XOR} * C$ of the PAL array 400-1. For example, AND gate 31-1 provides the boolean product of $A * B * C$ by selective connection of various ones of the 'N' input lines (represented by single line 32) to the non-inverted line 71(b) for input signal A and the inverted lines 71(a) of the input signals B and C.

The logic block 600 (Fig. 2) may have any number of logic arrays 400, for example twenty (20), which may be all of the same type or different. For example, instead of a PAL array as illustrated in Figure 3, some or all of the arrays may be a PLA like the array 200. Additionally, it is noted that a signal present on an input line 70 may be used both for user logic and to generate a control term by programming of the input array 100.

Figure 4 is an example of one type of macrocell 500-1 which may be employed in a PLD, for example, to receive the output of the PAL array 400-1. The macrocell includes an input line 51 connected to the output 35 of OR gate 34 of logic array 400-1. Flip flop 65 receives the logic output of the PAL array 400-1 and is configurable to operate as a D-type flip flop or as a T-type flip flop. The output Q of flip flop 65 is coupled to one input of a multiplexor 53, while the other input of this multiplexor is coupled directly to input line 51. The output of multiplexor 53 is coupled to the input 54 of output buffer 55, the output of which is connected to a three-state output circuit 67, which three-state output circuits are known in the art. The control terminal 56 of output buffer 55 receives control terms CT3-CT6 via multiplexor 57 and output enable control multiplexor 58. The initialize input INIT of flip flop 65 receives initialization control terms CT1 and CT2 via multiplexor 59. The clock input on line 62 receives clock signals via multiplexors 60 and 61, including control terms CT7, CT8 for asynchronous clock signals.

The Macrocell 500-1 is configurable to operate in various modes: Registered versus Combinatorial; Registered operation as a D' Flip-Flop or a T' Flip-Flop; Behavior of the Flip-Flop when an INIT signal is received (reset to logic '0' or set to logic '1'). These options are typically configured statically, that is they are set by programming associated memory elements and retain the desired functionality during the entire duration of operation.

It is desirable, however, to have other macrocell functions that are dynamic, such as, for example, the control of the output circuit 67 to be actively driven or set to a three-state condition. In a user's circuit design, a particular output line on a printed circuit board employing the above-described PLD may be shared by multiple outputs from a like number of devices. These outputs may go to one or more other devices as inputs. By using logic signals, the outputs of all of the devices that share this common line may be controlled in such a way that only one device at a particular point in time is actively driving the line, and all other devices are three state (if this is not done, and multiple devices are driving the line simultaneously, damage to the devices may occur). In a like fashion, using logic to control multiple recipients of this data can also be used. This is a technique that is commonly used in data busses that have multiple potential sources of, and destinations of data, to effectively

route source to destination. Both cases are applications where the PLA 200 is useful in generating complex control terms for the macrocells 500.

As a specific example of this, assume we have a device 'A' that could be a source of data that shares a common line with other devices. Also assume that there are 3
5 signal lines, coupled to input lines 70 from some controlling devices, that indicate when the PLD 100 is supposed to provide data. These signals, called 'Request_1', 'Request_1_Enable', and 'Request_2', are defined such that data is to be driven by output buffer 55 at any time when both Request_1 and Request_1_Enable are true, or at any time when Request_2 is true regardless of the state of the other two input signals. Therefore, the logic equations which
10 dynamically control the output buffer for this example are:

$$\begin{aligned} A_output_enable &= (Request_1 \& Request_1_Enable) \quad (EQ. 1) \\ &\# Request_2; \end{aligned}$$

15 Where the & represents a logical AND operation and the # represents a logical OR operation. In this simple example, using conventional devices, discussed previously, to control the output buffer 55 would require two passes through the logic array of the conventional devices (and therefore be slower), and uses an additional macrocell to create the needed logic. In the PLA 200, this equation may be generated in directly in a single pass.

20 In a similar fashion, dynamic logic may be created to control the clocking of the macrocell 500-1 and the signal that sets or resets the initialize input 'INIT' of macrocell 500-1 for similar advantages. Other dynamic functions, such as polarity control of the output, or macrocells that deploy dynamic configuration of registered versus combinatorial operation, or other operations not detailed here could also benefit from the use of a control term uPLA.

25 With reference to the macrocell 500-1, the control term signals are generated by PLA 200 as follows. (Fig. 2) The three input signals are routed to the input array 120 on lines 70. Via programmable connections in the array 120 the signals Request_1 and Request_1_Enable are routed to an input line 22 of an AND gate, such as gate 21-1. In the same array, the signal Request_2 is routed to some other AND gate input by itself, such as
30 gate 21-2. Both of these AND gates generate results that are available to all OR gates 24 via the routing effect of this PLA array. Since the desired function is an "Output Enable" control, this function must be generated on an OR gate that is associated with this function. Referring to our example macrocell in Figure 4, the Control Terms associated with the "Output Enable" function are CT3, CT4, CT5, and CT6, as these signals are coupled to output buffer 55 via

multiplexor 57, 58. In this implementation, for all macrocells in a logic block 600, the same 4 control terms are used for "Output Enable", and at each macrocell 500 the user can statically configure the output buffer 55 to be under dynamic control of any one of the Control Terms, or the buffer may be permanently turned on, or permanently turned off.

5 In the PLA 200, for our example, we show 8 OR gates. The output of the OR gate is referred to herein as a "Control Term". The output of the first OR gate (24-1) is sent to all macrocells in logic block 600 and in each macrocell is referred to as Control Term 1 or CT1. The output of OR gate 24-2 is CT2, and so forth. For our output enable example this means that the desired logic must be generated on either CT3, CT4, CT5 or CT6. Let's assume
10 that we use CT3 to generate the logic. The output of the two AND gates 21-1 and 21-2 are routed to the third OR gate, 24-3, where the final logic for the "Enable Output" equation (EQ.1 above) is generated. Note that this logic, now propagated via a signal line 300 to all macrocells in this logic block 600, may be used in any or all of the macrocells by proper configuration of the output enable control select multiplexor 58. Note also, that other output
15 enable logic equations may be generated on the remaining control terms for this function (CT4, CT5 & CT6), and they may be used on any combinations of outputs. In the example shown, there are eight control terms CT1-CT8. The communication channel in that case may be a simple bus consisting of eight conductive lines connecting the OR output of each OR gate to the respective control term input of each macrocell. It will be appreciated that many other
20 types of buses may be used.

 In a similar fashion, the output of the first two OR gates (24-1, and 24-2) are represented as CT1 and CT2 at all of the macrocells, and are used to control the Flip Flop asynchronous INIT feature. Likewise, the output of the last two OR gates (24-7, 24-8) are propagated to all Macrocells in the local block as LB_CT7_ACLK and LB_CT8_ACLK for
25 potential use as an Asynchronous (Equation based) clock by macrocells needing this functionality.

 Asynchronous clocks are those that have logic equations associated with them. Conventional (Synchronous) clocks are typically associated with pins that are dedicated for clock inputs, and are distributed to the flip flops 65 via special low skew clock networks that
30 guarantee highest performance to critical specifications, such as register set-up time and clock-to-output valid time. These Synchronous clocks do not have the ability to be modified by logic equations, and typically only offer the user the choice of using inverting or non-inverting polarity at a particular macrocell.

The flexibility to create a clock based on an equation leads to many possibilities. A simple example would be the ability to create a clock that runs only when a gating condition is true. For example, let's assume that we have a flip-flop 65 that we want to clock under several conditions (this flip-flop could represent a state in a state machine, and by controlling the clock, we control the conditions by which the states are allowed to change). The first input could be AS_CLK, a signal that we want to clock the flip-flop, but we only want this to happen when the AS_CLK_ENABLE signal is true. In addition, we want the flip-flop to clock whenever a third input, CLK_OVERRIDE is true, regardless of the state of the other clock inputs. This could be represented by the equation:

$$\text{FF_CLOCK} = \text{AS_CLK} \& \text{AS_CLK_ENABLE} \# \text{CLK_OVERRIDE}; \quad (\text{EQ. 2})$$

The capability of doing this Sum of Product clock is greatly enhanced by the availability of the PLA, in the same manner as the "Output Enable" example as discussed in detail above with respect to equation 1.

While the macrocell in Figure 4 is shown as receiving the output of only one logic array, from array 400-1, in practice additional logic structure may be inserted so that it may receive data from multiple arrays. For example, a programmable OR and a fixed XOR gate, in conjunction with a multiplexor, may be used to programmably combine the logic output from two user logic cells.

Using the PLA 200 for generating the control terms CT1-CT8 has the advantage of both increased speed and avoiding the starvation of logic gates from the neighboring user logic arrays. Note that the PLA employs both a fully programmable AND array (gates 21-2 through 21-L) and a fully programmable OR array (gates 24-1 through 24-0). This means that the output of every AND gate is available as an input to every OR gate. This inherent flexibility facilitates the implementation of complex Sum-of-Product equations in generating control signals for distribution to each cell. Additionally, the ability to use the output of one product term (AND gate) with more than one Sum Term (OR gate) increases effective density. For example, if the PLA 120 is 8 AND gates feeding 8 OR gates, and the number of inputs to the AND array is 36 (With true and complement = 72), then we can generate a Control Term that has an 8-wide OR gate (Sum Term), fed by 8 AND gates (Product Term), each of which has as many as 36 inputs. Without the PLA 120, we cannot generate a Sum of Products Equation in a single pass - we can only generate a single AND

gate - or - a single OR gate, which can be as wide as 36 inputs. Therefore, even the relatively simple Sum of Products equation 'Output Enable' (EQ.1 above) cannot be generated in a single pass with only simple control terms.

5 This ability to generate complex control terms means that, as compared to known prior art implementations, many complex control terms can be accomplished in one pass through the array, instead of two, which increases the speed of the PLD.

10 The process or technology by which the PLD of the invention is made is not important and any of the standard bipolar, NMOS or CMOS processes can be used. Also, it will be clear from the foregoing that the number of array elements, i.e., the array size, in any of the arrays can be varied without departing from the principles described herein. Particularly, the size of the PLA 200 will be dependent on the complexity of the control term needed to control the macrocells, which in turn is dependent on the complexity (number of features) of the macrocells.

15 Although preferred embodiments of the present invention have been shown and described, it will be appreciated by those skilled in the art that changes may be made in these embodiments without departing from the principles and spirit of the invention, the scope of which is defined in the claims.

20 The many features and advantages of the invention are apparent from the detailed specification and it is intended by the appended claims to cover all such features and advantages which fall within the true spirit and scope of the invention. Since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation illustrated and described, and accordingly all suitable modifications and equivalents may be resorted to, falling within the scope of the invention.

CLAIMS:

- 1) A programmable logic device, comprising:
a plurality of input lines (70) for carrying a plurality of input signals;
a first array of logic gates (400) coupled to said input lines, which first array implements a logic function and includes a logic output;
- 5 a macrocell (500-M) coupled to said logic output of said first array, said macrocell including an output (67) and a control term input (CTI); and
a control term programmable logic array (PLA)(200) comprising
a plurality of programmable AND gates (21), each AND gate having a respective AND output
and a plurality of inputs (22) each coupled by a programmable connection to associated ones
10 of said plurality of input lines (70) for receiving said input signals, and
a programmable OR gate (24-1), said OR gate having an OR output (25) which outputs a control term for said macrocell, and a plurality of inputs (26) each coupled via a programmable connection to each of said outputs (23) of said plurality of AND gates,
said control term input (CTI) of said macrocell being coupled to said output (25) of said OR
15 gate (24-1) of said control term PLA, and
said macrocell implementing a control function on said output of said first array (400) in response to a control term received at said control term input.
- 2) A programmable logic device according to claim 1, wherein said macrocell has
20 a plurality of control term inputs (CTI-CT8), and said control term PLA includes a plurality of OR gates (24) each (i) coupled via a programmable connection to each of said outputs of said AND gates (21) and (ii) each having an OR output (25) coupled to a said control term input (CTI-CT8) of said macrocell.
- 25 3) A programmable logic device according to claim 2, further comprising a plurality of said macrocells (500-1), and a communication channel (300) coupling each of said OR outputs (25) of said control term PLA to associated ones of said control term inputs (CTI-CT8) of each of said macrocells.

4) A programmable logic device according to claim 3, further comprising another, programmable logic array (400-2) for implementing user logic.

5) A programmable logic device according to claim 3, wherein said first array of logic gates (400-1) comprises a programmable array logic (PAL) (Fig. 3) comprising a plurality of AND gates (31), each AND gate having a plurality of inputs (32) coupled by a programmable connection to said input lines (70) and an AND output (33), and an OR gate (34) having a plurality of inputs each coupled by a non-programmable connection to each of said AND gates of said PAL.

6) A programmable logic device according to claim 3, wherein said first array of logic gates comprises a programmable logic array (PLA) (like 200) comprising a plurality of programmable AND gates, each AND gate having a respective AND output and a plurality of inputs each coupled by a programmable connection to associated ones of said plurality of input lines, and a programmable OR gate, said OR gate having an OR output and a plurality of inputs each coupled by a programmable connection to each of said AND outputs of said plurality of AND gates of said PLA.

7) A programmable logic device according to claim 1, further comprising a plurality of said macrocells (500), and a communication channel (300) coupling said OR output of said control term PLA to said control term input of each of said macrocells

8) A programmable logic device according to claim 1, wherein said macrocell includes an input (CT8) for receiving an asynchronous clock control term input, and said OR gate is programmed to output said asynchronous clock control term input.

9) A programmable logic device according to claim 1, wherein said macrocell includes an output buffer having an output enable control term input (CT3) and being switchable between an output enable state and an output disable state, and said OR gate being programmed to output said output enable control term.

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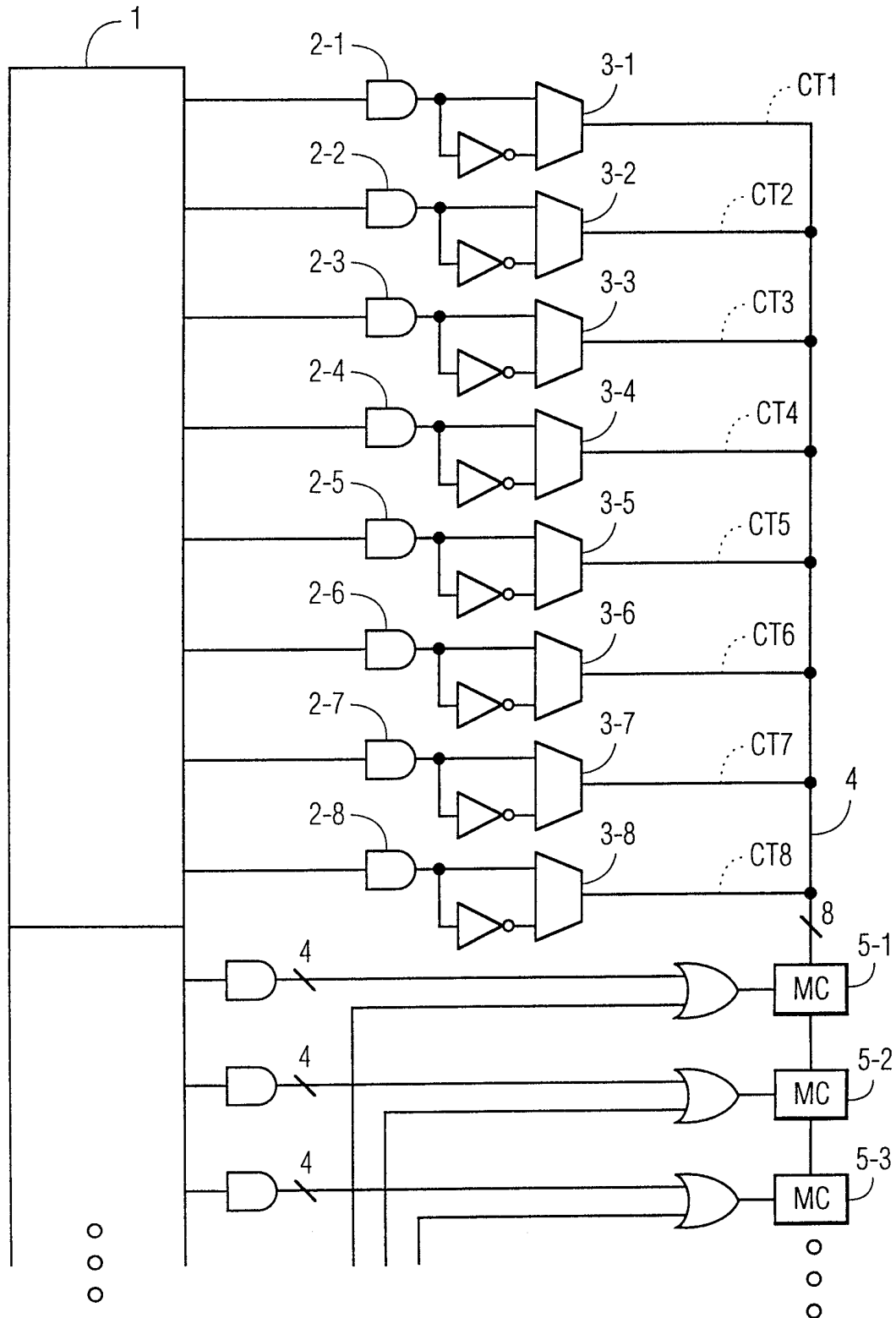


FIG. 1

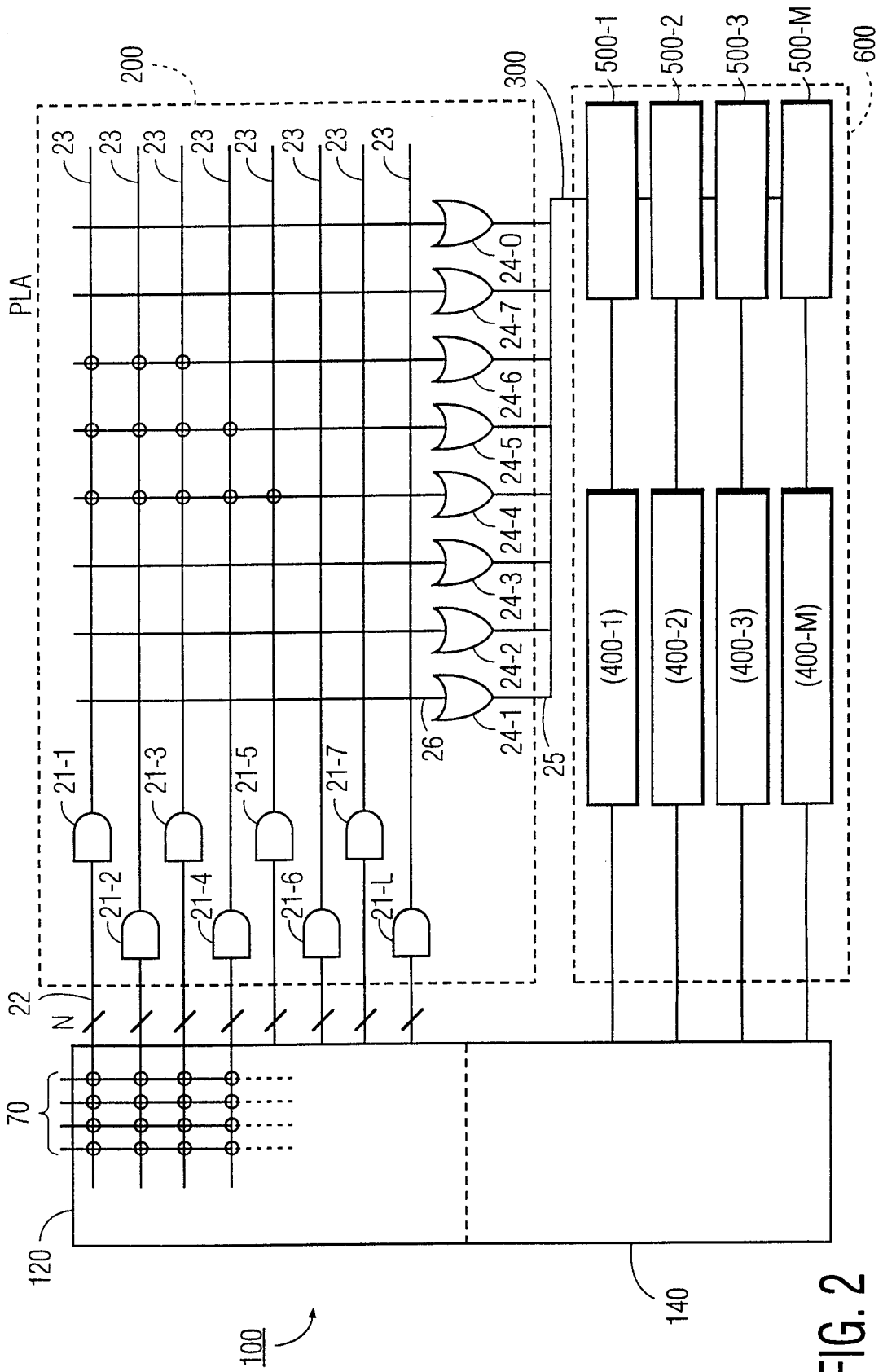


FIG. 2

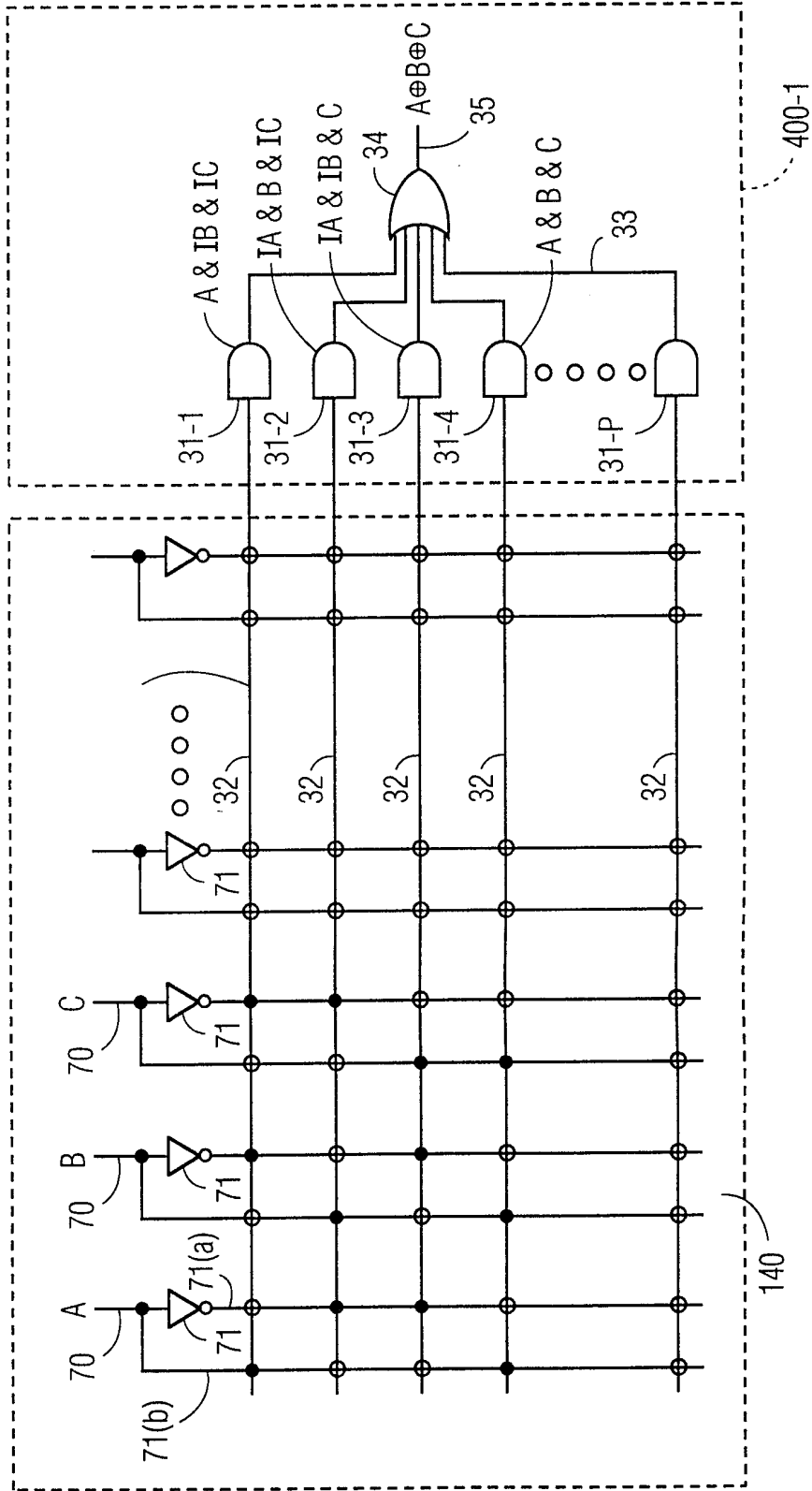


FIG. 3

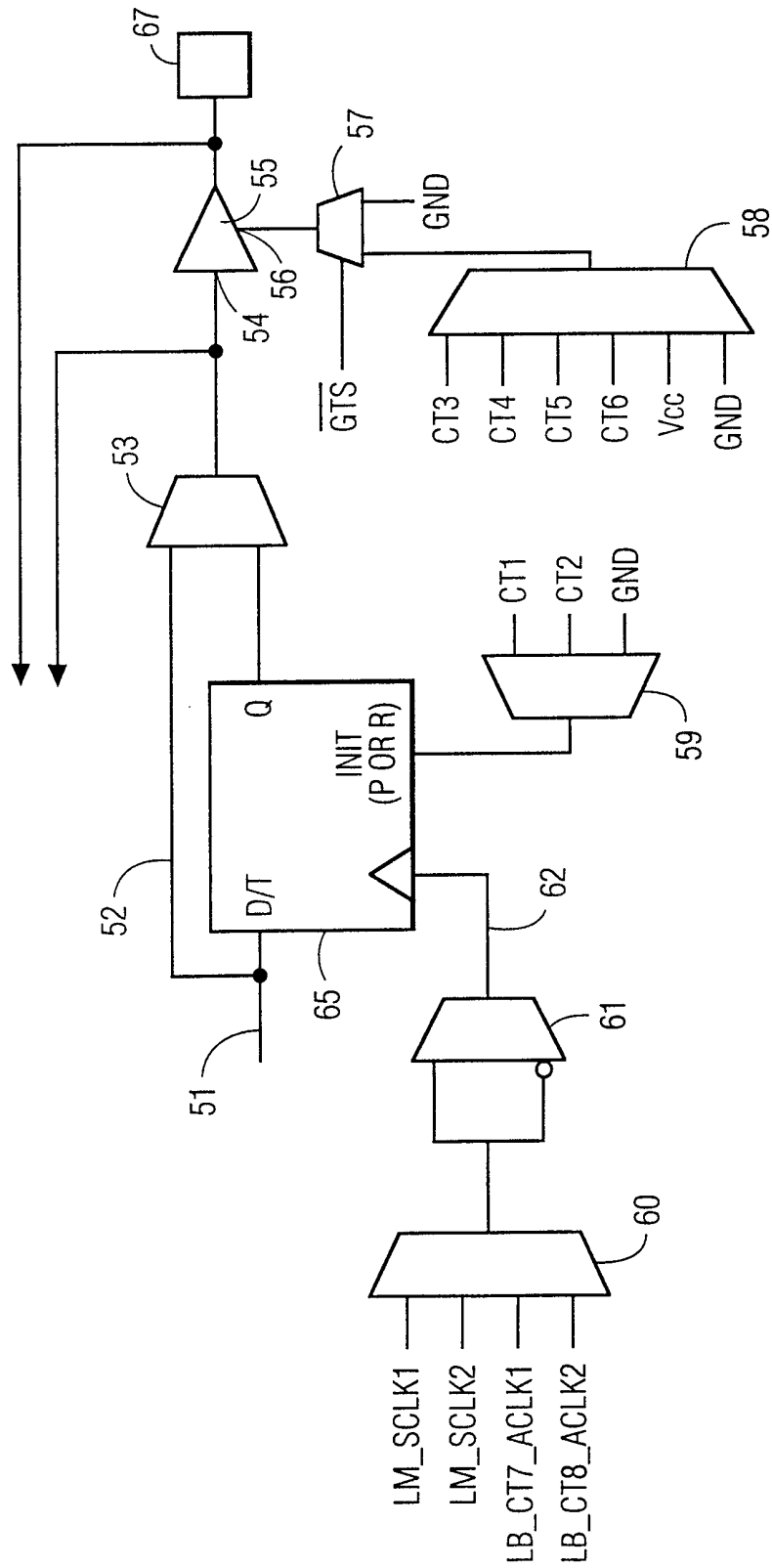


FIG. 4