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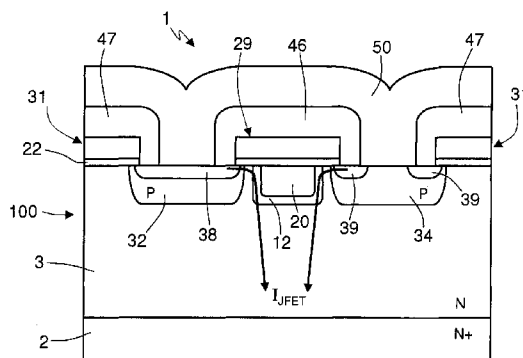


Fig.13

(57) Abstract: A vertical-conduction electronic device (100; 150), comprising: a semiconductor wafer (1) including a semiconductor layer (2, 3) having a first side (3a), a first type of conductivity (N), and a first doping level; a first body region (32) and a second body region (34), which have a second type of conductivity (P) and extend in the semiconductor layer (2, 3); an enriched region (12), having the first type of conductivity and a second doping " level higher than the first doping level, which extends in the semiconductor layer facing the first side (3a), between the first and second body regions (32, 34); a dielectric filling region (20), which extends in the semiconductor layer, facing the first side (3a), and completely surrounded by the enriched region (12); and a gate structure (29), which extends on the first side (3a) on the enriched region (12), on the dielectric filling region (20), on part of the first body region (32), and on part of the second body region (34).

VERTICAL SEMICONDUCTOR DEVICE AND MANUFACTURING PROCESS OF THE SAME

TECHNICAL FIELD

5 The present invention relates to a vertical-conduction electronic device and to a process for manufacturing the same. In particular, the present invention relates to a MISFET (Metal Insulator Silicon Field Effect Transistor) device.

BACKGROUND ART

10 As is known, the performance of vertical-conduction power MISFET devices is affected by the presence of parasitic components, which produce effects that vary according to the operating conditions. For instance, vertical MOSFET devices (VMOSs) comprise body regions, having a conductivity type
15 (e.g., of a P type), housed at a short distance from one another in a substrate or epitaxial layer having an opposite conductivity type (e.g., of an N type). Body regions extending alongside one another, together with the portion of the epitaxial layer that separates them, form a parasitic JFET,
20 which is activated when the VMOS device conducts.

The resistance of the parasitic JFET basically depends not only upon the operating conditions and the doping level of the epitaxial layer, but also upon its channel width, i.e., upon
25 the distance between body regions extending alongside one another. In practice, the greater the distance between the body regions, the lower the resistance of the JFET, and vice versa. On the other hand, the portion of epitaxial layer forming the channel of the JFET is overlaid by gate
30 electrodes, normally made of polysilicon, which are insulated only through a gate-oxide layer and remain capacitively coupled. The effect of the capacitive coupling, however, increases as the distance between the body regions increases, unlike the resistance of the parasitic JFET, which decreases.
35 Consequently, it is not possible to act on such a distance for reducing the resistance of the parasitic JFET, without

penalizing the dynamic characteristics of the VMOS device. Moreover, the increase in the distance between the body regions is in conflict also with the requirement of reducing the dimensions of the devices, which is of increasing importance in modern microelectronics.

Various measures have been proposed for overcoming these drawbacks.

A first measure envisages an enrichment implant for increasing doping in a surface layer of the wafer housing the VMOS device so as to increase the conductivity. Alternatively, the enrichment can be obtained by epitaxial growth of a layer having an appropriate doping level. In some cases, however, and especially for low-voltage devices, the maximum doping of the body regions differs only a little from the doping of the epitaxial layer. The surface enrichment extending to the entire wafer could thus interfere significantly with the threshold voltage and the length of the VMOS channel (which extends in the proximity of the surface of the body regions) and even jeopardize operation of the device (premature "punch-through"). For this reason, the surface enrichment is normally made selectively, for example with masked implants, and confined to portions of the epitaxial layer comprised between the body regions and set at a slight distance from the latter.

A further measure aimed at improving the dynamic performance regards the use of gate-oxide layers with differentiated thicknesses. More precisely, localized growths of oxide are performed above the areas forming the channel of the parasitic JFET. A solution of this type is described, for instance, in the patent document No. US 7,800,173. In this solution, however, the gate charge, the dynamic performance, and the capacitance associated to the oxide in the region between the cells are not optimized.

DISCLOSURE OF INVENTION

The aim of the present invention is to provide a vertical-conduction electronic device and a corresponding manufacturing process that will enable the drawbacks of the known art to be overcome, and in particular will enable a reduction of the parasitic resistance and of the dimensions, without jeopardizing the dynamic performance.

According to the present invention, a vertical-conduction electronic device and a corresponding manufacturing process are provided as defined in the annexed claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, preferred embodiments thereof are now described, purely by way of non-limiting example and with reference to the attached drawings, wherein:

- Figures 1-13 show manufacturing steps for forming a vertical-conduction electronic device (in particular, a VDMOS) according to one embodiment of the present invention;
- Figure 14 shows a vertical-conduction electronic device according to a further embodiment of the present invention;
- Figure 15 shows a schematic cross section of a semiconductor device according to one embodiment of the present invention; and
- Figure 16 shows a system that uses the electronic device according to any one of the embodiments of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Figure 1 shows a wafer 1 of semiconductor material in an initial step of a process for manufacturing a vertical-conduction metal-insulator-silicon FET (or vertical MISFET) device, in particular a vertical-conduction MOS, or VMOS, transistor, even more in particular a double-diffused vertical-conduction MOS (VDMOS) transistor. However, this must not be considered limiting in so far as it is possible to provide also vertical MISFET devices of some other type, such as for example IGBTs.

The wafer 1 comprises a substrate 2, of an N type (in particular having a heavy doping of an N+ type), with a front side 2a and a rear side 2b, opposite to one another. The wafer 1 further comprises a semiconductor layer 3 that is less doped (in the example, with a doping of an N type), for instance grown epitaxially on top of the front side 2a of the substrate 2 (in what follows, designated as "epitaxial layer 3"). The epitaxial layer hence has, in this step, a front side 3a of its own exposed and a rear side 3b coinciding with the front side 2a of the substrate 2.

The wafer 1 is, for example, of a pre-processed type. For instance, the wafer 1 comprises, in a way not shown in the figures, board-termination structures formed by field-oxide regions designed to delimit one or more active areas 4 in the epitaxial layer 3. The active area 4 houses the VDMOS device.

Next (Figure 2a), formed on the front side 3a of the epitaxial layer 3 is a protective layer 7 having the function of stopping layer for subsequent steps of etching and cleaning of the front 3a of the wafer 1. The protective layer 7 is, for example, made of silicon nitride or silicon oxide, or some other material. The protective layer 7 is, according to one embodiment, formed by chemical vapour deposition (CVD), and has a thickness comprised between approximately 10 nm and approximately 300 nm, for instance approximately 100 nm.

According to an alternative embodiment (not shown in the figures), the protective layer 7 is omitted.

The next step is formation of a trench 8 in the epitaxial layer 3. The trench 8 extends in the epitaxial layer 3 for a depth, measured starting from the front side 3a, comprised between approximately 0.1 μm and approximately 1.5 μm , for instance approximately 0.8 μm . In general, the depth of the

trench 8 depends upon the class of voltage of the device and is the greater the higher the class of voltage considered.

According to one embodiment, the trench 8 has the shape, in top plan view, of a strip, as shown in Figure 2b.

To form the trench 8, a photoresist layer 10 is formed on top of the protective layer 7. Then, by means of a step of photolithography, an opening is defined in the photoresist layer 10 until a portion of the protective layer 7 is exposed. Said opening has a shape, in top plan view, corresponding to the desired shape for the trench 8. The next step is that of etching the protective layer 7, for example using a dry etch. Other types of etching, for instance wet etching, can be used according to further embodiments. This is followed by a step of etching of the epitaxial layer 3, for example an anisotropic dry etch, using, as etching chemistry, a mixture of SF_6 and C_4F_8 . The trench 8 thus formed presents substantially vertical side walls 8' (i.e., extending substantially orthogonal to the front side 3a), and a bottom 8" extending in a plane substantially parallel to the front side 3a.

Then (Figure 3), there follows a step of formation of an enriched region 12 within the trench 8.

According to one embodiment, the enriched region 12 is formed by an enrichment implant, exploiting the mask formed by the protective layer 7 and the photoresist layer 10 (which protects the entire front side 3a except for the portion of the epitaxial layer 3 in which the trench 8 has been formed during the step of Figure 2a). Then, following upon the implantation step, the photoresist layer 10 is removed. The photoresist layer 10 can also be removed prior to the step of enrichment implantation. In this case, the mask for the enrichment implant is formed by just the protective layer 7.

In greater detail, in the embodiment described herein, in which an N-channel device is provided, the enriched region 12 is of an N type and is obtained using dopants such as phosphorus or arsenic, with a density comprised between 5 10^{13} atoms/cm³ and 10^{17} atoms/cm³. The implantation energy, moreover, is such that the dopant species extend in the epitaxial layer for a final depth, measured starting from the inner walls 8' and the bottom 8" of the trench 8, comprised between approximately 0.3 μ m and approximately 1.0 μ m, for 10 instance approximately 0.7 μ m. According to one embodiment, the implantation dose is approximately constant along the entire side walls 8' and the bottom 8" of the trench 8. As is known, to provide a constant implantation profile on the side walls 8' and on the bottom 8" it is possible to configure the 15 angle of implantation appropriately during the implantation step.

There is then carried out a step of thermal treatment in a hydrogen environment at high temperature (for example, 1000°C 20 - 1150°C) for annealing surface damage possibly caused during etching or enrichment implantation.

According to a different embodiment, in the case of a P-channel device, dopants such as boron or aluminium 25 substantially with the same concentrations indicated above can be implanted.

The enriched region 12 can be formed according to a technique different from the implantation of dopant species represented 30 in Figure 3, namely, by partial filling of the trench 8 through a process of epitaxial growth. Said variant is shown in Figure 4. Partial epitaxial filling of the trench 8 is preferably uniform and is obtained by growth of a layer of monocrystalline silicon with a doping of an N type (and with a 35 doping value higher than that of the epitaxial layer 3) according to the known art. For instance, the process of

epitaxial growth is carried out in a chamber for epitaxial growth in the presence of phosphorus or arsenic atoms in such a way that the region grown epitaxially will have a density of dopants comprised between 10^{13} atoms/cm³ and 10^{17} atoms/cm³. The enriched region 12 is thus obtained. The enriched region 12 thus formed extends over the inner walls 8' and on the bottom 8" of the trench 8 and has an approximately uniform thickness comprised between 0.3 μ m and approximately 1.0 μ m, for example approximately 0.7 μ m.

According to one embodiment, in order to obtain a uniform filling of the trench 8, an appropriate chemical etching agent is used within the epitaxial-growth reaction chamber, mixed with the source gas used for the epitaxial growth itself, said chemical agent being able to modulate appropriately the rate of epitaxial growth. In this way, a dynamic balancing is obtained between the epitaxial growth along the walls 8' and the bottom 8" of the trench 8 and the simultaneous removal of part of the layer grown so as to obtain an epitaxial layer that extends homogeneously over the walls 8' and on the bottom 8". In other words, there is obtained a balancing *in situ* (i.e., provided within the epitaxial-growth environment itself) of the growth and simultaneous etching of an epitaxial layer, such as to modulate appropriately and dynamically the shape of the regions of material grown and of the trench 8 in the filling step and thus obtain uniform filling of the trench 8 itself. In addition, the trench is prevented from closing at the top during the step of formation of the enriched region 12.

According to one embodiment, hydrochloric acid (HCl) is used as chemical etching agent, appropriately supplied into the reaction environment together with the silicon-source gas, for instance constituted by dichlorosilane (DCS - SiH₂Cl₂); the role of hydrochloric acid (HCl) is, as has been said previously, that of modulating the rate of epitaxial growth

appropriately. In the reaction environment there is moreover present a gas carrier, which enables modulation of the partial pressure of the reagent species and also participates in the overall reaction of epitaxial growth; by way of example,
5 molecular hydrogen (H_2) can be used as gas carrier.

As has been said, within the same reaction chamber as that used for the epitaxial growth there is moreover supplied an appropriate doping agent, such as to enable a desired dopant
10 profile of the enriched region 12 to be obtained. For instance, for this purpose an appropriate flow of phosphorus or arsenic is used to obtain a doping of an N type. In the case of a P-channel electronic device, it is possible to use diborane (B_2H_6).
15

During the epitaxial process, the competitive behaviour of the etching agent (in the example, HCl) and of the growth agent (in the example, DCS) is appropriately exploited so as to modulate the shape of the material grown within the trench 8
20 and prevent formation of defects (in particular, residual voids).

One embodiment envisages in particular that the filling step for epitaxial growth comprises one or more sub-steps, each of
25 which is characterized by an appropriate competitive action between etching and epitaxial growth, determined by a corresponding ratio between the flow of HCl and the flow of DCS supplied in the reaction environment (Φ_{HCl}/Φ_{DCS} ratio). This process is described in detail in the Italian patent
30 application No. TO2010A000642 and in the international patent application No. PCT/IB2011/001724.

By varying the value of the Φ_{HCl}/Φ_{DCS} ratio it is possible to modulate the rate of growth at the bottom 8" of the trench 8
35 in such a way as to render it faster than, the same as, or slower than the rate of growth at portions of the side walls

8' close to the front side 3a. An appropriate alternation of these steps prevents premature closing of the fronts of growth from the side walls before filling on the bottom is completed.

5 In general, in the course of these steps, the process evolves in growth regime, i.e., with a predominance of the epitaxial growth of material over etching of the material grown (and possibly pre-existing). When necessary, it is possible to increase the value of the $\Phi_{\text{HCl}}/\Phi_{\text{DCS}}$ ratio so as to cause the
10 process to evolve in the opposite direction (prevalence of etching of the material grown, in particular in the proximity of the surface of the wafer 1).

The partial-filling layer made of monocrystalline epitaxial
15 silicon thus obtained coats the bottom 8" and the side walls 8' of the trench 8 and forms the enriched region 12.

It is moreover pointed out that, in order to maintain a uniform distribution of dopant within the enrichment region
20 12, the flows of dopant within the growth chamber are regulated in such a way that the ratio between the flow of dopant Φ_D and the flow of HCl Φ_{HCl} (i.e., the ratio between the flows of the dopant species and of the etching agent) will remain constant during the entire process of epitaxial growth,
25 notwithstanding the variation of the $\Phi_{\text{HCl}}/\Phi_{\text{DCS}}$ ratio, for the reasons described previously of modulation of the epitaxial growth. Basically, the flow of dopant is accordingly varied and regulated as a function the flow of HCl. Evidently, it is, however, possible to obtain different doping profiles
30 according to the specific implementation requirements by appropriately varying the flow of the dopant species within the reaction environment during the process of filling of the deep trenches 4.

35 As shown in Figure 4, the trench 8 is only partially filled with the enriched region 12. This is even more true with

reference to the embodiment of Figure 3, where the trench 8 does not present a layer of partial filling and the enriched region 12 is formed by means of implantation.

5 Irrespective of whether the embodiment of Figure 3 or that of Figure 4 is adopted, after formation of the enriched region 12, the trench 8 is completely filled by dielectric material (dielectric filling region 20 in Figure 5a). The dielectric filling region 20 is formed by means of a step of deposition
10 (for example by CVD - Chemical Vapour Deposition) of dielectric material such as silicon oxide or silicon nitride. Alternatively, the dielectric filling region 20 is formed by thermal growth of dielectric material (in particular, silicon oxide - SiO_2), or using some other appropriate technique. In
15 any case, it is preferable to choose dielectric materials different from one another to form the dielectric filling region 20 and the protective layer 7 in such a way that, during successive steps of definition/removal of the dielectric filling region 20 or of the protective layer 7,
20 said step of definition/removal is selective towards one between the dielectric filling region 20 and the protective layer 7 and will not damage the other between the dielectric filling region 20 and the protective layer 7.

25 Figure 5b shows the wafer 1 of Figure 5a in top plan view. The wafer 1 has, in this embodiment, a structure made up of strips.

The process of filling of the trench 8 terminates with a
30 possible step of surface planarization (CMP - Chemical Mechanical Planarization) in order to remove portions of dielectric that have formed on top of the protective layer 7 (in particular, this occurs when the dielectric filling region 20 is formed by means of deposition). The protective layer 7
35 has, during this planarization step, the function of planarization-stopping layer. In fact, machines commonly used

for CMP are provided with sensors for monitoring the progression of the planarization step, and recognizing when a layer of a certain material (here, SiN) has been reached, automatically interrupting the CMP process.

5 In a different embodiment, the planarization is carried out by dry plasma etching (for example, using a plasma with a base of Ar, CF₄, CHF₃ and CO). Also in this case, the protective layer 7 is used as etch-stopping layer.

10 The protective layer 7 consequently remains on top of the front side 3a of the epitaxial layer 3 at the end of the planarization process. The protective layer 7 is then removed (Figure 6) by means of an etch of a wet type, using an appropriate etching chemistry. There is then obtained a wafer 15 1, the top surface of which is the front side 3a of the epitaxial layer 3.

At the end of the process of formation of the enrichment region 12 and of the dielectric filling region 20, the manufacturing process proceeds with formation of a semiconductor device, for instance a semiconductor device such as a vertical-channel MOSFET.

25 With reference to Figure 7, a thin gate dielectric layer 22 is formed, having, for example, a thickness of between 10 nm and 150 nm. The gate dielectric layer 22 can be formed via thermal oxidation, or else via deposition of an oxynitride layer or of a multilayer constituted by the superposition of successive layers of oxide and nitride.

30 On top of the gate dielectric layer 22 a polysilicon layer 24 is deposited for a thickness comprised between 100 nm and 700 nm. The polysilicon layer 24 may be intrinsic and doped subsequently by ion implantation, or, possibly, already doped in the deposition step.

A gate mask 26 is then provided (Figure 8), which protects the wafer 1 around the enriched region 12 and in the proximity of the field-oxide regions (not shown) and has body windows 27 alongside the enriched region 12.

The polysilicon layer 24 and the gate dielectric layer 22 are shaped using the gate mask 26 to form at least one first gate electrode 29 and second gate electrodes 31. In greater detail, the gate electrode 29, which comprises a portion 24' of the polysilicon layer 24, is set on the enriched region 12 and the dielectric filling region 20 and extends laterally for a stretch on both sides of the enriched region 12. The gate electrode 29 is electrically insulated from the underlying layers by means of the portion 22' of the gate dielectric layer 22 extending between the gate electrode 29 itself and the front side 3a of the epitaxial layer 3. Further gate electrodes 31 are located at the edges of the active area 4 and in part overlying the field-oxide regions.

Using once again the gate mask 26, there is then carried out (Figure 9), a body implantation, followed by a first process of thermal diffusion, to obtain at least a first body region 32 and a second body region 34, both of a P type. Thanks to the process of thermal diffusion, the first body region 32 and the second body region 34 extend partially also underneath the first gate electrode 29 and the second gate electrodes 31. In particular, the first and second body regions 32, 34 extend in the proximity of the enriched region 12. The body regions 32, 34 extend in the epitaxial layer 3 for a depth equal to, or smaller than, the depth at which the enriched region 12 extends. In general, the overall depth, in the epitaxial layer 3, of the trench structure 8 provided with the enriched region 12 is approximately smaller than or equal to the depth in the epitaxial layer 3 to which the first and second body regions 32, 34 extend.

The body regions 32, 34 are electrically coupled together in a known way, by means of a connection here not shown.

5 After the body implant and the first process of diffusion, the gate mask 26 is removed, and a source mask 35 is provided, as shown in Figure 10a. For instance, the source mask 35 has a first window 36a, above the first body region 32 and aligned respectively to the region of the first gate electrode 29 and
10 to the region of the second gate electrode 31 that coats part of the first body region 32. In addition, the source mask 35 has two second windows 36b, 36c that leave respective portions of the second body region 34 exposed, and is aligned, respectively, to the portion of the first gate electrode 29
15 and of the second gate electrode 31 that covers part of the second body region 34.

There is then carried out a source implantation, followed by a second process of thermal diffusion. In this step, dopants of
20 an N type are introduced in the wafer 1 through the source mask 35 and made to diffuse to obtain a first source region 38, housed in the first body region 32 and two second source regions 39, both housed in the second body region 34.

25 Figure 10b shows the wafer 1 of Figure 10a in top plan view, in which there may be noted the structure made up of strips of the regions formed according to the steps so far described (for greater clarity the mask 35 is here not shown). In particular, it may be noted that the body regions 32, 34, and
30 source regions 38, 39 extend substantially parallel to one another to form respective strips. The dielectric filling region 20 extends between the body regions 32, 34 right through them.

35 Next (Figure 11), the source mask 35 is removed, and an insulating layer 42 is deposited. The insulating layer 42 is

made, for example, of silicon oxide, with a thickness such as to incorporate the first gate electrode 29 and the second gate electrodes 31. Using a purposely provided mask (not illustrated here), the insulating layer 42 and the gate dielectric layer 22 are etched to obtain source windows 44, which expose partially the first source region 38 and the second source regions 39, as well as part of the second body region 34. There are thus delimited (Figure 12) first and second gate-insulation structures 46, 47 designed to protect and insulate electrically the first gate electrode 29 and, respectively, the second gate electrodes 31.

The manufacturing process is then completed with metallization steps (Figure 13), in which there are provided source contacts 50 by deposition of metal material and, moreover, gate and drain contacts (here not illustrated). A VDMOS transistor 100 is thus obtained, the structure of which is shown in Figure 13. The VDMOS transistor 100 includes a parasitic JFET, defined by the enriched region 12 and by the body regions 32, 34. When the VDMOS transistor 100 is active, a current I_{JFET} flows from the source regions 38, 39 to the substrate 2, which forms a drain terminal (not shown in Figure 13 is a drain metallization that is, however, present). The current I_{JFET} traverses channel regions (defined by surface portions of the body regions 32, 34), the enriched region 12 and part of the epitaxial layer 3. The parasitic JFET hence conducts. Its resistance, however, is low because the enriched region 12, which is heavily doped, has a high conductivity and, moreover, is affected only to a negligible extent by the effect of modulation of the body regions 32, 34. In addition, the enriched region 12 is substantially decoupled from the first gate electrode 29, since the coupling regions are limited in extension. The presence of the dielectric filling region 20 enables an increase of the final thickness of the gate dielectric (which hence extends not only on top of the epitaxial layer 3, but also within the latter) and

consequently enables reduction of the capacitance associated thereto. Said capacitance determines the rate of switching of the VDMOS transistor 100 in so far as to be able to turn on or turn off the VDMOS transistor 100 it is necessary to charge or discharge said capacitance. A capacitance of a reduced value enables higher switching speeds to be achieved.

In practice, then, the structure of the VDMOS transistor 100 according to the present invention enables abatement of the resistance of the parasitic JFET without sacrificing either the dimensions or the dynamic performance.

According to a further embodiment, shown in Figure 14, a VDMOS transistor 150 comprises a gate-dielectric structure 55 having a double thickness. Elements of the VDMOS transistor 150 that are similar to corresponding elements of the VDMOS transistor 100 of Figure 13 are designated by the same reference numbers and are not described any further herein.

In detail, the gate-dielectric structure 55 comprises a thin portion formed by the portion 22' of the gate dielectric layer 22, which extends between the first source region 38 and the second source region 39 that is closer to the enriched region 12, and a thick dielectric gate region 57, which is set substantially on top of the dielectric filling region 20. In general, the thick dielectric gate region 57 is set between the two body wells 32 and 34 without overlying them. The gate-dielectric structure 55 hence has a differentiated thickness: a first part, which is thinner with a thickness of between 10 nm and 150 nm, has the thickness of just the gate dielectric layer 22, whereas a second part, set between the first body region 32 and the second body region 34, in particular on top of the dielectric filling region 20, comprises also the thick dielectric gate region 57 and has a greater thickness, between 20 nm and 2 μ m. Also the first gate electrode 29 has a differentiated thickness, in a way

complementary to the gate-dielectric structure 55: the first gate electrode 29 has, in fact, a greater thickness where the gate-dielectric structure 55 is thinner and, vice versa, a smaller thickness where the gate-dielectric structure 55 is thicker.

Figure 15 shows, by way of example, a power MOSFET device, designated by 180, provided according to the present invention.

The power MOSFET device 180, of a planar type, has a structure made up of periodic strips (of the type shown in Figure 10b) given by the repetition of a plurality of elementary transistors (i.e., a plurality of VDMOS transistors 100 formed alongside one another on one and the same wafer 1), each of which is provided according to the teaching of the present invention. The power MOSFET device 180 is provided in the wafer 1, including the substrate 2 and the epitaxial layer 3. The power MOSFET device 180 hence comprises: a plurality of body regions (or wells) 182 (similar to the body wells 32, 34 described previously), with a doping of a P type and set at the top surface 3a of the epitaxial layer 3; source regions 184 (similar to the source regions 38, 39 described previously), with a doping of an N type, set within the body region 182; and an insulated-gate structure 186 (similar to the gate structure 29 described previously), in turn formed by the superposition of a silicon-oxide region and of a conductive region, for instance made of polysilicon, set at least partially on top of a source region 184 and extending between two adjacent body regions 182 of the power MOSFET device 180.

According to the present invention, between adjacent body regions 182, an enriched region 187 is present (similar to the enriched region 12 described previously), of an N⁺ type, extending in the epitaxial layer 3, facing the top surface 3a.

The enriched region 187 surrounds completely a dielectric filling region 189 (similar to the dielectric filling region 20), extending in the epitaxial layer 3, facing the top surface 3a. The gate structure 186 extends over the enriched
5 region 187 and over the dielectric filling region 189. A passivation layer 190 and a metallization layer 191 are set, in a way in itself known, on top of the top surface 3a of the epitaxial layer 3 and of the insulated-gate structures 186.

10 Figure 16 is a schematic illustration a user system 300 that comprises a user apparatus 301 and a control device 302 coupled thereto for supplying control signals S_c . The control device 302 comprises a circuit equipped with one or more examples of the VDMOS transistor 100 of Figure 13 (or,
15 alternatively, of the VDMOS transistor 150 of Figure 14). The user system 300 and the user apparatus 301 can be, for instance, a DC-DC converter system with a resistive or inductive load or a motor control system with an inductive load.

20 The advantages of the electronic device and of the corresponding manufacturing process according to the present invention emerge clearly from the above description.

25 In particular, the present invention enables significant abatement of the contribution of the parasitic JFET inherent in vertical-conduction MISFET structures without increasing the capacitance associated to the gate structure, and consequently improvement of the compromise between on-
30 resistance (the so-called " R_{on} ") and gate charge of the electronic device.

The structure with dielectric gate having a double thickness (Figure 14) presents the advantage of enabling a further
35 reduction in the output capacitance of the electronic device, to the advantage of the speed of response in use, thus

improving the levels of dynamic performance of the device.

Finally, it is evident that modifications and variations may be made to the process and to the device described, without
5 thereby departing from the scope of the present invention, as defined in the annexed claims.

In particular, it is possible to provide a P-channel electronic device.

10

Moreover, the dielectric that forms the dielectric region 20 can be of any type; in particular, it can be a dielectric different from the one used to form the dielectric gate 22'.

15 Moreover the process can be used to obtain MISFET devices different from VDMOS transistors. In one embodiment, for example, there may be provided IGBTs, multi-drain devices, or superjunction devices. The structure comprising the enriched region and the dielectric region internal to the enriched
20 region is present between all the body wells of said devices.

CLAIMS

1. A process for manufacturing a vertical-conduction electronic device (100; 150), comprising the steps of:

- 5 - providing a semiconductor wafer (1) including a semiconductor layer (2, 3) having a first type of conductivity (N) and a first doping level, the semiconductor layer (2, 3) having a first side (3a) and a second side (2b; 3b) opposite to one another;
- 10 - forming, in the semiconductor layer (2, 3), at least a first body region (32) and a second body region (34), having a second type of conductivity (P), characterized in that it further comprises the steps of:
- forming, in the semiconductor layer (2, 3) between the first
- 15 body region (32) and the second body region (34), a trench (8) defined by side walls (8') and a bottom (8");
- forming, in the trench (8) at the side walls and the bottom, an enriched region (12) having the first type of conductivity and a second doping level, higher than the first doping level;
- 20 - forming, in the trench (8), within the enriched region (12), a dielectric filling region (20); and
- forming a gate structure (29) above the enriched region (12), the dielectric filling region (20), part of the first body region (32), and part of the second body region (34).

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2. The process according to claim 1, wherein the step of forming the trench (8) comprises etching the semiconductor layer (2, 3) at the first side (3a) up to a depth comprised between approximately 0.1 μm and approximately 1.5 μm .

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3. The process according to claim 1 or claim 2, further comprising, prior to etching the semiconductor layer (2, 3), the steps of:

- 35 - forming, on top of the first side (3a) of the semiconductor layer (2, 3), a protective layer (7); and
- removing the protective layer (7) in a region of the

semiconductor layer (2, 3) in which it is desired to form the trench (8),

said process further comprising, after the step of forming the dielectric filling region (20), the step of removing from the semiconductor layer (2, 3) residue of dielectric material exceeding the trench (8) through a CMP technique or a plasma etching, until the protective layer (7) is reached.

4. The process according to any one of the preceding claims, wherein forming the gate structure (29) comprises:

- depositing a gate dielectric (22) on top of the first side (3a) of the semiconductor layer (2, 3);
- depositing a gate-electrode layer (24) on top of the gate dielectric (22);

- patterning the gate dielectric (22) and the gate-electrode layer (24) so as to form the gate structure (29) on the enriched region (12), on part of the first body region (32), and on part of the second body region (34).

5. The process according to any one of the preceding claims, further comprising:

- forming a first source region (38), having the first type of conductivity, in the first body region (32) and facing the first side (3a) of the semiconductor layer (2, 3); and

- forming a second source region (39), having the first type of conductivity, in the second body region (34), and facing the first side (3a) of the semiconductor layer (2, 3), the first and second source regions being formed at opposite sides of the enriched region (12).

6. The process according to any one of the preceding claims, wherein the step of forming the enriched region (12) comprises partially filling the trench (8) via an epitaxial growth of semiconductor material having the first type of conductivity and the second doping level, in such a way as to coat the side walls (8') and the bottom (8'') of the trench (8).

7. The process according to claim 6, wherein the step of forming the enriched region (12) further comprises modulating said epitaxial growth by means of a simultaneous chemical etching of the epitaxially grown semiconductor material so as to obtain a compact partial filling without voids of said trench (8).

8. The process according to claim 6 or claim 7, wherein the enriched region (12) has a thickness, measured starting from the side walls (8') and the bottom (8'') of the trench (8), comprised between approximately 0.3 μm and approximately 1.0 μm .

9. The process according to any one of claims 1-5, wherein the step of forming the enriched region (12) comprises implanting dopant species having the first type of conductivity at the side walls (8') and the bottom (8'') of the trench (8) in such a way as to provide an implanted region having the second doping level.

10. The process according to claim 9, wherein said implanted region extends in the semiconductor layer (3) for a thickness, measured starting from the side walls (8') and the bottom (8'') of the trench (8), comprised between approximately 0.3 μm and approximately 1.0 μm .

11. A vertical-conduction electronic device (100; 150), comprising:

- a semiconductor wafer (1) including a semiconductor layer (2, 3) having a first side (3a) and a second side (2b; 3b) opposite to one another, the semiconductor layer having a first type of conductivity (N) and a first doping level;
- a first body region (32) and a second body region (34), having a second type of conductivity (P) and extending in the semiconductor layer (2, 3); and

- an enriched region (12), having the first type of conductivity and a second doping level higher than the first doping level, which extends in the semiconductor layer (2, 3) facing the first side (3a), between the first and second body regions (32, 34),

characterized in that it further comprises:

- a dielectric filling region (20), extending in the semiconductor layer (2, 3), facing the first side (3a) and being completely surrounded by the enriched region (12); and

- a gate structure (29) extending on the first side (3a) above the enriched region (12), the dielectric filling region (20), part of the first body region (32), and part of the second body region (34).

12. The electronic device according to claim 11, wherein the enriched region (12) extends in the semiconductor layer (2, 3) for a depth comprised between approximately 0.1 μm and approximately 1.5 μm .

13. The electronic device according to claim 11 or claim 12, wherein the gate structure (29) comprises:

- a gate dielectric (22') extending on the first side (3a) of the semiconductor layer (2, 3), on the enriched region (12), on part of the first body region (32), and on part of the second body region (34); and

- a gate-electrode layer (24') extending on the first side (3a) of the semiconductor layer (2, 3), on the enriched region (12), on part of the first body region (32), and on part of the second body region (34).

14. The electronic device according to claim 13, wherein the dielectric filling region (20) is in direct contact with the gate dielectric (22') and an extension of said gate dielectric is provided in the semiconductor layer (2, 3).

15. The electronic device according to any one of claims 11-

14, wherein the gate dielectric (22') comprises a thick dielectric gate region (57), having a thickness greater than the thickness of the gate dielectric (22'), in the dielectric filling region (20), and wherein the gate-electrode layer (24') has a thickness, on the thick dielectric gate region (57), greater than its thickness outside the thick dielectric gate region (57).

16. The electronic device according to any one of claims 11-15, further comprising:

- a first source region (38), having the first type of conductivity, which extends in the first body region (32) and faces the first side (3a) of the semiconductor layer (2, 3); and

- a second source region (39), having the first type of conductivity, which extends in the second body region (34) and faces the first side (3a) of the semiconductor layer (2, 3), the first and second source regions extending at opposite sides of the enriched region (12).

17. The electronic device according to claim 16, comprising a metal source contact (50), extending above the gate electrode (24') and wherein the gate electrode (24') is electrically insulated from the metal source layer (50) by an insulating layer (46), the metal source contact (50) being in electrical contact with the first and second source regions (38, 39).

18. The electronic device according to any one of claims 11-17, wherein the enriched region (12) comprises a region of semiconductor material grown epitaxially, which is compact and without voids.

19. The electronic device according to any one of claims 11-17, wherein the enriched region (12) defines a curvilinear path between a first surface portion of the first side (3a) and a second surface portion of the first side (3a) through

the semiconductor layer (2, 3), said curvilinear path having, when considered along a lateral cross section of said electronic device, a thickness comprised between approximately 0.3 μm and approximately 1.0 μm .

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20. The electronic device according to any one of claims 11-17, wherein the enriched region (12) is an implanted region having the second doping level.

10 21. The electronic device according to claim 20, wherein said implanted region defines a curvilinear path between a first surface portion of the first side (3a) and a second surface portion of the first side (3a) through the semiconductor layer (2, 3), said curvilinear path having, when considered along a
15 lateral cross section of said electronic device, a thickness comprised between approximately 0.3 μm and approximately 1.0 μm .

22. The electronic device according to any one of claims 11-
20 21, wherein the dielectric filling region (20) extends in the semiconductor layer (2, 3) for a depth comprised between 0.1 μm and 1.5 μm .

23. The electronic device according to any one of claims 11-
25 22, wherein the dielectric filling region (20) is made of silicon oxide or silicon nitride.

24. The electronic device according to any one of claims 11-
23, wherein said electronic device (100, 150) is a charge-
30 balance power device, chosen from: a MISFET, a MOSFET, an IGBT, and a bipolar transistor.

25. A user system (300) comprising a user apparatus (301) and
a control device (302) coupled to the user apparatus (301),
35 characterized in that the control device (302) comprises a vertical-conduction electronic device (100; 150) according to

any one of claims 11-24.

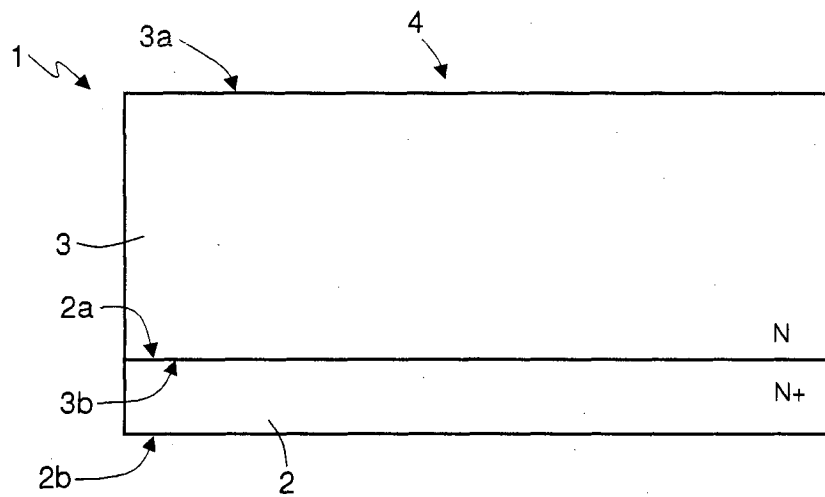


Fig.1

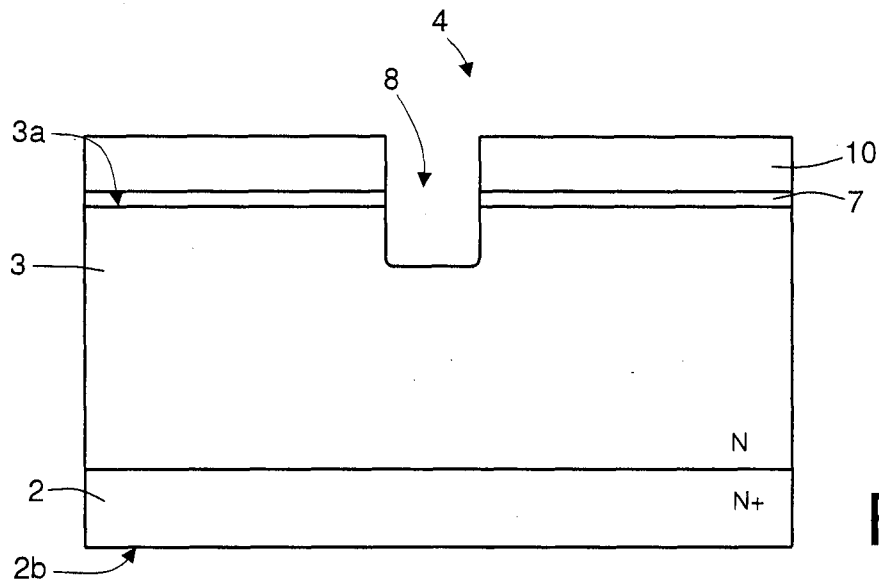


Fig.2a

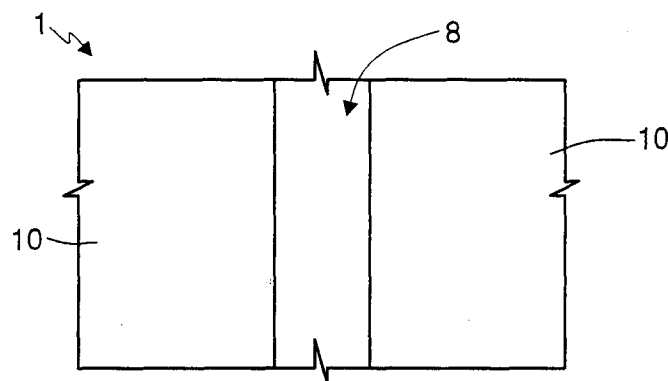


Fig.2b

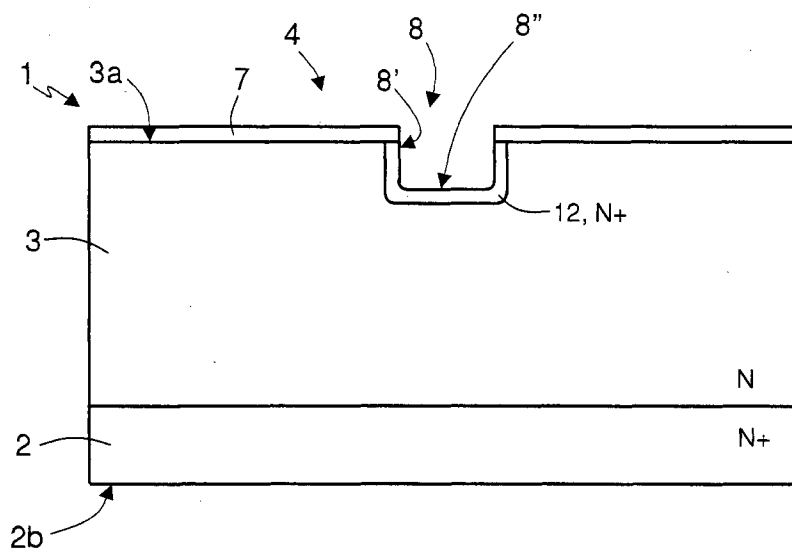


Fig.3

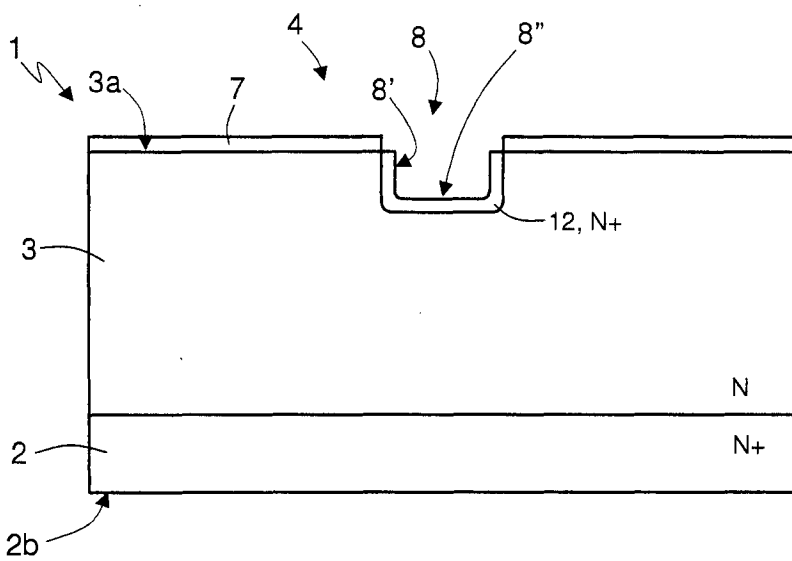


Fig.4

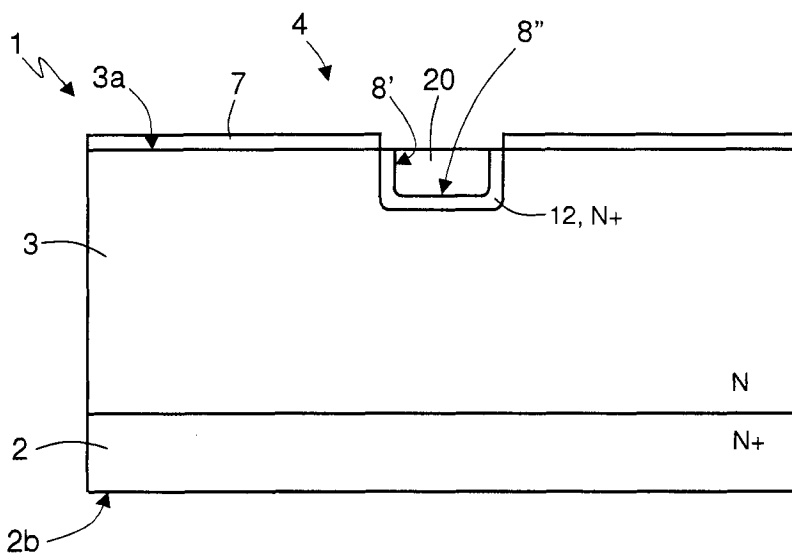


Fig.5a

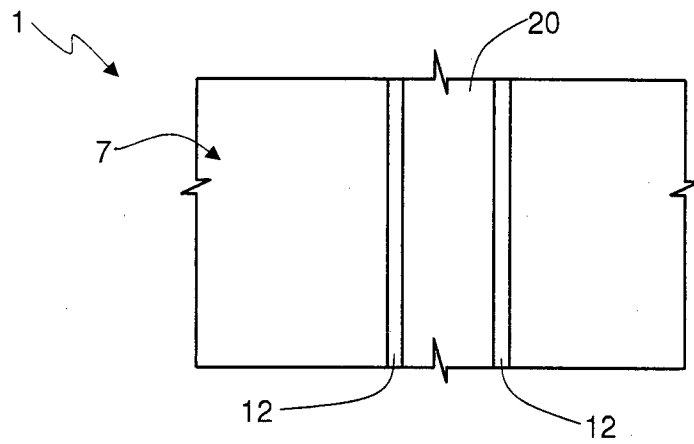


Fig. 5b

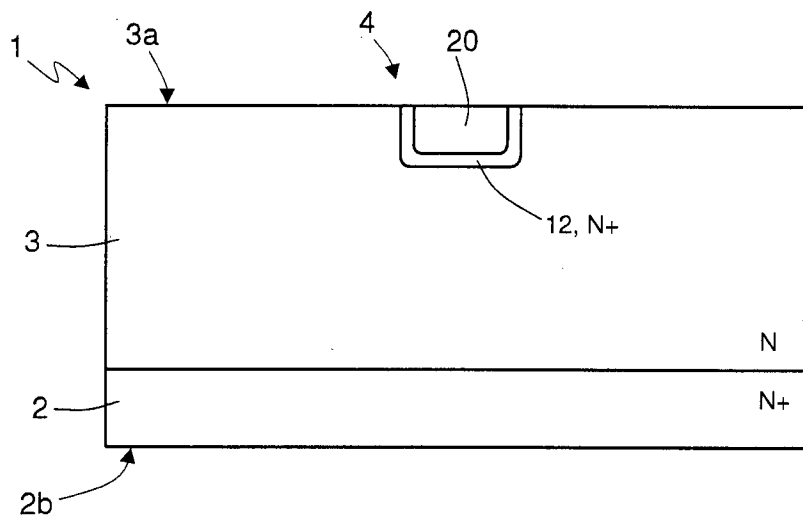


Fig. 6

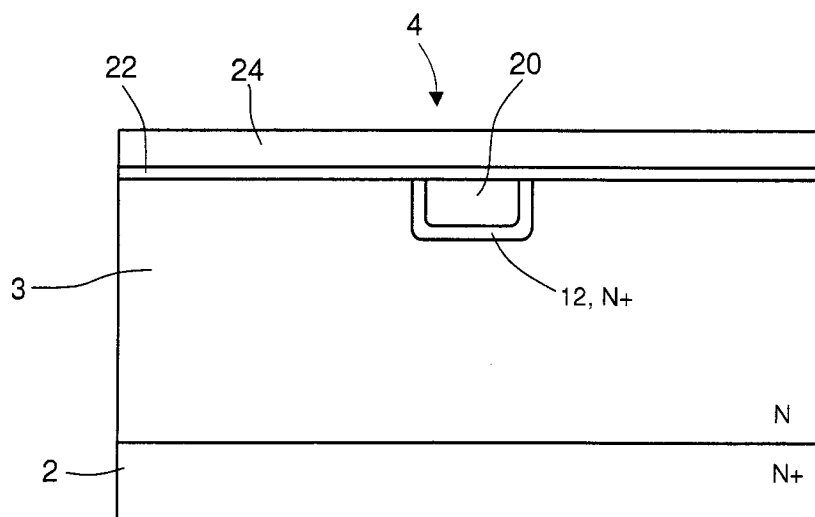


Fig. 7

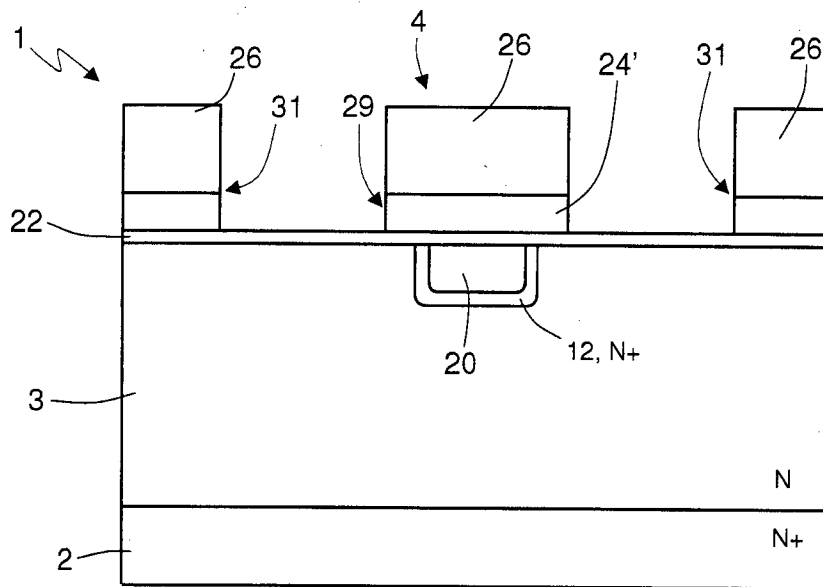


Fig.8

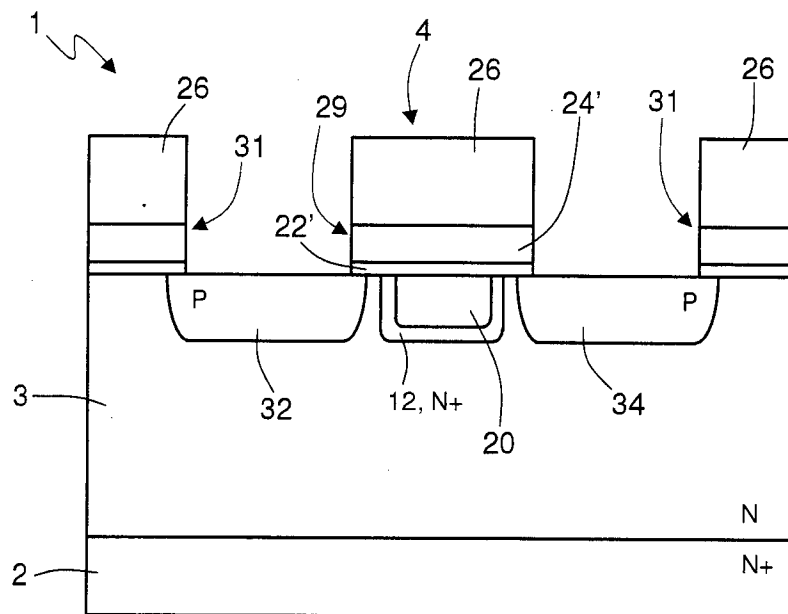


Fig.9

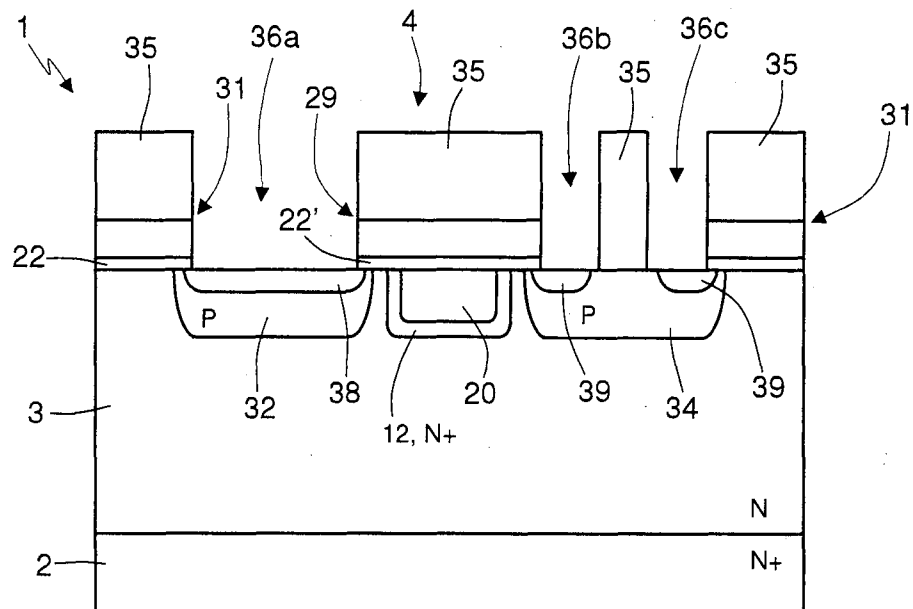


Fig.10a

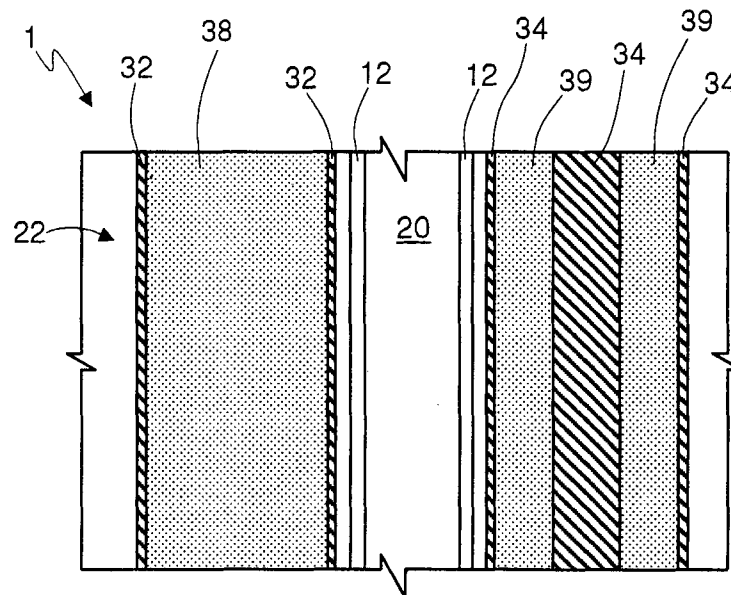


Fig.10b

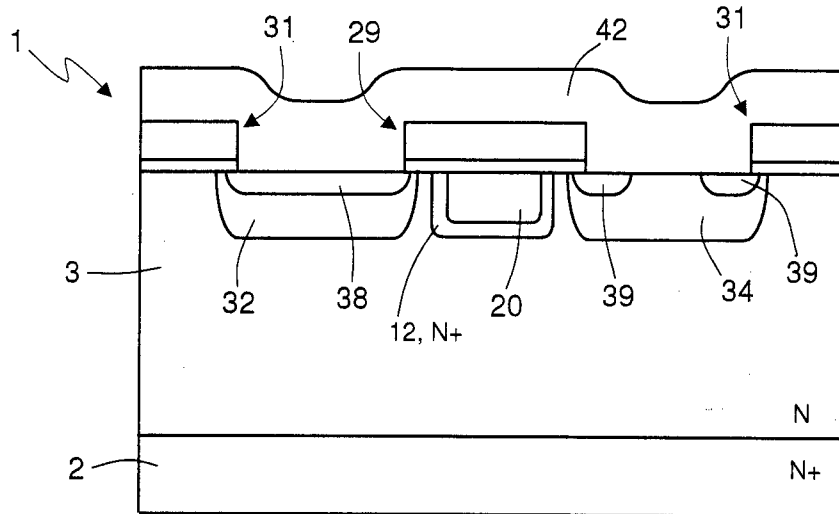


Fig.11

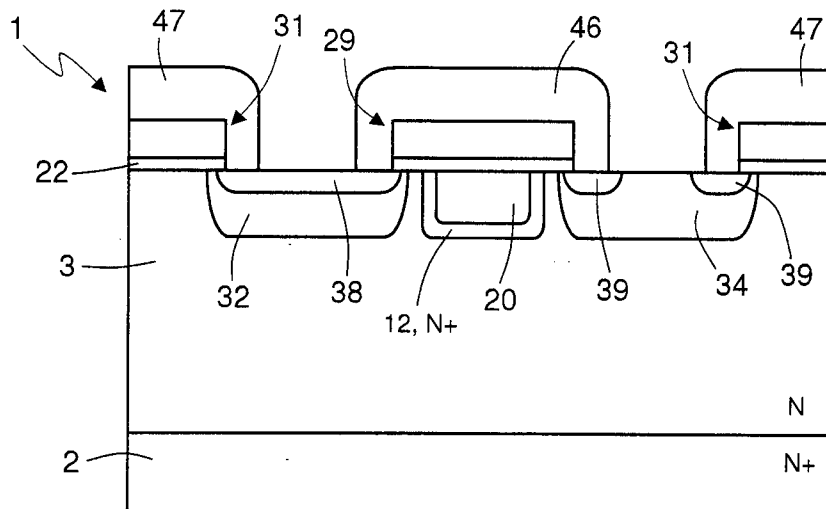


Fig.12

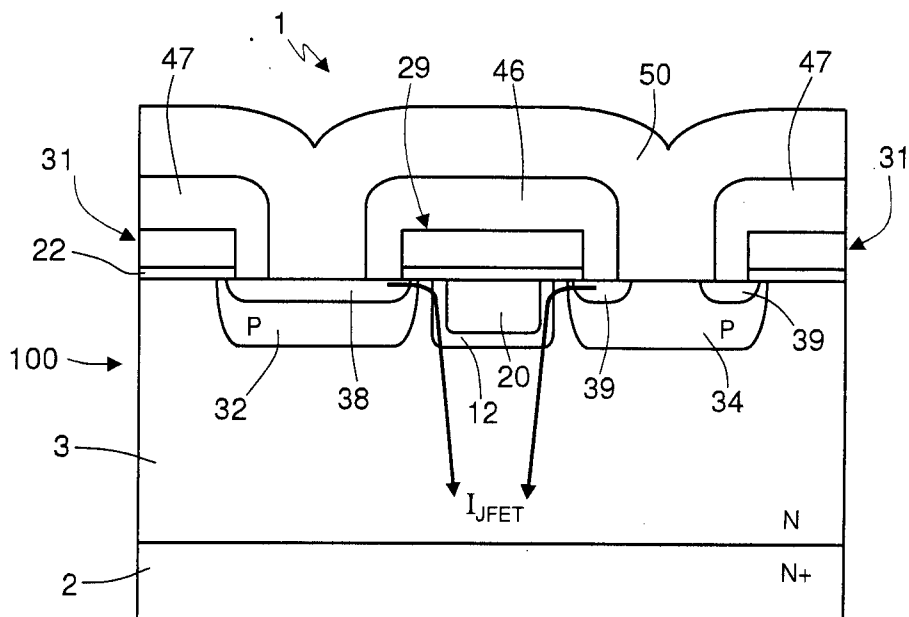


Fig.13

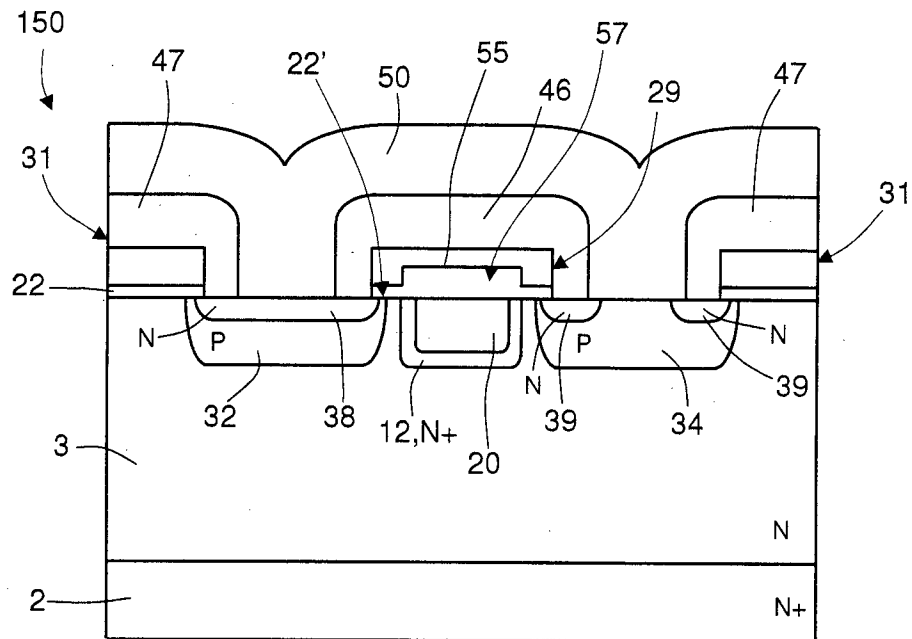


Fig.14

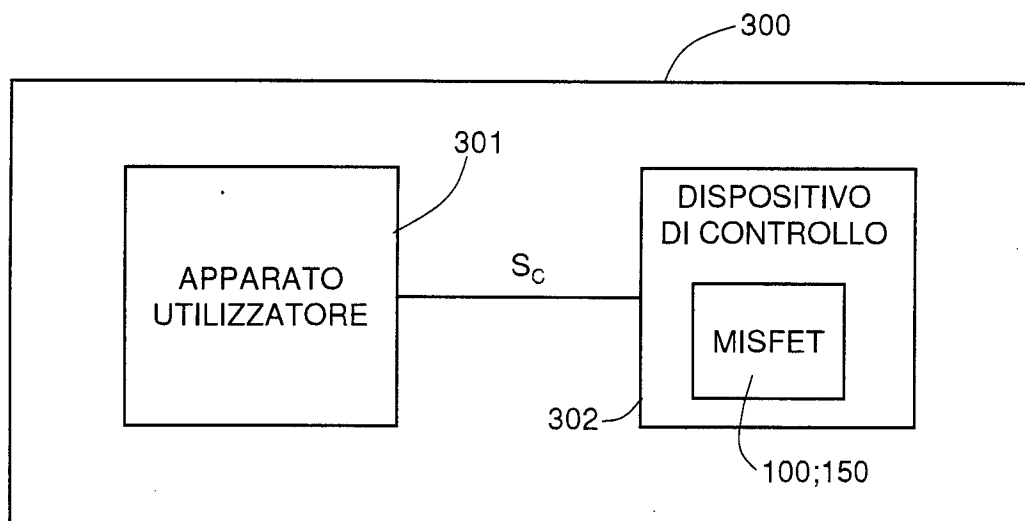


Fig.16

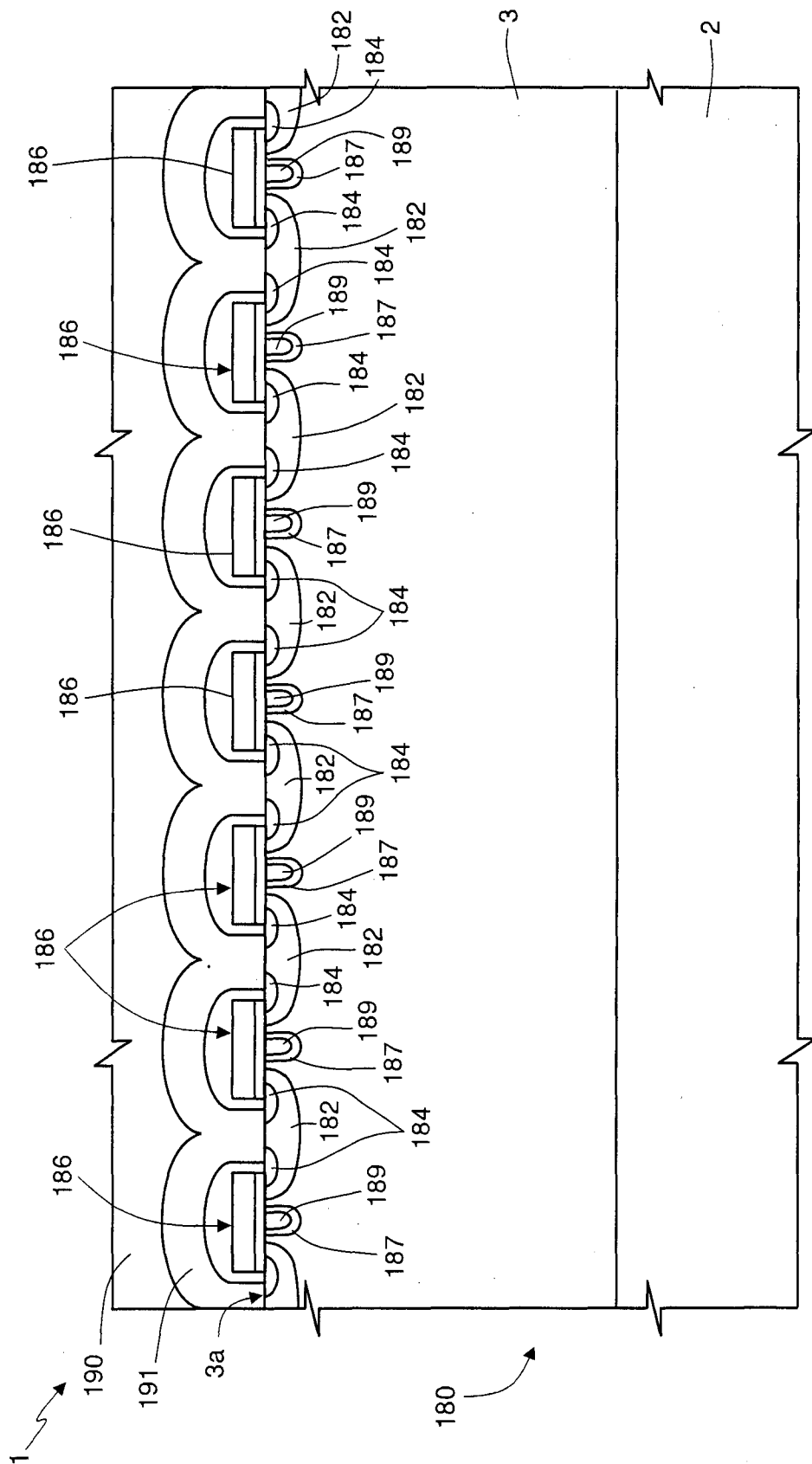


Fig.15

INTERNATIONAL SEARCH REPORT

International application No
PCT/IT2012/000060

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/78 H01L29/739 H01L29/08 H01L21/02 H01L21/336
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2004/075302 A1 (SEMICONDUCTOR COMPONENTS IND [US]; VENKATRAMAN PRASAD [US]) 2 September 2004 (2004-09-02)	1-5, 9-14, 16-24
Y	page 2, line 14 - page 5, line 31; figure 1	6-8,25
	page 8, line 3 - line 15; figure 3	

X	EP 0 119 400 A1 (NISSAN MOTOR [JP]) 26 September 1984 (1984-09-26)	1,2,4,5, 11-14, 16-18, 22-24
	page 4, line 1 - page 7, line 5; figures 2(A)-2(I)	

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Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

11 October 2012

Date of mailing of the international search report

26/10/2012

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INTERNATIONAL SEARCH REPORT

International application No

PCT/IT2012/000060

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/155286 A1 (SALIH ALI [US]) 12 August 2004 (2004-08-12) paragraph [0018]; figure 2 -----	1,4,5, 11,13, 14,16, 17,23,24
X	EP 1 455 397 A2 (ST MICROELECTRONICS SRL [IT]) 8 September 2004 (2004-09-08) paragraph [0022] - paragraph [0033]; figures 5,6c,7c -----	11-18, 20,23,24
Y	WO 2012/020290 A2 (ST MICROELECTRONICS SRL [IT]; SAGGIO MARIO GIUSEPPE [IT]; MURABITO DOM) 16 February 2012 (2012-02-16) page 7, line 35 - page 10, line 35; figure 3c -----	6-8
Y	US 2008/211021 A1 (BATTIATO ORAZIO [IT] ET AL) 4 September 2008 (2008-09-04) figures 13,18,23,24 -----	25

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IT2012/000060

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US 2008211021 A1	04-09-2008	US 2008211021 A1 US 2010167481 A1	04-09-2008 01-07-2010