United States Patent [19]

Schroder et al.

[11] **3,735,385**

[45] **May 22, 1973**

[54] **CIRCUIT ARRANGEMENT FOR CHARACTER DISPLAY**

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[22] Filed: **May 14, 1971**

[21] Appl. No.: **143,346**

[30] **Foreign Application Priority Data**

June 13, 1970 Germany.....P 20 29 247.1

[52] **U.S. Cl.** .....**340/324 AD**, 340/172.5

[51] **Int. Cl.**.....**G06f 3/14**

[58] **Field of Search** .....340/324 A, 324 AD

[56] **References Cited**

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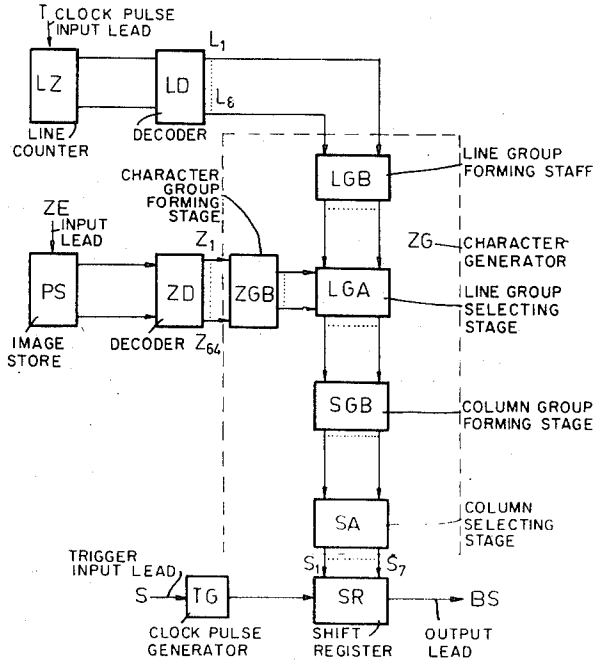
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[57] **ABSTRACT**

A device for forming image signals for a cathode-ray tube wherein signals are generated corresponding to line segments and column segments of characters to be displayed and wherein the line segment and the column segment signals are combined and stored in a shift register that contains the information corresponding to a plurality of characters whereby the character forming apparatus may operate asynchronously with the display apparatus.

5 Claims, 4 Drawing Figures



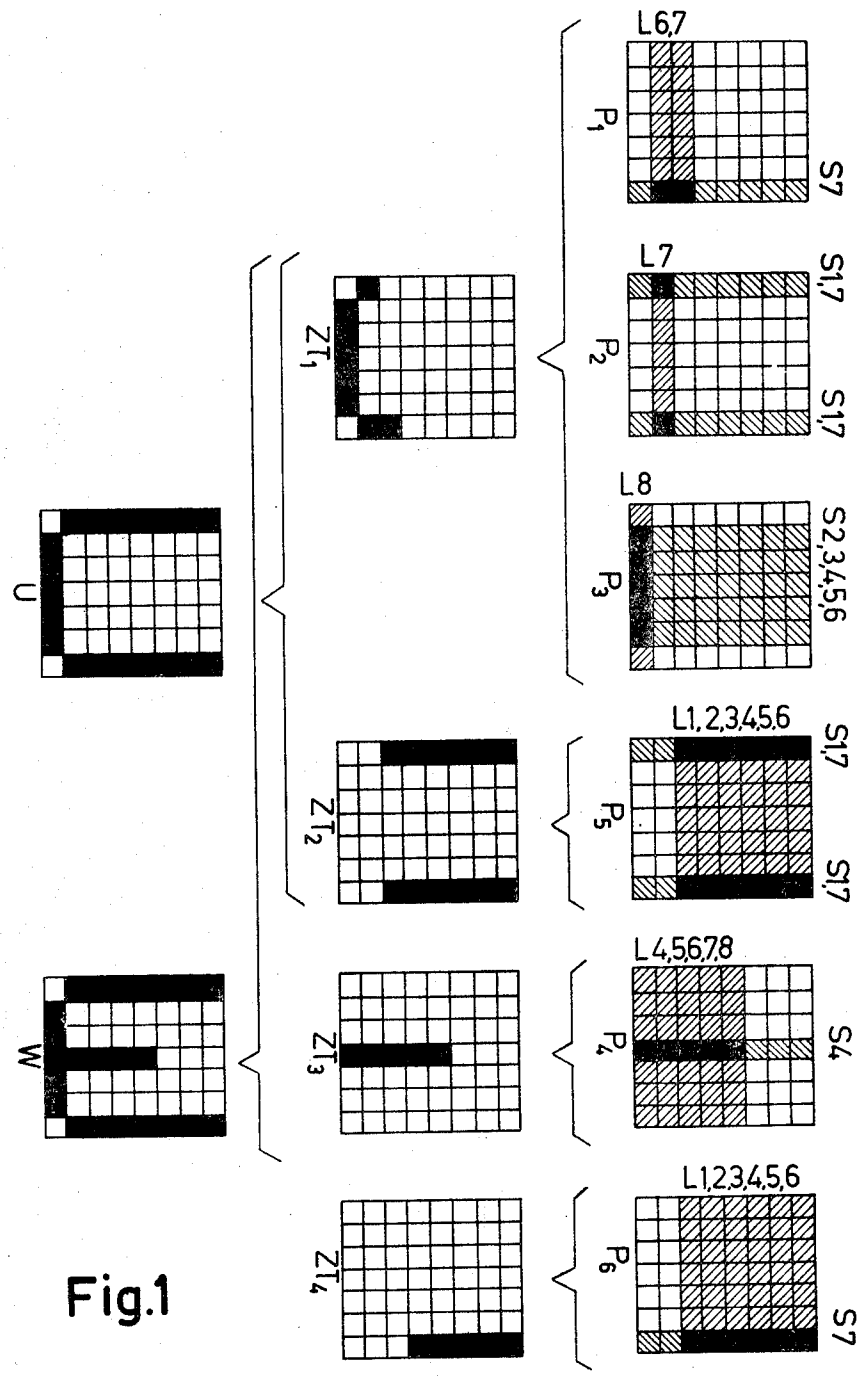


Fig.1

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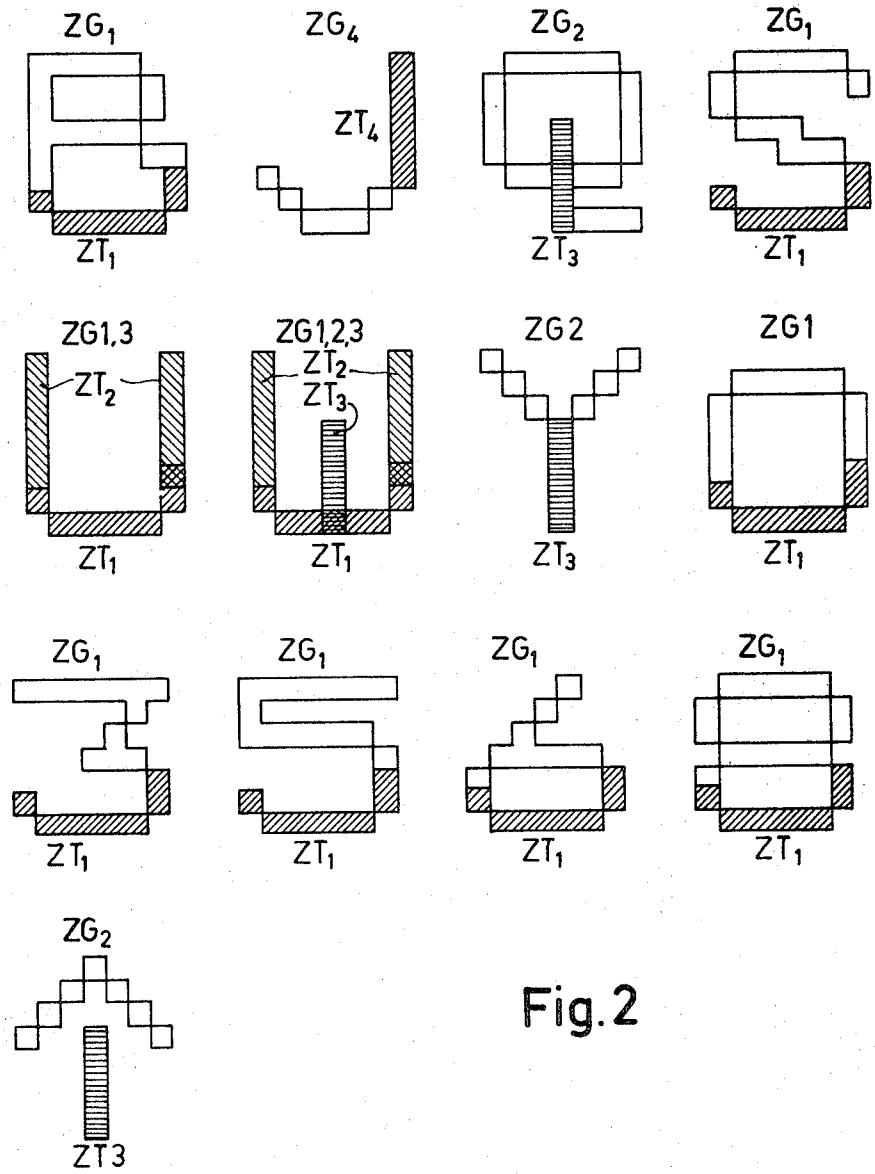


Fig. 2

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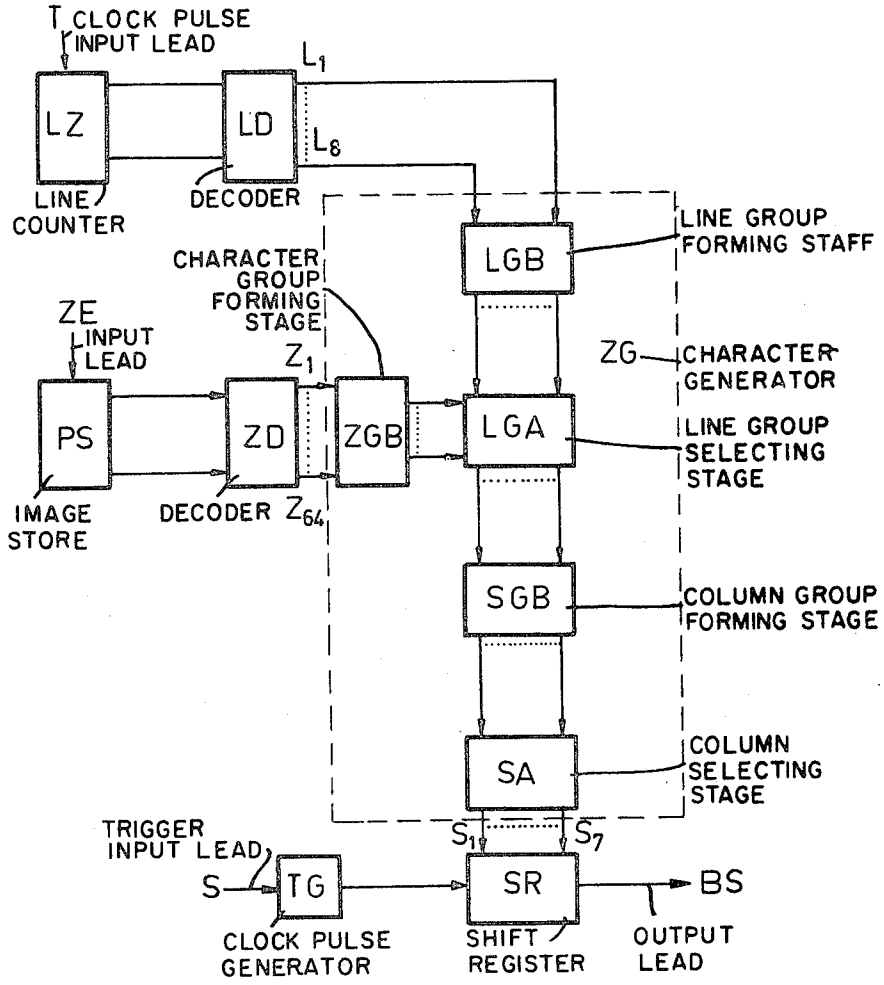


Fig. 3

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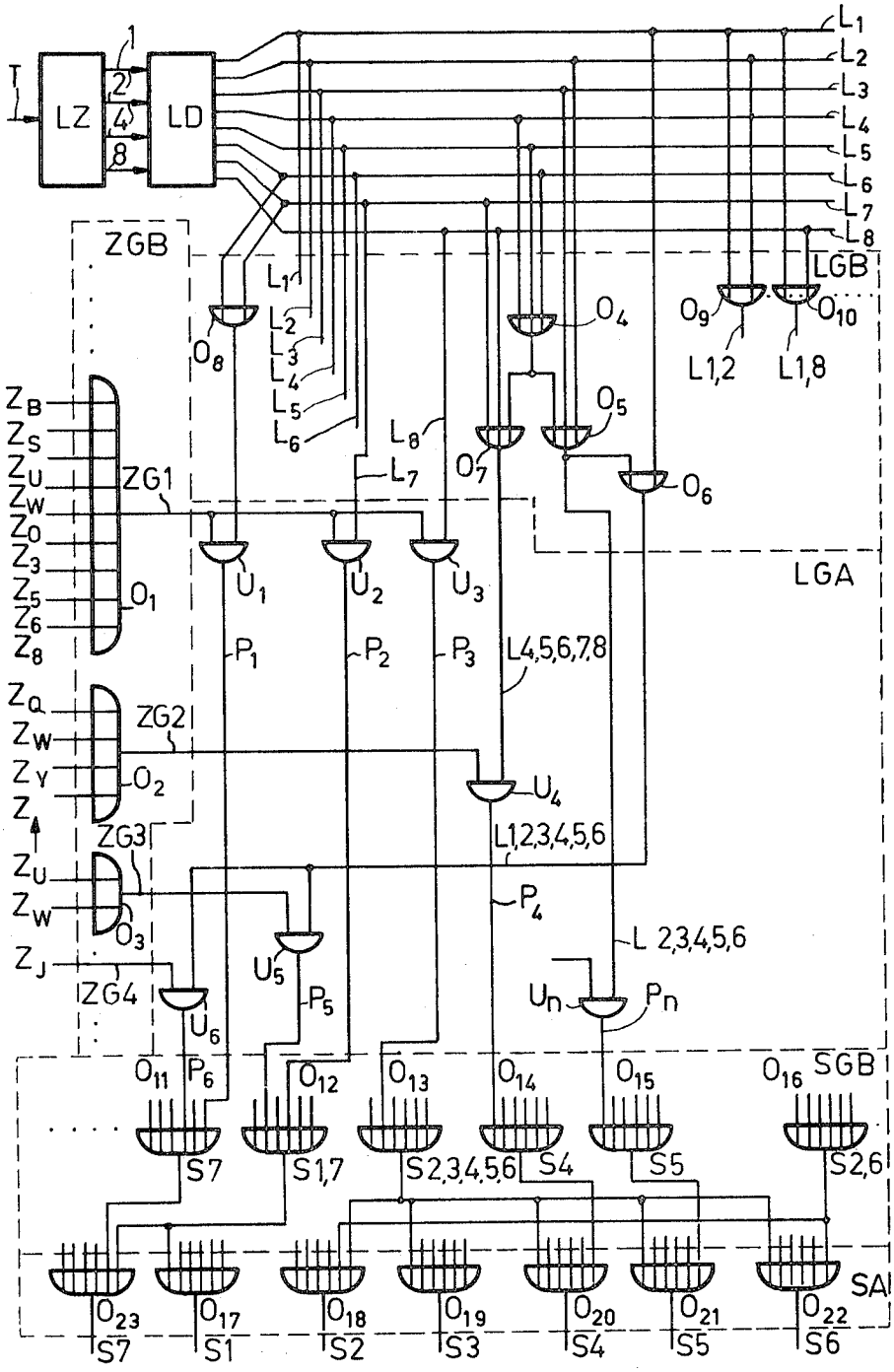


Fig. 4

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CIRCUIT ARRANGEMENT FOR CHARACTER DISPLAY

The invention relates to an arrangement for controlling the intensity of the electron beam of a cathode ray tube when displaying characters which consist of image dots arranged according to a matrix on the screen of the cathode-ray tube, which arrangement includes a line counter and a character generator.

In order to facilitate the exchange of data between electronic data processing machines and the personnel operating them, display apparatus are used which convert the machine data into a legible text. For this purpose, fixed content stores are used which convert a symbol offered in an arbitrary code into a pattern of dots and strokes which corresponds to legible types.

Such an arrangement is described, for example in the British Patent application No. 30155/70 corresponding to U.S. Pat. No. 3,696,387 in which the characters are built up from character parts with the use of a diode matrix. The said arrangement is unsuitable for construction as integrated-circuit and hence is comparatively expensive. The signals have to pass through a comparatively large number of gate circuits, and this number may be different for different characters. In particular if the characters succeed one another at a high speed (or if the column or line frequencies are high) transit-time differences may occur which are due to tolerances in the switching times of the circuit element and may become so large that they cannot be compensated for by a synchronizing stage, so that the shapes of the characters are adversely affected.

The invention avoids this disadvantage by the use of only a small number of series-connected electronic circuit elements, and an arrangement according to the invention is characterized in that the character generator comprises a line group forming stage, by which the signals from at least two of the outputs of a decoder connected to the outputs of the line counter may be combined at a time to form line group signals, a character group forming stage, by which the signals from a number of the character inputs may be combined to form character group signals, a line group selecting stage, in which the signal from each character group may always select one line group, a column group forming stage, in which the signals from line groups selected in the line group selecting stage may be combined to form the column group signals, and a column group selecting stage, which distributes the column group signals over the corresponding column outputs the signals at the column output being capable of controlling the intensity of the electron beam. Thus, for each matrix point at most four electronic circuit elements are connected in series. Building up the characters in three steps results in a reduction in the number of parallel-connected electronic circuit elements also.

In conjunction therewith, a preferred embodiment according to the invention is characterized in that the signals for controlling the electron beam during the display of all the matrix dots of a succeeding character which lie on a given line jointly appear at one output per column during the display of a preceding character, and in that on termination of the display of a line of a character a control signal always transfers the information appearing at the outputs of the character generator to one storage location of a store, and in that the intensity of the electron beam may successively be controlled by the information contents of the storage locations. Thus, the information appears at the outputs in parallel form. This enables comparatively slow gate circuits to be used for the character generator, because the overall delay time of the gage circuits may be equal to the duration of the display of an entire character, whereas hitherto it could be equal only to a dot of a character. In particular, comparatively cheap permanent stores manufactured by means of MOST techniques may be used.

A preferred embodiment of an arrangement according to the invention is characterized in that the store is a shift register and in that during the display of that part of the character which is stored in this shift register the information contained in it is shifted to the output of the shift register in synchronism with the electron beam, the information appearing at this output controlling the intensity of the electron beam. This shift register may be manufactured in another technique than is the permanent store, permitting a high clock pulse frequency and hence a high character display frequency to be used.

A preferred embodiment of an arrangement according to the invention is further characterized in that the character group forming stage and the line group forming stage consist of or-gates, the line group selecting stage consists of and-gates, and the column group forming stage and the column group selecting stage consist of or-gates. This embodiment is highly suitable to be constructed in integrated-circuit form.

Still another preferred embodiment of an arrangement according to the invention is characterized in that the matrix consists of image dots arranged according to vertical lines and horizontal columns. This is equivalent to replacing the word "column" by the word "row" and vice versa.

An embodiment of the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

FIG. 1 shows the construction of characters from character parts and column and line groups by means of a dot matrix,

FIG. 2 shows character parts which occur in different characters,

FIG. 3 is a block schematic diagram of an embodiment according to the invention, and

FIG. 4 shows details of the arrangement shown in FIG. 3 illustrating, by way of example, the generation of the characters U and W.

FIG. 1 shows how the characters U and W may be built up in a matrix comprising 8 rows and 7 columns. The U is built up from character parts ZT1 and ZT2, and the W from character parts ZT1, ZT2 and ZT3. The character parts may in turn be built up from dot groups. For example, the character part ZT1 is built up from dot groups P1, P2 and P3, the character part ZT2 from the dot group P5, and the character part ZT3 from the dot group P4. The dot groups are built up from combinations of column groups and row groups. For example, the dot group P2 is built up as a combination of a row group L7, which comprises the seventh row, and of the column group S1,7 which comprises the first and seventh columns. The column group S1,7 is used inter alia to form the dot group P5.

FIG. 2 shows the character of a character assortment which may be built up inter alia from the character parts ZT1, ZT2, ZT3 and ZT4. These characters may

be subdivided into four character groups ZG1 to ZG4, according to their construction from various character parts:

ZG1: B, S, U, W, **0, 3, 5, 6, 8**;
ZG2: Q, W, Y, **0, 3, 5, 6, 8**;
ZG3: U, W, O, **3, 5, 6, 8**;
ZG4: J.

When building the known character shapes from matrix elements, with a view to the legibility of the characters shapes must be chosen in which the characters are made up from the smallest possible number of character parts, which each may be used for many characters, and these character parts in their turn must be made up from the smallest possible number of column and/or row groups, which may be used in common for many character parts.

FIG. 3 is a block circuit diagram of a character display arrangement according to the invention, which comprises an input lead ZE, an image store PS, a decoder ZD, a character group forming stage ZGB, a clock pulse input lead T, a line counter LZ, a decoder LD, a line group forming stage LGB, a character generator ZG, a line group selecting stage LGA, a column group forming stage SGB, a column selecting stage SA, shift register SR, an output lead BS, a clock pulse generator TG and a trigger input lead S.

Through the lead ZE the characters are supplied, for example in a six-bit code, to the image store PS. At the output of the store the information of the stored characters is decoded by a decoder ZD. In the embodiment shown by way of example, it is assumed that in there are **64** possible output signals (**Z1** to **Z64**) which, in the manner described with reference to FIG. **2**, are combined to form character groups in the character group forming stage ZGB associated with the character generator ZG. Under the control of the clock pulse T, the line counter LZ counts the matrix lines (horizontal rows of dots) to be displayed. The contents of this counter are decoded by the decoder LD and the output signals of this decoder are combined in the line group forming stage LGB to form the line groups. In accordance with the character decoded in the decoder ZD, the character group forming stage ZGB selects those groups in the line group selecting stage LGA which are required to display the character which at that instant forms the contents of the image store PS and has been decoded by the decoder ZD. In the column group forming stage SGB the output signals of the line group selecting stage LGA form the column groups required for display in the with the line to be displayed at this instant and with the character decoded by ZD. In the column selecting stage SA the output signals of the column group forming stage SGB will then select the columns which are to be displayed as matrix dots in accordance with the character interrogated by the output of the image store PS and with the contents of the line counter LZ. The signals which correspond to the seven matrix columns are stored in the shift register SR, which thereupon under the control of the clock pulse generator TG, which is adapted to be triggered, effects a parallel-to-series conversion of the set of pulses, so that a corresponding luminance signal may be taken from the lead BS.

FIG. **4** shows details of the circuit arrangement shown in FIG. **3** and includes, in addition to the aforementioned circuit elements, or-gates **01** to **023**, and gates **U1** to **U6** and Un, and input leads Z_B, Z_S, Z_U, . . . , Z_I. The circuit arrangement operates as follows:

We will assume that the character U is to be displayed. The code of this character is obtained at the output of the image store and, after decoding in the decoder ZD, transferred via a character input lead Z_U to the or-gates **01** and **03**. The input lead Z_U is one of the leads **Z1** to **Z64** of FIG. **3**. From the character group forming stage ZGB, which in the arrangement shown in FIG. **4** includes the or-gates **01** to **03**, the signal on the lead Z_U is transferred to the row group selecting stage LGA, with the result that in this stage the and-gates U_1, U_2, U_3 and U_5 are put into a state of readiness. Under the control of the clock pulse T the line counter LZ counts the rows to be displayed. The contents of the counter LZ are decoded in the decoder LD to form signals on the leads **L1** to **L8**. During the lines **1** to **6** the or-gate **012** is energized via the or-gates **04, 05** and **06** and via the and-gate **U5**, so that the or-gate **012** selects the columns **S1** and **S7** via the or-gates **017** and **023** and thus forms the character part **ZT2**. In a similar manner the control signals for the dot groups **P1, P2** and **P3** (of FIG. 1) are generated, with the result that via **011, 012** and **013** and via **017** and **023** the character part ZT1 is formed. In a similar manner the character "W" is displayed by adding the character part ZT3 during the lines **4** to **8** via **04, 07, U4, 014** and **020**. The input signals for the or-gates **01** to **03** correspond to the character groups described with reference to FIG. **2**. Through leads **S1** to **S7** the pulse pattern is applied to the shift register SR.

The circuit arrangement is highly suitable for construction by means of not-and gates, because starting from the decoders LD and ZD it alternately consists of and-gates and or-gates. The or-gates of the column group forming stage SGB may in this case be designed as wired-or.

What is claimed is:

1. An arrangement for controlling the intensity of the electron beam of a cathode ray tube when displaying characters which consist of image dots arranged according to a matrix on the screen of the cathode-ray tube, which arrangement includes a line counter and a character generator, characterized in that the character generator comprises a line group forming stage wherein the signals from at least two of the outputs of a decoder connected to the outputs of the line counter may be combined at a time to form line group signals, a character group forming stage, by which the signals from a number of the character inputs may be combined to form character group signals, a line group selecting stage, in which the signal from each character group may always select one line group, a column group forming stage, in which the signals from line groups selected in the line group selecting stage may be combined to form the column group signals, and a column group selecting stage, which distributes the column group signals over the corresponding column outputs the signals at the column output being capable of controlling the intensity of the electron beam.

2. An arrangement as claimed in claim **1**, the column group selecting stage further comprising means for providing signals for controlling the electron beam during the display of all the matrix dots of a succeeding character which lie on a given line jointly at one output per column during the display of a preceding character, and responsive to the termination of the display of a

line of a character a control signal for transferring the information appearing at the outputs of the character generator to one storage location of a store, the intensity of the electron beam being successively controlled by the information contents of the storage locations.

3. An arrangement as claimed in claim 2, wherein the store is a shift register and in that means are provided during the display of that part of the character which is stored in this shift register for shifting the information therein contained to the output of the shift register in synchronism with the electron beam, the information appearing at this output controlling the intensity of the electron beam.

4. An arrangement as claimed in claim 1, wherein the character group forming stage and the line group forming stage consist of or-gates, the line group selecting stage consists of and-gates, and the column group forming stage and the column group selecting stage consist of or-gates.

5. An arrangement as claimed in claim 1, wherein the said matrix consists of image dots arranged according to vertical lines and horizontal columns.

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