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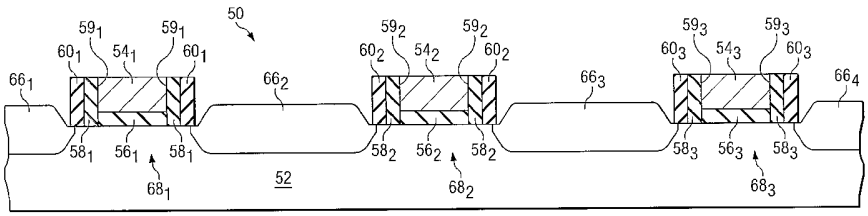
(54) **Title:** IMPROVED RECESSED DRAIN EXTENSIONS IN TRANSISTOR DEVICE



(57) **Abstract:** A method of forming an integrated circuit transistor (50) is provided. A gate structure (54_x) with sidewalls (59_x) is formed in fixed position relative to a first semiconductor region (52) of a substrate. At least a first layer (58_x, 60_x) is formed adjacent the sidewalls. At least one recess (62_x) is formed in the first semiconductor region and extending laterally outward from the gate structure. The material of the first semiconductor region is oxidized to form an oxidized material in the recess. At least a portion of the oxidized material is stripped from the recess and a second semiconductor region (66_x) is formed in the recess.

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IMPROVED RECESSED DRAIN EXTENSIONS IN TRANSISTOR DEVICE

The present embodiments relate to electronic circuit manufacture and are more particularly directed to improving recessed drain extensions in a transistor device.

BACKGROUND

Semiconductor devices are prevalent in all aspects of electronic circuits, and an element often used in such circuits is the transistor. Thus, effort is made to improve transistor design. One approach currently being implemented involves creating so-called "silicon strain" in the transistor channel through use of recessed silicon-germanium (SiGe) drain extensions. Generally, various steps occur in this context. First, a transistor gate stack is formed in a fixed relationship relative to a semiconductor substrate. Next, a portion or all of the gate sidewall is built. When only a portion of the sidewall is built, that portion is sometimes referred to as a "spacer" and typically includes one or more layers formed on the vertical side surfaces of the transistor gate. Next, an etch is performed into the silicon substrate, thereby forming a "recess" laterally extending outward from both sides of the transistor gate and its sidewall or sidewall spacer. The recess is thereafter filled with an epitaxial deposition of SiGe, with the resulting SiGe regions being the "drain extensions." Due to differences in the structures of the SiGe and the silicon (Si) substrate beneath it, a lattice mismatch is created between these two different semiconductor materials -- the SiGe lattice being larger than that of the underlying silicon. The lattice mismatch forms a "strain" in the transistor channel located beneath the transistor gate stack. This strain has been found to enhance mobility in the transistor channel, thereby improving device performance.

While the preceding approach to recessed SiGe drain extensions has improved upon other transistor technologies, there are certain drawbacks associated with this approach. Specifically, in order to perform the epitaxial deposition of SiGe in the device recesses as discussed above, a high-quality surface at the location of the recess is desirable. However, it has been observed that the imperfections of, and at, the silicon surface of the recess may compromise the quality of the epitaxial SiGe deposition.

Indeed, the prior art has implemented certain approaches in attempting to reduce this effect -- a particular approach depending on the extent to which the sidewall spacer is completed at the time the approach is taken. Specifically, in one approach taken when only two layers of

the sidewall spacer are in place (sometimes referred to as an "offset spacer," meaning that the entirety of all layers forming the spacing sidewall are not yet completed), the recess is formed and then a hydrofluoric (HF) acid wash is used at that point to remove impurities in the recess, followed by the epitaxial SiGe deposition. Note that the HF wash does not affect the sidewall spacer layers to a large extent at that point because typically the second sidewall spacer layer is nitride, which is resistant to the HF and, thus, protects the underlying layer between it and the transistor gate. Alternatively, in another approach taken when the entire spacing sidewall is complete by adding more layers to it, the recess is formed and a remote plasma with a fluorine-based chemistry is used. While this latter approach is workable when the spacing sidewall is complete, it is not preferable when cleaning the drain recesses at offset spacer layers due to the then-exposed nitride spacer layer, which cannot properly resist the fluorine plasma chemistry.

Thus, in view of the above, there arises a need to address the drawbacks of the prior art, as is achieved by the preferred embodiments described below.

SUMMARY

Example embodiments of a method of forming an integrated circuit transistor are described. In one aspect, the method forms a gate structure in a fixed position relative to a first semiconductor region. The gate structure has a first sidewall and a second sidewall. At least a first layer is formed adjacent the first sidewall and the second sidewall. At least one recess is formed in the first semiconductor region, with the recess extending laterally outward from the gate structure. The recess is oxidized to form an oxidized material therein, and a second semiconductor region is formed in the at least one recess after at least a portion of the oxidized material is stripped.

Other aspects are also disclosed and claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1a and 1b (Prior Art) are cross-sectional view at different processing steps of a prior art integrated circuit semiconductor device.

FIGS. 2a – 2c are cross-sectional views at different processing steps of an integrated circuit semiconductor device according to example preferred embodiments of the invention.

FIG. 3 is a flow chart of a method of forming a device as illustrated in FIGS. 2a - 2c.

DETAILED DESCRIPTION OF THE EMBODIMENTS

FIGS. 1a – 1b illustrate a prior art integrated circuit semiconductor device 10 in connection with which recessed drain extensions are formed according to the prior art. As shown in FIG. 1a, device 10 is formed in connection with a silicon semiconductor substrate 12. Overlying substrate 12 are three gate conductors 14_1, 14_2, and 14_3, where typically each gate conductor 14_x is formed at a same time and with a material such as polysilicon. Each gate conductor 14_x is separated from substrate 12 by a respective gate insulator 16_1, 16_2, and 16_3, and the combination of conductor and respective gate insulator is sometimes referred to as a "gate stack." Along each sidewall 19_x of each gate conductor 14_x is formed a first sidewall layer 18_x, typically formed of an oxide, where often that oxide is grown on the sidewall 19_x of the corresponding polysilicon gate structure. For example, with respect to gate 14_1, it has a first sidewall layer 18_1 formed adjacent its two sidewalls 19_1. Additionally, a second sidewall spacer 20_x, typically formed as a nitride, is formed along each first sidewall layer 18_x. For example, with respect to gate 14_1, it has a second sidewall spacer layer 20_1 formed along each of the two first sidewall layers 18_1. Typically the nitride is formed by depositing a nitride layer over device 10 and etching the nitride layer to form the resulting layers 20_x shown in FIG. 1a. Note that the sidewall spacers 18_x and 20_x are sometimes referred to in the art as "offset spacers," and they combine with additional later-formed spacers (not shown) to form in their entirety what is sometimes referred to generally as a "sidewall" or "spacing sidewall."

FIG. 1b illustrates the prior art device 10 of FIG. 1a after additional processing steps. First, recesses 22_1, 22_2, 22_3, and 22_4 are formed adjacent and extending laterally outward from each combination of gate conductor/sidewall spacers that was formed in connection with FIG. 1a. The recess is a removal of some of the silicon that forms substrate 12, and in device 10 is located between each pair of successive gate structures. According to the prior art, after all recesses 22_x are created, a cleaning step is performed to prepare the upper surface of substrate 12 in these recesses. The chemistry of this cleaning step is selected in view of the fact that nitride, in the form of sidewall spacer layer 20_x, is presently the outermost layer protecting the sidewalls 19_x of each gate conductor 14_x. Thus, according to the prior art, after all recesses 22_1 - 22_4 are created, a hydrofluoric (HF) acid wash is applied to device 10 and, thus, in each recess 22_x. Next, an epitaxial SiGe deposition is performed to grow SiGe regions 24_1 through 24_4 in the

respective areas of recesses 22_1 through 22_4. As shown in FIG. 1b, each SiGe region tends to bow upward at its center. The SiGe regions are sometimes referred to as "drain extensions" because they effectively extend the drain (or source) of each transistor beyond that of the conventional region (and/or dopants) located in the underlying substrate and laterally outward of the sidewalls 19_x of the corresponding transistor gate. With the formation of the SiGe regions, there is a lattice mismatch between the SiGe material and the adjacent silicon of substrate 12. This mismatch creates a "strain" in the transistor channel located underneath each gate 14_x and respective insulator 16_x. As already mentioned, the strain has been found to improve mobility and, therefore, transistor operation. Various additional processing steps (not shown) are thereafter typically taken with respect to device 10 so as to create additional device aspects, to interconnect devices, or for other purposes.

FIGS. 2a - 2c and 3 illustrate various processing steps in the fabrication of a semiconductor device 50 according to example preferred embodiments. FIGS. 2a - 2c and 3 are not intended to be exhaustive of all processing steps, but depict only some of the steps to focus on particular aspects of the example embodiments. As seen in example method 100 of FIG. 3, a step 110 is performed, to form gate structures and sidewall spacer layers in a fixed position relative to a device substrate (or a well or other region within a substrate). This may occur in the same manner as with the prior art device described in connection with FIG. 1a. FIG. 2a shows device 50 with a silicon semiconductor substrate 52. Overlying substrate 52 are three gate conductors 54_1, 54_2, and 54_3, preferably formed at a same time and with a material such as polysilicon. Each gate conductor 54_x is separated from substrate 52 by a respective gate insulator 56_1, 56_2, and 56_3. A first sidewall layer 58_x is formed, preferably of an oxide, along each sidewall 59_x of each gate conductor 54_x. That oxide may be grown on each adjacent sidewall 59_x of the corresponding polysilicon gate structure. Additionally, a second sidewall spacer 60_x is formed, preferably as a nitride, along each first sidewall layer 58_x. The nitride is preferably formed by depositing a nitride layer over device 50 and etching it to form the resulting layers 60_x shown in FIG. 2a. Continuing with FIG. 3, the flow of method 100 continues from step 110 to step 120, wherein recesses are formed in the semiconductor region in which the transistor source(s)/drain(s) are being formed. For the example of FIG. 2a, this region is substrate 52. Thus, FIG. 2a illustrates recesses 62_1, 62_2, 62_3, and 62_4 formed by removing some of the silicon

that forms substrate 52 in the areas adjacent each combination of gate conductor/sidewall spacer. Recesses 62_1 - 62_4 may be formed using any of numerous techniques as ascertainable by one skilled in the art, and this process may be performed in an asher. With each recess 62_x, a material may be formed therein in a subsequent step so as to be adjacent the transistor channel underlying each gate stack, as detailed later.

Continuing with FIGS. 2a and 3, after step 120, a step 130 is performed. Here, however, unlike the prior art which proceeds with an immediate clean, in a preferred embodiment step 130 recesses 62_1 - 62_4 are oxidized. This is preferably achieved by exposing device 50 to an oxidizing environment using an asher. The use of an asher is favorable because it is equipment that is common in semiconductor processing, so should be readily available for other processing steps in addition to step 130. Indeed, as mentioned above, such an asher may be used to perform step 120 to form recesses 62_1 - 62_4. In such case, device 50 may remain in the same asher equipment to thereafter perform step 130, without the need to move integrated circuit 50 between different equipments to accomplish these different steps. In any event, the oxidization of step 130 penetrates into the surface of recesses 62_1 - 62_4 to thereby remove any surface contaminants, while also consuming embedded contamination or silicon damage in substrate 52, some or all of which may occur as a result of the recess etch of step 120. The respective oxidized regions that result from step 130 are indicated by dashed lines shown below each of recesses 62_1 - 62_4 in FIG. 2a. In a preferred embodiment, the depth of the oxidized regions is on the order of 15 to 20 Angstroms, although that depth may differ in different implementations. Indeed, preferably during the development of a specific set of processing steps consistent with method 100, the desired depth of these oxidized regions may be determined empirically by experimenting with different depths and measuring the performance of the resulting device once it is completed with other steps, where such performance might be the quality of the interface between each recess and the subsequent Si-Ge formed therein and as further appreciated below.

FIG. 2b illustrates device 50 during a subsequent processing step, shown by step 140 in FIG. 3. In step 140, the oxidized regions (dashed line regions below recesses 62_1 - 62_4 in FIG. 2a) are stripped from device 50. In one preferred embodiment, this strip is performed with a dilute hydrofluoric (HF) acid solution. In another preferred embodiment, the strip may be performed with a so-called "standard clean 1 (SC-1) process," in which hydrogen peroxide and

ammonium hydroxide and water are used as cleaning agents. While not drawn to scale, for sake of illustrating the effect, FIG. 2b demonstrates that the strip will consume silicon and remove silicon oxide, thereby causing the silicon recess to become slightly deeper. In any event, once a strip directed to oxidized regions 64_1 - 64_4 has been performed, method 100 continues from step 140 to step 150.

Step 150 represents an option to repeat the oxidization and stripping steps 130 and 140, if wanted. Thus, step 150 is shown as a decision step to cause a loop back if, for example, more contaminant or damages are to be removed from the recesses 62_1 - 62_4. In actual implementation, this decision step may be established by a counter or the like, that counts down to cause a desired number of repetitions of steps 130 and 140. As shown in FIG. 3, if step 150 is answered in the affirmative ("Yes"), then the flow returns to repeat steps 130 and 140. A need for, or number of times of, repetition may be based on the anticipated depth of the contaminants and extent of damage caused by the recess-forming step 120. That is, if contaminants are perceived to be present below a certain depth within substrate 52, then one way to address this may be to perform steps 130 and 140 a first time to remediate a first portion of those contaminants and then to repeat steps 130 and 140, one or more times, to remove remaining portions of those contaminants. Of course, the cost of additional repetitions should be weighed against the sufficiency of addressing the contaminants and/or damage in substrate 52 with a minimum number of steps and any extra time that may be required to move the integrated circuit from an asher to a different piece of equipment. In any event, at some point no further repetition occurs and the process moves from step 150 to step 160. FIG. 2b shows device 50 with the oxidized regions removed.

FIG. 2c illustrates device 50 following a next step 160 in which SiGe regions 66_1 - 66_4 are formed in recesses 62_1 - 62_4, respectively. In the preferred embodiment, SiGe regions may be grown in the same manner as in the prior art, such as by an epitaxial SiGe deposition. Again, the completed regions will tend to bow upward in each respective center. However, due to the improved steps described above, an improved interface exists between each SiGe region 66_x and the silicon of substrate 52 that is in contact with that region. With this improved interface there is an improvement in the SiGe deposition leading to strain created in the channel area, shown as

channel areas 68_1, 68_2, and 68_3, below each respective gate insulator 56_1, 56_2, and 56_3 and its associated gate conductor 54_1, 54_2, and 54_3. Thus, device performance is improved.

Completing device 50 in FIG. 2c, after the SiGe drain extension regions are formed in step 160, method 100 continues to step 170. Step 170 generally indicates that other device processing steps are taken, and those steps may be readily selected by one skilled in the art. For example, additional layers may be formed adjacent the sidewall spacer layers 58_x and 60_x so as to form complete sidewalls, doping may be performed, and connectivity between devices may be achieved. Eventually, therefore, a working transistor is created for each gate conductor 54_x, and the performance of that device will be improved, as compared to the prior art, due to the inventive teachings set forth above.

From the above, it may be appreciated that the described example embodiments provide improved recessed drain extensions in a transistor device. Those skilled in the art to which the invention relates will appreciate that various alternatives, substitutions, modifications and/or additions can be made to the described embodiments, without departing from the scope of the invention.

CLAIMS

1. A method of forming an integrated circuit transistor, comprising:

providing a first semiconductor region;

forming a gate structure in a fixed position relative to the first semiconductor region, the gate structure having a first sidewall and a second sidewall;

forming at least a first layer adjacent the first sidewall and the second sidewall;

forming at least one recess in the first semiconductor region and extending laterally outward from the gate structure;

oxidizing the at least one recess such that an oxidized material is formed therein;

stripping at least a portion of the oxidized material; and

forming a second semiconductor region in the at least one recess after stripping.

2. The method of claim 1, wherein the first semiconductor region comprises silicon; and wherein the second semiconductor region comprises silicon germanium.

3. The method of claim 1 or 2, further comprising repeating the oxidizing and stripping steps at least once before forming the second semiconductor region.

4. The method of any of claims 1 - 3, wherein the step of forming the at least one recess and the oxidizing step are both performed while remaining in the same piece of equipment.

5. The method of any of claims 1 - 4, wherein the stripping step comprises stripping with a chemistry selected from a group consisting of hydrofluoric acid and a standard clean 1 (SC-1) process.

6. The method of any of claims 1 - 5, wherein the step of oxidizing forms oxidized material on the order of 15 to 20 Angstroms in depth.

7. The method of any of claims 1 - 6, wherein the step of forming at least a first layer adjacent the first sidewall and the second sidewall comprises forming a first layer adjacent the first sidewall and adjacent the second sidewall; and forming a second layer adjacent the first layer; the first layer comprising oxide and the second layer comprising nitride.

8. The method of any of claims 1 - 7:

wherein the gate structure comprises a first gate structure;

wherein the method forms a plurality of integrated circuit transistors;

wherein the step of forming a gate structure further forms a second gate structure in a fixed position relative to the first semiconductor region, the second gate structure having a first sidewall and a second sidewall;

wherein the step of forming at least a first layer further forms at least a first layer adjacent the first sidewall and the second sidewall of the second gate structure; and

wherein the step of forming at least one recess comprises forming the at least one recess in the first semiconductor region and extending laterally outward from the first gate structure to the second gate structure.

9. An integrated circuit transistor, formed by steps comprising the method as defined in any of claims 1 – 8.

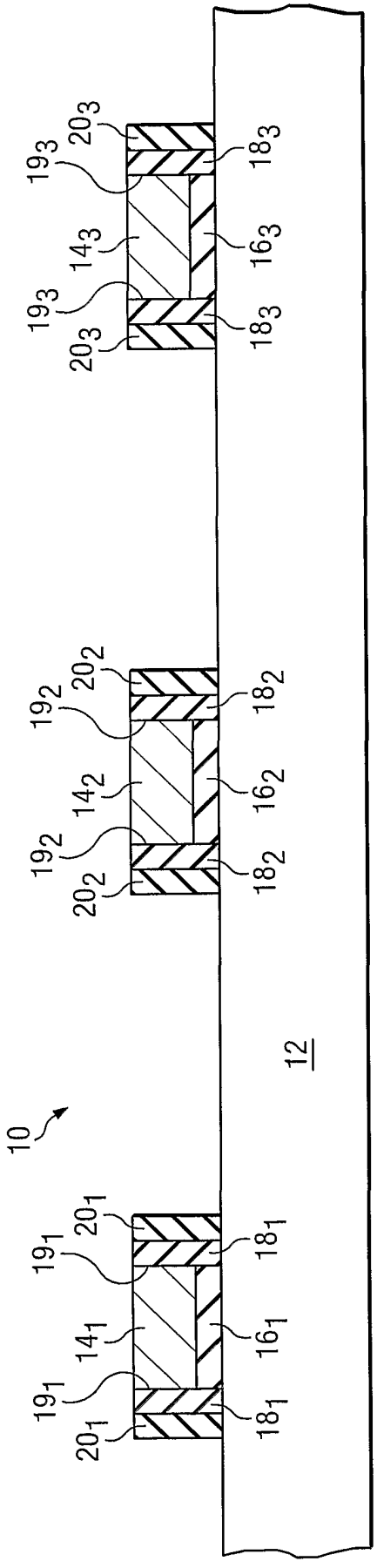


FIG. 1a
(PRIOR ART)

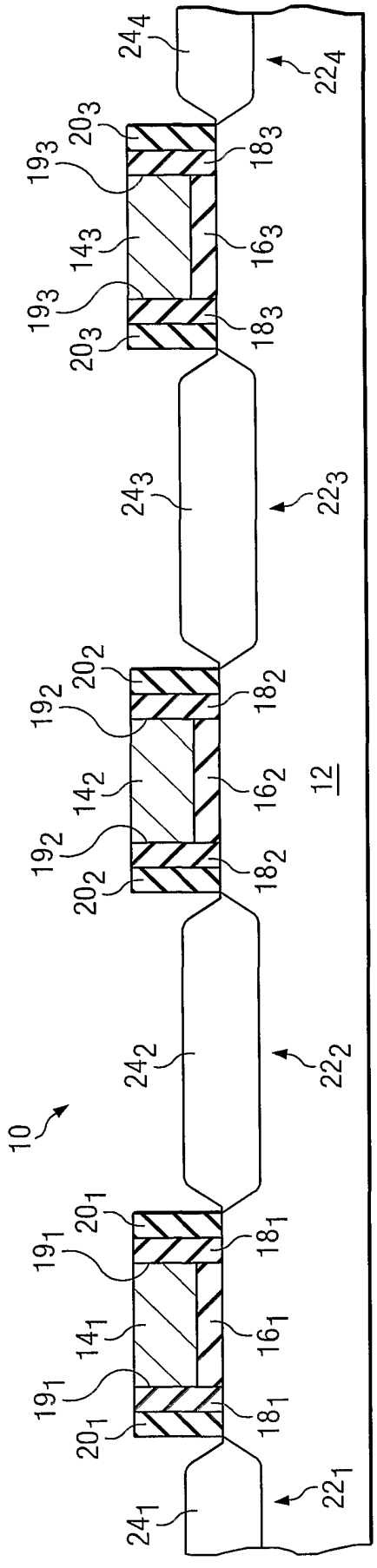


FIG. 1b
(PRIOR ART)

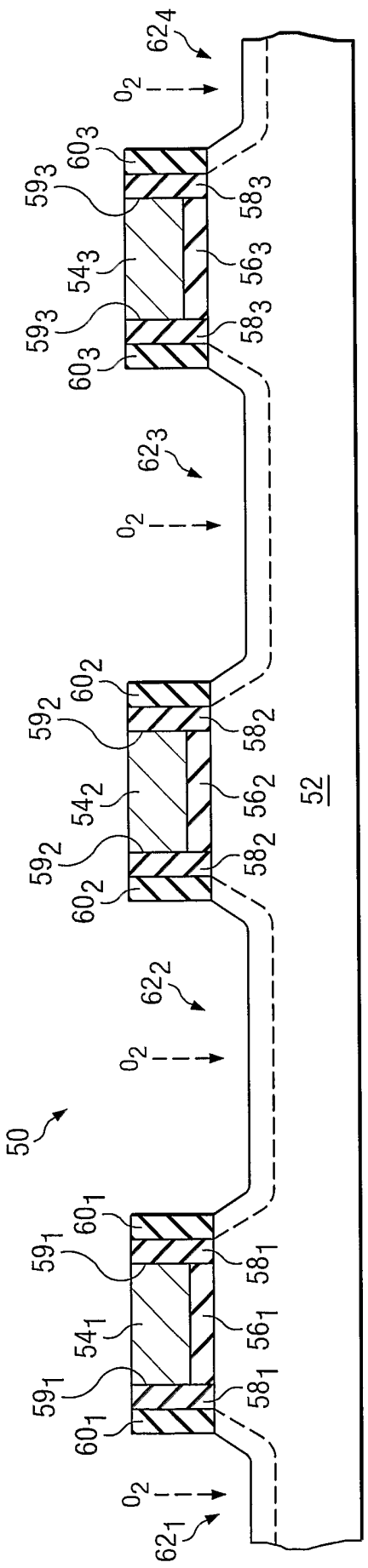
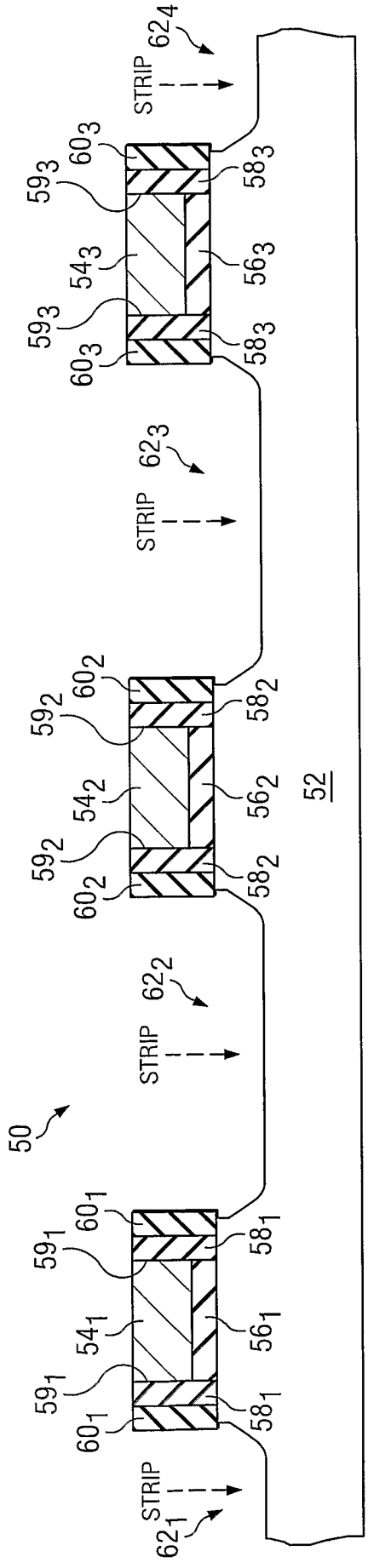

50
52
O_2
62_1
62_2
62_3
62_4
58_1
58_2
58_3
59_1
59_2
59_3
60_1
60_2
60_3
54_1
54_2
54_3
56_1
56_2
56_3

FIG. 2a


50
52
STRIP
62_1
62_2
62_3
62_4
58_1
58_2
58_3
59_1
59_2
59_3
60_1
60_2
60_3
54_1
54_2
54_3
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56_2
56_3

FIG. 2b

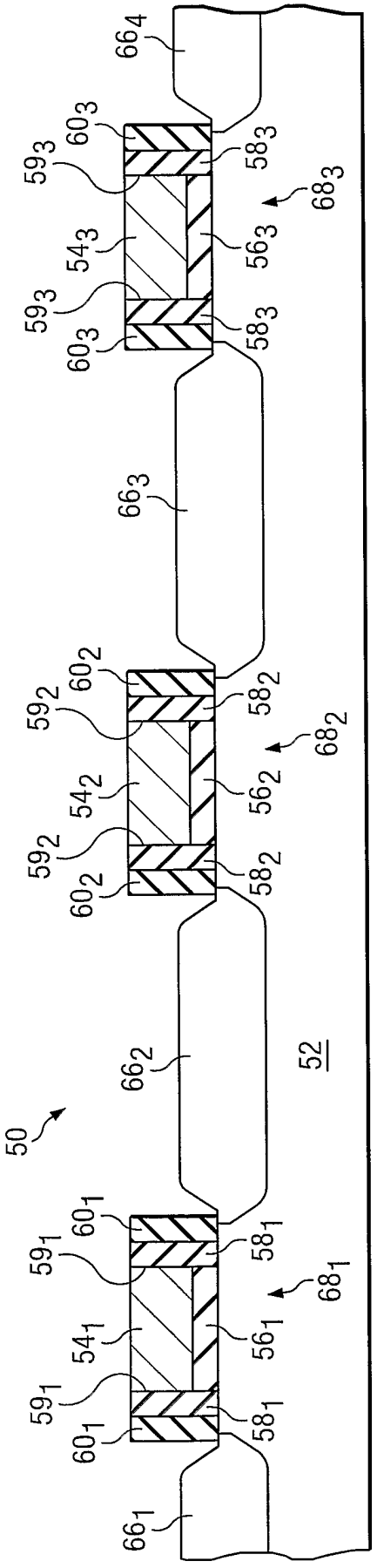
50
52
66_1
66_2
66_3
66_4
68_1
68_2
68_3
59_1
59_2
59_3
60_1
60_2
60_3
54_1
54_2
54_3
56_1
56_2
56_3
58_1
58_2
58_3

FIG. 2c

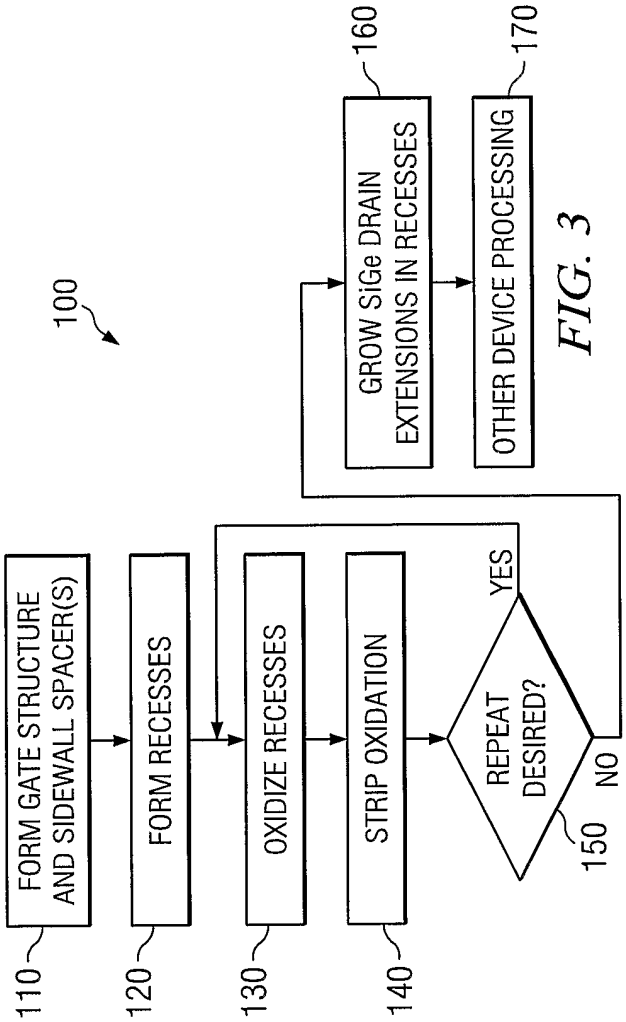
100
FORM GATE STRUCTURE AND SIDEWALL SPACER(S)
FORM RECESSES
OXIDIZE RECESSES
STRIP OXIDATION
REPEAT DESIRED?
YES
NO
GROW SiGe DRAIN EXTENSIONS IN RECESSES
OTHER DEVICE PROCESSING
110
120
130
140
150
160
170

FIG. 3