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(54) Abstract Title
Electrostatic discharge protection for integrated circuits

(57) A chip assembly comprises a chip 9 mounted on a support 7, a terminal 6 and discharge means 8 for discharging a charge accumulated on or transferred to the terminal. The discharge means such as a diode or zener diode is connected to an RF common mode node 5 for voltage controlled oscillator circuits 2 on the chip.

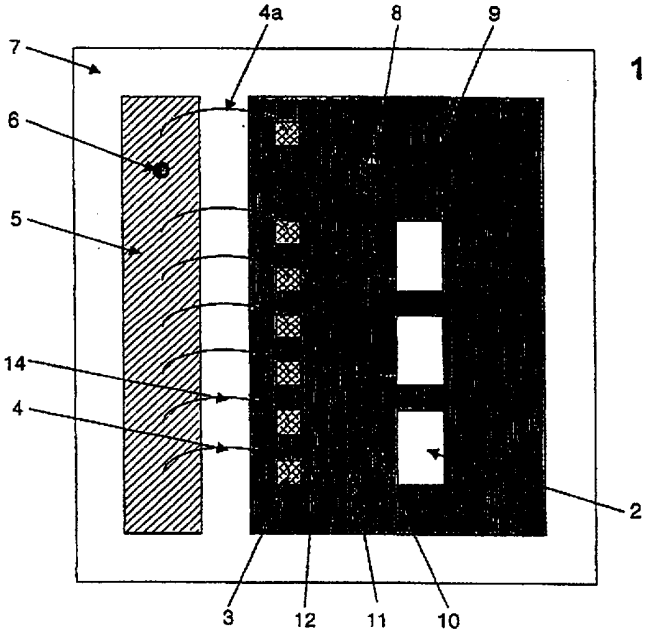

Fig. 1

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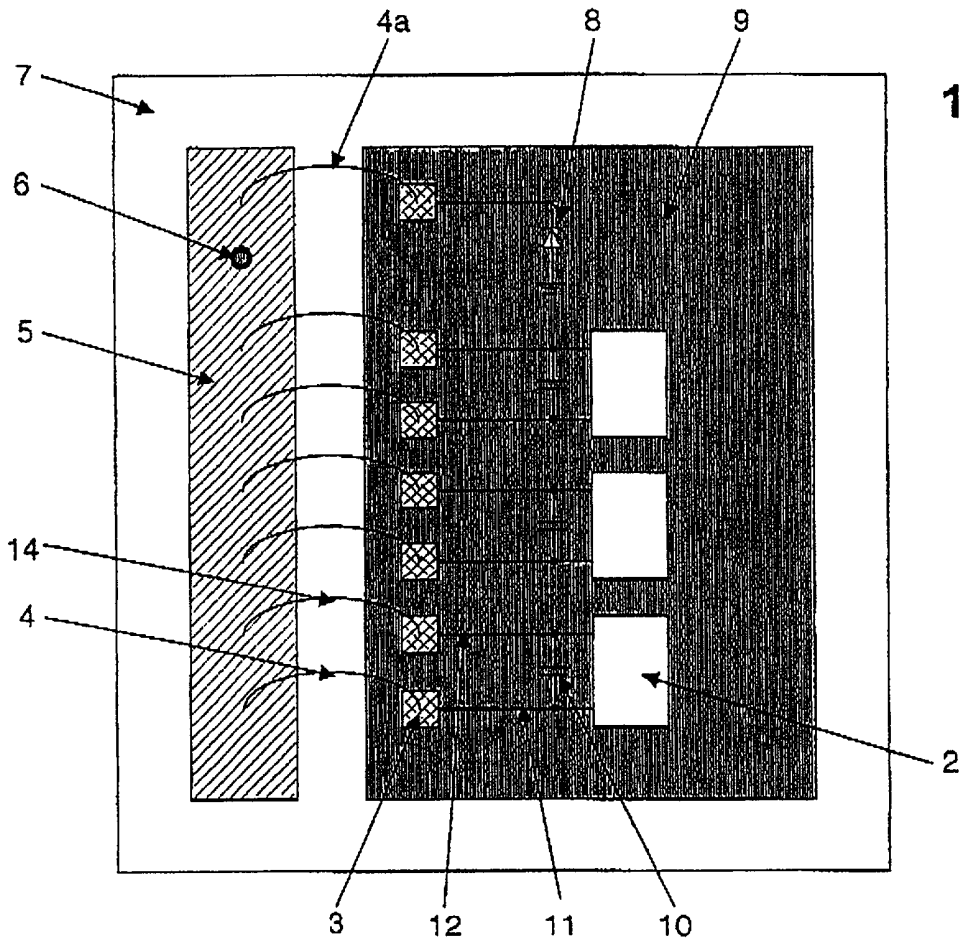

Fig. 1

ESD-Protection of Integrated Circuit

The present invention relates to electrostatic discharge protection in integrated circuits, in particular the invention relates to discharge protection in a chip assembly comprising a chip mounted on a support, said chip assembly comprising at least one terminal and discharge means for discharging a charge accumulated on or transferred to said terminal.

In modern chip-making the dimensions of the chip parts have been ever decreasing. Further these components exhibit high impedances. This has led to problems, because with decreased dimensions and increased impedances, the chips become more vulnerable to electrostatic discharges.

The high impedance of the chip allows potentially harmful electrostatic charges to accumulate on the external terminals or be transferred thereto during manufacture, handling, storing, transport or mounting etc. of the chip.

These charges may be so large that they cause breakdown in the isolating layers of the active parts, e.g. transistors, resulting in a damaging discharge of the accumulated charge through the insulating layers of the active parts.

Even though the individual active part is damaged or even destroyed, this may not always be immediately apparent from the exterior of the chip, but may show only months later. In fact, sometimes the circuit will work, but with decreased performance.

It is well known in the art to overcome these problems by introducing protection means in the chip. A typical way is to introduce a zener diode between the terminal and ground and/or a diode between the terminal and the supply

voltage.

However, the use of additional components such as zener and other diodes has the drawback that they load the terminal. In low frequency applications this is normally not a problem, but in RF circuits even the capacitance of a diode may load the circuit sufficiently to have significant influence on its performance. In particular this is the case in RF oscillator circuits, where the oscillation frequency is a function of capacitances and inductances associated with the circuit or incorporated therein.

In many semiconductor devices the active circuits are embodied as balanced circuits. There are several reasons for this. One reason is that it helps reducing the necessary supply voltage and thus reduces the power consumption of the chip. Another reason is that using balanced circuits obviates the need for a reference potential, and makes the individual circuits less likely to pick up noise transmitted from other circuits on the chip through the semiconducting material.

It is an object of the invention to provide a RF semiconductor chip with an electrostatic discharge protection means, without the above drawbacks.

According to the invention this object is achieved with a chip assembly according to the opening paragraph, characterised in that the discharge means is connected to an RF common mode node, which is preferably on the support.

Preferably the discharge means is located within the chip, so that it can be provided during chip manufacture.

The discharge means is preferably a diode or a zener-diode or a combination thereof, depending on the polarity of the charge to be sinked, and whether it should be sinked to DC ground or to supply voltage.

The invention will now be explained in greater detail using a non-limiting example, and with reference to fig.1, which schematically shows a chip assembly according to the invention.

In fig. 1 there is shown a chip assembly 1 according to the invention.

The chip assembly comprises a support 7 on which a chip 9 in mounted by means of gluing or similar mounting method.

The chip comprises a number of different circuits. In the present example three of these circuits are embodied as balanced voltage controlled oscillators or VCO's 2. Each of the VCO's 2 comprise a pair of balanced on-chip leads 11 and 12 leading to respective connection pads 3 on the chip 9.

Between the leads 11 and 12 of each pair of leads there is provided a capacitance 10.

The connection pads 3 on the chip are connected to a metal covered area 5 on the support 7, by means of bondwires 4.

The leads 11 and 12 and the bondwires 4 and 14, together with the capacitance 10, form the essential parts of LC circuit determining the operating frequency for the respective VCO 2 to which they are connected.

Because the VCO-circuits 2 are balanced, the metal covered area 5 constitutes a common mode node for each of the individual VCO-circuits 2, to which node the circuit is connected via the bondwires 4 and 14, and the on-chip leads 11 and 12. i.e. the metal covered area 5 constitutes a node with an undefined but essentially fixed potential around which the RF signals are balanced during

operation of the chip 9. The operation of the individual balanced circuits 2 are largely independent of this potential.

This allows several circuits such as VCO's 2 to be connected to the same metal covered area 5 essentially without influencing each other i.e. they may operate independently, e.g. at different frequencies.

Further, this allows current supply for the VCO's via a pin 6 connecting the metal covered area 5 to the exterior of the chip assembly 1.

If charge accumulates on or is transferred to this pin 6 during manufacture, handling, storing, transport or mounting etc. of the chip there is, as described above, the potential risk of a destructive discharge within the chip, e.g. in the transistors thereof.

To overcome this risk the chip has been provided with a discharge means 8, in this exemplary embodiment in the form of a zener diode 8. The zener diode 8 is at one end connected to DC ground, and at the other to the metal covered area 5, by means of a bondwire 4a. The polarity and the zener voltage of the diode 8 are chosen so that during normal operation the zener diode 8 blocks the DC supply voltage i.e. prevents it form short circuiting to the DC ground.

If charge accumulates on, or is transferred to, the pin 6 or the metal covered area 5, the potential on the metal covered area 5 will exceed the zener voltage of the zener diode 8, and thus be short circuited to DC ground without harming circuits 2 on the chip.

Because the zener diode 8 is connected to the metal covered area 5, which during operation of the chip constitutes an RF common mode node, i.e. a node with an undefined but essentially constant potential around which the RF

signals are balanced, the presence of the zener diode 8 and the inevitable inductance of the bondwire 4a does not have much influence on the operation of the VCO's 2. Rather, since the metal covered area 5 has an essentially constant DC potential, the capacitances and inductances of the diode 8 and the bondwire has no significant effect on it.

Providing the discharge means 8 between the common mode node, in the form of the metal covered area 5, not only provides a DC path for the accumulated charge to ground, which does not load the circuits 2, but further allows several basically independent balanced circuits 2 on the chip 9 to share the same discharge means.

In the present embodiment the common mode node is in the form of a metallized area 5 outside the chip 9, whereas both the circuits 2 and the discharge means 8 are on the chip 9.

This is however not a prerequisite for the invention.

In principle the zener diode 8 could be a separate component placed on the support 7, but for manufacturing reasons it is desirable to provide this component on the chip 9, thus allowing it to be manufactured cheaply together with the other circuits 2, and further not necessitating separate mounting thereof in the chip assembly 1.

Conversely, the common mode node could be provided within the chip 9 instead of being connected thereto via the sets of bondwires 11 and 12, and the bondwire 4a to the discharge means 8.

In connection with VCO's the present embodiment is however preferred, because it allows the use of the bondwires 11 and 12 to provide tuning inductances for the VCO's 2.

Regardless of the fact that the above explanation of the present invention has been based on an embodiment with VCO's, the skilled person will appreciate that it may be used for various other balanced circuits on a chip without deviating from the inventive concept.

CLAIMS

1. Chip assembly comprising a chip mounted on a support, said chip assembly comprising at least one terminal and discharge means for discharging a charge accumulated on or transferred to said terminal, characterized in that said discharge means is connected to a common mode node for at least one circuit on the chip.

2. Chip assembly according to claim 1, characterized in that the common mode node is located on the support.

3. Chip assembly according to claims 1 or 2, characterized in that said discharge means is located on the chip.

4. Chip assembly according to any one of the preceding claims, characterized in that said discharge means comprises a diode.

5. Chip assembly according to any one of the preceding claims, characterized in that said discharge means comprises a zener diode.

6. Chip assembly according to any one of the preceding claims, characterized in that said common mode node represents a RF common mode node for more than one circuit on the chip.

7. Chip assembly according to any one of the preceding claims, characterized in that said chip comprises a voltage controlled oscillator.

8. Method for protecting a chip against electrostatic discharge, characterized providing an electrostatic discharge means between a common mode node and ground and/or voltage supply.

Patent Office

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Other: ON LINE,W.P.I.,EPODOC,JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	WO 92/16019 A1	VLSI TECHNOLOGY (See common node VDD)	1,8
X	US 5889644	MICRON TECHNOLOGY (See common node 20,Fig.3)	1,8
X	US 5875086	NEC (See common node 16a,Fig.5)	1,8
X	US 5751507	CYPRESS (See common node 24,Fig.2)	1,8
X	US 5748425	TEMIC TELEFUNKEN (See common node VL1 or VL2)	1,8
X	US 5598313	I.B.M.	1,8

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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