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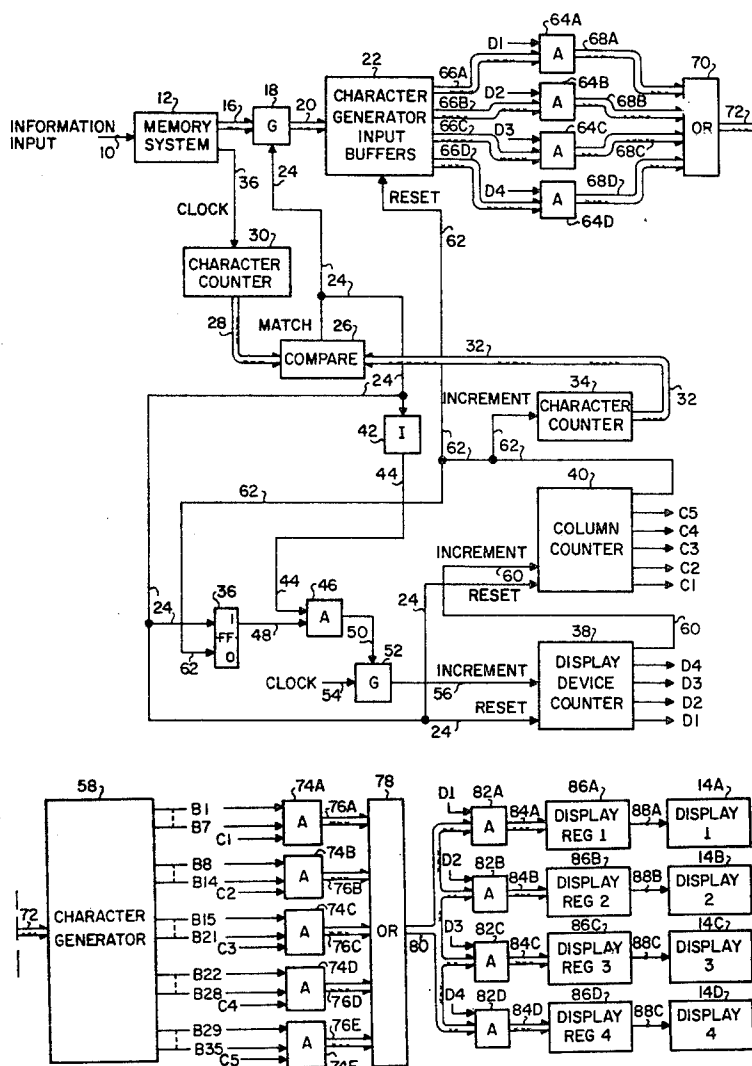
[54] CHARACTER DISPLAY SYSTEM
6 Claims, 3 Drawing Figs.

[52] **U.S. Cl.**..... 340/324
[51] **Int. Cl.**..... G08b 23/00
[50] **Field of Search**..... 340/322,
324, 334, 339

[56] References Cited
UNITED STATES PATENTS

3,273,140	9/1966	Foster	340/334
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ABSTRACT: A system for displaying characters on a plurality of display devices each of which is of a type which requires its display to be refreshed at a predetermined rate. Information to be displayed is stored in a memory means in a first code and is cyclically applied by said memory means to a character generator which generates corresponding characters in a second display code. Characters to be displayed in a given display position on each of the display devices are sequentially applied to the character generator with the output from the character generator being applied to control the display of at least a portion of the character applied to its input on the appropriate display device.



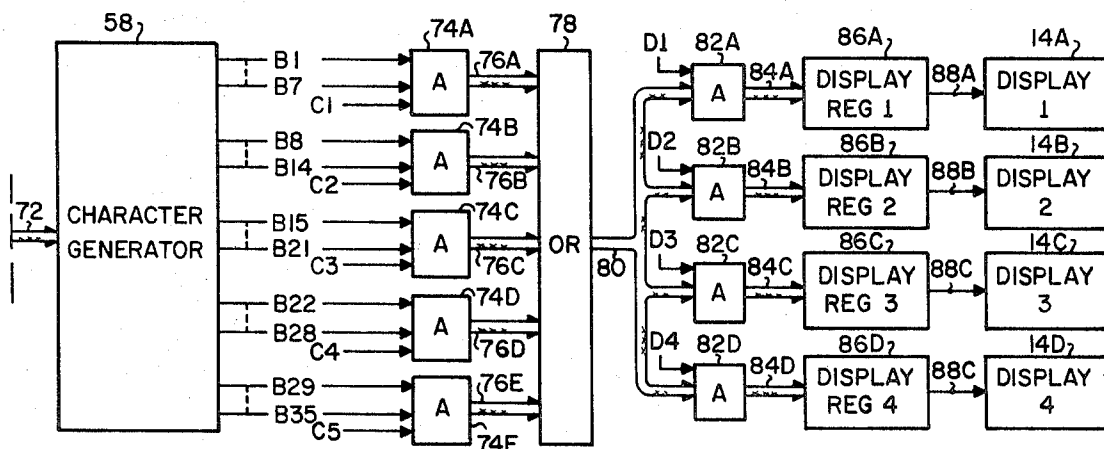


FIG. 1B

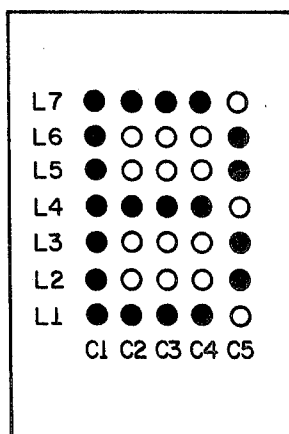


FIG. 2

CHARACTER DISPLAY SYSTEM

CHARACTER DISPLAY SYSTEM

This invention relates to a character display system and more particularly to an improved system which utilizes a single character generator to maintain the display on a plurality of display devices.

While some display systems, such as those using neon lamps, contain storage within the display element so that additional storage devices and refreshing of the display are not required, faster and more versatile displays, such as cathode-ray tube (CRT) display systems, require that the display be periodically refreshed. The information to be displayed is stored in a memory device which is cyclically accessed and utilized to refresh the display on the display tube. If the tube is refreshed at a high enough rate, a flicker-free display is obtained; in other words, the display appears to be continuously present.

There are two standard methods presently utilized for performing the refresh operation: The first of these methods involves passing information applied to the system in, for example, a four to seven bit transmission code, through a character generator which generates the 35- to 50-bit video-code equivalent of the received character, and then storing the video-code character in a memory device in a position corresponding to the position on the display at which the received character is to appear. This scheme, which permits a single character generator to be utilized to control the display on an almost unlimited number of display devices, makes efficient use of the character generator. However, since the storage device must store video-code, the storage requirements are six to seven times as great as would be required if the received transmission code was stored. Therefore, such savings as may be effected by sharing the character generator a number of display devices are substantially lost in the increased memory costs.

A second method utilized in display systems of this type has the incoming transmission code stored directly in a memory device and applies the output from the memory device through the character generator to control the display on the display device. This method has the advantage of requiring a relatively small amount of storage. Also, since the number of bits accessed from memory for each character is substantially less, the memory device utilized may also operate at lower speed. However, when a system of this type is utilized with a number of display devices, a number of character generators may be required in order to permit refresh of the display devices to be performed at a fast enough rate to prevent flicker. For example, assume that a display device must be refreshed at a rate of at least 50 times per second in order to achieve a good flicker-free display. This means that a refresh must occur every 20 milliseconds. If it takes 5 milliseconds to refresh a single display screen, then a single character generator could be used for only four display devices regardless of the speed of the character generator itself. This means that if there were even five display devices in the system, two character generators would be required; while if there were 10 display devices in the system, three character generators would be required. Since character generators are relatively expensive components, it is desirable to use as few of these components in a system as possible.

It is, therefore, a primary object of this invention to provide an improved character display system.

More specifically, it is an object of this invention to provide a character display system which permits a single character generator to be utilized at optimum capacity to control the display devices while requiring a minimum of information storage.

In accordance with these objects, this invention provides a character display system which includes a plurality of display devices, such as CRTs, each of which has a plurality of character display positions and each of which requires that the

display be refreshed at a predetermined rate. The information to be displayed on each of the display devices is stored in a first code, for example the transmission code, in a memory means, and is cyclically applied to a character generator which is adapted to receive character information in the first code and to generate corresponding character information in a second video or display code. Information is applied from the memory means to the character generator starting with a character which is to be displayed in a given character position on a display device, and followed in sequence by the characters which are to be displayed in the corresponding display position on the other display devices. Each time this sequence of character is applied to the character generator, one or more bits at the output from the character generator may be utilized to control the display on the corresponding display device. Assume that $1/N$ of the output bits from the character generator are utilized to control the display each time a character is applied to the character generator input, the sequence of characters for the given display position must be cycled through the character generator N times before the characters for the next character position on the display may be applied to the character generator. This sequence of operations is repeated four succeeding characters of a frame until the frame is completed. The sequence of operations is then repeated starting again at the beginning of the frame.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention as illustrated in the accompanying drawings.

IN THE DRAWINGS:

FIGS. 1A and B when combined as shown in FIG. 1 form a schematic block diagram of an illustrative embodiment of the invention.

FIG. 2 is a diagram illustrating a single display character on one of the display devices.

Referring now to FIG. 1A it is seen that the information to be displayed is received over a line 10 and stored in memory system 12. Line 10 may, for example, be the output from a modem and may contain information in a six bit transmission code. Each character of the received input is stored in a position in memory system 12 corresponding to a display position on a particular display device at which the information is to be displayed. This storage is accomplished utilizing standard techniques which do not form part of the present invention and will not be described further.

While memory 12 may be a recirculating delay line with the information for the various display devices being stored in succeeding time slots thereof, or a random access magnetic core memory, for purposes of the present discussion memory 12 will be assumed to be a rotating magnetic drum with the information to be displayed on each of the display devices being stored on a separate track thereof. Therefore, there is a track for display 1, a track for display 2, etc., and each track contains the characters to be displayed on the corresponding display device in sequential order.

For illustrative purposes, four display devices, 14A-14D (FIG. 1B) will be assumed. In an actual system, a larger number of display devices would in all likelihood be utilized. Four tracks on memory 12 are thus utilized, the output of each of the tracks being applied through a corresponding line 16 to a gate 18. Gates 18 are conditioned to pass the character information applied to them through lines 20 to character generator input buffer 22 when there is a signal on match output line 24 from compare circuit 26. The inputs to compare circuit 26 are output lines 28 from character counter 30 and output line 32 from character counter 34. Character counter 30 is stepped by clock signals on output line 36 from memory system 12. Character counter 30 thus contains, at any given time, an indication of the character which is presently being accessed on each of the tracks of memory 12. As will be seen shortly, character counter 34 indicates the next character position on the display devices which is to be refreshed. Therefore, when compare circuit 26 generates a signal on

match line 24, this indicates that the character presently being accessed in memory 12 is the next character which is to be refreshed on the display devices. Gates 18 are thus conditioned to pass the code for this character position on each of the tracks of memory 12 through lines 20 to be stored in the corresponding buffer 22. There is a buffer 22 for each of the display devices 14 or, in other words, four buffers for the illustrative embodiment.

The signal on match line 24 is also applied to set flip-flop 36 to its ONE state and to reset display device counter 38 and column counter 40. When the loading of the characters into buffers 22 has been completed, character counter 30 is incremented while the count in character counter 34 remains unchanged. There is, therefore, no longer a successful comparison in compare circuit 26 and inverter 42 thus applies a signal through line 44 to one input of AND gate 46. The other input to AND gate 46 is ONE-side output line 48 from flip-flop 36. AND gate 46 is thus fully conditioned at this time to generate an output signal on line 50 which signal is applied to condition gate 52 to pass clock pulse on line 54 to line 56. The clock applied to line 54 may be derived from clock line 36 by multiplication or division and should be at a rate such that a complete cycle of counters 36 and 40 is completed during the time required for one revolution of the drum in memory 12.

As was just indicated, counters 38 and 40 were reset to generate output signals on line D1 and C1 respectively when a match signal appeared on line 24. Display device counter 38 indicates the display device which is to have access to character generator 58 at any given time. It is incremented by a clock signal on line 56 and has four output lines D1—D4 which correspond to display devices 14A—14D respectively. Each time counter 38 is incremented from its D4 position to its D1 position, a signal is generated on line 60 which signal is applied to increment column counter 40. The significance of column counter 40 may be ascertained by referring to FIG. 2 where a single character of the display is shown. From this figure it is seen that each character is formed from a 5×7 matrix of dot or bit positions with the columns of the matrix being labeled C1—C5 respectively and the lines of the matrix being labeled L1—L7. Character generator 58 thus has 35 output lines each line corresponding to one of the 35 bits of the display matrix. For the embodiment of the invention shown in FIG. 1, only seven of these lines, the lines corresponding to one column, are utilized each time a character is applied to the character generator. Therefore, each set of character codes stored in buffer 22 must be cycled through the character generator five times to form complete characters on display devices 14. Column counter 40 indicates which column of the characters will be mapped on the display devices during each cycle. Output lines C1—C5 from column counter 40 correspond to columns C1—C5 of the display character matrix. When counter 40 is stepped from generating an output on line C1, a signal appears on overflow line 62 which signal is applied to increment character counter 34 and to reset input buffers 22 and flip-flop 36. The significance of these operations will be described later.

When the loading of the characters into input buffers 22 has been completed, there are signals on the D1 and the C1 clock lines. The signal on the D1 clock line is applied to fully condition AND gate 64A to pass the bits for the character in a buffer 22 for display device 1 through lines 68A, OR gate 70, and lines 72 to character generator 58. Character generator 58 generates outputs on selected ones of its B1—B35 output lines, the lines being those required in video-code to display the character applied to the character generator input. Since only the C1 output line of the outputs from column counter 40 has a signal on it at this time, only AND gate 74A of the gates 74 is conditioned. The signals on the B1—B7 lines, the bit lines for column 1, are thus passed through AND gate 74A, lines 76A, OR gate 78, and lines 80 leading to AND gates 82. Since there is a signal on the D1 line at this time, AND gate 82A is conditioned to pass the bit signals on lines 80 through lines 84A to be stored in display register 86A. The bits to be

displayed in column 1 of the character on display device 1 are thus stored in display register 86A. These bits are sequentially applied through line 88A, under control of display device 14A, to control the mapping of the first column of the character, the circuit timing being such that this mapping is completed before the D1 line is again energized.

The next clock signal applied to line 54 steps device counter 38 to generate an output on the D2 line. This causes the character in the second buffer 22 to be applied through AND gate 64B to character generator 58. Since there is still a signal on the C1 line, the resulting outputs on the B1—B7 lines from character generator 58 are applied through AND gate 74A and now condition AND gate 82B to be stored in display register 86B. The mapping of the first column of the character on the second display device 14B is thus arranged. Succeeding clock pulses on line 54 result in the first column for the characters stored in the third and fourth input buffer 22 being loaded into display registers 86C and 86D respectively.

When the loading of the first column into display register 86D has been completed, the next clock pulse applied to line 54 results in display device counter 28 being restored to its initial condition with an output on the D1 line and in a signal appearing on overflow line 60 which signal increments column counter 40 to generate an output on the C2 line. The sequence of operation described above is then repeated with the character codes in buffers 22 being sequentially applied through AND gates 64 to character generator 58 and with the B8—B14 outputs from the character generator being passed through now conditioned AND gate 74B and the AND gates 82A—82D respectively to cause the second column of each of the characters to be stored in the corresponding one of the display registers 86. This results in the second column for each of the characters being mapped on the corresponding display device.

Each time a clock pulse appears on line 54 when display device counter 38 is generating an output on its D4 output line, column counter 40 is incremented and counter 38 begins a new cycle. The bit codes for the 3rd, 4th and 5th columns of the characters stored in buffers 22 are thus stored in display registers 86A—86D during succeeding cycles of counter 38 and utilized to control the mapping of these columns on the display devices. When counter 40 is generating an output on its C5 line and an overflow signal appears on line 60, the refresh of the characters loaded into buffer 22 has been completed and the circuit is ready to initiate the refreshing of a new set of characters. Counters 38 and 40 are thus both incremented to their initial condition and an overflow signal appears on line 62 from counter 40 which signal is applied to increment the character count in counter 34, to reset input buffers 22, and to reset flip-flop 36 to its ZERO state. Flip-flop 36 being reset to its ZERO state deconditions AND gate 46 thus preventing clock pulses on line 54 from being applied to display device counter 38. Counters 38 and 40 thus remain in their initial condition.

Nothing further happens until the character count in counter 30 is again equal to the character count in counter 34. As was indicated previously, the timing of the circuit is such that this occurs almost immediately after the signal appears on line 62. When a match signal again appears on line 24, gates 18 are conditioned to store the new set of characters in buffer 22, flip-flop 36 is restored to its ONE state, and reset signals are applied to counters 38 and 40. When the loading of characters into buffer 22 is completed, inverter 42 again fully conditions AND gate 46 and a new cycle of operation, identical to that described above, is initiated.

It should be noted that no mention has been made as to how character counter 34 is initially set. While some means could be provided for initially setting this counter, it is not necessary since all character positions of the frame are sequentially refreshed at a high frequency and the point at which the refresh begins is of little importance. When it is desired to change the display, new information is applied through line 10 to memory 12. During the following refresh cycle, this new in-

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formation is applied to character generator 22 and is written on the display in place of the information which was previously there.

While four display devices have been shown as being serviced by a single character generator 58 in the embodiment of the invention of FIGS. 1A and 1B, it is apparent that a substantially larger number of displays may be serviced by the character generator utilizing the teachings of this invention. The number of displays which may be serviced is a function of the speed of character generator 58, the refresh time and frequency required for the display devices, and the size of display registers 86. Since display registers 86 increase the cost of the system, it is desirable to keep the size of these registers as small as possible or to eliminate them completely. However, to eliminate registers 86, it is necessary to cycle each character through character generator 58 35 times during each refresh cycle. To accomplish this, while still maintaining the required refresh frequency, would require the use of either an exceptionally high speed character generator or a reduction in the number of display devices serviced. The circuit designer must therefore arrive at a cost trade-off compromise between the number of display devices to be serviced by a single character generator and the amount of storage which each of the registers 86 is to provide.

While a drum memory with a separate track for each display device, and a separate input buffer 22 for each display device, have been assumed in the circuit of FIG. 1A, it is fully within the contemplation of this invention to have all the stored information within a single recirculating delay line with the characters being retrieved from the delay line and stored in a single buffer in the sequence described above. Other similar modifications would suggest themselves to those skilled in the art. While specific circuitry for characters generator 58 and display devices 14 have not been provided in the above description, examples of the circuitry suitable for this purpose may be found in U.S. Letters Pat. No. 3,440,646, entitled "Code Conversion Means," issued Apr. 22, 1969 to E. M. Dean, and No. 3,500,327 entitled "Data Handling Apparatus," issued Mar. 10, 1970 to R. D. Belcher, et al. Both of these Patents are assigned to the assignee of the instant application.

While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made without departing from the spirit and scope of the invention.

What I claim is:

1. A character display system comprising:

a plurality of display devices, each of said display devices having a corresponding plurality of character display positions and being of a type which requires its display to

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be refreshed at a predetermined rate;

memory means adapted to store in a first code the information to be displayed on each of said display devices;

a character generator adapted to receive character information in said first code and to generate corresponding character information in a second display code;

first means for cyclically applying the characters stored in said memory means to said character generator, with the characters which are to be displayed in the corresponding display position of each of the display devices being sequentially applied to said character generator; and

second means for applying the output from said character generator to control the display of at least a portion of the character applied to its input on the appropriate display device.

2. A system of the type described in claim 1 wherein, each time the character generator has an input applied to it, its output is utilized to control the display of a 1/N portion of the character; and

wherein said first means is operative to sequentially apply the characters for a given display position to said character generator a total of N times before applying a character for any other display position to said character generator.

3. A system of the type described in claim 2 including means operative each time a character is applied to the character generator for selecting the proper 1/N portion of the character generator output to control the display.

4. A system of the type described in claim 1 wherein, each time a character is applied to the character generator, its output is utilized to control the display of at least two bits of the character; and including

means associated with each of said display devices for storing the character generator outputs applied thereto.

5. A system of the type described in claim 1 including means for indicating the display device for which the character applied to said character generator is intended; and

wherein said first means for directing a character for the indicated display device from said memory means to said character generator; and

wherein said second means includes switching means responsive to said indicating means for directing the output from said character generator to the indicated display device.

6. A system of the type described in claim 1 wherein the number of display devices served by a character generator of a given speed, and the portion of the character which has its display controlled each time a character is applied to the character generator are selected so as to maximize the number of display devices serviced while still refreshing at a fast enough rate to provide a flicker-free display.

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