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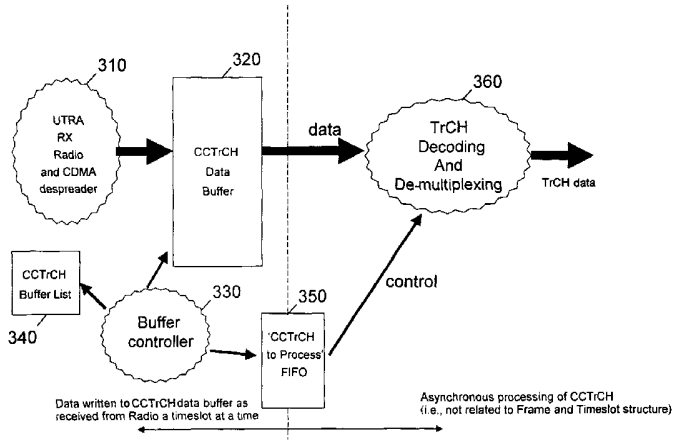
[Continued on next page]

(54) Title: METHOD AND ARRANGEMENT FOR ASYNCHRONOUS PROCESSING OF CCTrCH DATA



340

(57) Abstract: A method and arrangement for processing of CCTrCH data in a UMTS system, by: receiving CCTrCH data across a plurality of radio frames and timeslots (310); storing the received CCTrCH data (320); and upon receipt of complete data for a CCTrCH, processing the stored CCTrCH data through channel processing asynchronously to the received timeslot structure (360). Preferably, the received CCTrCH data is stored in a single RAM memory in link-list form, whereby each timeslot of received CCTrCH data can be independently accessed in the memory. This method of buffering the different parts of the received CCTrCH data, so that they can be recombined before the TrCH decoding and de-multiplexing, is both memory efficient and spreads out the processing load over time.

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METHOD AND ARRANGEMENT FOR ASYNCHRONOUS PROCESSING OF CCTrCH DATA

Field of the Invention

This invention relates to Universal Mobile Telecommunication Systems (UMTS), and particularly to decoding and de-multiplexing in such systems.

Background of the Invention

In the field of this invention it is known that, in UMTS Terrestrial Radio Access (UTRA) Time Division Duplex (TDD) mode, Coded Composite Transport Channel (CCTrCH) data is can be split across multiple timeslots in consecutive Radio Frames. This is determined by the Transmission Time Interval (TTI), which is typically 10, 20, 40, 80 ms, or 1, 2, 4, 8 Radio Frames.

As a UTRA system is packet based the data received which needs to be processed is non-deterministic in size and in frequency. Therefore to store and process the data efficiently a scheme is required that can buffer and process this data effectively.

Heretofore, schemes used for CCTrCH processing have had the disadvantage of compromised efficiency since they do not efficiently store the data prior to processing and

they do not take advantage of the fact that not all the timeslots in a radio frame are used to receive data.

A need therefore exists for processing of CCTrCH data wherein the abovementioned disadvantage(s) may be alleviated.

Statement of Invention

In accordance with a first aspect of the present invention there is provided a method for processing of CCTrCH data as claimed in claim 1.

In accordance with a second aspect of the present invention there is provided an arrangement for processing of CCTrCH data as claimed in claim 7.

The arrangement may be comprised in user equipment for use in a UMTS system.

The arrangement may alternatively be comprised in a base station for use in a UMTS system.

In essence, the invention is based in part on the idea of processing the CCTrCH data asynchronously to the timeslot structure rather than processing each CCTrCH in the timeslot in which it was received. This has the advantage of increasing the amount of time available to process the CCTrCH as not all timeslots in a frame are receive timeslots (whereas if each CCTrCH is processed in

the individual timeslot it is received then the processing time associated with transmit timeslots is not used).

Brief Description of the Drawings

One method and arrangement for asynchronous processing of CCTrCH data incorporating the present invention will now be described, by way of example only, with reference to the accompanying drawing(s), in which:

FIG. 1 shows a block schematic diagram illustrating time domain UTRA framing;

FIG. 2 shows a block schematic diagram illustrating multiplexing and channel coding in UTRA;

FIG. 3 shows a block schematic diagram illustrating an arrangement for buffering and control of CCTrCH incorporating the present invention;

FIG. 4 shows a block schematic diagram illustrating a RAM arrangement split up into "slots" of data, as used in the arrangement of FIG. 3; and

FIG. 5 shows a flowchart illustrating CCTrCH buffer controller flow, as used in the arrangement of FIG. 3; and

FIG. 6 shows a block-schematic diagram of a UMTS system in which the invention is used.

Description of Preferred Embodiment

In a UMTS Terrestrial Radio Access Network (UTRAN) there are two modes of operation: UTRA Frequency Division Duplex (FDD) and UTRA Time Division Duplex (TDD). In UTRA TDD users are separated in both the code domain and time domain. In the time domain employed in UTRA framing, illustrated in FIG. 1, 4096 radio frames make up a super frame with each radio frame consisting of 15 timeslots. A timeslot can be allocated to either Uplink (UL) or Downlink (DL) transmission.

In a typical TDD system the UL and DL transmissions have to be synchronized to reduce interference. In addition DL broadcast signaling and UL random access signaling has to be supported. This leads to a possible partitioning of the radio frame as shown below:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
DL	DL	DL	DL	DL	DL	DL	DL	UL	UL	UL	UL	UL	UL	UL

UTRA specifies the processing that is applied to the Transport Channel (TrCH) data by Layer 1 (L1), as shown in FIG. 2.

Transport Blocks (blocks of a defined number of bits) are submitted by the media access control (MAC) to L1 for

processing. A Transport Block typically corresponds to a MAC protocol data unit (PDU) or corresponding unit. Layer 1 processes each Transport Block as shown in FIG. 2 to build up CCTrCHs. Firstly, cyclic redundancy check (CRC) attachment is performed at 205; then, transport block (TrBk) concatenation/code block segmentation is performed at 210. Next, channel coding is performed at 215; then, radio frame equalisation is performed at 220. Next, first interleaving is performed at 225; then, radio frame segmentation is performed at 230, and rate matching is performed at 235. A number of rate-matched data streams are multiplexed together on a single transport channel at 240; then, the resultant multiplexed data stream is processed by bit scrambling at 245. The bit-scrambled data stream is segmented into a number of physical channels at 250; then, second interleaving is performed on each of the segmented physical channel data streams at 255. Finally, physical channel mapping is performed at 260 to produce a number of CCTrCHs for physical channels such as PhCH#1 and PhCH#2. These CCTrCHs are mapped onto timeslots in known manner.

Each CCTrCH can be split across multiple timeslots in consecutive Radio Frames. This is determined by the Transmission Time Interval (TTI), which is typically 10, 20, 40, 80 ms or 1, 2, 4, 8 Radio Frames.

As a UTRA system is packet based the data received which needs to be processed is non-deterministic in size and in frequency. Therefore to store and process the data efficiently an architecture is required that can buffer

and process this data effectively. The maximum throughput for the CCTrCH processing is fixed for a particular system; however the number, size and frequency of CCTrCHs that are processed are dynamically allocated. The storage and processing strategy must therefore be flexible to efficiently process the data.

Since the CCTrCH received have different TTI periods and can be allocated to different timeslots in a Radio frame, timeslots of data for different CCTrCH are received interleaved with each other. This means that the receiver has to recombine and re-order the received data into the CCTrCHs that were sent, before they can be processed by the TrCH decoder and de-multiplexing process.

Heretofore, schemes used for CCTrCH processing have had the disadvantage of compromised efficiency, such as by use of a dedicated buffer per CCTrCH (in this case each buffer needs to be sized for the largest CCTrCH that can be received, requiring a large amount of redundant memory).

As referred to above, the present invention is based in part on the idea of processing the CCTrCH data asynchronously to the timeslot structure rather than processing each CCTrCH in the timeslot in which it was received. This has the advantage of increasing the amount of time available to process the CCTrCH as not all timeslots in a frame are receive timeslots (whereas if each CCTrCH is processed in the individual timeslot it is

received then the processing time associated with transmit timeslots is not used).

Asynchronous Processing Overview

FIG. 3 shows the block diagram of a proposed arrangement 300 to buffer and process the CCTrCH data with improved efficiency. Data is received from a radio unit as it is de-spread by the front end of the detection process 310. This is synchronous to the timeslot and frame structure in a UTRA TDD system. The way the data for each CCTrCH is stored in buffer 320, under control of a buffer controller 330, will be described below in greater detail.

The data for a CCTrCH can be split over Radio Frames and timeslots within the Radio Frame. As each 'timeslot worth' of data is received it is buffered in the RAM of the CCTrCH data buffer 320 in the order that it is received in such a way that the data for each CCTrCH is associated together; this is achieved by use of a 'linked-list' scheme, the start of each 'linked-list' in the data buffer 320 being added to the buffer list 340. Once all the data for one CCTrCH has been received, an indication of this CCTrCH is added to a 'CCTrCH to Process' FIFO buffer 350. The FIFO 350 acts as a queue of CCTrCHs that need to be processed by the TrCH decoding and de-multiplexing process 360. The TrCH decoding and de-multiplexing process can then process the received CCTrCHs that are indicated in the FIFO asynchronously to the timeslot structure. Once the CCTrCH has been

processed, the area in the buffer RAM that this CCTrCH occupied can be reused by another CCTrCH.

CCTrCH Buffer RAM Structure

The CCTrCH data buffer RAM format must be flexible enough to allow different CCTrCHs of different sizes and different numbers of timeslots to be stored efficiently. For this reason a single RAM was chosen and the CCTrCH data is stored using a link-list format. Due to the packet based nature of the received CCTrCH data, the data associated with each CCTrCH will not be sequential in the CCTrCH buffer RAM. However, the link-list approach allows all the data in each CCTrCH to be linked together.

The RAM is split up into "slots" of data of the format shown in FIG. 4. This consists of three header fields: address of next slot 410, Number of bits in slot 420 and status 430.

The amount of data 440 in the slot is chosen to be a common multiple of the amount of data that could be received in a timeslot per CCTrCH. A CCTrCH with more data can be stored in the RAM by using multiple slots. The 'number of bits in slot' header field 420 allows for the fact that the amount of data in a CCTrCH might not be an integer multiple of the slot size.

The status field 430 is used to store such information as whether or not the slot is available for use and whether or not it is the last slot in the 'linked-list' for the

CCTrCH buffer.

A separate list 340 is kept of the first slot in each CCTrCH that is stored in the RAM. This is termed the CCTrCH buffer list and is used to identify each CCTrCH that is in the CCTrCH buffer RAM. The CCTrCH buffer is assigned a CCTRCH ID at this point. This ID can be used to identify each CCTrCH in the CCTrCH buffer RAM 320.

CCTrCH data is added to the buffer RAM by finding the next available slot in the RAM. The address of the next slot in the RAM is updated dynamically as a link list to point to the next slot in the RAM for that CCTrCH. Thus by finding the first slot in the RAM for a CCTrCH from the CCTrCH buffer list it is possible to trace the slots for that CCTrCH through the CCTrCH buffer RAM.

Referring now also to the flowchart of FIG. 5, which illustrates how the buffer controller works, CCTrCH data is added to the CCTrCH buffer RAM as follows:

i) A new CCTrCH. If the data received is for a new CCTrCH then the address of the first available slot in the CCTrCH RAM is added to the CCTrCH buffer list as a new CCTrCH buffer and assigned a CCTrCH ID, as shown at 510. The CCTrCH data received is added to slots one at a time, until all the data has been added to the buffer RAM. This is achieved by find the next available slot in the CCTrCH buffer RAM 320 (as shown at 520), and adding CCTrCH data to the slot (as shown at

530). As each slot is used the address of the next slot is added in the appropriate field (as shown at 540). This process is continued (as shown at 550) until all the data in the current received timeslot for the CCTrCH been copied. When all the data for the CCTrCH been received (as shown at 560), the CCTrCH ID and first slot address are added to the to 'CCTrCH to Process' FIFO 360 (as shown at 570).

ii) An existing CCTrCH. The first slot in the CCTrCH is found from the CCTrCH buffer list 340 (as shown at 580). The slots already received for the CCTrCH are traced through the CCTrCH buffer RAM to find the last slot in the RAM for this CCTrCH (as shown at 590). The next slot field can then be updated with the next available slot address (as shown at 520), and the CCTrCH data received is added to available slots one at a time until all the data has been added to the buffer RAM (as shown at 530). As each slot is used, the address of the next slot is added in the appropriate field (as shown at 540).

An improvement would be in addition to store the address of the last slot in the 'linked-list' in the CCTrCH buffer list 340. This means that to add new CCTrCH data to the 'linked-list' the last slot address of the data already in the ram can be read directly from the CCTrCH buffer list 340 and the 'linked-list' would not need to be traced through the RAM to find the last slot address.

When all the data for a CCTrCH has been added to the CCTrCH buffer RAM, then the CCTrCH data can be processed by the TrCH decoder and de-multiplexing processing. This is indicated by adding the address of the first slot in the CCTrCH buffer RAM into the 'CCTrCH to Process' FIFO along with its CCTrCH ID (as shown at 570).

When the CCTrCH has been processed, the slots in the RAM that are used to store the CCTrCH data can be de-allocated. This allows the slots to be re-used for other CCTrCHs.

Asynchronous TrCH processing

Once all the data for a CCTrCH has been received, the TrCH decoding and de-multiplexing processing can begin. This processing can be carried out asynchronously to the timeslot structure. This has the advantage of spreading the processing over the whole of the radio frame and thus allowing more time for the data to be processed.

The TrCH processing waits for a valid CCTrCH ID to be added by the buffer controller to the 'CCTrCH to Process' FIFO. This indicates that there is a complete CCTrCH of data to process.

The TrCH processing can then read the CCTrCH slot by slot from the CCTrCH data buffer by following the link list through the RAM. When the data has been processed, the TrCH processor signals back to the buffer controller via

another FIFO that the slots in the RAM that the CCTrCH uses can be freed up for use by another CCTrCH.

Referring now also to FIG. 6, a UMTS system 600 includes a user terminal 610 (commonly referred to as 'User Equipment') which communicates over a CDMA radio link with a base station 630 (commonly referred to as a 'Node B'). The Node B 630 is controlled by a radio network controller 640, which communicates with other system infrastructure shown collectively as 650. Such a system (insofar as it has been described up to this point) is well known and need not be described further. However, it will be understood that the arrangement 300 described above for buffering and control of CCTrCH may be advantageously implemented in either a UE 610 or a Node B 630 of the system as shown in the figure.

It will be appreciated that the method described above for buffering and control of CCTrCH may be carried out in software running on a processor (not shown), and that the software may be provided as a computer program element carried on any suitable data carrier (also not shown) such as a magnetic or optical computer disc.

It will be also be appreciated that the method described above for buffering and control of CCTrCH may alternatively be carried out in hardware, for example in the form of an integrated circuit (not shown) such as an FPGA (Field Programmable Gate Array) or ASIC (Application Specific Integrated Integrated Circuit).

In conclusion, therefore, it will be understood that the asynchronous processing of CCTrCH data described above provides an efficient scheme for buffering the received data from the radio and asynchronously processing the CCTrCH in a way that is both memory efficient and spreads out the processing load over time.

Claims

1. A method for processing of CCTrCH data in a UMTS system, comprising the steps of:

receiving CCTrCH data across a plurality of timeslots;

storing the received CCTrCH data; and

upon receipt of complete data for a CCTrCH, processing the stored CCTrCH data through channel processing asynchronously to individual received timeslots.

2. The method of claim 1 wherein the step of storing the received CCTrCH data comprises storing the received CCTrCH data in memory in link-list form, whereby each timeslot of received CCTrCH data can be independently accessed in the memory.

3. The method of claim 2 wherein the step of storing the received CCTrCH data comprises storing each timeslot of received CCTrCH data in the form of a memory slot having a header portion and a data portion, the header portion including an indication of the address in the memory of the next timeslot of data.

4. The method of claim 3 wherein the header portion also includes an indication of the number of bits of CCTrCH data in the timeslot.

5. The method of claim 3 wherein the header portion also includes an indication of the status of the memory slot.

6. The method of any preceding claim wherein the step of processing comprises storing in a buffer an indication of the CCTrCH for which complete data has been received.

7. An arrangement for processing of CCTrCH data in a UMTS system, comprising:

means for receiving CCTrCH data across a plurality of timeslots;

means for storing the received CCTrCH data; and

means for, upon receipt of complete data for a CCTrCH, processing the stored CCTrCH data through channel processing asynchronously to individual received timeslots.

8. The arrangement of claim 7 wherein the means for storing the received CCTrCH data comprises means for storing the received CCTrCH data in memory in link-list form, whereby each timeslot of received CCTrCH data can be independently accessed in the memory.

9. The arrangement of claim 8 wherein the means for storing the received CCTrCH data comprises means for storing each timeslot of received CCTrCH data in the form of a memory slot having a header portion and a data portion, the header portion including an indication of the address in the memory of the next timeslot of data.

10. The arrangement of claim 9 wherein the header portion also includes an indication of the number of bits of CCTrCH data in the timeslot.

11. The arrangement of claim 9 wherein the header portion also includes an indication of the status of the memory slot.

12. The arrangement of any one of claims 7 to 11 wherein the means for processing comprises a buffer for storing an indication of the CCTrCH for which complete data has been received.

13. User equipment for use in a UMTS system, the user equipment comprising the arrangement of any one of claims 7 to 12.

14. A base station for use in a UMTS system, the base station equipment comprising the arrangement of any one of claims 7 to 12.

15. A computer program element comprising computer program means for performing substantially the method of any one of claims 1 to 6.

16. An integrated circuit comprising the arrangement of any one of claims 7 to 12.

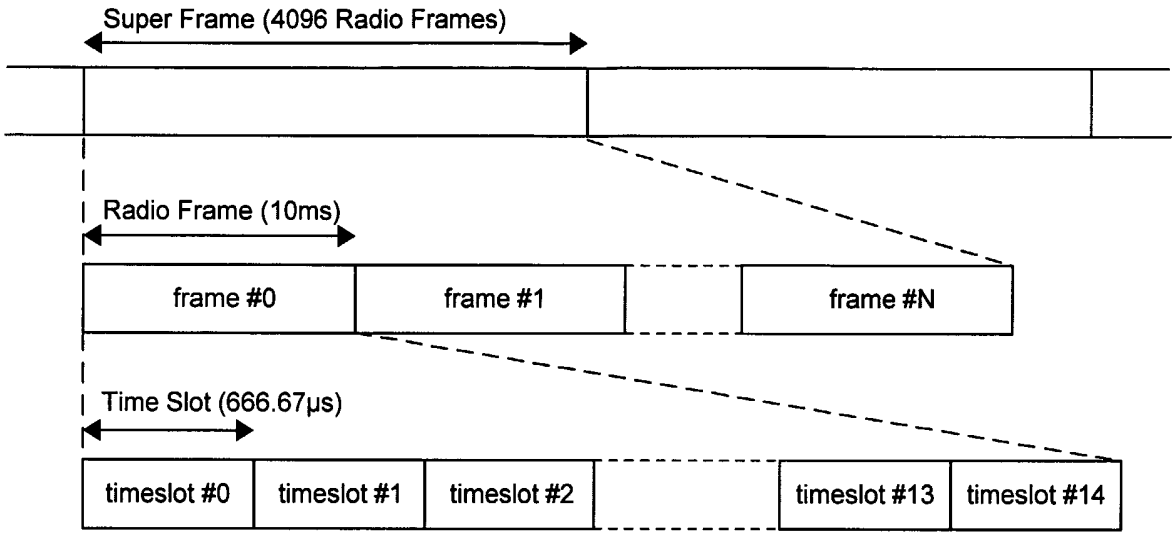
Super Frame (4096 Radio Frames)
Radio Frame (10ms)
frame #0
frame #1
frame #N
Time Slot (666.67μs)
timeslot #0
timeslot #1
timeslot #2
timeslot #13
timeslot #14

FIG. 1

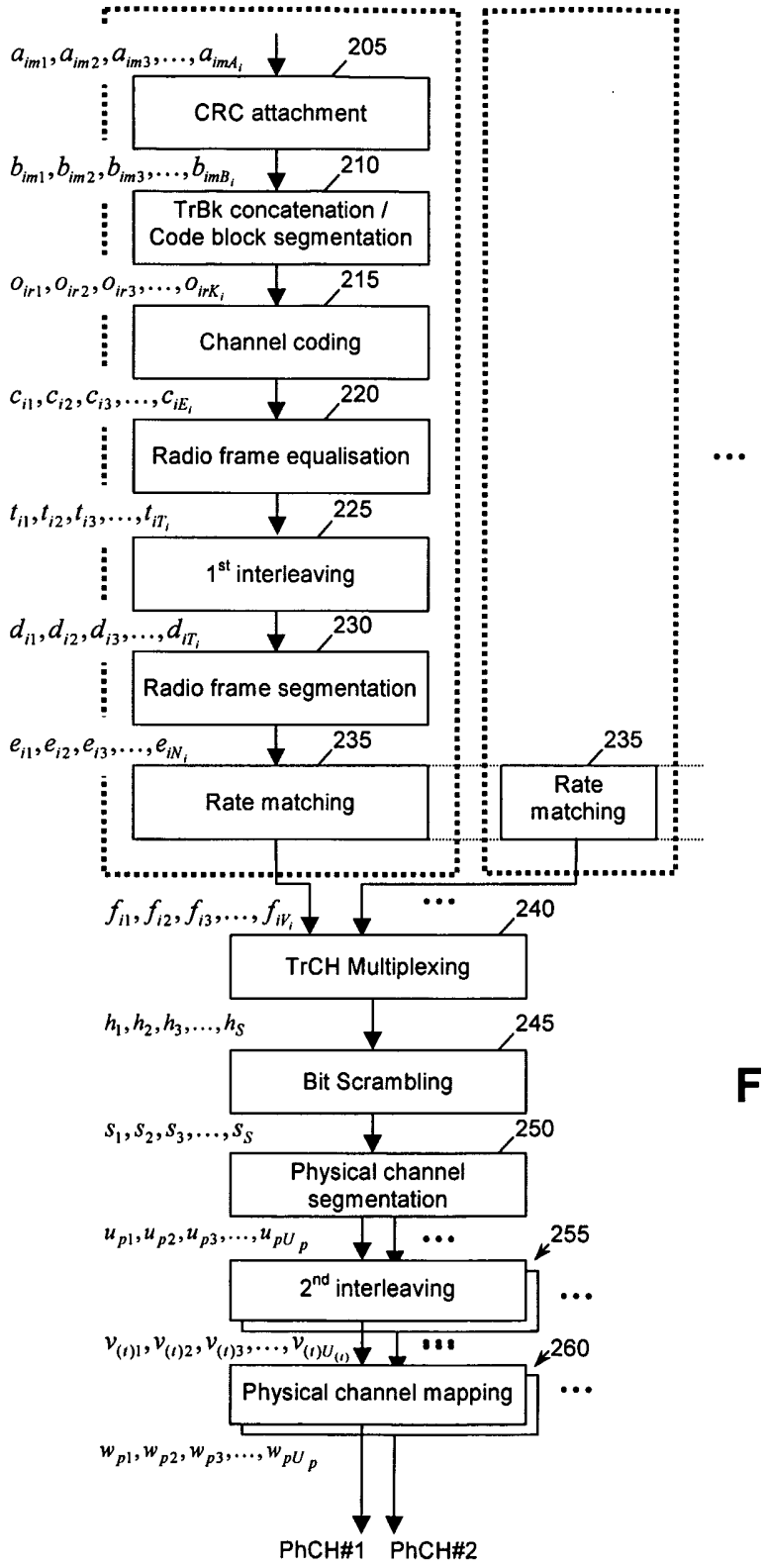
$a_{im1}, a_{im2}, a_{im3}, \ldots, a_{imA_i}$
205
CRC attachment
$b_{im1}, b_{im2}, b_{im3}, \ldots, b_{imB_i}$
210
TrBk concatenation / Code block segmentation
$o_{ir1}, o_{ir2}, o_{ir3}, \ldots, o_{irK_i}$
215
Channel coding
$c_{i1}, c_{i2}, c_{i3}, \ldots, c_{iE_i}$
220
Radio frame equalisation
$t_{i1}, t_{i2}, t_{i3}, \ldots, t_{iT_i}$
225
1st interleaving
$d_{i1}, d_{i2}, d_{i3}, \ldots, d_{iT_i}$
230
Radio frame segmentation
$e_{i1}, e_{i2}, e_{i3}, \ldots, e_{iN_i}$
235
Rate matching
235
Rate matching
$f_{i1}, f_{i2}, f_{i3}, \ldots, f_{iV_i}$
240
TrCH Multiplexing
$h_1, h_2, h_3, \ldots, h_S$
245
Bit Scrambling
$s_1, s_2, s_3, \ldots, s_S$
250
Physical channel segmentation
$u_{p1}, u_{p2}, u_{p3}, \ldots, u_{pU_p}$
255
2nd interleaving
$v_{(t)1}, v_{(t)2}, v_{(t)3}, \ldots, v_{(t)U_{(t)}}$
260
Physical channel mapping
$w_{p1}, w_{p2}, w_{p3}, \ldots, w_{pU_p}$
PhCH#1
PhCH#2

FIG. 2

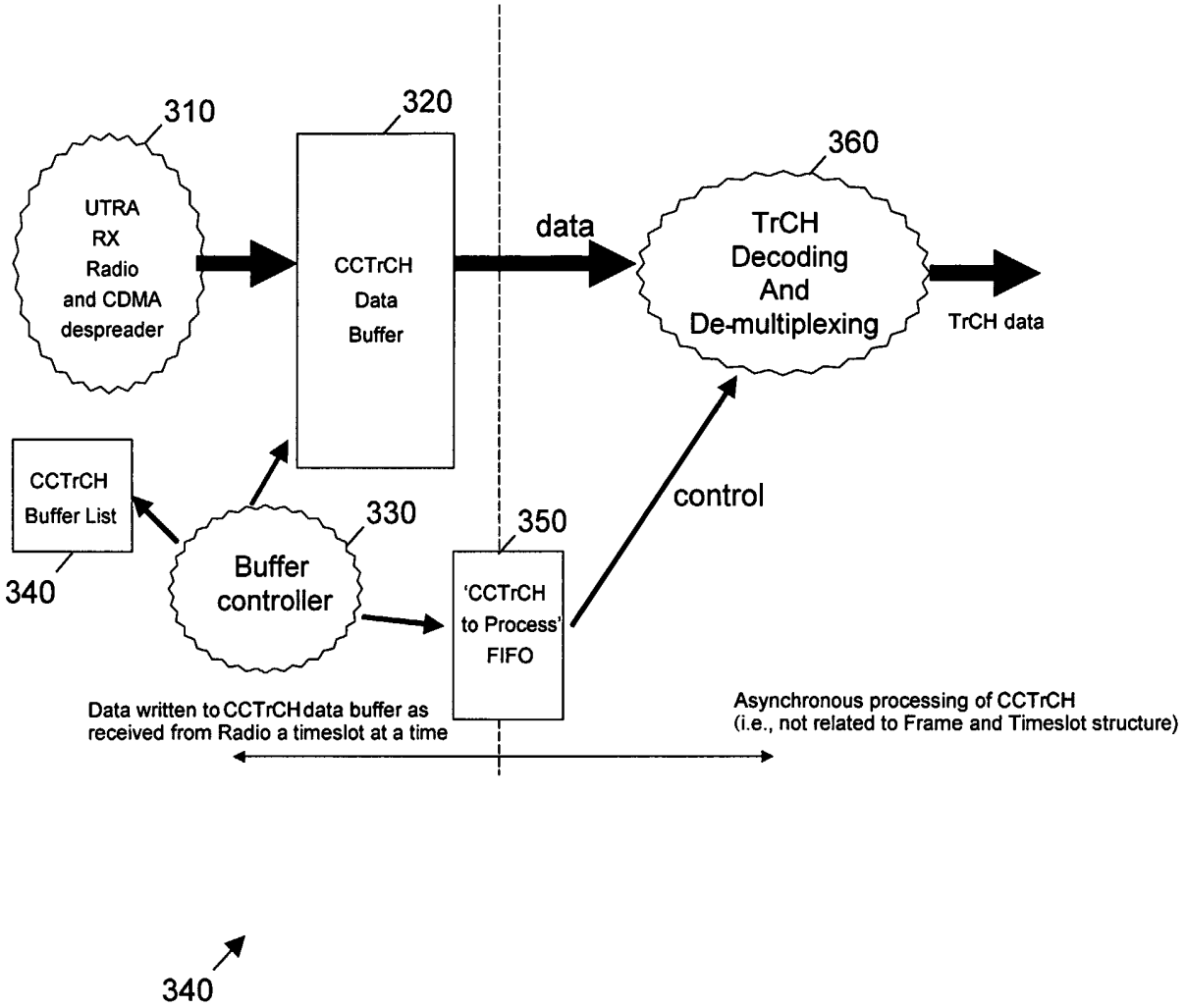
310
320
360
UTRA
RX
Radio
and CDMA
despreader
CCTrCH
Data
Buffer
data
TrCH
Decoding
And
De-multiplexing
TrCH data
CCTrCH
Buffer List
340
330
Buffer
controller
350
'CCTrCH
to Process'
FIFO
control
Data written to CCTrCH data buffer as
received from Radio a timeslot at a time
Asynchronous processing of CCTrCH
(i.e., not related to Frame and Timeslot structure)
340

FIG. 3

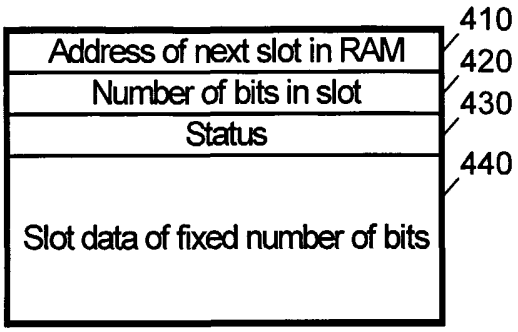
410
Address of next slot in RAM
420
Number of bits in slot
430
Status
440
Slot data of fixed number of bits

FIG. 4

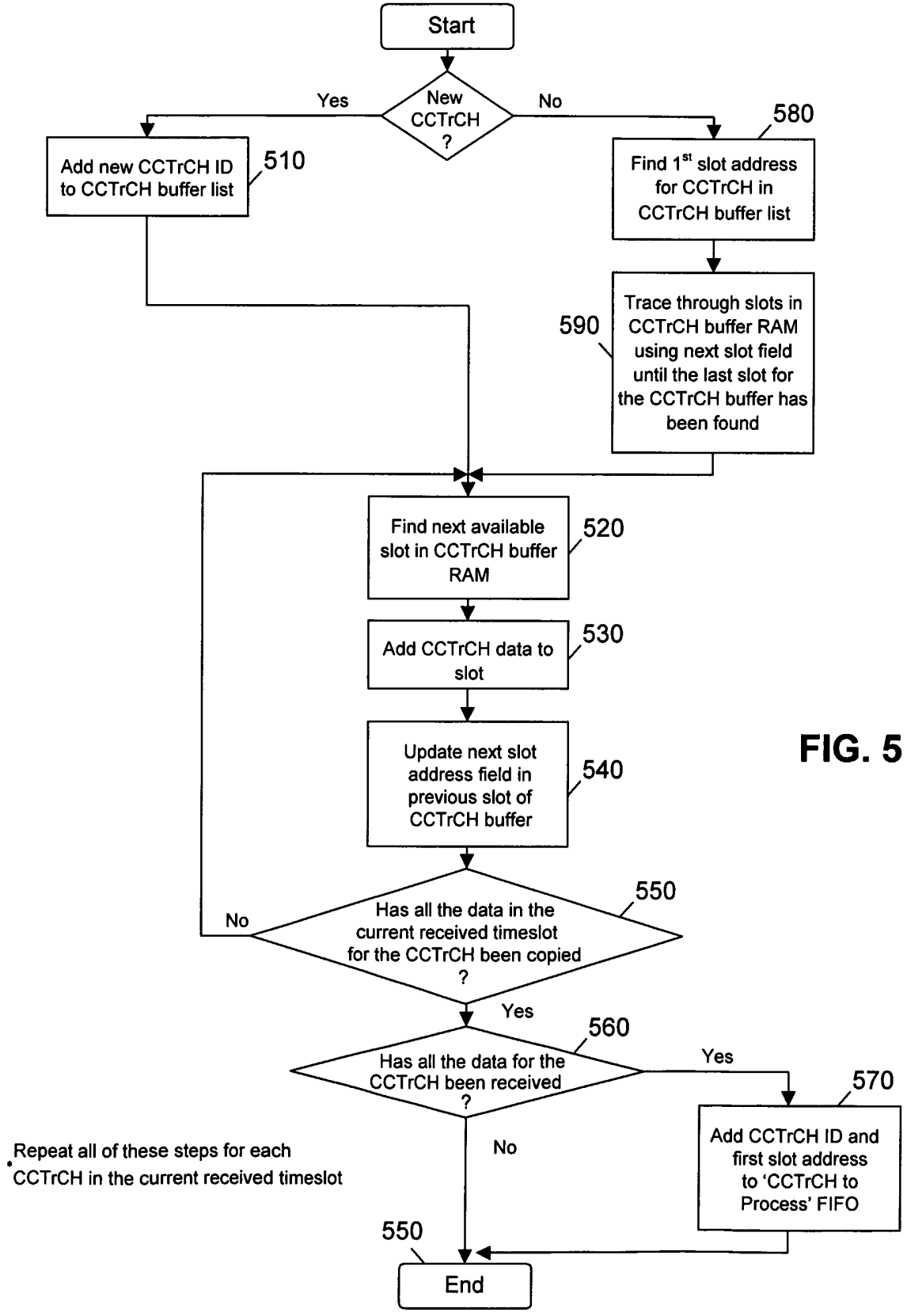
Start
New CCTrCH ?
Yes
No
Add new CCTrCH ID to CCTrCH buffer list
510
Find 1st slot address for CCTrCH in CCTrCH buffer list
580
Trace through slots in CCTrCH buffer RAM using next slot field until the last slot for the CCTrCH buffer has been found
590
Find next available slot in CCTrCH buffer RAM
520
Add CCTrCH data to slot
530
Update next slot address field in previous slot of CCTrCH buffer
540
Has all the data in the current received timeslot for the CCTrCH been copied ?
550
No
Yes
Has all the data for the CCTrCH been received ?
560
Yes
No
Add CCTrCH ID and first slot address to 'CCTrCH to Process' FIFO
570
Repeat all of these steps for each CCTrCH in the current received timeslot
550
End

FIG. 5

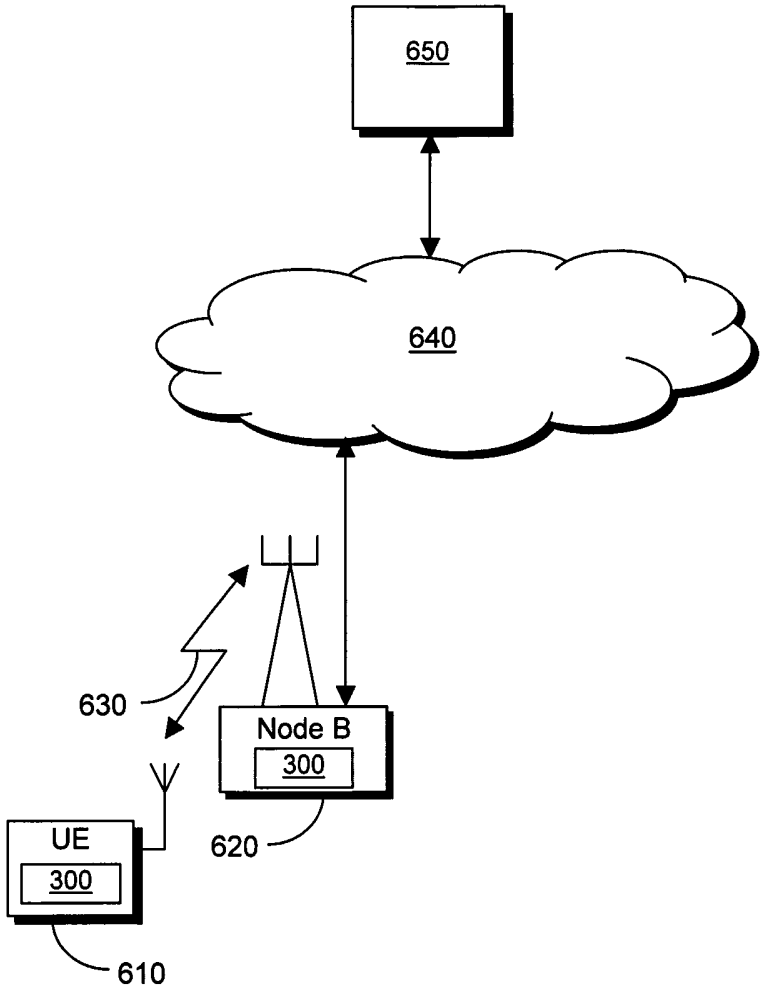

FIG. 6

INTERNATIONAL SEARCH REPORT

Internati Application No
PCT/GB 02/04731

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B1/707

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	WO 02 21715 A (QUALCOMM INC) 14 March 2002 (2002-03-14) page 9, line 15 -page 10, line 34 page 13, line 28 -page 15, line 12 page 17, line 25 - line 34 page 20, line 1 -page 22, line 28; figures 3,6	1-16
A	EP 0 758 168 A (NIPPON TELEGRAPH & TELEPHONE) 12 February 1997 (1997-02-12) claims 41,43,44,50,51; figure 6B	1-16
A	EP 0 998 052 A (HITACHI LTD) 3 May 2000 (2000-05-03) paragraphs '0024!,'0026!,'0027!,'0044!,'0045!; figures 1,5	1-16

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
29 January 2003	05/02/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Sorrentino, A

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 5 862 189 A (DELARUELLE ANTOINE ET AL) 19 January 1999 (1999-01-19) abstract; figure 2 column 2, line 1 - line 31 column 10, line 40 -column 11, line 51 column 14, line 53 - line 64	1-16

INTERNATIONAL SEARCH REPORT

Inf ation on patent family members

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