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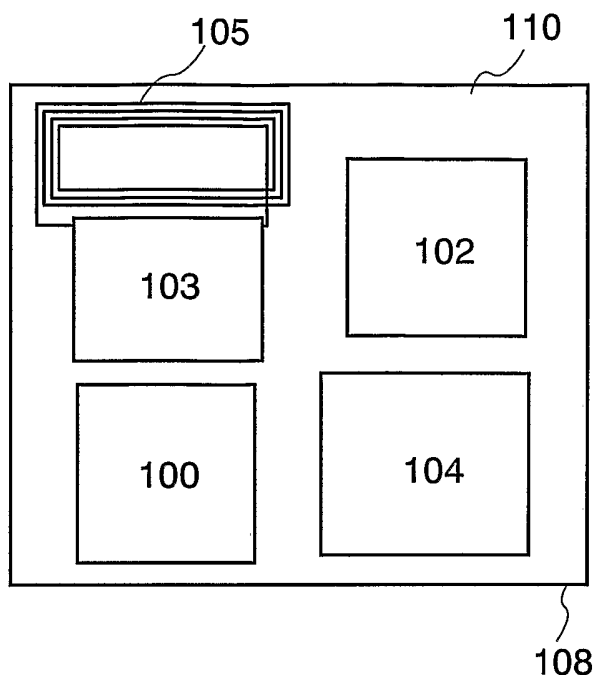
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(54) Title: SEMICONDUCTOR DEVICE AND COMMUNICATION SYSTEM



(57) Abstract: It is an object of the present invention to provide a semiconductor device in which a sophisticated integrated circuit using a polycrystalline semiconductor is formed over a substrate which is weak with heat such as a plastic substrate or a plastic film substrate and a semiconductor device which transmits/receives power or a signal without wires, and a communication system thereof. One feature of the invention is that a semiconductor device, specifically, a processor, in which a sophisticated integrated circuit is fixed to a plastic substrate which is weak with heat by a stripping method such as a stress peel of process method to transmit/receive power or a signal without wires, for example, with an antenna or a light receiving element.

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DESCRIPTION

SEMICONDUCTOR DEVICE AND COMMUNICATION SYSTEM

5 TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device in which a plastic material is used for a substrate and an integrated circuit is formed using a thin film transistor thereover, specifically, a processor. Moreover, the invention relates to a communication system having
10 the semiconductor device.

BACKGROUND ART

[0002]

A liquid crystal display panel, in which a pixel portion and a driver circuit are
15 integrated over the same glass substrate utilizing a thin film transistor (hereinafter, also referred to as a "TFT") using a crystalline semiconductor film having a thickness of several ten nanometers, is developed. Further, technique for manufacturing a CPU (Central Processing Unit) having a function as a center of a computer using high-performance polycrystalline silicon which is superior in a crystalline property, is reported (For example,
20 refer to Non-Patent Document 1: Imaya, A., "CG Silicon technology and its application", AM-LCD 2003 Digest, p.1, 2003 and Non-Patent Document 2: Lee, B.Y., et al., "A CPU on a glass substrate using CG-Silicon TFTs", ISSCC Digest, p. 164, 2003). According to such technical progress, feasibility of a system panel integrating a display function and a function of a computer realized by a CPU over a glass substrate has been increased.

25 [0003]

A liquid crystal display panel is applied as a display means attached to various electronic devices and a study of using plastic or a plastic film as a substrate for a display substrate mainly used as a portable electronic device has been advanced. A plastic material has a feature capable of being thinned since the plastic material has low specific gravity,
30 lightweight, and has high impact resistance compared with glass.

[0004]

However, a plastic material is generally poor in heat resistance; therefore, a highest temperature of processing is required to be lowered and a high-quality crystalline semiconductor film has not been able to be formed even today. Hence, a system panel as described above had not been able to be realized.

5

DISCLOSURE OF INVENTION

[0005]

In view of the foregoing backgrounds, it is an object of the present invention to provide a semiconductor device in which a sophisticated integrated circuit using a polycrystalline semiconductor is formed over a substrate which is weak with heat such as a plastic substrate or a plastic film substrate and a semiconductor device which transmits/receives power or a signal without wires, and a communication system thereof.

[0006]

In view of the foregoing problems, one feature of the invention is that a semiconductor device, specifically, a processor, in which a sophisticated integrated circuit is fixed to a plastic substrate which is weak with heat by a stripping method such as a stress peel of process (hereinafter, also referred to as a SPOP) method to transmit/receive power or a signal without wires, for example, with an antenna or a light receiving element.

[0007]

One specific mode of the invention is a semiconductor device which comprises an integrated circuit and an antenna, wherein the integrated circuit has a transistor over a plastic substrate, and a semiconductor film of the transistor has a thickness of from 10 nm to 200 nm.

[0008]

Another mode of the invention is a semiconductor device which comprises an integrated circuit and a light receiving element, wherein the integrated circuit has a transistor fixed to a plastic substrate, and a semiconductor film of the transistor has a thickness of from 10 nm to 200 nm.

[0009]

For example, a thin film transistor can be used for a transistor in which at least a channel formation region is formed from an island-shaped semiconductor film which has a film thickness of from 10 nm to 200 nm.

[0010]

One kind selected from polycarbonate, polyarylate, and polyethersulfone can be used for the plastic substrate.

[0011]

5 A semiconductor device mounted with such an antenna can provide a communication system which receives power or a signal from a reader/writer device without wires, specifically, with an antenna. Further, a semiconductor device mounted with a light receiving element can also provide a communication system which receives power or a signal from a reader/writer device without wires, specifically, with an antenna or a light receiving element.

10 [0012]

According to the invention, poor connection or the like of a connector can be eliminated by transmitting/receiving power or a signal without wires. Further, a problem with handling or the like due to a wiring connecting each of the devices can be eliminated. Thus, an added value of a processor can be enhanced by transmitting/receiving power or a signal without wires. A battery or the like is not required to be mounted since power can be received without wires, and thus, a further lightweight electronic device can be achieved.

[0013]

According to the invention, a semiconductor device, specifically, a processor, which is superior in impact resistance or flexibility can be obtained by forming a sophisticated integrated circuit such as an arithmetic means over a plastic substrate.

20

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIGS. 1A and 1B are views showing a processor of the present invention;

25 FIGS. 2A to 2E are views showing a step for manufacturing a processor of the invention;

FIGS. 3A and 3B are views showing a step for manufacturing a processor of the invention;

30 FIG. 4 is a view showing a structure of a thin film transistor which a processor of the invention has;

FIG. 5 is a view showing a structure of a thin film transistor which a processor of the

invention has;

FIGS. 6A and 6B are views showing a usage mode of a processor of the present invention;

FIG. 7 is a diagram showing an arithmetic processing means which a processor of the
5 invention has;

FIG. 8 is a diagram showing an arithmetic processing means which a processor of the invention has;

FIG. 9 is a diagram showing an arithmetic processing means which a processor of the invention has;

10 FIGS. 10A and 10B are views showing a car mounted with a processor of the invention;

FIGS. 11A and 11B are views showing a usage mode of a processor of the present invention;

15 FIGS. 12A and 12B are an electronic device mounted with a processor of the invention; and

FIG. 13 is a diagram showing an arithmetic processing means which a processor of the invention has.

BEST MODE FOR CARRYING OUT THE INVENTION

20 [0014]

Hereinafter, embodiment modes according to the present invention are described in detail with reference to the drawings. However, it is easily understood by those who are skilled in the art that embodiments and details herein disclosed can be modified in various ways without departing from the purpose and the scope of the present invention. Therefore,
25 it should be noted that the description of embodiment modes to be given below should not be interpreted as limiting the present invention. Further, through the whole drawings of the embodiment modes, portions having like components or similar functions are denoted by like numerals and will not be further explained.

[0015]

30 (Embodiment Mode 1)

In this embodiment mode, a configuration of a processor is described.

[0016]

FIG. 1A shows a processor 108 having an arithmetic processing means (that serves as a so-called CPU) 100, a storage means 102, a power supply circuit 103, an interface (I/F) 104, and an antenna 105. A memory can be used for the storage means 102, for example, ROM,
5 RAM, SRAM, or a nonvolatile memory. The antenna 105 is connected to the power supply circuit 103, then power received from the antenna is inputted to the power supply circuit 103, and then the power can be supplied to the arithmetic processing means 100, the storage means 102, and the interface (I/F) 104.

[0017]

10 According to the processor 108 shown in FIG. 1A, poor connection or the like of a connector can be eliminated by transmitting/receiving power or a signal without wires, specifically, with an antenna. Further, a problem with handling or the like due to the state of the processor provided with a number of wirings can be eliminated. Thus, an added value of a processor can be enhanced by transmitting/receiving power or a signal without wires.

15 [0018]

The arithmetic processing means 100, the storage means 102, the power supply circuit 103, and the interface (I/F) 104 (these correspond to a sophisticated integrated circuit) are formed so as to have an element formation region having a transistor in which at least a channel formation region is formed by an island-shaped semiconductor film which is formed
20 over an insulating surface 110 to have a film thickness of from 10 nm to 200 nm. Specifically, a thin film transistor (TFT) can be used as a transistor.

[0019]

FIG. 1B illustrates a configuration of a processor in the case of receiving a signal using light. A configuration shown in FIG. 1B is required to receive light and therefore has a
25 light receiving element 120 in addition to the configuration of FIG. 1A. A photodiode formed over the insulating surface 110 can be used for the light receiving element 120. The photodiode can be manufactured through the same step as that of the thin film transistor. The processor 108 shown in FIG. 1B can receive a signal using the light receiving element 120 and can receive power using the antenna 105. Consequently, a signal and power can be
30 separately received; therefore, the load of each circuit and the load of signal processing can be reduced. Thus, the processor 108 enables to receive a number of signals.

[0020]

According to the processor shown in FIG. 1B, poor connection or the like of a connector can be eliminated in the similar way as in FIG. 1A. Further, a problem with handling or the like due to the state of the processor provided with a number of wirings can be eliminated. Thus, an added value of a processor can be enhanced by transmitting/receiving power or a signal without wires.

[0021]

In the processor shown in FIGS. 1A and 1B, a sophisticated integrated circuit is formed using a polycrystalline semiconductor film by a SPOP method without being limited by a process temperature, then, the sophisticated integrated circuit is directly stripped to be fixed over a plastic substrate or a plastic film substrate; therefore, an initial performance of an integrated circuit is not detracted. Consequently, lightweight is attained and a processor which is superior in impact resistance can be obtained. Such a processor provided with a number of sophisticated integrated circuits is referred to as a systematized processor.

[0022]

The sophisticated integrated circuit of the invention is not limited to a thin film transistor manufactured by a SPOP method. A thin film transistor may be manufactured by forming a polycrystalline semiconductor film over a plastic substrate or a plastic film substrate with continuous oscillation laser (CW laser) irradiation or pulsed oscillation laser (pulse laser) irradiation. For example, by means of a stripping method other than a SPOP method, a stripping layer formed over a glass substrate may be eliminated by laser irradiation, and an element formation region may be fixed over a plastic substrate or a plastic film substrate. Further, a glass substrate may be eliminated by etching or the like and an element formation region may be fixed over a plastic substrate or a plastic film substrate.

[0023]

Next, an example of a configuration of the arithmetic processing means 100 is described. In this embodiment mode, the arithmetic processing means 100 having a RISC configuration is taken as an example. A RISC configuration has a simple configuration since the number of clocks per one instruction is determined compared with a CISC configuration. Further, a RISC configuration has a feature of carrying out pipeline processing.

[0024]

FIG. 7 shows an arithmetic processing means 100 having integer arithmetic units: an ALU1 (201) and an ALU2 (202), a load store unit (218), a branch prediction unit (209), and floating point arithmetic units: a FPU1 (203) and FPU2 (204) as an execution unit (200), and further having a general register (215), a primary data cache (206), a data cache controller (216), an instruction cache controller (217), a primary instruction cache (211), a bus interface (212), and a second cache (213).

[0025]

In such the arithmetic processing means 100, the ALU1 (201) and the ALU2 (202) perform integer arithmetic, and the FPU1 (203) and the FPU2 (204) perform floating point arithmetic. Each of an arithmetic result is stored in the general register (215). The instruction cache controller (217) controls an instruction fetch and a decode from an external memory, and the primary instruction cache (211). Branch prediction is performed according to the branch prediction unit (209). The data cache controller (216) controls the flow of data among an external bus, the primary data cache (206), and the load store unit (218). The bus interface (212) is an interface portion between the external bus and an inside of a CPU. In this embodiment mode, a configuration provided with the second cache (213) is used; however, the second cache (213) is not always required.

[0026]

The arithmetic processing means 100 shown in FIG. 7 is a comparatively simple configuration as a CPU; therefore, an area in which the arithmetic processing means is occupied can be reduced and low power consumption can be attained. As a result, the arithmetic processing means is preferably used for a small-sized semiconductor device such as an ID chip.

[0027]

FIG. 8 shows a configuration of an arithmetic processing means 100 which has a different configuration from that of FIG. 7. FIG. 8 shows the arithmetic processing means 100 having integer arithmetic units: an ALU1 (201) and an ALU2 (202), floating point arithmetic units: a FPU1 (203) and a FPU2 (204), and a memory interface (memory IF) (205) as an execution unit (200), and further having a primary data cache (206), a reservation station (207), an instruction decoder (208), a branch prediction unit (209), an instruction fetch unit (210), a primary instruction cache (211), a bus interface (212), and a second cache (213).

The arithmetic processing means 100 shown in FIG. 8 has a feature of being provided with the reservation station 207.

[0028]

In such the arithmetic processing means 100, the ALU1 (201) and the ALU2 (202) perform integer arithmetic, and the FPU1 (203) and the FPU2 (204) perform floating point arithmetic. Each of the arithmetic result is stored in a general register (not shown). The instruction fetch unit (210) performs an instruction fetch from the primary instruction cache (211), and the instruction decoder (208) decodes an instruction based on information from the branch prediction unit (209). The reservation station (207) is a block for performing scheduling to execute the decoded instruction in the execution unit. Then, the result of the execution unit is stored in the primary data cache (206). The bus interface (212) is an interface portion between an external bus and an inside of a CPU. In this embodiment mode, a configuration provided with the second cache (213) is used; however, the second cache (213) is not always required.

15 [0029]

By providing such the reservation station (207), scheduling an instruction can be performed, the efficiency of pipeline processing can be enhanced, and operation speed can be improved.

[0030]

20 FIG. 9 shows a configuration of an arithmetic processing means 100 which has a different configuration from that of FIGS. 7 and 8. FIG. 9 shows the arithmetic processing means 100 having integer arithmetic units: an ALU1 (201) and an ALU2 (202), floating point arithmetic units: a FPU1 (203) and FPU2 (204), and a memory interface (memory IF) (205) as an execution unit (200), and further having a primary data cache (206), a reservation station (207), a primary instruction cache (211), a bus interface (212), a second cache (213), a renaming unit (220), an instruction issue unit (221), a zero-order cache (222), and a predecoder (223). A general register 215 is included in the similar way as in FIG. 7; therefore, the description is omitted. The arithmetic processing means 100 shown in FIG. 9 has a feature of being provided with the renaming unit 220 in addition to the reservation station 207 to enhance the efficiency of pipeline processing and dividing the decode of the instruction into two steps.

25

30

[0031]

In such the arithmetic processing means 100, the ALU1 (201) and the ALU2 (202) perform integer arithmetic, and the FPU1 (203) and the FPU2 (204) perform floating point arithmetic. Each of the arithmetic result is stored in a general register (not shown). The
5 predecoder (223) performs an instruction fetch from the primary instruction cache, performs predecode, and stores in the zero-order cache (222). The instruction issue unit (221) fetches a code predecoded from the zero-order cache, and decodes the code based on information of the branch prediction unit 209. The reservation station (207) performs scheduling to execute the decoded instruction in the execution unit. Based on information of the renaming unit
10 (220), an advanced optimization can be performed. Then, the result of the execution unit is stored in the primary data cache (206). The bus interface (212) is an interface portion between an external bus and an inside of a CPU. In this embodiment mode, a configuration provided with the second cache (213) is used; however, the second cache (213) is not always required.

15 [0032]

In this embodiment mode, an advanced optimization is performed by providing the renaming unit (220) as well as the reservation station (207), and high operation speed is realized by dividing the decode into two steps.

[0033]

20 A configuration of the arithmetic processing means 100 according to the invention is not limited to the configuration mentioned in any one of FIGS. 7 to 9, and an element which is not required among the above elements may be appropriately deleted, and another element may be appropriately added. Further, a known arithmetic processing means, namely a configuration of a CPU can be used. For example, a Complex Instruction Set Computer
25 (CISC) structure or a Reduced Instruction Set computer (RISC) structure can be used. FIG. 13 shows a block diagram of a CPU. The CPU is a CISC having a standard structure including an ALU (Arithmetic and Logic Unit) 1, a general register 2, an instruction analyzer 3, and the like. According to the invention, this CISC configuration of a CPU can be used. In addition, VLIW (Very Long Instruction Word) can be also employed. The width of the
30 bus may be from 8bit to 32bit, or 32bit or more.

[0034]

(Embodiment Mode 2)

In this embodiment mode, a step for manufacturing a sophisticated integrated circuit by a SPOP method with a thin film transistor as a transistor in which at least a channel formation region is formed from an island-shaped semiconductor film which has a film thickness of from 10 nm to 200 nm is described.

[0035]

First, as shown in FIG. 2A, a metal film 11 is formed over a first substrate 10. The first substrate may have rigidity capable of withstanding a subsequent stripping step, and for example, a glass substrate, a quartz substrate, a ceramic substrate, a silicon substrate, a metal substrate, or a stainless steel substrate can be used as the first substrate. A single layer formed from an element selected from W, Ti, Ta, Mo, Nd, Ni, Co, Zr, Zn, Ru, Rh, Pd, Os, and Ir, or an alloy material or a compound material containing the element as its main component, or a lamination thereof can be used as the metal film. As a method for manufacturing the metal film, for example, a sputtering method using a metal target may be used. The metal film may be formed to have a film thickness of from 10 nm to 200 nm, preferably, from 50 nm to 75 nm.

[0036]

A film formed from the above metal which is nitrided (for example, tungsten nitride or molybdenum nitride) may be used instead of the metal film. In addition, a film formed from an alloy of the above metal (for example, an alloy of W and Mo: W_xMo_{1-x}) may be used instead of the metal film. In this case, a sputtering method using a plurality of targets such as a first metal (W) and a second metal (Mo) or using a target of the alloy of a first metal (W) and a second metal (Mo) in a deposition chamber may be used. Further, nitrogen or oxygen may be added to the metal film. A metal film may be formed by ion-implanting nitrogen or oxygen therein, or a metal film may be formed by a sputtering method in a nitride atmosphere or an oxygen atmosphere in the deposition chamber or a metal film may be formed by using a nitride metal target.

[0037]

A stripping step can be controlled and a process margin can be expanded by appropriately setting a method for forming the metal film. Specifically, a heat temperature

for stripping or the necessity of the heat treatment can be controlled.

[0038]

Subsequently, a layer to be stripped 12 having an element formation region is formed over the metal film 11. In this layer to be stripped, an oxide film having silicon is stacked so as to be in contact with the metal film. The layer to be stripped may have an antenna. The layer to be stripped 12 is preferably provided with an insulating film having nitrogen, such as a silicon nitride (SiN) film or a silicon nitride oxide (SiON or SiNO) film so that the insulating film is in contact with the metal film to prevent impurities or dust from the metal film or the substrate from penetrating. The insulating film serves as a base film of the thin film transistor.

[0039]

As the oxide film having silicon, silicon oxide, silicon oxynitride, or the like may be formed by a sputtering method or a CVD method. A film thickness of the oxide film having silicon is desirably approximately twice or more that of the metal film. In this embodiment mode, the silicon oxide film is formed so as to have a film thickness of from 150 nm to 200 nm by a sputtering method using a silicon target.

[0040]

When the oxide film having silicon is formed, oxide (metal oxide) 13 having the metal is formed over the metal film. Thin metal oxide formed over the surface of the metal film by treating with an aqueous solution having sulfuric acid, hydrochloric acid, or nitric acid, an aqueous solution in which hydrogen peroxide water is mixed with sulfuric acid, hydrochloric acid, or nitric acid, or ozone water can be used as the metal oxide. Further, plasma treatment in an oxygen atmosphere or oxidation treatment which generates ozone by ultraviolet irradiation in an atmosphere containing oxygen may be carried out as other methods, and furthermore, the metal oxide may be formed by heating at a temperature of from 200°C to 350°C with a clean oven.

[0041]

The metal oxide may be formed to have a film thickness of from 0.1 nm to 1 μm , preferably from 0.1 nm to 100 nm, and more preferably from 0.1 nm to 5 nm.

[0042]

The oxide film having silicon, the base film, or the like is collectively referred to as

an insulating film. In other words, a metal film, metal oxide, an insulating film, and a semiconductor film are stacked. In addition, the metal film and the metal oxide film can be referred to as a stripping layer.

[0043]

5 A semiconductor element, for example, a thin film transistor (TFT) in which at least a channel formation region is formed from an island-shaped semiconductor film which has a film thickness of from 10 nm to 200 nm is formed by performing a predetermined manufacturing step on a semiconductor film. This semiconductor element includes the arithmetic processing means 100, the storage means 102, the power supply circuit 103, and the interface (I/F) 104. An insulating film containing carbon such as DLC or carbon nitride (CN) or an insulating film containing nitrogen such as silicon nitride (SiN) or silicon nitride oxide (SiNO or SiON) is preferably provided as a protective film which protects the semiconductor element.

[0044]

15 After forming the above layer to be stripped 12, specifically, after forming the metal oxide, heat treatment is appropriately carried out to crystallize the metal oxide. For example, in the case of using W (tungsten) for the metal film, the metal oxide of WO_2 or WO_3 becomes a crystal condition when heat treatment is carried out at a temperature of 400°C or more. In such the heat treatment, a temperature or the necessity of the heat treatment may be determined according to the metal film to be selected. In other words, the metal oxide may be crystallized according to need to strip easily.

[0045]

25 In the case where heating is performed after forming a semiconductor film of the layer to be stripped 12, hydrogen in the semiconductor film can be diffused. There is a case that valence of the metal oxide varies due to this hydrogen.

[0046]

30 Further, the number of steps for manufacturing a semiconductor element may be reduced by using the heating step both as a manufacturing step of a semiconductor element and a heating step. For example, heat treatment can be performed with a heating oven or laser irradiation in the case of forming a crystalline semiconductor film.

[0047]

Then, the layer to be stripped 12 is pasted to a support substrate 14 with a first adhesive agent 15. A substrate having higher rigidity than that of the first substrate 10 is preferably used for the support substrate 14. An adhesive agent which can be stripped, for example, an ultraviolet stripping type adhesive agent which is stripped by ultraviolet, a heat stripping type adhesive agent which is stripped by heat, a water-soluble adhesive agent which is stripped by water, a two-sided tape, or the like may be used for the first adhesive agent 15.

[0048]

Then, the first substrate 10 provided with the metal film 11 is stripped by a physical means (FIG. 2C). Although the figure is not shown since it is a schematic view, the first substrate is separated within layers of the crystallized metal oxide, or at an interface between the metal oxide and the metal film or at an interface between the metal oxide and the layer to be stripped. Thus, the layer to be stripped 12 can be stripped from the first substrate 10.

[0049]

At this time, it is preferably that a part of the substrate is cut to scratch the vicinity of an stripping interface, namely the interface of the metal film and the metal oxide film therebetween with a cutter or the like in order to perform stripping easily.

[0050]

And then, as shown in FIG. 2D, the layer to be stripped 12 which is stripped is pasted and fixed to a second substrate (for example, a plastic substrate) 17 which is to be a transcriptional body with a second adhesive agent 16. An ultraviolet cured resin, specifically, an epoxy resin based adhesive agent or an adhesive agent such as a resin additive; a two-sided tape; or the like may be used for the second adhesive agent 16. In the case where the second substrate has an adhesive property, the second adhesive agent is not required.

[0051]

A plastic material or the like such as polyethylene terephthalate, polycarbonate, polyarylate, or polyethersulfone can be used for the second substrate. Such the second substrate is referred to as a plastic substrate. Such the plastic substrate has flexibility and is lightweight. Irregularity of the surface may be reduced, and rigidity, resistance, and stability may be enhanced by performing coating treatment on the plastic substrate.

[0052]

Then, the first adhesive agent 15 is removed to strip the support substrate 14 (FIG.

2E). Specifically, ultraviolet irradiation, heating, or washing may be carried out to strip the first adhesive agent.

[0053]

Further, removing the first adhesive agent and curing the second adhesive agent may be carried out in one step. For example, in the case where a pair of a heat stripping type resin and a heat curing type resin, or a pair of an ultraviolet stripping type resin and an ultraviolet curing resin are used for a pair of the first adhesive agent and the second adhesive agent, respectively, the removing and curing can be carried out by one time heating or ultraviolet irradiation.

10 [0054]

The sophisticated integrated circuit fixed to the plastic substrate can be formed as described above.

[0055]

15 There is a case that the metal oxide 13 is wholly removed from the sophisticated integrated circuit or a case that a part or most of the metal oxide 13 is dotted (remains) in the lower surface of the layer to be stripped. In the case where the metal oxide 13 remains, the layer to be stripped may be fixed to the plastic substrate after removing by etching or the like. In this case, the oxide film having silicon may be removed.

[0056]

20 The sophisticated integrated circuit of the invention is formed using an island-shaped semiconductor film which has a film thickness of from 10 nm to 200 nm, while a film thickness of an IC manufactured with a silicon wafer is approximately 50 μm ; therefore, the sophisticated integrated circuit becomes extremely thin. As a result, a processor of the invention can be formed to be extremely thin, flexible, and lightweight. Consequently, a processor which is superior in impact resistance and flexibility can be obtained.

25 [0057]

Further, backgrinding which causes a crack or the trace of polishing is not required unlike the IC manufactured with a silicon wafer, and the variation of the thickness is approximately several hundred nm at most since the variation depends on the variation of the semiconductor film or the like at the time of depositing, and thus, the variation can be drastically reduced compared with the variation of from several to several ten μm by

30

backgrinding.

[0058]

A substrate provided with an element formation region can be reused by a SPOP method as described above, and consequently, the price per one processor can be reduced.

5 Further, the substrate provided with an element formation region is not required to transmit laser light; therefore, the degree of freedom of design can be increased.

[0059]

(Embodiment Mode 3)

10 Even in a SPOP method using a metal film, a stripping layer which can be selectively removed is formed and the stripping layer is removed. And then, an element formation region may be fixed over a plastic substrate or a plastic film substrate. In this embodiment mode, the case where the stripping layer is selectively removed is described.

[0060]

15 As shown in FIG. 3A, a stripping layer 30 and a layer to be stripped having an element formation region 31 are sequentially formed over an insulating surface 110. The element formation region 31 has an arithmetic processing means 100, a storage means 102, a power supply circuit 103, an interface (I/F) 104, and an antenna 105. A manufacturing method or a structure of the layer to be stripped having the element formation region 31 is the same as that of Embodiment Mode 2; therefore, the description is omitted.

20 [0061]

The stripping layer 30 may be a film having silicon, and the state may be any one of an amorphous semiconductor, a semi-amorphous semiconductor (also referred to as SAS) in which an amorphous state and a crystal state is mixed, and a crystalline semiconductor. SAS includes a microcrystal semiconductor in which a crystal grain of from 0.5 nm to 20 nm can be
25 observed in an amorphous semiconductor. These stripping layers 30 can be formed by a sputtering method, a plasma CVD method, or the like. The stripping layer 30 may have a film thickness of from 30 nm to 1 μm , and the film thickness can be 30 nm or less if the thin film formation limit of a deposition device of the stripping layer allows.

[0062]

30 An element such as phosphorous or boron may be added to the stripping layer 30. The element may be activated by heat or the like. The reaction speed of the stripping layer,

namely an etching rate can be improved by adding the element.

[0063]

As for the layer to be stripped, an insulating film is formed in a region being in contact with the stripping layer 30 so that the element formation region 31 is not etched. The insulating film can serve as a base film of a thin film transistor. A single layer structure of an insulating film having oxygen or nitrogen such as silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y) ($x>y$), or silicon nitride oxide (SiN_xO_y) ($x>y$) ($x, y=1, 2 \dots$), or a lamination thereof can be used for the insulating film. For example, in the case of using lamination of three layers, a silicon oxide film can be used as a first insulating film; a silicon oxynitride film, as a second insulating film; and a silicon oxide film, as a third insulating film. The silicon oxynitride film is preferably used for these insulating films considering impurity diffusion from the insulating surface 110 or the like; however, there is concern that the silicon oxynitride film has low adhesion between the stripping layer and a semiconductor film of a TFT. Therefore, a lamination of three layers provided with a silicon oxide film having high adhesion between the stripping layer, the semiconductor film, and the silicon oxynitride film may be used.

[0064]

In the above state, a groove 32, a hole, or the like exposing the stripping layer 30 is formed other than the element formation region 31, and an etching agent 35 is introduced into the groove 32, the hole, or the like. For example, a support substrate 33 provided with the hole 34 or the like is fixed to the insulating surface 110, and then, the etching agent 35 is introduced into the hole 34 and the groove 32 as shown in FIG. 3B. Consequently, the stripping layer 30 can be removed.

[0065]

Gas or liquid containing halogen fluoride can be used as an etching gas. For example, ClF_3 (chlorine trifluoride) can be used as halogen fluoride. The stripping layer 30 is selectively etched with such the etching gas. More specifically, the stripping layer can be removed using a low pressure CVD device in the following condition: a temperature is 350°C ; a flow of ClF_3 is 300 sccm; a pressure is 6 Torr; and time is 3 hours.

[0066]

Thus, the stripping layer 30 is removed and the insulating layer 110 is stripped. And

then, the element formation region 31 can be fixed over a plastic substrate or a plastic film substrate.

[0067]

Even in the case of selectively removing the stripping layer as described above, the substrate provided with the element formation region 31 can be reused. Consequently, the price per one processor can be reduced. Further, the substrate provided with an element formation region is not required to transmit laser light; therefore, the degree of freedom of design can be increased.

[0068]

10 (Embodiment Mode 4)

In this embodiment mode, a structure of a TFT is described.

[0069]

FIG. 4 shows one example to which a top-gate TFT is applied. A stripping layer 30 and first insulating films 36 and 301 which are stacked are formed over a first substrate 110 corresponding to an insulating surface, and an element formation region, namely an element formation layer 45 is provided thereover. At least the first insulating film 301 serves as a base film for a semiconductor film 302. A second insulating film 303 covering the semiconductor film 302 and serving as a gate insulating film is provided. A conductive film which serves as a gate electrode 304 is formed over the second insulating film 303, and a third insulating film 305 which serves as a protective layer and a fourth insulating film 306 which serves as an interlayer insulating film are provided thereover. Further, a fifth insulating layer 308 which serves as a protective layer may be formed on the upper side of the insulating film 306.

[0070]

25 The semiconductor film 302 is formed from a semiconductor having a crystalline structure (crystalline semiconductor), and a non-single crystal semiconductor or a single crystal semiconductor can be used. Especially, a crystalline semiconductor in which an amorphous semiconductor or a microcrystal semiconductor is crystallized by laser light irradiation, a crystalline semiconductor crystallized by heat treatment, or a crystalline semiconductor crystallized by combining heat treatment and laser light irradiation is preferably applied. A crystallization method using a metal element such as nickel having an

30

enhancing property for crystallizing a silicon semiconductor can be applied to heat treatment.

[0071]

In the case of crystallizing by laser light irradiation, the semiconductor film can be crystallized by continuous oscillation laser light irradiation. In addition, the semiconductor film can be crystallized while continuously moving a molten zone, in which the semiconductor film is molten, in a direction of the laser light irradiation by irradiation with a high repetition rate intense pulsed light having a repetition rate of 10 MHz or more and a pulse width of 1 nanosecond or less, preferably from 1 to 100 picoseconds. A crystalline semiconductor film having a large grain diameter and a crystal grain boundary which extends in one direction can be obtained by such a crystallization method which irradiates the semiconductor film with a laser light. Electron field effect mobility of a transistor can be enhanced by setting a moving direction of a carrier to the direction in which the crystal grain boundary extends. Electron field effect mobility of $400 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more can be enhanced.

[0072]

As described above, in the case of forming the stripping layer 30 from tungsten (W), heat treatment at a temperature of 400°C or more is required to strip without failing at an interface between the stripping layer and the layer to be stripped 12. The heating step can be used together with heat crystallization step of the semiconductor film.

[0073]

The gate electrode 304 can be formed from a polycrystalline semiconductor to which metal or one conductive type impurity is added. In the case of using metal, tungsten (W), molybdenum (Mo), titanium (Ti), tantalum (Ta), aluminum (Al), or the like can be used. In addition, metal nitride in which the above metal is nitrated can be used. A structure of stacking a first layer formed from the metal nitride and a second layer formed from the metal may be used. In the case of using a lamination structure, a so-called hat shape in which the edge portion of the first layer protrudes beyond the edge portion of the second layer may be used. At this time, barrier metal can be formed by forming the first layer from metal nitride. In other words, the metal in the second layer can be prevented from diffusing into the second insulating film 303 or the semiconductor film 302 which is the lower layer of the second insulating film 303.

[0074]

Various structures such as a single drain structure, an LDD (Low concentration drain) structure, or a Gate Overlapped LDD structure can be applied to a transistor formed by combining the semiconductor film 302, the second insulating film 303, the gate electrode 304, and the like. In addition, a single-gate structure, a multigate structure in which transistors, to which gate voltage of the same electric potential equivalently is applied, are connected in series, or a dual-gate structure in which a semiconductor film is interposed with gate electrodes from above and below can be applied.

[0075]

The fourth insulating layer 306 can be formed from an inorganic insulating material such as silicon oxide or silicon oxynitride or an organic insulating material such as an acrylic resin or a polyimide resin. In the case of using a coating method such as spin coating or roll coating, silicon oxide formed by coating an insulating film material dissolved in an organic solvent and then by performing heat treatment can be used. For example, an insulating layer which can be formed by forming a coating film including a siloxane bond and then by performing heat treatment at a temperature of from 200°C to 400°C can be used. When an insulating film formed by a coating method is used as the fourth insulating film 306, the surface can be planarized. An insulating film can be planarized by a reflow step. When a wiring is formed over a thusly planarized insulating film, disconnection thereof can be prevented. Further, a method for forming a wiring over the planarized insulating film can be effectively used in the case of forming a multilayer wiring.

[0076]

A wiring 307 is formed over the fourth insulating film 306. The wiring is preferably formed by a combination of a low resistant material such as aluminum (Al) and barrier metal using a high melting point metal material such as titanium (Ti) or molybdenum (Mo), such as a lamination structure of titanium (Ti) and aluminum (Al) or a lamination structure of molybdenum (Mo) and aluminum (Al). The wiring 307 can be provided so as to be intersected with a wiring formed from the same layer as that of the gate electrode 304, specifically, a scanning line. Further, a multilayer wiring structure can be formed by stacking a plurality of insulating films having the similar function to the fourth insulating film 306 and then forming a wiring over the insulating films.

[0077]

FIG. 5 shows one example of applying a bottom-gate TFT. The stripping layer 30 and the insulating film 36 are sequentially formed over the first substrate 110, and the element formation layer 45 is provided thereover. The element formation layer 45 is provided with the gate electrode 304, the second insulating film 303 which serves as a gate insulating film, the semiconductor film 302, a channel protective layer 309, the third insulating film 305 which serves as a protective layer, and the fourth insulating film 306 which serves as an interlayer insulating layer. The fifth insulating film 308 which serves as a protective layer may be formed thereover. The wiring 307 can be formed over the third insulating film 305 or the fourth insulating film 306.

10 [0078]

Thus, a thin film transistor used for a sophisticated integrated circuit may be a top-gate type or a bottom-gate type. The thin film transistor may be used by combining top-gate type and bottom-gate type. In other words, the invention is not limited to the structure of a thin film transistor.

15 [0079]

Such a stripping method of a sophisticated integrated circuit can employ Embodiment Mode 2 or 3.

[0080]

(Embodiment Mode 5)

20 In this embodiment mode, an exchange of a signal or power between a reader/writer device 400 and a processor 108 is described.

[0081]

As shown in FIG. 6A, when the processor 108 is held up over the reader/writer device 400 having an antenna 405, power is supplied from the reader/writer device 400. The power is supplied to a power supply circuit 103 through the antenna 105 in which the processor 108 has. Consequently, the processor 108 can perform arithmetic processing of the arithmetic processing means 100 or write into the storage means 102.

25 [0082]

As shown in FIG. 6B, a display means 410 may be provided for the reader/writer device 400. A light emitting device having a self-light emitting element, a liquid crystal display device, or other display device can be used as a display means. Information on the

30

processor 108 can be displayed with the display means 410.

[0083]

Such the reader/writer 400 and the processor 108 can receive power or a signal without wires. The processor 108 can transmit/receive information between the display
5 means and the processor without wires.

[0084]

Power can be supplied from a plurality of the reader/writer devices 400. Consequently, power can be appropriately obtained without running out of power even in the case of moving with carrying the processor 108.

10 [0085]

When a plurality of reader/writer device 400 is provided, the processor 108 can perform arithmetic processing by sharing. For example, in the case of performing from a first arithmetic processing to a third arithmetic processing, the processing may be made to carried out from a first reader/writer device to a third reader/writer device, respectively.

15 Thereafter, arithmetic processing is combined with the processor 108, and thus, a certain result can be obtained.

[0086]

According to the processor of the present invention, poor connection or the like of a connector can be eliminated. Further, a problem with handling or the like due to a wiring
20 connecting each of the devices can be eliminated. Thus, an added value of a processor can be enhanced by transmitting/receiving power or a signal without wires.

[0087]

This embodiment mode can be freely combined with the above embodiment modes.

[0088]

25 (Embodiment Mode 6)

In this embodiment mode, a case where a processor according to the present invention is applied to a car 150 as a vehicle is described.

[0089]

FIG. 10A shows a case where a processor 108 is mounted on the car 150. The
30 processor 108 of the invention has translucency, which is different from a processor manufactured using a silicon wafer; therefore, the processor 108 may be mounted on a

windshield of the car. Such the processor 108 can exchange power or a signal with a reader/writer device 400 provided for an external portion of the car 150.

[0090]

For example, the key of the car 150 can be unlocked or/and locked using the
5 processor 108. The fare payment in case of passing a toll road can be carried out using the processor 108. Further, security can be enhanced according to the processor 108 having a sophisticated integrated circuit of the invention. The processor 108 having a sophisticated integrated circuit of the invention can serve a number of functions.

[0091]

10 As shown in FIG. 10B, a signal can be transmitted from the processor 108 with the reader/writer device 400 mounted on the car 150. Consequently, the key of the car 150 can be unlocked or/and locked.

[0092]

In the case of carrying the processor 108 of the invention, in which power or a signal
15 is transmitted/received without wires, a problem with handling or the like due to a wiring connecting each of the devices can be eliminated.

[0093]

The description is made using a car in this embodiment mode; however, the processor of the invention may be applied to a bicycle, a motorcycle, or the like.

20 [0094]

This embodiment mode can be freely combined with the above embodiment modes.

[0095]

(Embodiment Mode 7)

25 A CPU formed over a plastic substrate can be mounted on various electronic devices, and according to this, an electronic device can be realized, in which lightweight, or small-sizing and thinning is attained. In this embodiment mode, a case where a processor according to the present invention is mounted on an electronic device is described.

[0096]

30 FIG. 11A shows a mode of mounting a processor of the invention on a display panel in which a material of liquid crystal or electroluminescence is utilized. The display panel has a pixel portion 502 which is formed using a TFT over a plastic substrate 501 and displays

information such as an image or a characteristic, and a driver circuit portion 503 for displaying by controlling a signal which is to be inputted to the pixel portion 502. The pixel portion 502 is provided with an information input means such as an input function using a touch pen, and a thin computer can be realized by mounting the processor 108 of the invention on the plastic substrate 501 or manufacturing by the same step.

[0097]

Further, a memory 506, a communication circuit 505, or an antenna 507 in an external portion of the processor 108 may be provided. Consequently, connecting lines or connecting to the internet by a new means without wires, in addition to a means without wires provided for the processor can be carried out. FIG. 11B shows a thin computer 508 provided with such a function. A glass substrate or a printed board formed from an epoxy resin or the like is not required to be used by using the plastic substrate 501 as a substrate on which the pixel portion 502 and the processor 108 of FIG. 11A are mounted; therefore, integration of a pixel portion or various circuits over one substrate, namely systemization, can be realized. Information can be inputted using a pen 510 by providing an information input means such as an input function using a touch pen for the pixel portion 502.

[0098]

FIG. 12A shows an IC card 601 on which the processor 108 of the invention is mounted, and an antenna 603 may be formed in an external portion of the processor. Consequently, communication can be performed with a reader/writer device by a new means without wires, in addition to a means without wires provided for the processor. According to the processor 108 formed over the plastic substrate of the invention, an IC card having a thickness nearly equal to a conventional magnetic prepaid card can be realized. In other words, as shown in FIG. 12B, when the processor 108 is formed to have a thickness of from 3 μm to 10 μm and films 601a and 601b formed from polyethylene terephthalate having a thickness of 0.1 μm are each pasted to the upper side and the lower side of the processor 108, an IC card having a thickness of from 0.2 mm to 0.3 mm which is almost equal to a thickness of the film, can be realized.

[0099]

According to the processor of the invention, information and communication equipment such as a computer or a telephone set mounted with the processor can be completed

as described above, and further, the processor can be applied to a commodity distribution system such as an IC tag.

[0100]

Thus, an added value of a processor, namely an electronic appliance as described above, can be enhanced by transmitting/receiving power or a signal without wires. A battery or the like is not required to be mounted since power can be received without wires, and thus, a further lightweight electronic device can be achieved.

[0101]

This embodiment mode can be freely combined with the above embodiment modes.

10 [Embodiment]

[0102]

(Embodiment 1)

In this example, an electric characteristic of a thin film transistor in the case of stripping by using a SPOP method as shown in Embodiment Mode 2 is shown.

15 [0103]

Table 1 shows an electric characteristic of an n-channel thin film transistor (channel length L/channel width W=8 μm /20 μm) before and after stripping.

[0104]

[Table 1]

20

	before transcription Vd=3.3V	after transcription Vd=3.25V
Ion[A/m] (Vg=3.3V)	4.69	3.75
Icut[$\mu\text{A}/\text{m}$]	0.18	0.19
μ (MAX) [cm^2/Vs]	413	389
S value[V/decade]	0.114	0.156
Vth[V]	1.90	1.95

25

[0105]

As shown in Table 1, an electric characteristic of an n-channel thin film transistor is not so much influenced before and after stripping.

[0106]

30

Table 2 shows an electric characteristic of a p-channel thin film transistor (channel length L/channel width W=8 μm /20 μm) before and after stripping.

[0107]

[Table 2]

5

	before transcription Vd=3.3V	after transcription Vd=3.25V
I _{on} [A/m] (V _g =3.3V)	9.93	9.70
I _{cut} [μA/m]	6.65	5.41
μ(MAX) [cm ² /Vs]	241	250
S value[V/decade]	0.109	0.107
V _{th} [V]	-0.48	-0.48

[0108]

As shown in Table 2, an electric characteristic of a p-channel thin film transistor is
10 not so much influenced before and after stripping.

This application is based on Japanese Patent Application serial No. 2004-176289 filed
in Japan Patent Office on June 14th, 2004, the entire contents of which are hereby
incorporated by reference.

CLAIMS

1. A semiconductor device comprising:

a processor being fixed to a plastic substrate by an adhesive agent, the processor

5 comprising:

an integrated circuit; and

an antenna connected to the integrated circuit,

wherein the integrated circuit comprises a thin film transistor, and

wherein a semiconductor film of the thin film transistor has a thickness of from 10

10 nm to 200 nm.

2. A semiconductor device comprising:

a processor being fixed to a plastic substrate by an adhesive agent, the processor

comprising:

15

an integrated circuit; and

a light receiving element,

wherein the integrated circuit comprises a thin film transistor, and

wherein a semiconductor film of the thin film transistor has a thickness of from 10

nm to 200 nm.

20

3. A semiconductor device according to claim 1 or claim 2, the integrated circuit comprises an arithmetic processing means having an arithmetic and logic unit and register.

4. A semiconductor device comprising:

25

an integrated circuit; and

an antenna,

wherein the integrated circuit comprises a transistor fixed to a plastic substrate, and

wherein a semiconductor film of the transistor has a thickness of from 10 nm to 200

nm.

30

5. A semiconductor device comprising:

an integrated circuit; and
a light receiving element,
wherein the integrated circuit has a transistor fixed to a plastic substrate, and
wherein a semiconductor film of the transistor has a thickness of from 10 nm to 200
5 nm.

6. A semiconductor device according to any one of claims 1, 2, 4 and 5 wherein the
plastic substrate is one selected from the group consisting of polycarbonate, polyarylate, and
polyethersulfone.

10

7. A semiconductor device according to any one of claims 1, 2, 4 and 5 wherein the
semiconductor device is incorporated into an electronic apparatus selected from the group
consisting of a display panel, a computer, a telephone set, an IC tag and an IC card.

15

8. A semiconductor device according to any one of claims 1, 2, 4 and 5 wherein the
integrated circuit comprises an arithmetic processing means, a storage means, a power supply
circuit and an interface.

9. A communication system comprising:

20

a semiconductor device having an integrated circuit and an antenna connected to the
integrated circuit, the integrated circuit comprising:

a transistor fixed to a plastic substrate by an adhesive agent,

wherein a semiconductor film of the transistor has a thickness of from 10 nm to 200
nm, and

25

wherein a power or a signal is received from a reader/writer by the antenna.

10. A communication system comprising:

a semiconductor device having an integrated circuit and a light receiving element, the
integrated circuit comprising:

30

a transistor fixed to a plastic substrate by an adhesive agent,

wherein a semiconductor film of the transistor has a thickness of from 10 nm to 200

nm, and

wherein a power or a signal is received from a reader/writer by the light receiving element.

- 5 11. A communication system according to claim 9 or claim 10, wherein information on the semiconductor device is displayed on display means provided for the reader/writer.

FIG.1A

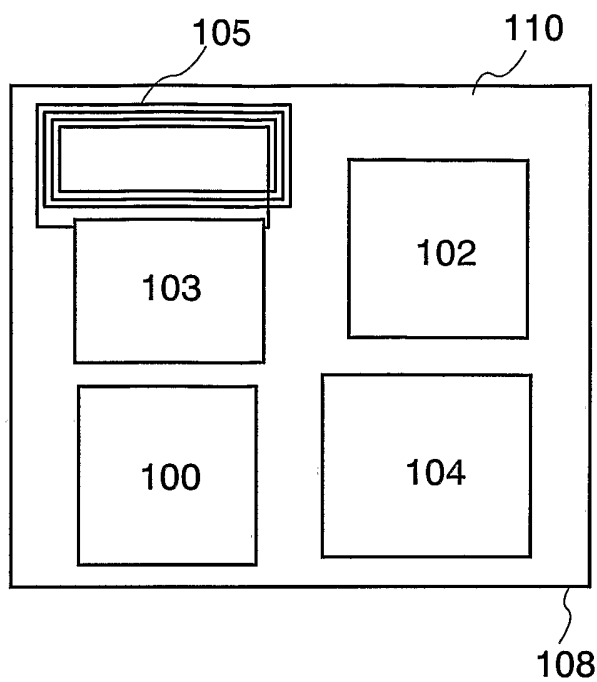


FIG.1B

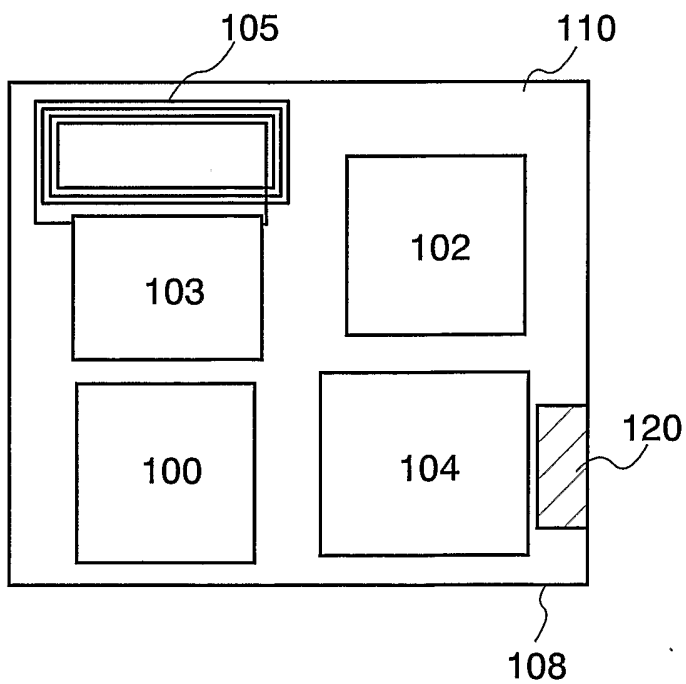


FIG.2A

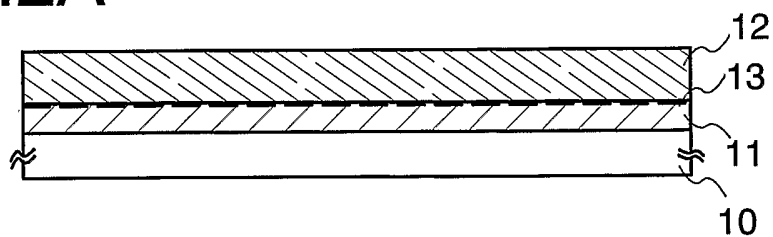


FIG.2B

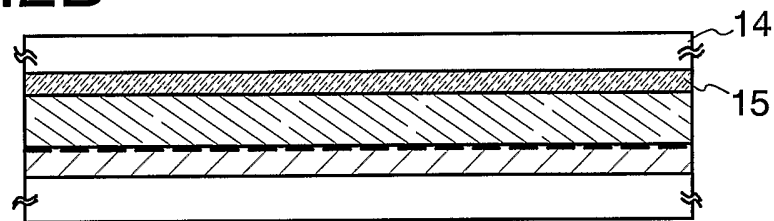


FIG.2C

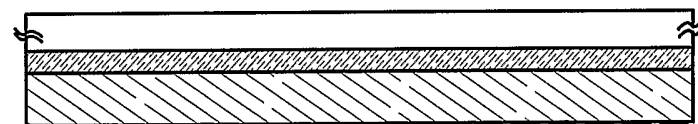


FIG.2D

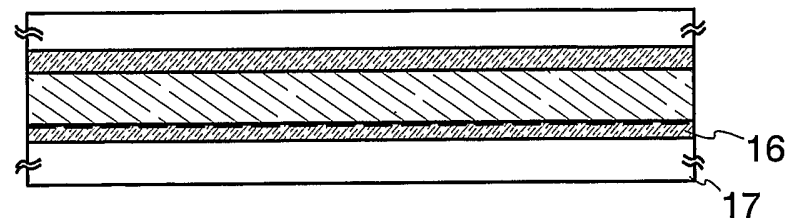


FIG.2E



FIG.3A

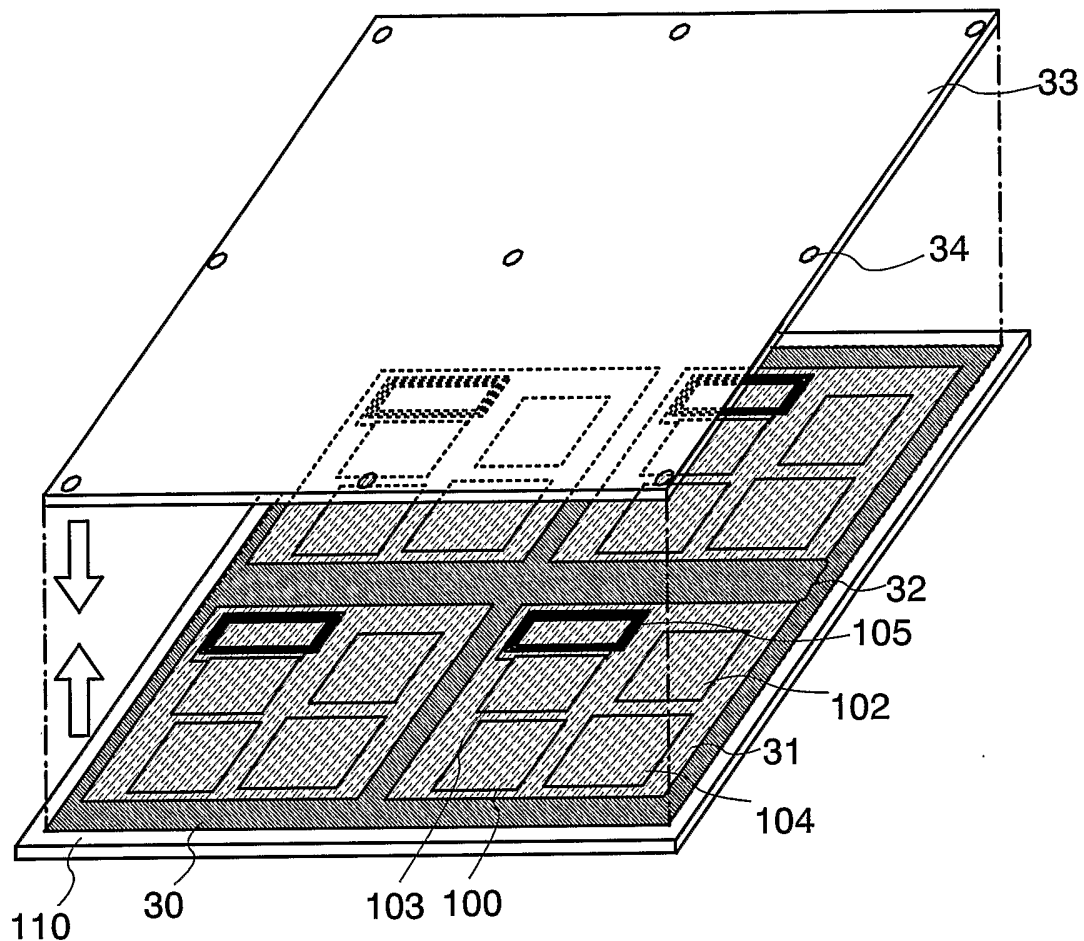
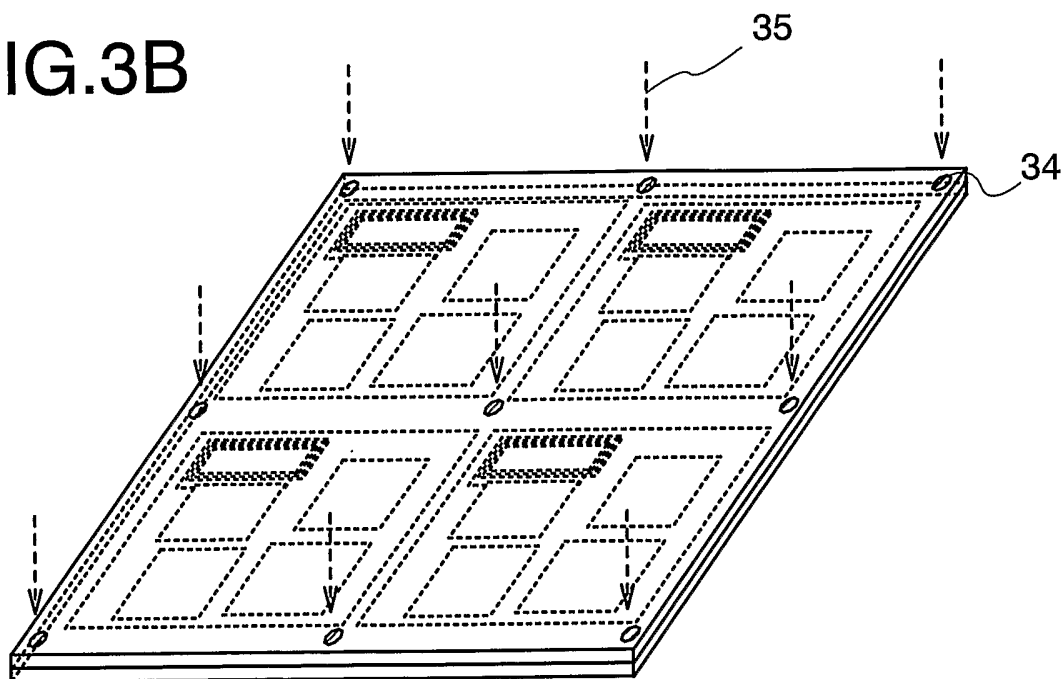


FIG.3B



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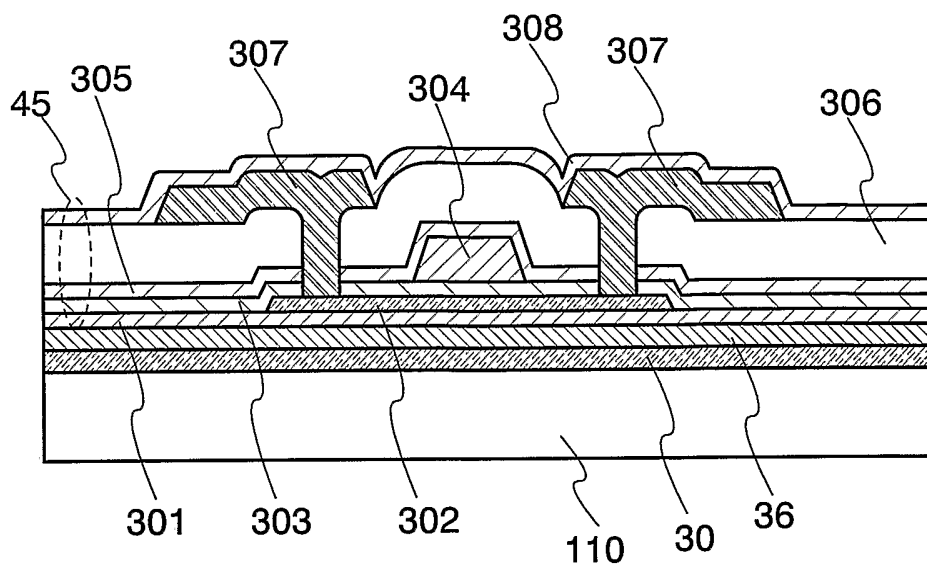


FIG.4

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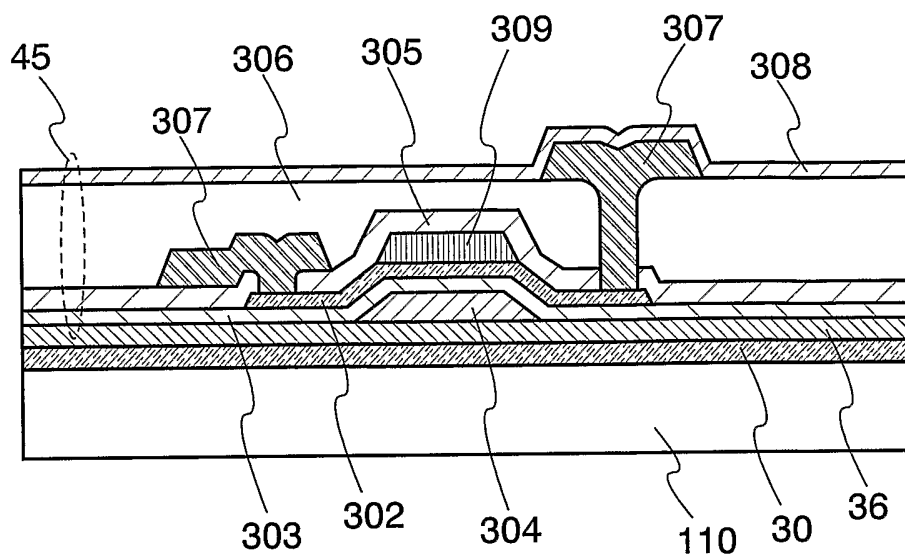


FIG.5

FIG.6A

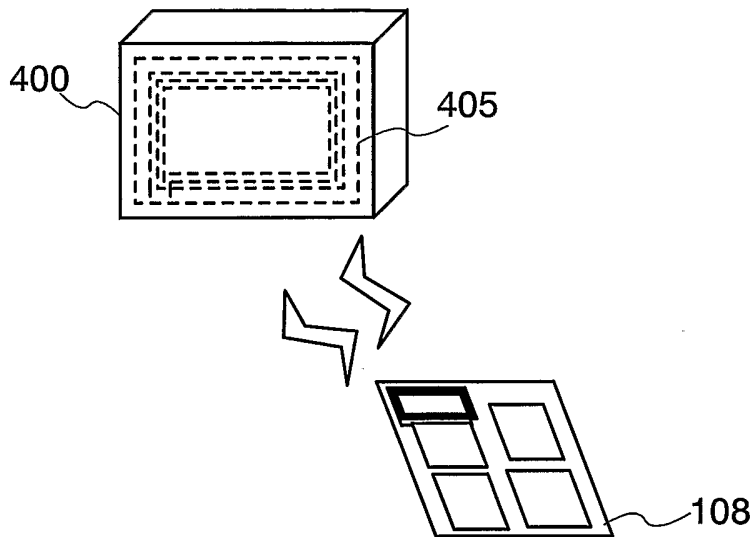
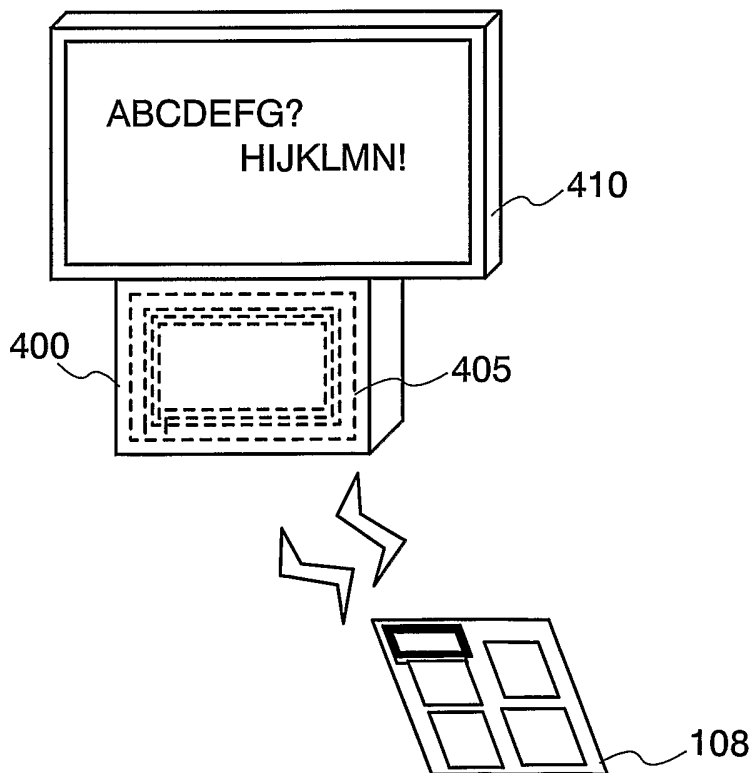


FIG.6B



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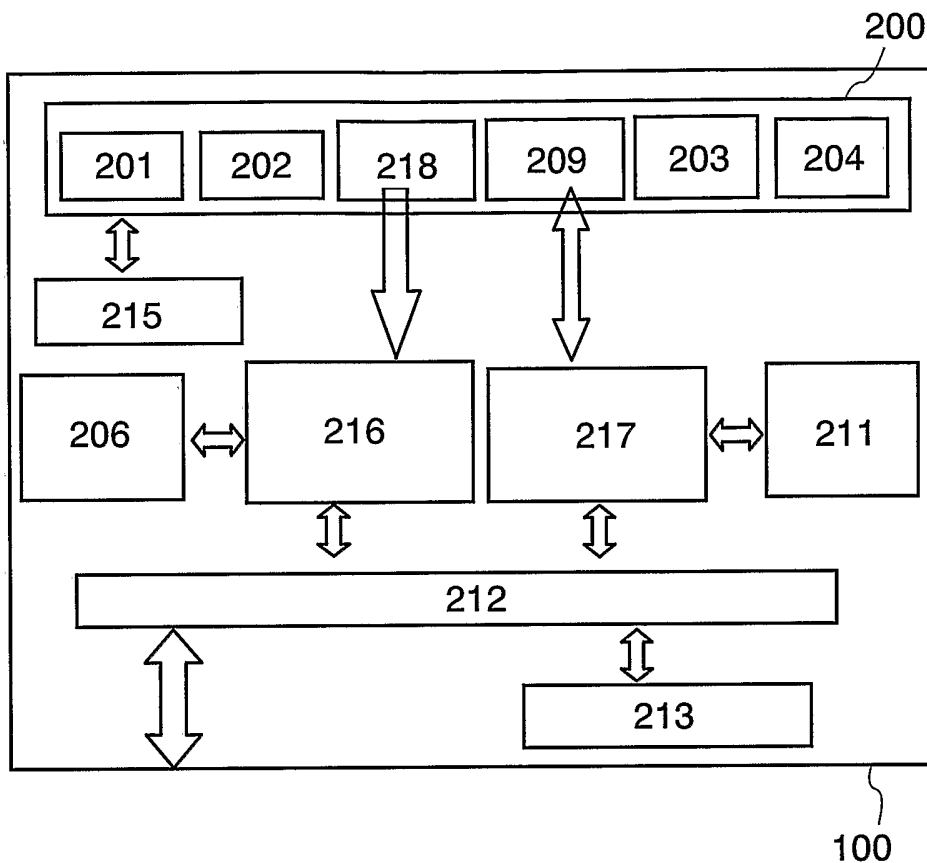


FIG. 7

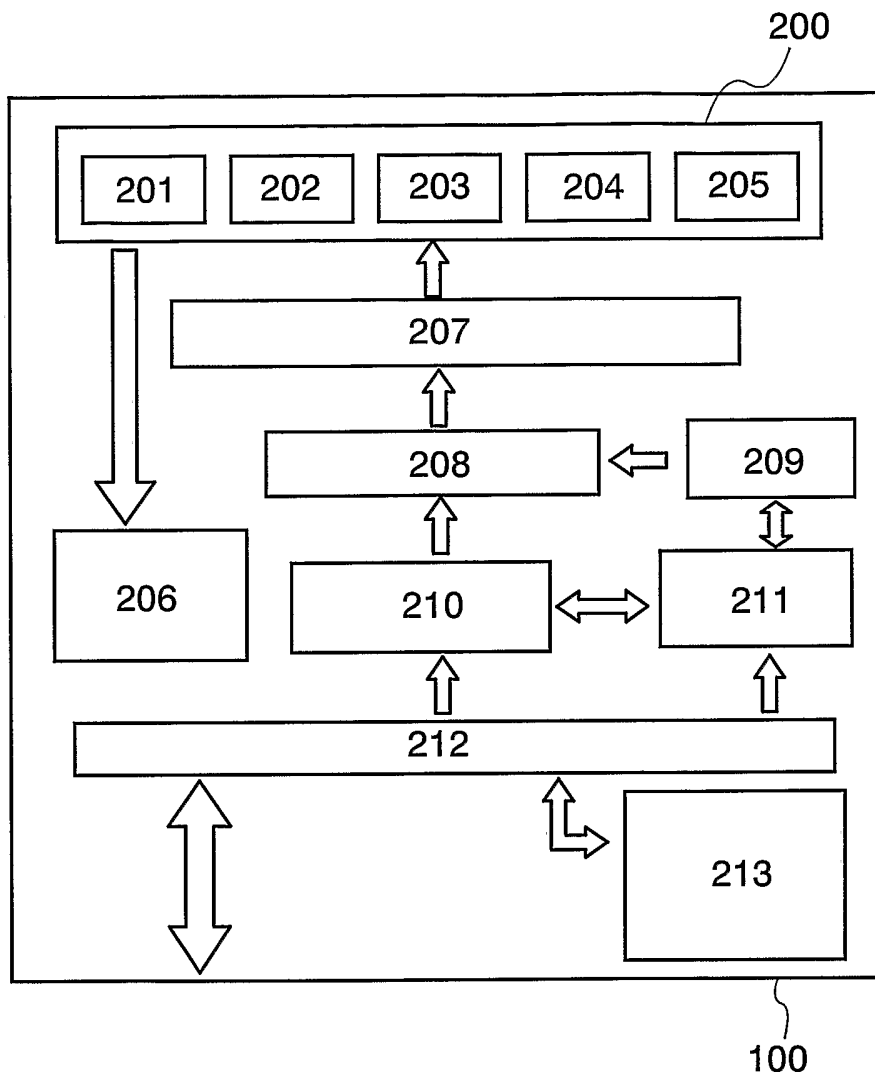


FIG.8

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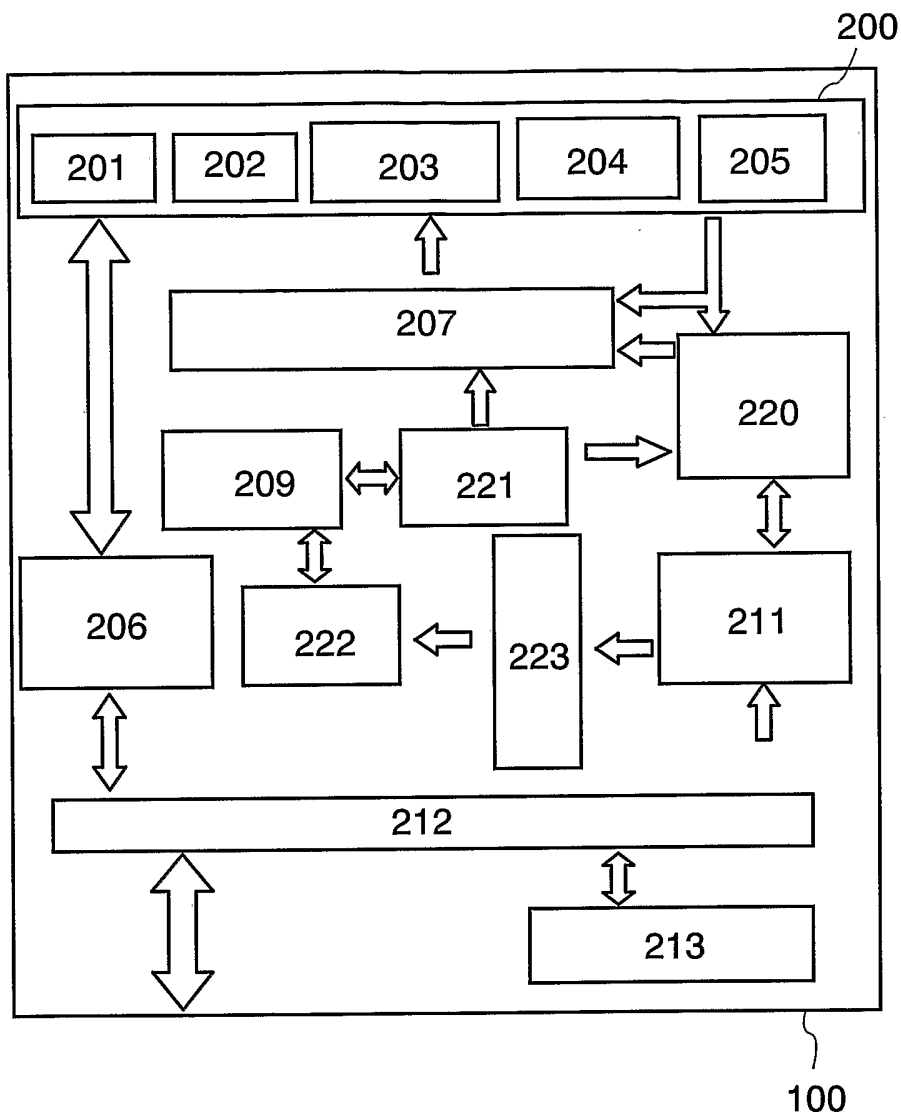


FIG.9

FIG.10A

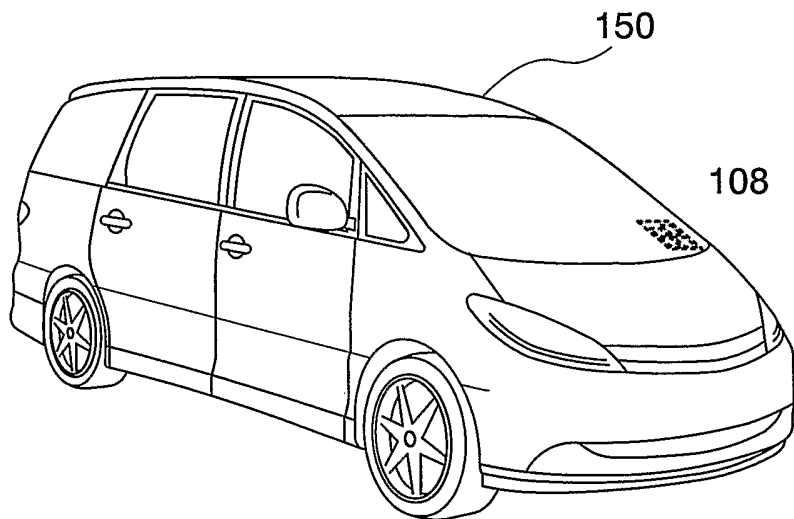


FIG.10B

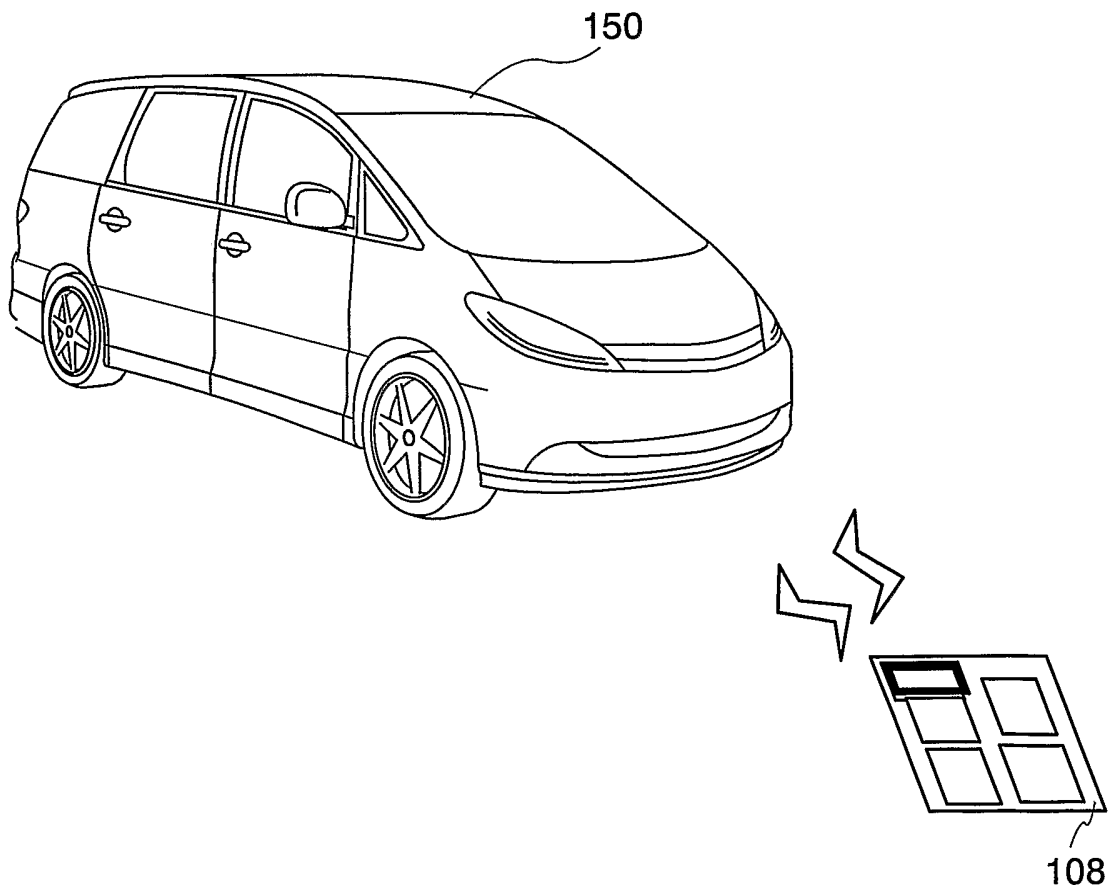


FIG.11A

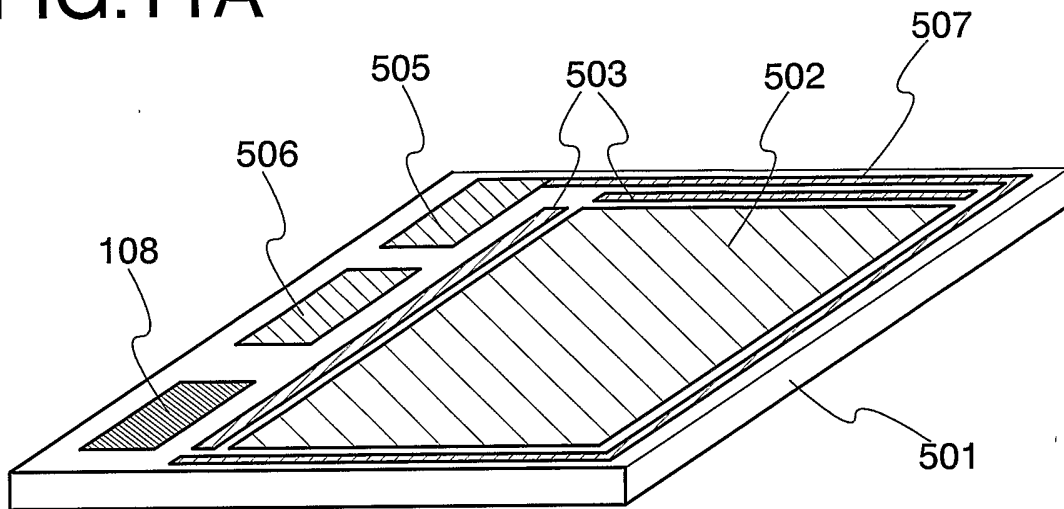
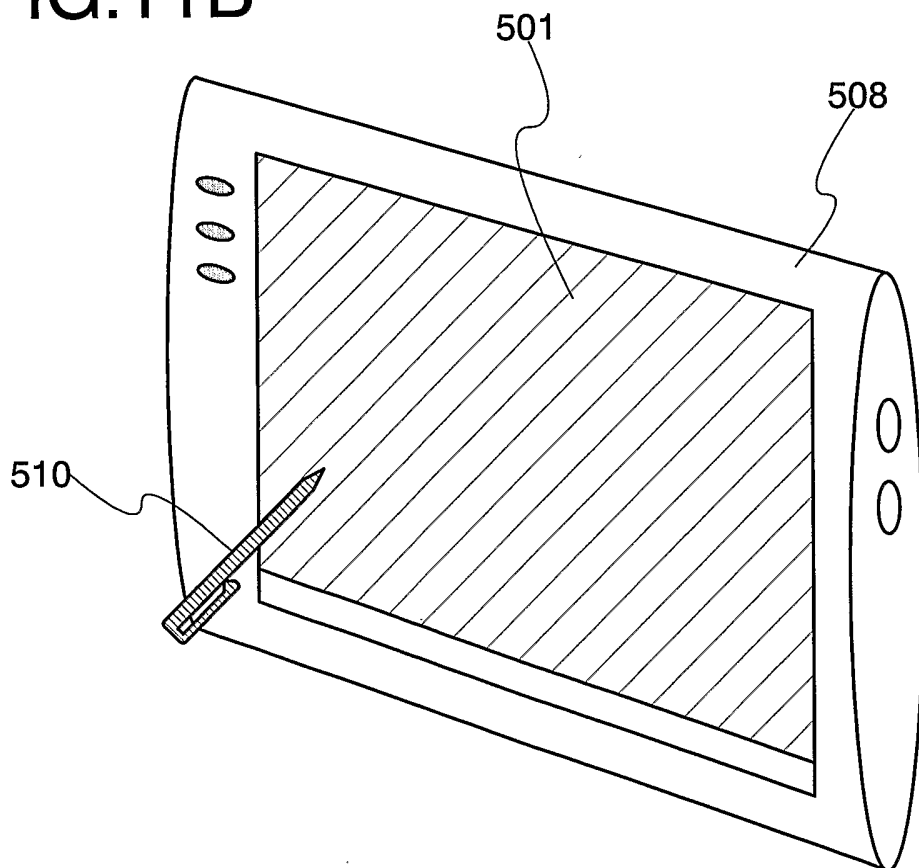


FIG.11B



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FIG.12A

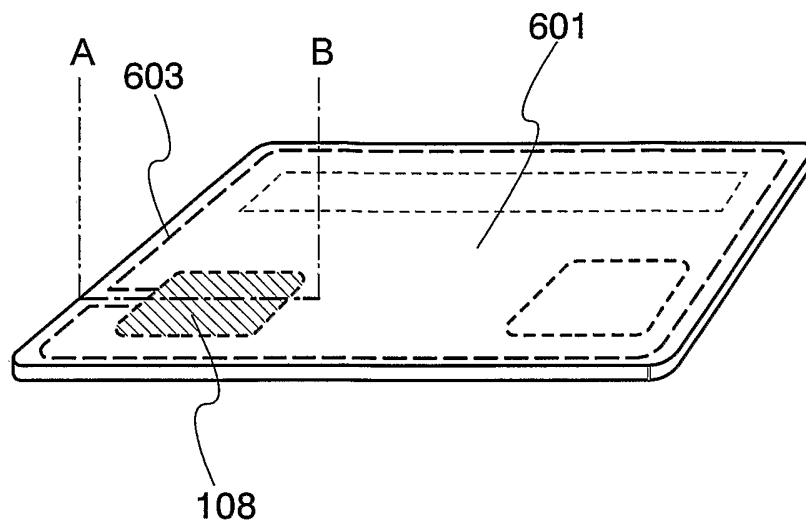


FIG.12B

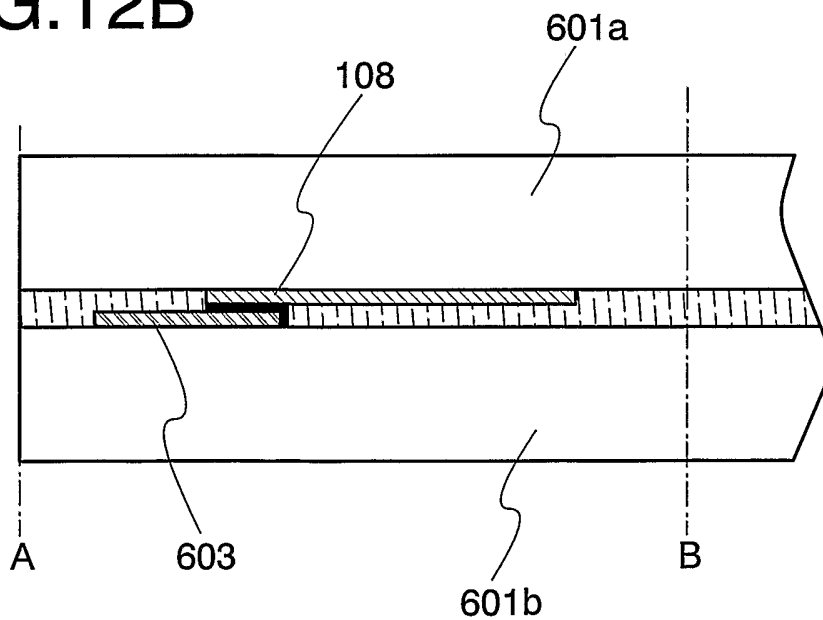
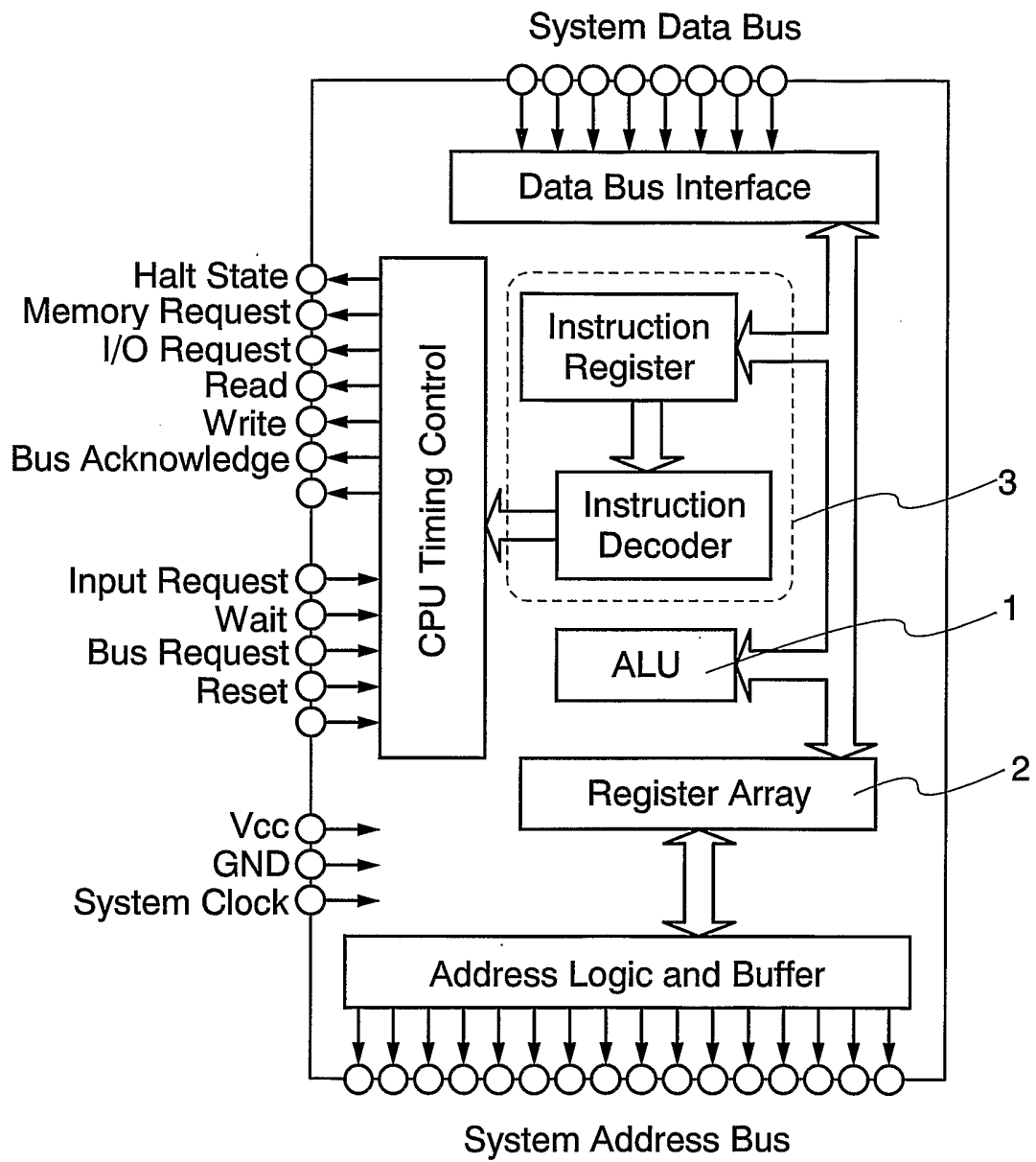


FIG.13



EXPLANATION OF REFERENCE

1: ALU (Arithmetic and Logic Unit), 2: a general register, 3: an instruction analyzer, 10: substrate, 11: metal film, 12: layer to be stripped, 13: oxide (metal oxide), 13: metal oxide, 14: support substrate, 15: adhesive agent, 16: adhesive agent, 17: plastic substrate, 30: stripping layer, 31: element formation region, 32: groove, 33: support substrate, 34: hole, 35: etching agent, 36: insulating film, 45: element formation layer, 100: arithmetic processing means, 102: storage means, 103: power supply circuit, 104: interface (I/F), 105: antenna, 108: processor, 110: insulating surface (substrate), 120: light receiving element, 150: car, 206: primary instruction cache, 207: reservation station, 208: instruction decoder 209: branch prediction unit, 210: instruction fetch unit, 211: primary instruction cache, 212: bus interface, 213: second cache, 215: general register, 216: data cache controller, 217: instruction cache controller, 218: load store unit, 220: renaming unit, 221: instruction issue unit, 222: zero-order cache, 223: predecoder, 301: insulating film, 302: semiconductor film, 303: insulating film, 304: gate electrode, 305: insulating film, 306: insulating film, 307: wiring, 308: insulating film, 309: channel protective layer, 400: reader/writer device, 405: antenna, 410: display means, 501: plastic substrate, 502: pixel portion, 503: driver circuit portion, 505: communication circuit, 506: memory, 507: antenna, 508: computer, 510: pen, 601: IC card, 603: antenna

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2005/011098

A. CLASSIFICATION OF SUBJECT MATTER		
Int.Cl. ⁷ H01L29/786, G06K19/077, H01L21/336, 21/822, 27/04, 27/12		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
Int.Cl. ⁷ H01L29/786, G06K19/077, H01L21/336, 21/822, 27/04, 27/12		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Published examined utility model applications of Japan 1922-1996 Published unexamined utility model applications of Japan 1971-2005 Registered utility model specifications of Japan 1996-2005 Published registered utility model applications of Japan 1994-2005		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2004-103719 A(CANON INC.), 2004.04.02, Paragraphs [0005]-[0022] (Family: none)	1-4, 7-9
Y		5-6, 10-11
Y	JP 2003-195973 A(SHARP CORPORATION), 2003.07.11, Paragraphs [0002]-[0031] (Family: none)	5-6, 10-11
Y	JP 11-020360 A(SEIKO EPSON CORPORATION), 1999.01.26, Paragraph [0168](Family: none)	6
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
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