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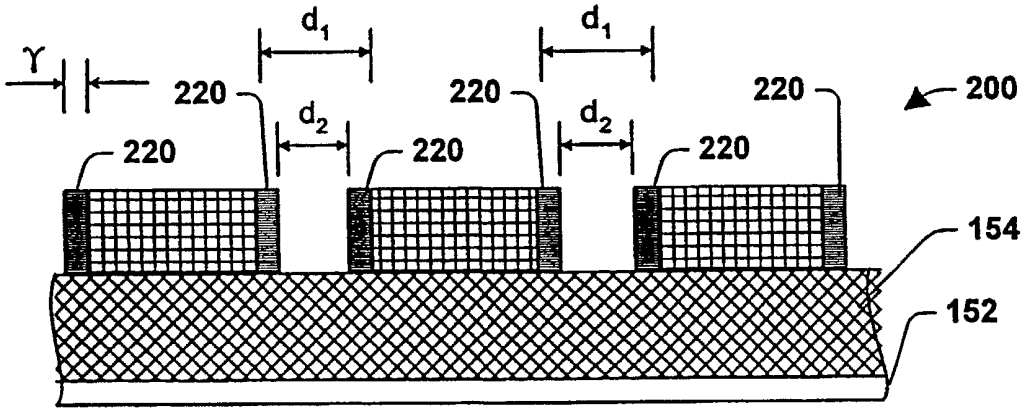
(54) Title: METHOD TO PRODUCE HIGH DENSITY MEMORY CELLS AND SMALL SPACES BY USING NITRIDE SPACER



(57) Abstract: The present invention relates to a method for forming an etch mask. A photoresist layer is patterned, wherein d_1 is a smallest space dimension of an exposed area of a layer underlying the photoresist layer. An ARC layer under the photoresist layer is etched. A nitride layer is formed to be conformal to the patterned ARC layer and exposed portions of an underlayer underlying the patterned ARC layer. The nitride layer is etched to form nitride sidewalls, the nitride sidewalls reducing the smallest space dimension of the exposed underlayer area to d_2, wherein $d_2 < d_1$.

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METHOD TO PRODUCE HIGH DENSITY MEMORY CELLS AND SMALL SPACES BY USING NITRIDE SPACER

Technical Field

The present invention generally relates to semiconductor processing, and in particular to a method for producing small space patterns *via* employment of a conformal nitride layer.

Background Art

In the semiconductor industry, there is a continuing trend toward higher device densities. To achieve these high densities there has been and continues to be efforts toward scaling down device dimensions (*e.g.*, at submicron levels) on semiconductor wafers. In order to accomplish such high device packing density, smaller and smaller feature sizes are required. This may include the width and spacing of interconnecting lines, spacing and diameter of contact holes, and the surface geometry such as corners and edges of various features.

The requirement of small features with close spacing between adjacent features requires high resolution photolithographic processes. In general, lithography refers to processes for pattern transfer between various media. It is a technique used for integrated circuit fabrication in which a silicon slice, the wafer, is coated uniformly with a radiation-sensitive film, the resist, and an exposing source (such as optical light, x-rays, or an electron beam) illuminates selected areas of the surface through an intervening master template, the photo mask, for a particular pattern. The lithographic coating is generally a radiation-sensitive coating suitable for receiving a projected image of the subject pattern. Once the image is projected, it is indelibly formed in the coating. The projected image may be either a negative or a positive image of the subject pattern. Exposure of the coating through the photomask causes the image area to become either more or less soluble (depending on the coating) in a particular solvent developer. The more soluble areas are removed in the developing process to leave the pattern image in the coating as less soluble polymer.

The spacing between adjacent lines of an integrated circuit is an important dimension, and ever continuing efforts are made toward reducing such spacing dimension. The wavelength of light used in the photolithographic process along with the lithographic tool set employed in the process generally dictate the spacing dimension. For example, a tool set designed to provide lines and/or spaces at .18μm does not achieve consistent lines and/or spacing at its minimum range of .18μm but rather is employed to generate lines and/or spacing above the minimum range (*e.g.*, .20μm) with fairly consistent results.

In view of the above, it would be desirable for a technique which allows for a particular lithographic tool set to be employed and achieve consistent lines and/or spacing between lines at the minimum range of the tool set and even below the minimum range.

Disclosure of the Invention

The present invention relates to a method for employing a photolithographic tool set and achieving substantially consistent spacing dimensions below the minimum range of the tool set. A given photolithographic tool set is employed to pattern a photoresist layer in a desired fashion. The tool set is capable of achieving a smallest spacing dimension between adjacent lines of d_1. After the photoresist layer is patterned, an etch step is performed to etch the pattern in an underlying ARC layer. Next, a nitride layer is conformably deposited over the patterned ARC layer. Thereafter, a directional etch is performed to remove a particular amount of the nitride layer (preferably a thickness equivalent to the thickness of the nitride layer residing over an ARC portion). The directional etch leaves nitride sidewalls along the patterned ARC portions which result in a reduction in dimension size of exposed areas interposed between adjacent ARC portions. Thus a spacing dimension size (d_2) of exposed areas is substantially less than the spacing dimension size (d_1) of exposed areas prior to the depositing the nitride layer. An etch step is performed to etch layers underlying the ARC layer. Adjacent lines etched from one of the underlayers will have a smallest spacing design dimension of d_2 as compared to d_1. Thus, the present invention provides for achieving spacing dimensions between lines at and below a minimum patterning range for a particular lithographic tool set.

One aspect of the invention relates to a method for forming an etch mask. A photoresist layer is patterned, wherein d_1 is a smallest space dimension of an exposed area of an ARC layer underlying the photoresist layer. The ARC layer is etched. A nitride layer is formed to be conformal to the patterned ARC layer and exposed portions of an underlayer underlining the ARC layer. The nitride layer is etched to form nitride sidewalls, the nitride sidewalls reducing the smallest space dimension of the exposed underlayer area to d_2, wherein $d_2 < d_1$.

Another aspect of the invention relates to a method for producing a small space pattern in a semiconductor layer. A photoresist layer of a semiconductor structure is patterned with a photolithographic tool set, a minimum printed space dimension of the patterned photoresist being d_1, wherein d_1 is the smallest space dimension consistently printable by the photolithographic tool set. A nitride layer is formed to be conformal to a patterned ARC layer underlying the photoresist layer and exposed portions as an underlayer underlying the ARC layer, d_1 being the smallest dimension of the exposed portions. The nitride layer is etched an amount substantially equivalent to a minimum thickness parameter (γ) of the nitride to leave nitride sidewalls such that the smallest dimension of the exposed portions is now d_2, wherein $d_2 < d_1$.

Another aspect of the invention relates to method of forming closely spaced lines from a polysilicon layer. A semiconductor structure is used, the semiconductor structure including: the polysilicon layer; and a patterned anti-reflective coating (ARC) layer over the polysilicon layer, wherein a smallest dimension of at least one exposed portion of the polysilicon layer equals d_1. A nitride layer is formed to conform to an exposed surface of the semiconductor structure. The nitride layer is etched so as to leave nitride portions along sidewalls of the ARC layer, the nitride portions reducing the smallest dimension of the at least one exposed portion of the polysilicon layer to d_2, wherein $d_2 < d_1$.

Still another aspect of the invention relates to a method of forming closely spaced lines from a polysilicon layer. A photolithographic tool set is used to pattern a photoresist layer of a semiconductor structure wherein d_1 is a smallest space dimension consistently printable by the photolithographic tool set, the semiconductor structure including: the polysilicon layer; an anti-reflective coating (ARC) layer over the polysilicon layer; and the patterned photoresist layer over the ARC layer, wherein a smallest dimension of at least one exposed portion of the ARC layer equals d_1. The ARC layer is etched. The photoresist layer is removed. A nitride layer is formed to conform to remaining portions of the ARC layer and exposed portions of a polysilicon layer underlying the ARC layer. The nitride layer is etched so as to leave nitride sidewalls, the nitride sidewalls reducing the smallest dimension of the at least one exposed portion of the polysilicon layer to d_2, wherein $d_2 < d_1$. The polysilicon layer is etched, wherein a smallest space dimension between at least two adjacent lines is substantially equal to d_2.

To the accomplishment of the foregoing and related ends, the invention, then, comprises the features hereinafter fully described and particularly pointed out in the claims. The following description and the annexed drawings set forth in detail certain illustrative embodiments of the invention. These embodiments are indicative, however, of but a few of the various ways in which the principles of the invention may be employed. Other objects, advantages and novel features of the invention will become apparent from the following detailed description of the invention when considered in conjunction with the drawings.

Brief Description of the Drawings

Fig. 1a is a schematic cross-sectional illustration of lines formed in accordance with the present invention;

Fig. 1b is a schematic cross-sectional illustration of a ratio of line width to space width in accordance with the present invention;

Fig. 2 is schematic cross-sectional illustration of a semiconductor structure including a polysilicon layer, an anti-reflective coating layer and a photoresist layer patterned with a tool set;

Fig. 3 is a schematic illustration of the semiconductor structure of Fig. 2 undergoing an etch step to etch a layer underlying the patterned photoresist layer in accordance with the present invention;

Fig. 4 is a schematic cross-sectional illustration of the structure of Fig. 3 after the underlayer etch step is complete, and illustrating the structure undergoing a photoresist stripping process in accordance with the present invention;

Fig. 5 is a schematic cross-sectional illustration of the structure of Fig. 4 after the photoresist has been removed in accordance with the present invention;

Fig. 6 is a schematic cross-sectional illustration of the structure of Fig. 5 undergoing a deposition process to conformably deposit a nitride layer on the structure in accordance with the present invention;

Fig. 7 is a schematic cross-sectional illustration of the structure of Fig. 6 after the nitride deposition step is substantially complete in accordance with the present invention;

Fig. 8 is a schematic cross-sectional illustration of the structure of Fig. 7 undergoing a directional etch step in accordance with the present invention;

Fig. 9 is a schematic cross-sectional illustration of the structure of Fig. 8 after the directional etch step is substantially complete in accordance with the present invention;

Fig. 10 is a schematic cross-sectional illustration of the structure of Fig. 9 undergoing a poly etch step to form lines in accordance with the present invention;

Fig. 11 is a schematic cross-sectional illustration of the structure of Fig. 10 after the poly etch step is substantially complete in accordance with the present invention;

Fig. 12 is a schematic cross-sectional illustration of the structure of Fig. 11 undergoing a stripping process to remove remaining portions of the nitride layer and ARC layer in accordance with the present invention;

Fig. 13 is a schematic cross-sectional illustration of the structure of Fig. 12 substantially complete in relevant part in accordance with the present invention; and

Fig. 14 is a schematic cross-sectional illustration of floating gates formed in accordance with the present invention.

Modes of Carrying Out the Invention

The present invention will now be described with reference to the drawings. Fig. 1a illustrates a set of lines 50_A, 50_B and 50_C (collectively referred to by reference numeral 50) formed in accordance with the present invention. The lines 50 are formed employing a photolithographic tool set (not shown) having a minimum feature printing dimension of d_M. More particularly, the smallest spacing between lines printable by the tool set has a dimension of d_M. However, consistent printing at the minimum spacing dimension d_M is typically not possible. The tool set is capable of printing consistently at a spacing dimension of d_1 (which is larger than d_M). As can be seen from Fig. 1a, the present invention provides for employing the particular tool set to form the lines 50 such that a spacing dimension (d_2) between adjacent lines, respectively, is achieved. The dimension d_2 is substantially less than dimensions d_M and d_1.

Fig. 1b illustrates a ratio of line width to space width in accordance with the present invention. As is known, small spacing between adjacent lines having relatively large width is very difficult to achieve. The present invention provides for achieving a ratio of line width to space width of up to about 20:1. Lines 50_D and 50_E have widths, respectively, about twenty times greater than the space between the lines 50_D and 50_E.

Figs 2-11 illustrate in greater detail how the present invention provides for forming the lines 50 having a spacing dimension there between, respectively, of d_2 using the tool set which has a minimum print feature dimension of d_M (which is substantially greater than d_2).

Thus, the present invention provides for a method for employing a conventional tool set to obtain minimum space dimensions well below the minimum space parameter typically achievable by

the tool set. As a result, the present invention provides for a relatively low cost alternative to purchasing new photolithographic tool sets for achieving reduced spacing between lines.

Fig. 2 illustrates a structure 100 which includes an oxide layer 152, a polysilicon layer 154, an anti-reflective coating layer 162 (*e.g.*, SiON having a thickness within the range of 800A to 1500A) and a patterned photoresist layer 164. Formation of the structure 100 is well known in the art, and further detail regarding such is omitted for sake of brevity. The photoresist layer 164 has been patterned *via* a photolithographic tool set (*e.g.*, deep ultra-violet (DUV)) tool set capable of patterning lines separated by distances equal to or greater than .18 μm). The patterned photoresist layer 164 will serve as a mask for the underlying layers during etch steps to form the lines 50. The distance d_1 is representative of the smallest space parameter consistently achievable by the photolithographic tool set.

Fig. 3 illustrates an etch step 166 to etch exposed portions of the ARC layer 162.

Fig. 4 illustrates a photoresist stripping step 168 to remove remaining portions of the photoresist layer 164.

Fig. 5 illustrates a structure 169 formed after the etch step 166 and the stripping step 168 are substantially complete.

Fig. 6 illustrates a nitride deposition step 170 performed on the structure 169 to form a nitrogen layer conformal to the exposed surface of the structure 169. More particularly, the etched ARC layer 162 is exposed to a nitrogen based chemistry to form a conformal nitride coating 180 (Fig. 17) on the ARC layer 162. It is to be appreciated that one skilled in the art could readily tailor without undue experimentation a suitable chemistry to form the conformal nitride coating 80. The etch chemistry and duration thereof may be suitably tailored to form the nitride coating at substantially any desired thickness (*e.g.*, between about the range of 10-1000A).

Fig. 8 illustrates a directional etch step 190 being performed to remove a predetermined thickness of the nitride layer 180. Preferably, a dry directional etch is performed to remove an amount of the nitride layer 180 equivalent to the conformal thickness of the nitride layer 180.

Substantial completion of the etch step 190 results in a structure 200 shown in Fig. 9. The structure 200 includes nitride sidewalls 220 which result in exposed portions of the polysilicon layer 154 having a dimension of d_2. The dimension d_2 is less than the dimension d_1 (Fig. 2). The dimension d_2 may be controlled *via* the controlling the thickness (γ) of the nitride layer 180. For example, the dimension d_2 may be controlled according to the following relationship:

$$d_2 = d_1 - 2\gamma$$

Since there are two nitride sidewalls 220 within a particular dimension d_1, the value of d_2 equals d_1 less twice the nitride layer thickness (γ).

Next, referring to Fig. 10, a poly etch 230 is performed to etch exposed portions of the polysilicon layer 154 so as to form lines 250 (Fig. 11) having a spacing there between, respectively, of d_2.

Fig. 12 illustrates a stripping step 260 to remove remaining portions of the ARC layer 162 and nitride sidewalls 220.

Fig. 13 illustrates a structure 300 including the lines 250 having a spacing dimension between adjacent lines (*e.g.*, 250_A and 250_B) substantially equal to d_2. Thus, for example, if a .18μm tool set were employed to pattern the photoresist 164 with a spacing dimension d_1 = .20μm and the nitride layer 80 was formed to have a thickness (γ) of .03μm, the resulting spacing dimension between adjacent lines 50_A and 50_B would be approximately .14μm= (.20μm - 2(.03μm)). The minimum space dimension (d_M) for the .18μm tool set employed is .18μm, and such minimum space dimension typically would be difficult to achieve consistently in accordance with conventional techniques. However, by employing the present invention the same .18μm tool set can be employed to achieve with substantial consistency minimum space dimensions between lines at and below the minimum space dimension parameter of the tool set.

Employing the present invention achieves with substantial consistency minimum space dimensions between lines at and below the minimum space dimension parameter of a particular tool set employed.

Although the present invention has been described primarily in the context of forming lines, it is to be appreciated that the present invention may be applied to forming other features (*e.g.*, floating gates of flash memory devices and/or embedded flash memory devices) where achieving small space dimension between adjacent features is desired. For example, as shown in Fig. 14 the principles of the present invention may be employed in the formation of closely spaces floating gates 350_A, 350_B and 350_C of a memory device 360.

The present invention provides for a method for employing a particular photolithographic tool set to obtain minimum space dimensions well below the minimum space parameters typically obtainable by the tool set.

What has been described above are preferred embodiments of the present invention. It is, of course, not possible to describe every conceivable combination of components or methodologies for purposes of describing the present invention, but one of ordinary skill in the art will recognize that many further combinations and permutations of the present invention are possible. Accordingly, the present invention is intended to embrace all such alterations, modifications and variations that fall within the spirit and scope of the appended claims.

Claims

What is claimed is:

1. A method for forming an etch mask, comprising the steps of:

patterning a photoresist layer, wherein d_1 is a smallest space dimension of an exposed area of an ARC layer underlying the photoresist layer;

etching the ARC layer;

forming a nitride layer to be conformal to the patterned ARC layer and exposed portions of an underlayer underlying the patterned ARC layer; and

etching the nitride layer to form nitride sidewalls, the nitride sidewalls reducing the smallest space dimension of the exposed underlayer area to d_2, wherein $d_2 < d_1$.

2. The method of claim 1 further including the step of forming the nitride layer to have a minimum thickness of γ.

3. The method of claim 1, further including forming the nitride layer to have a thickness (γ) with the range of about 10-1000A.

4. The method of claim 1, further including the step of using a dry directional etch to etch the nitride layer.

5. The method of claim 11, further including the step of predetermining the dimension d_2 according to the relationship $d_2 = d_1 - 2\gamma$, wherein γ is a thickness of the nitride layer.

6. A method for producing a small space pattern in a semiconductor layer, comprising the steps of:

patterning a photoresist layer of a semiconductor structure with a photolithographic tool set, a minimum printed space dimension of the patterned photoresist being d_1, wherein d_1 is the smallest space dimension consistently printable by the photolithographic tool set;

forming a nitride layer to be conformal to a patterned ARC layer underlying the photoresist layer and exposed portions an underlayer underlying the ARC layer, d_1 being the smallest dimension of the exposed portions; and

etching the nitride layer an amount substantially equivalent to a minimum thickness parameter (γ) of the nitride layer to leave nitride sidewalls such that the smallest dimension of the exposed portions is now d_2, wherein $d_2 < d_1$.

7. The method of claim 6, further including forming the nitride layer to have a thickness (γ) with the range of about 10-1000A.

8. The method of claim 6, further including the step of using a dry directional etch to etch the nitride layer.

9. The method of claim 6, further including the step of predetermining the dimension d_2 according to the relationship $d_2 = d_1 - 2\gamma$.

10. A method of forming closely spaced lines from a polysilicon layer, comprising the steps of:

using a semiconductor structure including: the polysilicon layer; an anti-reflective coating (ARC) layer over the polysilicon layer, wherein a smallest dimension of at least one exposed portion of the polysilicon layer equals d_1;

forming a nitride layer to conform to an exposed surface of the semiconductor structure; and

etching the nitride layer so as to leave nitride portions along sidewalls of the ARC layer, the nitride portions reducing the smallest dimension of the at least one exposed portion of the polysilicon layer to d_2, wherein $d_2 < d_1$.

11. The method of claim 10, further including the step of forming the nitride layer to have a thickness (γ).

12. The method of claim 11, further including the step of predetermining the dimension d_2 according to the relationship $d_2 = d_1 - 2\gamma$.

13. The method of claim 10 further including the step of using SiON in the ARC layer.

14. The method of claim 10 wherein the features are lines and a ratio of line width to space width is between the range of about 20: 1 to 1:1.

15. The method of claim 10 wherein the features are lines and a ratio of line width to space width is between the range of about 20: 1 to 10:1.

16. The method of claim 10, wherein the features are floating gates.

17. A method of forming closely lines from a polysilicon layer, comprising the steps of:

patterning a photoresist layer of a semiconductor structure wherein d_1 is a smallest space dimension printed on the photoresist layer; the semiconductor structure including: the polysilicon layer; an anti-reflective coating (ARC) layer over the polysilicon layer; and the patterned photoresist layer over the ARC layer, wherein a smallest dimension of at least one exposed portion of the ARC layer substantially equals d_1;

etching the ARC layer;

removing the photoresist layer;

forming a nitride layer to conform to remaining portions of the ARC layer and exposed portions of a polysilicon layer underlying the ARC layer; and

etching the nitride layer so as to leave nitride sidewalls, the nitride sidewalls reducing the smallest dimension of the at least one exposed portion of the polysilicon layer to d_2, wherein $d_2 < d_1$; and

etching the polysilicon layer, wherein a smallest space dimension between at least two adjacent lines is substantially equal to d_2.

18. The method of claim 17, further including the step of predetermining the dimension d_2 according to the relationship $d_2 = d_1 - 2\gamma$, wherein γ is a thickness dimension of the nitride layer.

19. The method of claim 18, further including the step of forming the nitride layer to have a thickness (γ) with the range of about 10-1000A.

20. The method of claim 17 wherein the ARC layer includes SiON.

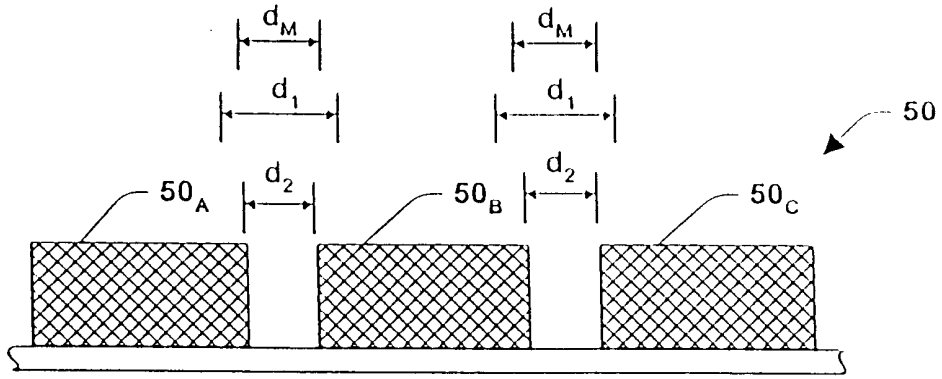

Fig. 1a

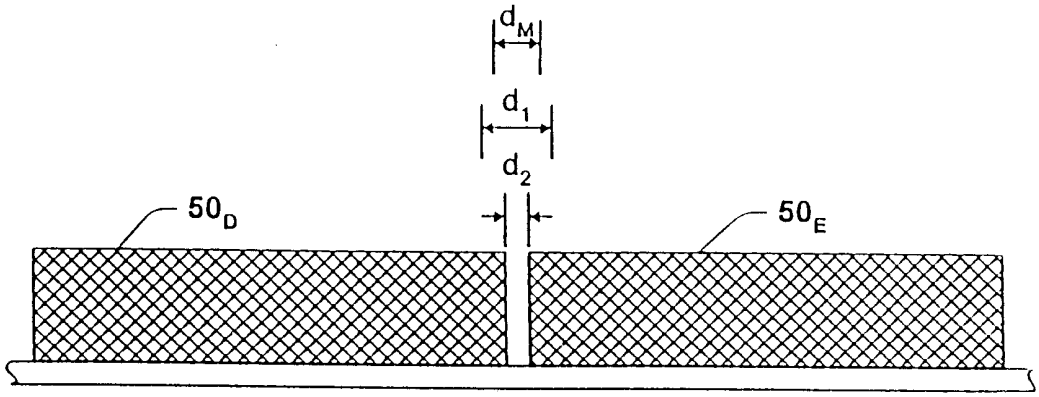

Fig. 1b

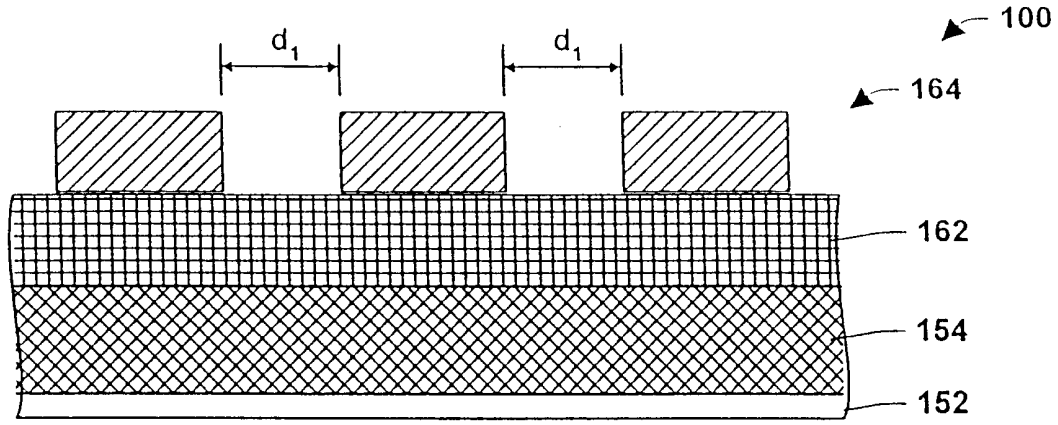

Fig. 2

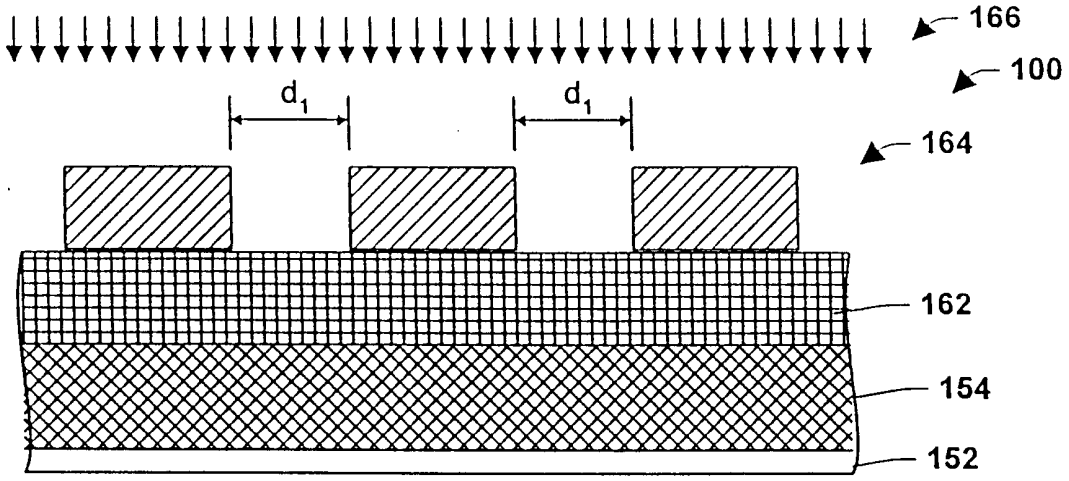

Fig. 3

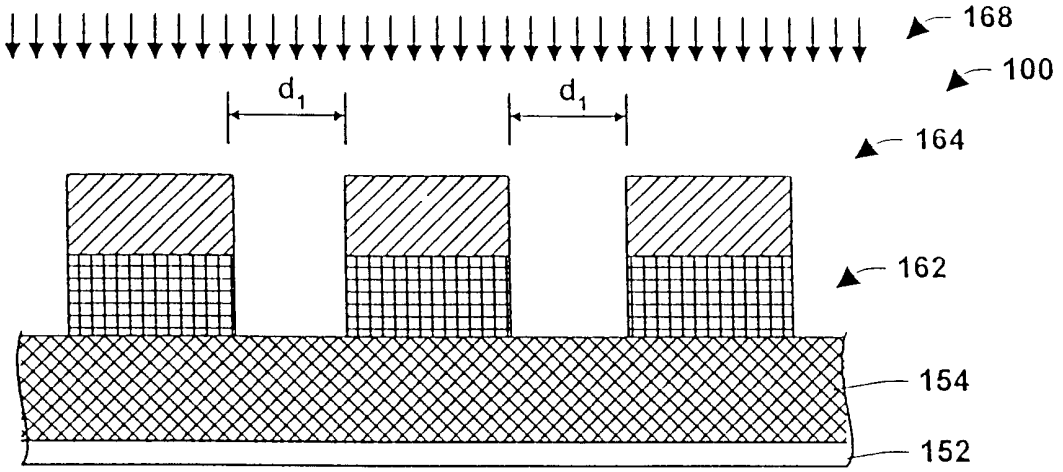

Fig. 4

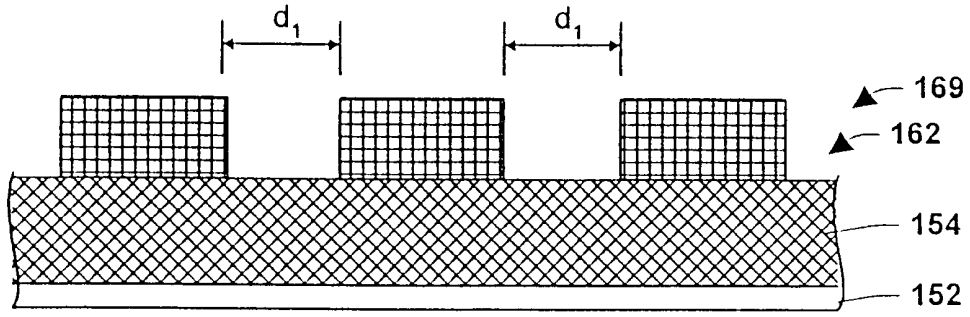

Fig. 5

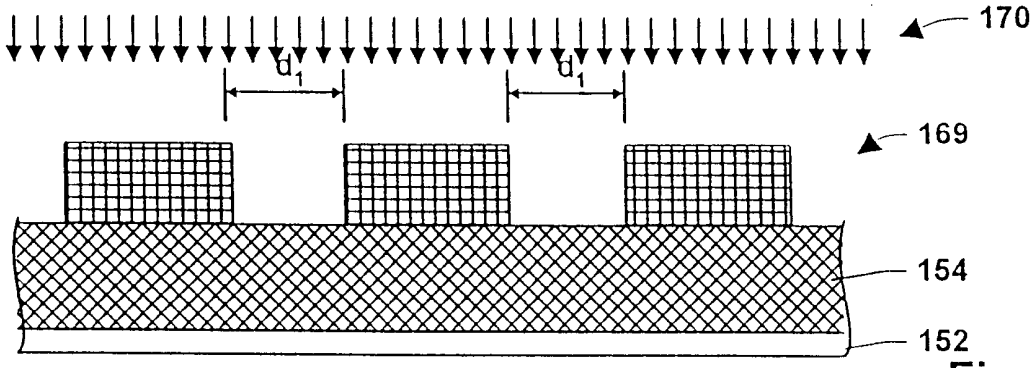

Fig. 6

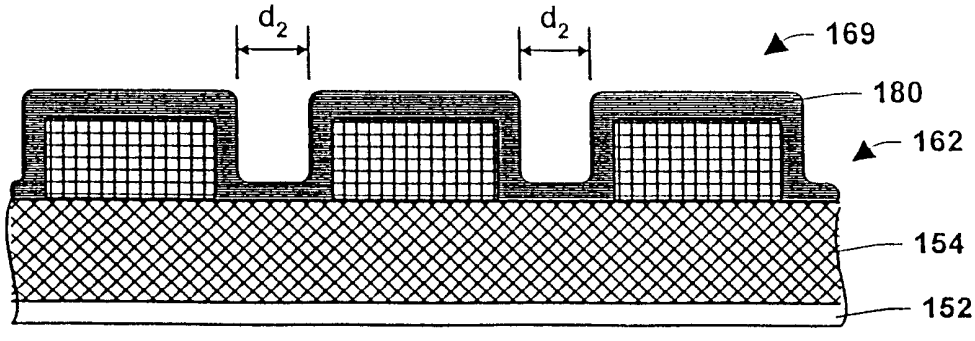

Fig. 7

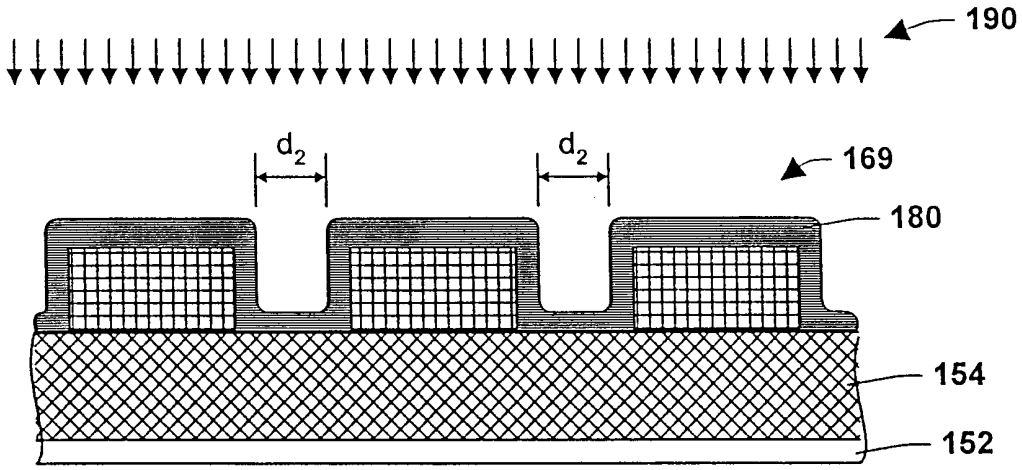

Fig. 8

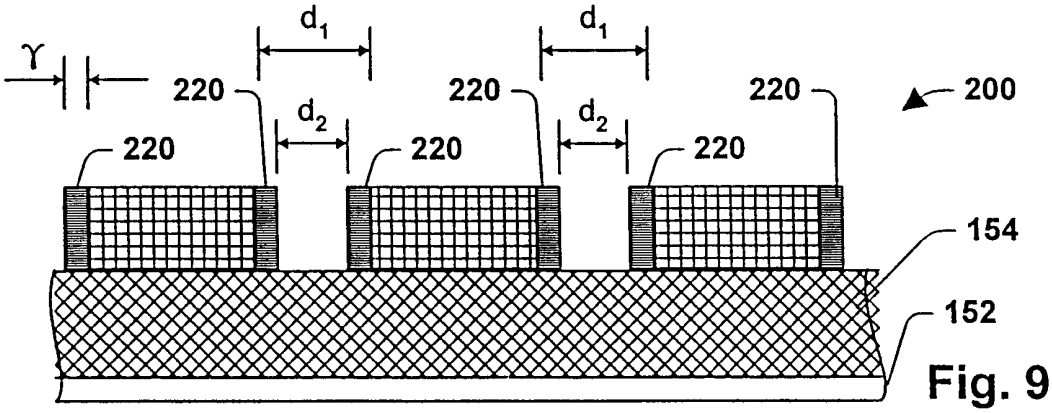

Fig. 9

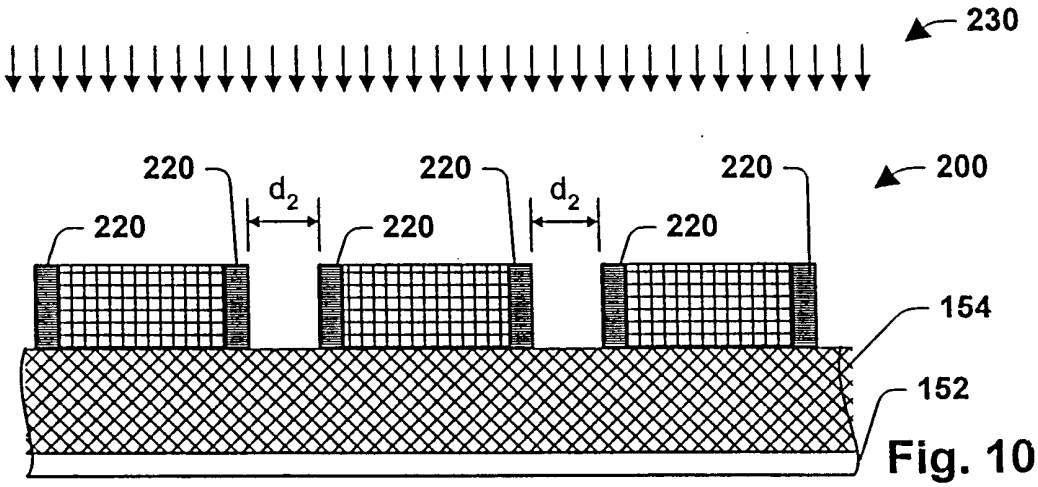

Fig. 10

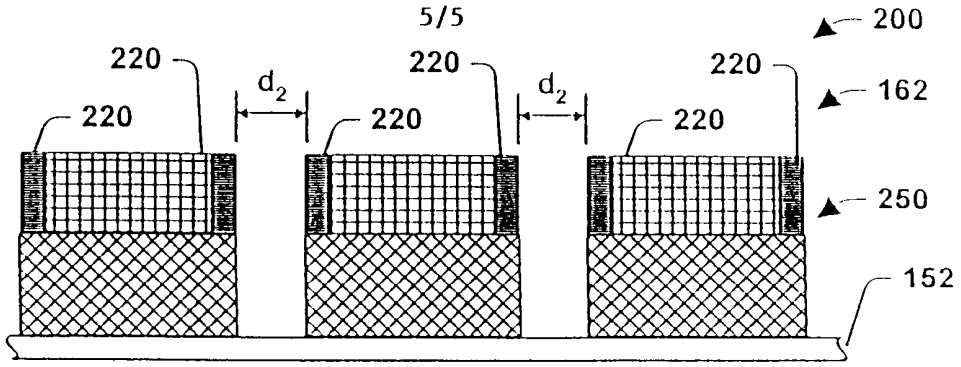

Fig. 11

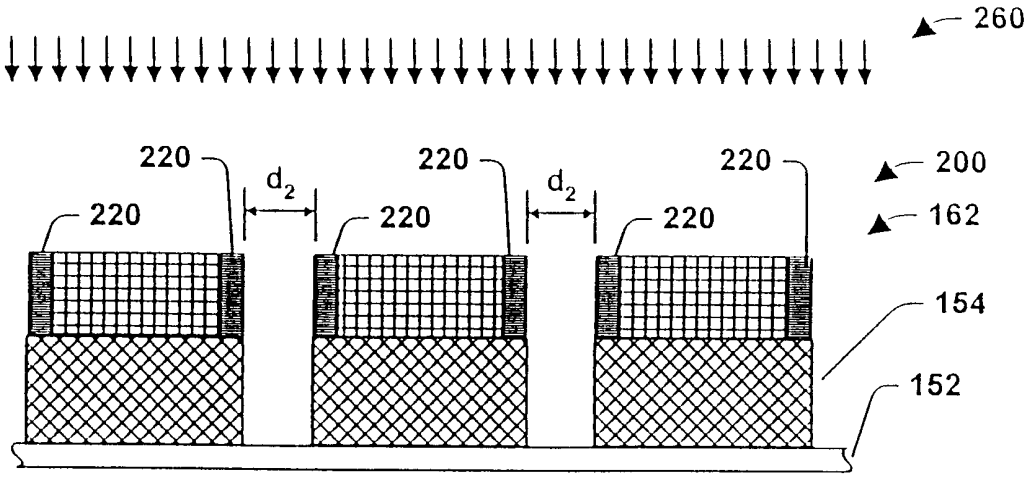

Fig.12

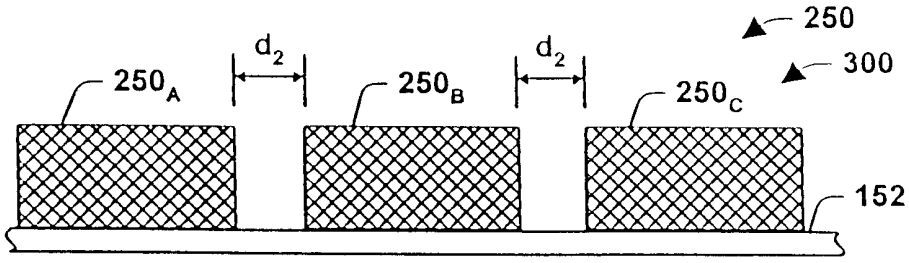

Fig. 13

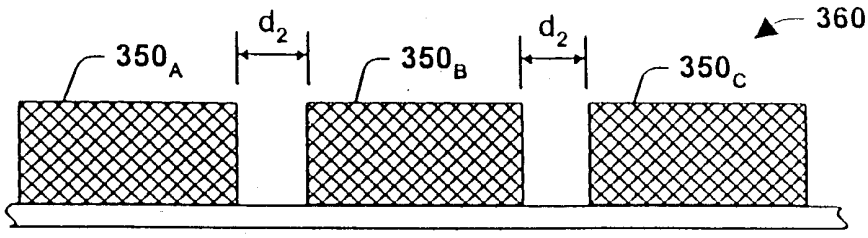

Fig. 14

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/06585

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/033 H01L21/308

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 4 792 534 A (TSUJI HITOSHI ET AL) 20 December 1988 (1988-12-20) column 2 -column 3; figures 1A-1D column 5, line 40 - line 47 ---	1,2,4-6, 8,9 10-13, 16-18,20
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
12 July 2000	20/07/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Szarowski, A

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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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