



(51) International Patent Classification:

H04L 12/10 (2006.01) *H04L 25/02* (2006.01)
H04L 12/40 (2006.01) *H04B 3/54* (2006.01)

(21) International Application Number:

PCT/US2017/042893

(22) International Filing Date:

19 July 2017 (19.07.2017)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

62/366,308	25 July 2016 (25.07.2016)	US
62/458,522	13 February 2017 (13.02.2017)	US
15/653,170	18 July 2017 (18.07.2017)	US

(71) Applicant: **LINEAR TECHNOLOGY CORPORATION** [US/US]; 1630 McCarthy Blvd., Milpitas, California 95035 (US).

(72) Inventor: **GARDNER, Andrew J.**; 1630 McCarthy Blvd., Milpitas, California 95035 (US).

(74) Agent: **OGONOWSKY, Brian D.**; Patent Law Group LLP, PO Box 61839, Sunnyvale, California 94088 (US).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,

CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: COMMUNICATIONS SYSTEM USING HYBRID COMMON MODE CHOKE AND KELVIN SENSING OF VOLTAGE

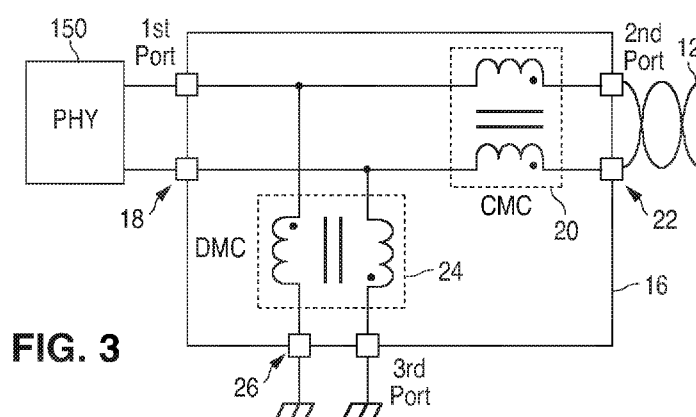


FIG. 3

(57) Abstract: In a communications system that conducts differential data via a pair of wires (12), AC common mode noise is undesirably coupled to the wires (12) in a noisy environment. A hybrid common mode choke, HCMC (16), attenuates the AC common mode noise while passing the differential data to a PHY (150). The HCMC (16) includes a CMC (20) (windings with the same polarity) and a differential mode choke (24) (windings with opposite polarities). The CMC (20) attenuates the AC common mode noise, and the DMC (24) passes the attenuated AC common mode noise to termination circuitry (26) to eliminate it. Also disclosed is a technique for Kelvin sensing the DC voltage at the pair of wires (12), in a PoDL system, by detecting the voltage on wires (12) that do not carry DC current, so as to provide a more accurate measurement.



COMMUNICATIONS SYSTEM USING HYBRID COMMON MODE CHOKE AND KELVIN SENSING OF VOLTAGE

Andrew J. Gardner

5 CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based on and claims priority from United States Provisional Application Serial No. 62/366,308, filed July 25, 2016, by Andrew J. Gardner, and is also based on and claims priority from United States Provisional Application Serial No. 62/458,522, filed February 13, 2017, by Andrew J. Gardner, both applications incorporated
10 herein by reference.

FIELD OF THE INVENTION

One invention relates to communication systems using differential data over a twisted wire pair and, in particular, to techniques for improving the common mode and differential mode loss characteristics. Another invention relates to Power Over Data Lines (PoDL)
15 systems, where power from a Power Sourcing Equipment (PSE) is transmitted to a Powered Device (PD) over a single wire pair that also used for conducting differential data signals, typically Ethernet signals, and enabling a more accurate measurement of voltage in the system.

BACKGROUND

20 It is known to transmit power over data lines to power remote equipment. In this way, the need for providing any external power source for the Powered Devices (PDs) can be eliminated. One form of this technology is Power Over Data Lines (PoDL) where power is transmitted over a single, twisted wire pair along with the differential data. PoDL is likely to become a popular technique, especially in automobiles.

25 Fig. 1 illustrates a known configuration of a PoDL system copied from US 2016/0308683. A media dependent interface (MDI) connector 160 is coupled to a twisted wire pair (not shown) carrying both differential data and a DC voltage. The coupling for both ends of the PoDL system may be identical.

A PHY 150 outputs differential data and receives differential data via the MDI connector 160, a common mode choke (CMC) 210, and AC coupling capacitors C1 and C2. PHY 150 represents the physical layer in the OSI model and is a transceiver that typically includes signal conditioning and decoding circuitry for presenting bits to the next stage. The term PHY is a term of art and is defined by various IEEE standards, depending on the particular application. The PHY is typically an integrated circuit. A digital processor (not shown) is coupled to the PHY 150 for processing the data.

If the circuit of Fig. 1 is on the PSE side, DC voltage from a power source 140 is coupled to the wires by separate inductors 142. The inductors 142 block AC and pass DC.

The wires from the MDI connector 160 are terminated by resistors R1 and R2 and capacitors C3 and C4 to minimize reflections.

Fig. 2 illustrates another prior art circuit where differential data is transmitted through a twisted wire pair 12, and common mode noise is filtered out by the CMC1 and CMC2. Since no DC voltage is conducted, AC coupling capacitors may not be needed.

A CMC is an in-line transformer with two windings in series with the twisted wire pair. As shown by the dots on the CMC windings, the windings have the same polarity, so the magnetic field generated by a differential mode signal is substantially cancelled out. Thus, the CMC presents little inductance or impedance to differential-mode currents. Common-mode currents, however, see a high impedance due to the combined inductance of the windings.

In both configurations, the CMCs ideally eliminate or greatly attenuate common mode RF noise while providing no loss for the differential or DC voltage signals. However, CMCs have constraints which impede their ideal performance. Such constraints include inter-winding capacitance, DC resistance (DCR) of the windings, and core loss. The CMCs must also present to the differential data a low insertion loss and a high return loss.

Some applications need to achieve very low bit error rates in a noisy environment, such as in a factory. Conventional CMCs alone cannot accomplish this without increasing the differential data insertion loss. The user can replace the unshielded twisted wire pair (typically an Ethernet CAT-5 cable) with a shielded cable, but this adds significant expense.

What is needed is a termination technique for differential data communications that provides a more robust technique for filtering out common mode noise.

Additionally, in some PoDL applications, the user requires to know the actual voltage at certain nodes in the system. In some applications, the voltage at the MDI connector is specified. However, this voltage cannot be measured downstream of the CMCs due to the direct current resistance (DCR) of the windings, where variations in DC current vary the losses through the windings. It is not desirable to add more connections to the MDI (possibly carrying a high PoDL current) since this may result in additional parasitic capacitance loading. It would be better to detect the MDI voltage at the PD or PSE without any connection directly at the MDI. What is needed is a technique to accurately detect the MDI voltage at the PSE or PD.

SUMMARY

Two inventions are disclosed herein. One invention is a termination technique for differential data twisted wire pairs that increases the rejection of AC common mode RF noise on the twisted pair. The other invention is a technique for accurately measuring the DC voltage transmitted on a twisted wire pair in a PoDL system.

A hybrid common mode choke (HCMC) is disclosed that has three ports, where each port consists of two terminals. A first port is coupled to a PHY. The second port is a first end of a common mode choke (CMC), where the windings have the same polarity (dots on the same ends). The third port is a first end of a differential mode choke (DMC) having windings with opposite polarities (dots on opposite ends). The second ends of the CMC and DMC are coupled to the first port. The third port is coupled to a suitable termination for AC common mode noise. The HCMC may be a single module.

The CMC has a large common mode impedance and a low differential mode impedance between its two ports. The transmission of an AC common mode signal between the first and second ports is substantially impeded by the CMC, while the transmission of a differential mode signal is not substantially impeded by the CMC. Conversely, the transmission of an AC common mode signal through the DMC to the third port is not substantially impeded by the DMC, while the transmission of an AC differential mode signal is substantially impeded by the DMC. Therefore, the DMC only passes the unwanted AC common mode noise signal to the third port that has already passed through the CMC.

Therefore, the CMC substantially blocks AC common mode noise and the DMC removes any remaining AC common mode noise (diverts the AC common mode noise to the third port).

Since the DMC improves the AC common mode rejection, the CMC windings can have a lower inductance value, reducing the DCR of the CMC windings and improving the overall efficiency of the system by increasing the differential mode return loss of the CMC. Alternatively, the CMC inductance can stay the same and the overall AC common mode rejection may be increased by the shunting action of the DMC.

This allows the use of a conventional twisted wire pair (e.g., a CAT-5 cable) in a noisy environment rather than a more expensive shielded cable.

The third port can be connected to a suitable termination for the AC common mode RF noise in order to reduce reflections, such as ground (if no DC is being conducted by the twisted wire pair) or to capacitors connected to ground, or the third port terminals can be tied together and connected to a single capacitor to ground.

The hybrid CMC substantially improves upon the prior art common mode insertion loss (i.e., reduces common mode noise) while achieving high differential mode return loss and low differential mode insertion loss.

A technique for accurately measuring the DC voltage at the twisted wire pair in a PoDL system is also disclosed. In conventional systems, the voltage from the PSE is detected at the output of the PSE, but high DC currents create voltage drops, such as across the CMC where the windings have a direct current resistance (DCR). So the measured voltage is higher than the voltage actually being applied at the ends of the twisted wire pair.

In a PoDL application, the second port of the HCMC is coupled to a conventional media dependent interface (MDI) connector, which is coupled to a twisted wire pair. To accurately measure the voltage applied to the twisted wire pair, it is sometimes impractical to connect additional wires at the MDI connector and measure the voltage directly at the MDI connector. A solution is to provide AC-coupled termination resistors at the inputs of the MDI connector and measure the voltage between the resistors and their associated capacitors. The AC-coupled termination resistors to ground reduce signal reflections, and substantially no DC current is conducted due to the AC coupling to ground. Therefore, there is no voltage drop across the resistors. Thus, the voltage sensing uses highly accurate Kelvin sensing, since the

sensing is not performed on conductors carrying DC current. Kelvin sensing refers to the voltage detection being done on very low current-carrying wires rather than on high current wires. The voltage sensing may be performed by a conventional voltage sensor in the PSE or PD.

5 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates one end of a conventional PoDL system that enables Ethernet communication and power transmission over a single pair of wires. The other end is identical except for the PSE or PD.

Fig. 2 illustrates CMCs between a PHY and a twisted wire pair, carrying differential
10 data signals, for filtering out common mode noise.

Fig. 3 illustrates a hybrid CMC being used to terminate the wires by coupling the DMC terminals (third port) to ground to improve AC common mode insertion loss.

Fig. 4 illustrates the hybrid CMC being used to terminate the wires by coupling the DMC terminals (third port) to ground via AC coupling capacitors.

15 Fig. 5 illustrates the hybrid CMC being used to terminate the wires by coupling the DMC terminals (third port) together and then to ground via AC coupling capacitors.

Fig. 6 illustrates the hybrid CMC in a PoDL system where the wires are terminated by resistors and AC coupling capacitors between the MDI connector and the CMC.

20 Fig. 7 illustrates a technique applied to the circuit of Fig. 7 for accurately measuring the DC voltage at the MDI connector.

Fig. 8 illustrates another technique for accurately measuring the DC voltage as the MDI connector.

Elements in the various figures that are the same or equivalent are labeled with the same numeral.

25 DETAILED DESCRIPTION

Fig. 3 illustrates the use of a hybrid common mode choke (HCMC) 16. The HCMC 16 has three ports, where each port consists of two terminals. The first port 18 is a first end

of a CMC 20, and a second 22 port is the other end of the CMC 20. If the HCMC 16 is incorporated in a PoDL system, AC coupling capacitors may be coupled between the first port 18 and the PHY 150 (a transceiver). A twisted wire pair 12, for carrying differential data, may be coupled to the second port 22. An MDI connector may be used to connect
5 between the second port 22 and the twisted wire pair 12. The two windings of the CMC 20 have the same polarity (dots are at the second port end), so the CMC 20 impedes (greatly attenuates) common mode noise signals. The first end of the CMC 20 is also coupled to a differential mode choke (DMC) 24 which is a transformer with windings having opposite polarities (dots on opposite ends). The other end of the DMC 24 is the third port 26. The
10 third port 26 may be coupled to a suitable AC termination to minimize reflections.

The DMC 24 blocks AC differential signals generated by the PHY 150 and from the wire pair 12, due to the opposite polarities of the windings.

The HCMC 16 substantially reduces common mode noise on the wire pair 12 while achieving a high differential mode return loss (damps reflections) and low differential mode
15 insertion loss.

The CMC 20 has a large common mode impedance due to its windings having the same polarity, so common mode noise on the wire pair 12 is blocked. The CMC 20 has a low differential mode impedance between its two ports due to its windings having the same polarity, so differential data passes freely. The CMC 20 also freely passes any DC voltage
20 from a PSE voltage source in a PoDL system. If a PoDL system is used, the DC voltage may be connected to the twisted wire pair 12 using the inductors 142 in Fig. 1, or the DC voltage may be connected to the third port 26, where the power supply absorbs the AC common mode noise that passes through the DMC 24

Conversely, by action of the DMC 24, the transmission of an AC common mode
25 signal between the CMC 20 and the third port 26 is not substantially impeded by the DMC 24 while the transmission of an AC differential mode signal is substantially impeded by the DMC 24. In this way, circuitry connected to the third port 26 can be used to substantially eliminate any AC common mode signals that have passed through the CMC 20. Such circuitry connected to the third port 26 may include ground, as shown in Fig. 3, assuming the
30 system is not a PoDL system.

Other circuitry coupled to the third port 28 to terminate the wires and eliminate the AC common mode signals are shown in Figs. 4 and 5. Fig. 4 illustrates the third port 26 being connected to ground via AC coupling capacitors 30 and 32 to terminate the wires and eliminate the AC common mode signals. Fig. 5 illustrates the two terminals of the third port 26 being connected together and then to ground via an AC coupling capacitor 34 to terminate the wires and eliminate the AC common mode signals.

Since the DMC 24 improves the AC common mode rejection, the CMC 20 windings can have a lower inductance value, resulting in a lowering of the DCR of the CMC 20 and improving the overall efficiency of the system. Core loss is also reduced. This also allows the use of a conventional twisted wire pair 12 (e.g., a CAT-5 cable) in a noisy environment rather than a more expensive shielded cable.

A technique for accurately measuring the voltage at the twisted wire pair will now be described with reference to Figs. 6-8. In conventional systems, the DC voltage from the PSE is detected at the output of the PSE, but high DC currents create voltage drops, such as across the CMC where the windings have a direct current resistance (DCR). So the measured voltage is higher than the voltage actually being applied at the ends of the twisted wire pair. Some applications require the accurate measurement of the voltage applied to the twisted wire pair.

Fig. 6 illustrates a PoDL system where AC-coupled termination resistors 40 and 41 are coupled to the terminals of the MDI connector 160 to eliminate reflections on the twisted wire pair 12. A PSE 48 provides a DC voltage on the twisted pair via the DMC 24. No DC voltage flows through the resistors 40 and 41 due to the capacitors 42 and 43 blocking DC. Therefore, there is no DC voltage drop across the resistors 40 and 41.

In cases where the DC voltage at the MDI connector 160 is required to be measured, to accurately measure the voltage applied to the twisted wire pair 12, it is sometimes impractical to connect additional wires at the MDI connector 160 (possibly carrying a high current) and measure the voltage directly at the MDI connector 160.

As shown in Fig. 7, conductors 49 are connected at the nodes between the resistors 40 and 41 and their associated capacitors 42 and 43. The conductors 49 lead to a conventional DC voltage sensing device within the PSE 48. The voltage sensing device may generate an analog or digital signal identifying the voltage, or the sensed voltage is otherwise used for

determining proper operation of the system. In one embodiment, the voltage sensing device is an analog-to-digital converter that generates a digital signal corresponding to the analog voltage.

Thus, the voltage sensing uses highly accurate Kelvin sensing, since the sensing is not performed on conductors carrying DC current. Kelvin sensing refers to the voltage detection being done on very low current-carrying wires rather than on high current wires.

The same Kelvin sensing is done on the PD side, shown in Fig. 7, where the PD 50 contains the DC voltage sensing device, such as for determining if the system meets certain requirements. The DC voltage is tapped off AC-coupled resistors 52 and 53, connected to ground via capacitors 54 and 55, using conductors 56.

Accordingly, the voltage in and out of the twisted wire pair 12 is accurately measured in the PSE or PD using Kelvin sensing at the MDI connector terminals.

The capacitors across the DC voltage terminals of the PSE 48 and PD 50 smooth the DC voltage.

Fig. 8 illustrates another embodiment of the Kelvin sensing, where the DC voltage is tapped from the nodes of the AC-coupled resistors 58 and 59, connected to ground via capacitors 61 and 62. Since no DC current flows through the resistors 58 and 59, there is no voltage drop. Therefore, the DC voltage at the ends of the twisted wire pair 12 is accurately measured.

In Fig. 8, the AC coupling capacitors C1 and C2 couple the AC differential data to the PHY 150, and the CMC 66 at the input of the PHY 150 removes AC common mode noise signals.

The PSE 48 provides DC voltage to the twisted wire pair 12 via a CMC 68 and a DMC 70. Both allow DC voltage to pass, while AC voltage is blocked. An identical configuration is provided on the PD side for measuring voltage at the twisted wire pair 12.

While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects and, therefore, the

appended claims are to encompass within their scope all such changes and modifications that are within the true spirit and scope of this invention.

CLAIMS

What is claimed is:

1. A system for filtering AC common mode signals from a pair of wires carrying differential data comprising:

5 a first port having two first terminals coupled to a transceiver that receives the differential data;

a second port having two second terminals coupled to the pair of wires;

a third port having two third terminals connected to AC termination circuitry;

10 a common mode choke (CMC) coupled between the second port and the first port, the CMC comprising a first transformer with two windings having the same polarity; and

a differential mode choke (DMC) coupled between the first port and the third port, the DMC comprising a second transformer with two windings having opposite polarities,

15 wherein the CMC attenuates AC common mode signals on the pair of wires and substantially passes the differential data, and

20 wherein the DMC substantially passes the AC common mode signals that pass through the CMC from the pair of wires and applies the AC common mode signals to the termination circuitry to further attenuate the AC common mode signals prior to being received by the transceiver.

2. The system of claim 1 wherein the AC termination circuitry comprises a first capacitor coupled between one of the third terminals and a reference voltage, and a second capacitor coupled between another of the third terminals and the reference voltage.

25 3. The system of claim 1 wherein the AC termination circuitry comprises a first capacitor coupled between the two third terminals and a reference voltage.

4. The system of claim 1 wherein the AC termination circuitry comprises the two third terminals connected to a reference voltage.

5. The system of claim 1 further comprising a DC voltage source coupled to the pair of wires via a DC-coupling circuit, wherein the DC voltage source also acts as the AC termination circuitry.

6. The system of claim 5 where the DC-coupling circuit comprises one or more
5 inductors.

7. The system of claim 5 wherein the DC coupling circuit comprises the DMC, and the DC voltage is coupled to the third port.

8. The system of claim 1 wherein the transceiver comprises a PHY coupled to the first port via AC-coupling circuitry.

10 9. The system of claim 8 wherein the AC-coupling circuitry comprises capacitors in series with the two first terminals and the PHY.

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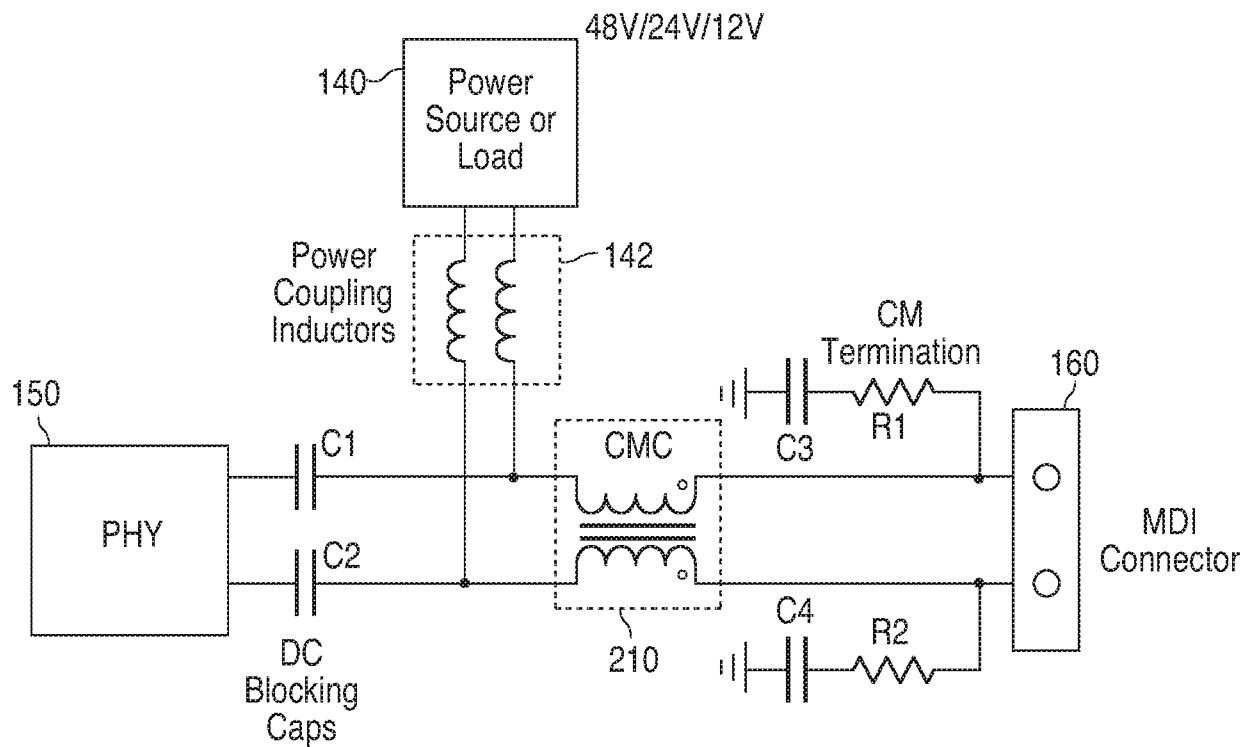


FIG. 1
(PRIOR ART)

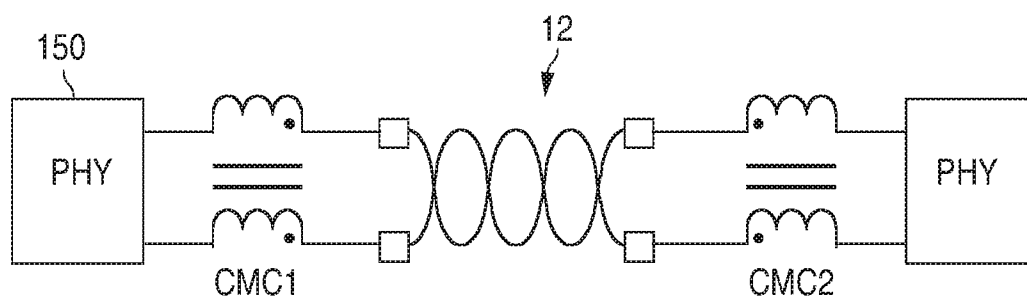
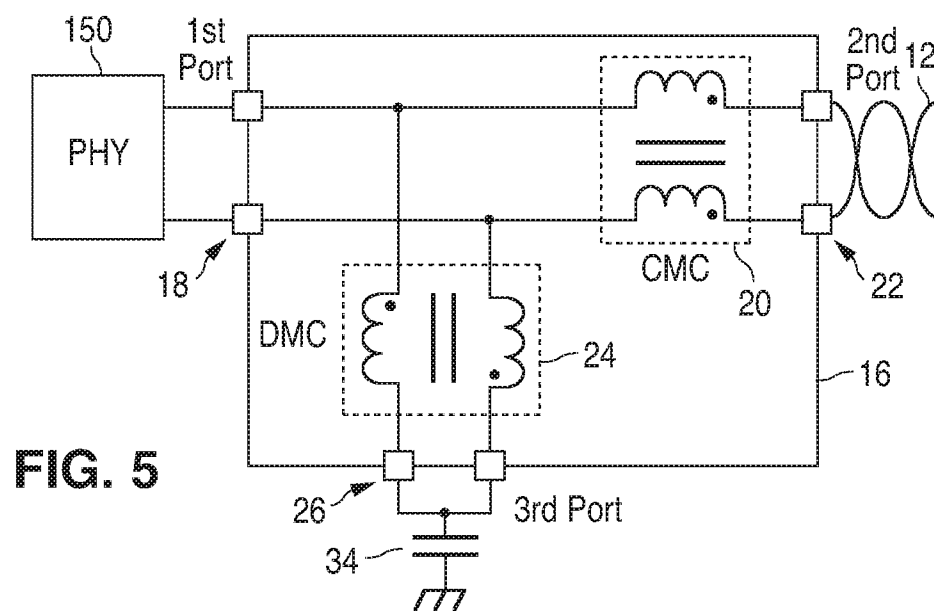
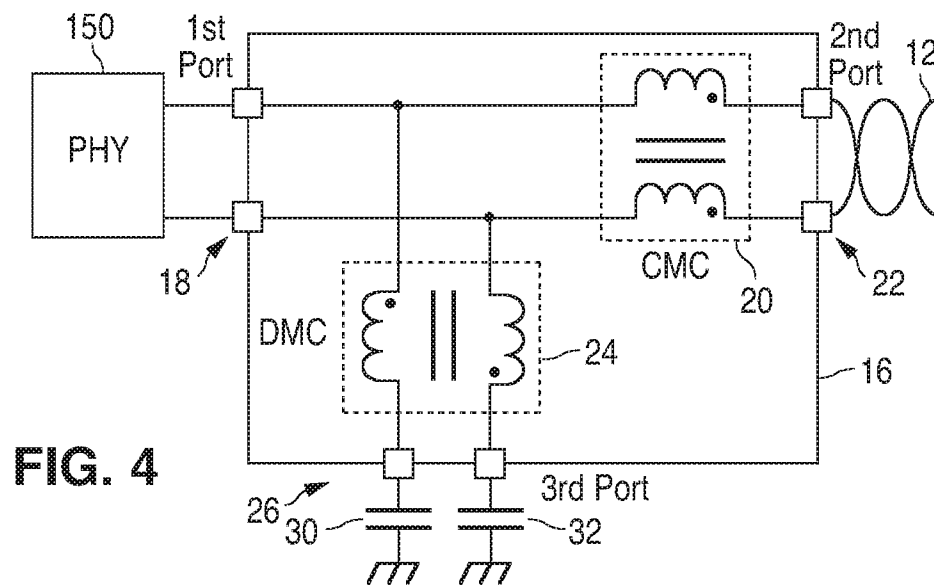
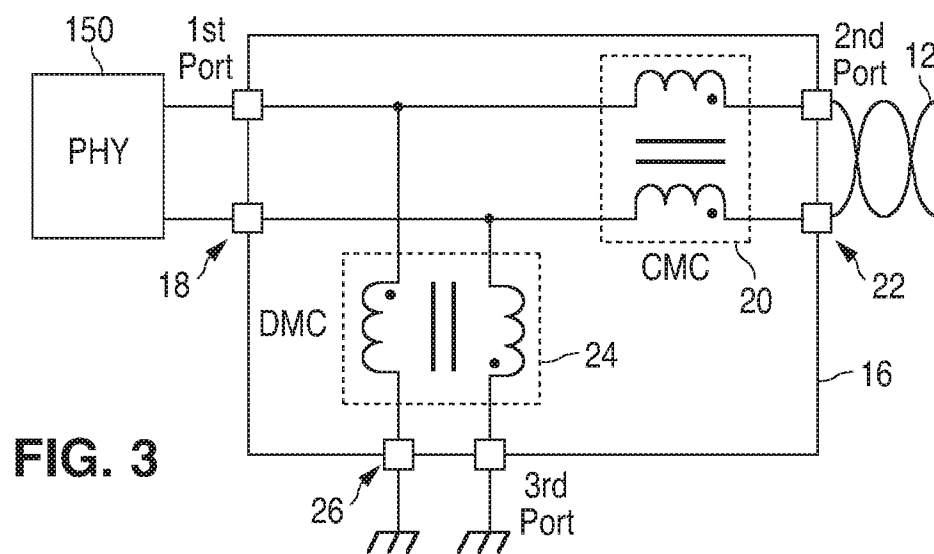
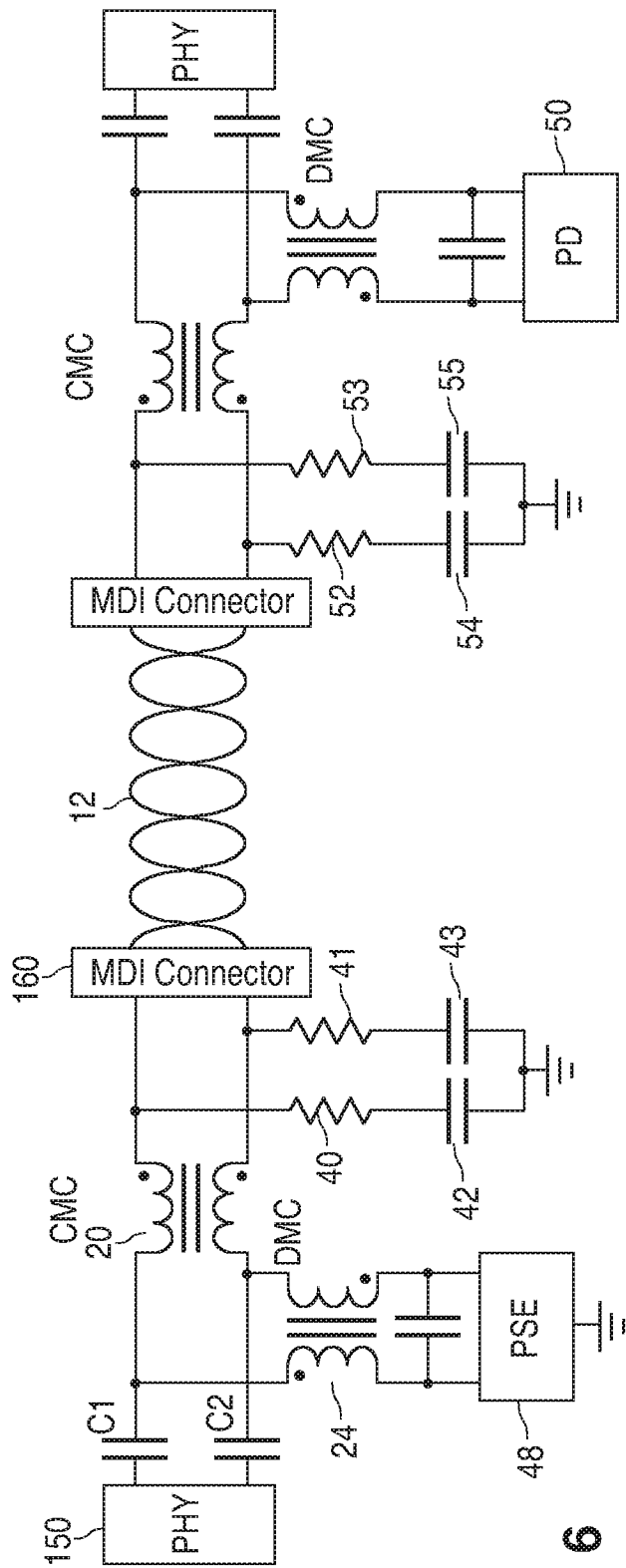
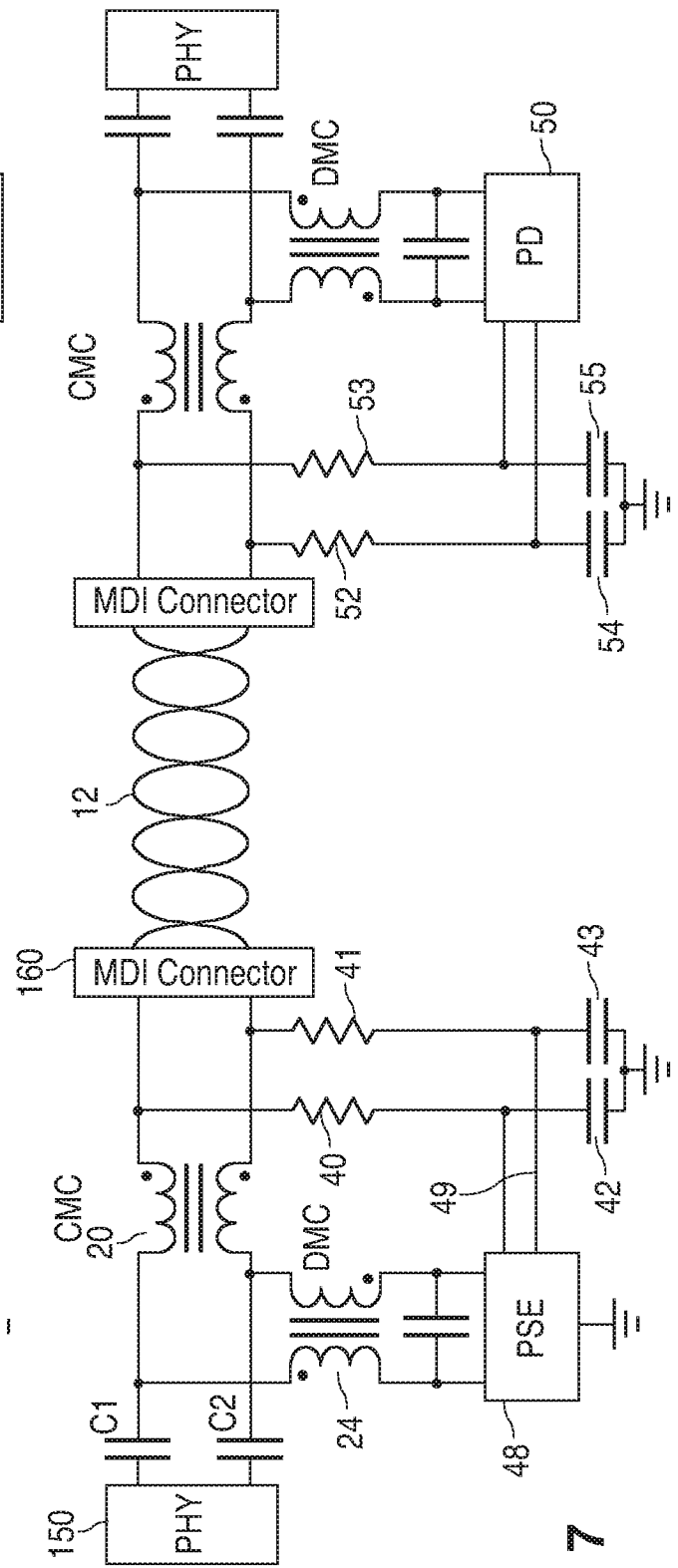


FIG. 2
(PRIOR ART)





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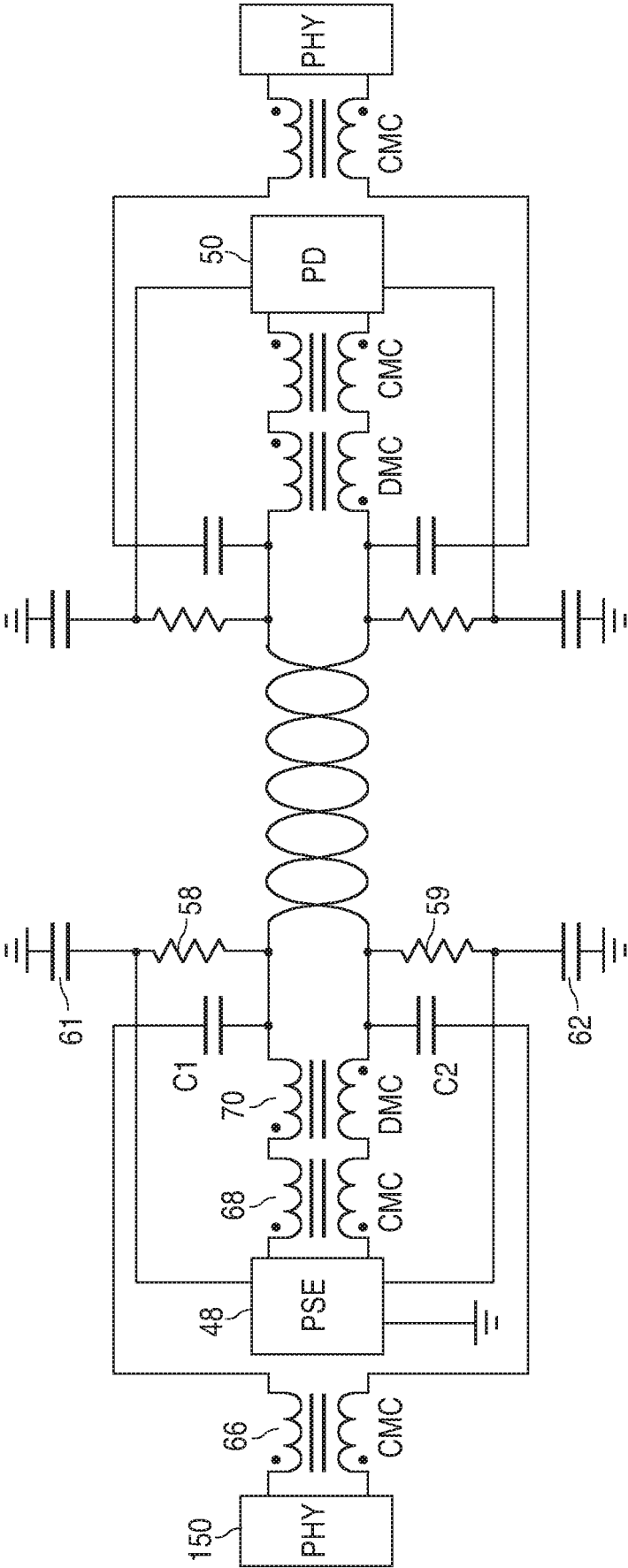


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/042893

A. CLASSIFICATION OF SUBJECT MATTER

INV. H04L12/10 H04L12/40 H04L25/02 H04B3/54
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04L H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2005/025064 A2 (THUNDER CREATIVE TECHNOLOGIES [US]; WASHBURN ROBERT D [US]; MCCLANAHAN) 17 March 2005 (2005-03-17) figure 1G page 8, line 15 - page 10, line 23 page 6, line 16 - line 22 -----	1-9
X	US 6 492 880 B1 (CHIAPPE JIM [US] ET AL) 10 December 2002 (2002-12-10) figure 2 column 2, line 58 - column 3, line 60 -----	1-9
X,P	US 2016/308683 A1 (PISCHL NEVEN [US] ET AL) 20 October 2016 (2016-10-20) cited in the application	1,5-9
A,P	figures 1b,2 -----	2-4

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Further documents are listed in the continuation of Box C.

☒

See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search

20 September 2017

Date of mailing of the international search report

29/09/2017

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Nold, Michael

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2017/042893

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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