



(86) Date de dépôt PCT/PCT Filing Date: 1999/06/30
(87) Date publication PCT/PCT Publication Date: 2000/01/06
(45) Date de délivrance/Issue Date: 2008/08/12
(85) Entrée phase nationale/National Entry: 2000/12/22
(86) N° demande PCT/PCT Application No.: GB 1999/002053
(87) N° publication PCT/PCT Publication No.: 2000/000833
(30) Priorité/Priority: 1998/06/30 (GB9813982.7)

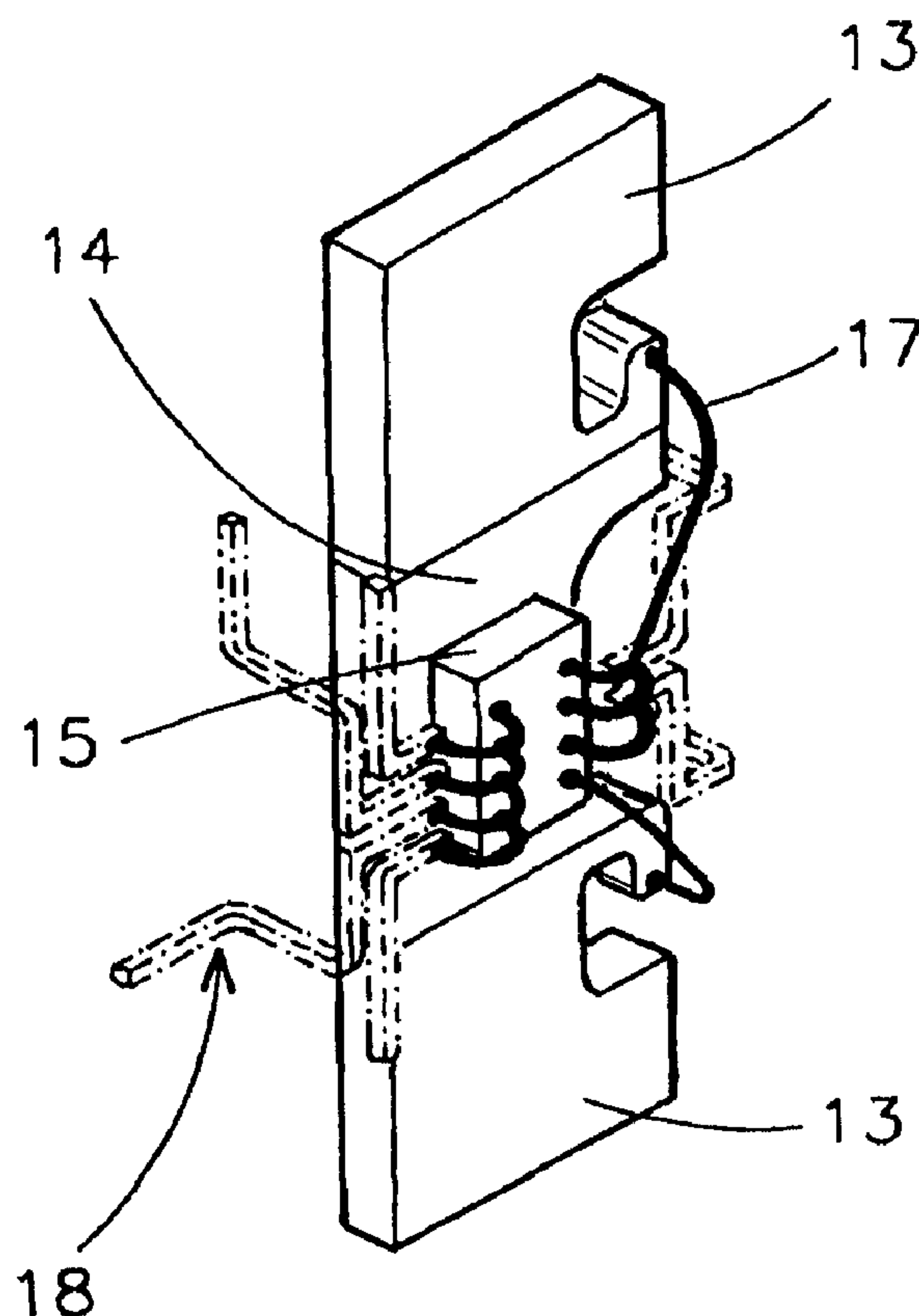
(51) Cl.Int./Int.Cl. *G01R 1/20* (2006.01),
G01R 1/30 (2006.01), *G01R 19/25* (2006.01)

(72) Inventeurs/Inventors:
SKERRITT, ROBERT CHARLES, GB;
CROSIER, MARK DAVID, GB;
MURRAY, MARTIN ANTHONY, GB;
REEDER, BRIAN MARTIN, GB

(73) Propriétaire/Owner:
EATON ELECTRIC LIMITED, GB

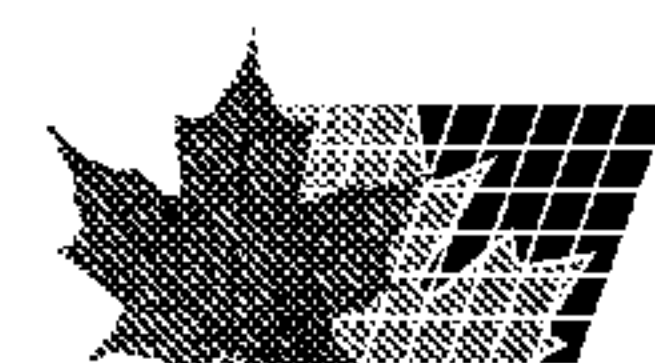
(74) Agent: MARKS & CLERK

(54) Titre : DETECTEUR DE COURANT ET APPAREIL DE MESURE DE COURANT CONTENANT CE DETECTEUR
(54) Title: CURRENT DETECTOR AND CURRENT MEASUREMENT APPARATUS INCLUDING SUCH DETECTOR



(57) Abrégé/Abstract:

A current sensor comprising a rigid metallic link member having two end portions of conductive material and an intermediate portion interconnecting the end portions, said intermediate portion being formed of a resistive material, and an integrated circuit analog to digital converter mounted on said link member, said converter having analog input terminals connected to respective ones of said two end portions and digital output terminals for connection to a processing apparatus.



**PCT**WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

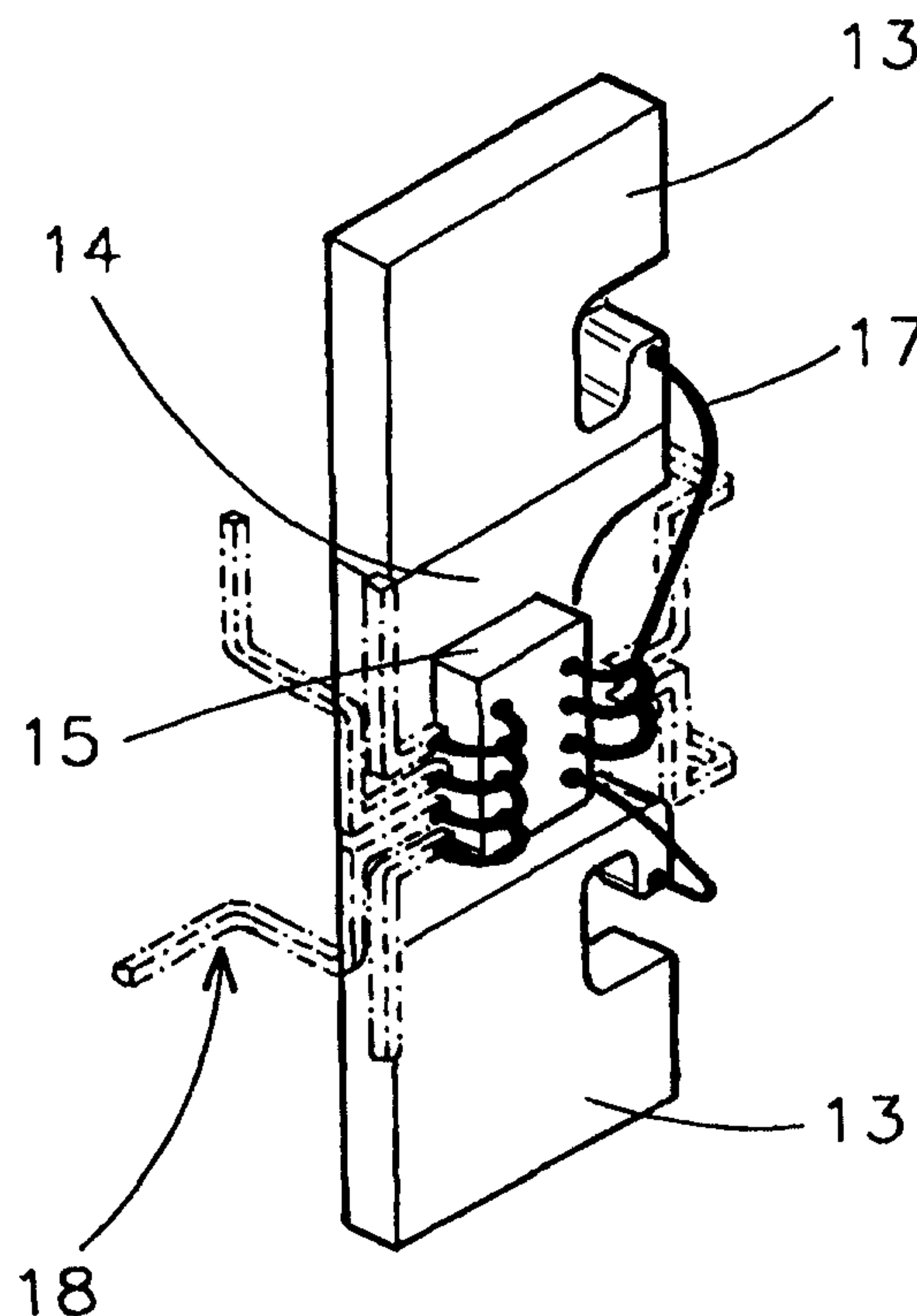
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁷ : G01R 1/20, 1/30	A1	(11) International Publication Number: WO 00/00833 (43) International Publication Date: 6 January 2000 (06.01.00)
<p>(21) International Application Number: PCT/GB99/02053</p> <p>(22) International Filing Date: 30 June 1999 (30.06.99)</p> <p>(30) Priority Data: 9813982.7 30 June 1998 (30.06.98) GB</p> <p>(71) Applicant (for all designated States except US): MEM LIMITED [GB/GB]; Turkey Shore, Holyhead, Anglesey, Gwynedd LL65 2DH (GB).</p> <p>(72) Inventors; and (75) Inventors/Applicants (for US only): SKERRITT, Robert, Charles [GB/GB]; 2 Charleston Close, Penrhyn Bay, Conwy LL30 3HX (GB). CROSIER, Mark, David [GB/GB]; 4 Sunrise Terrace, Gors Avenue, Holyhead, Isle of Anglesey LL65 1PD (GB). MURRAY, Martin, Anthony [GB/GB]; 47 Penrhos Road, Bangor LL57 2AX (GB). REEDER, Brian, Martin [GB/GB]; 'Samona', Lon Crecrist, Trearddur Bay, Isle of Anglesey LL65 2AZ (GB).</p> <p>(74) Agents: CARPENTER, David et al.; Marks & Clerk, Alpha Tower, Suffolk Street Queensway, Birmingham B1 1TT (GB).</p>		<p>(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).</p> <p>Published With international search report.</p>

(54) Title: CURRENT DETECTOR AND CURRENT MEASUREMENT APPARATUS INCLUDING SUCH DETECTOR

(57) Abstract

A current sensor comprising a rigid metallic link member having two end portions of conductive material and an intermediate portion interconnecting the end portions, said intermediate portion being formed of a resistive material, and an integrated circuit analog to digital converter mounted on said link member, said converter having analog input terminals connected to respective ones of said two end portions and digital output terminals for connection to a processing apparatus.



CURRENT DETECTOR AND CURRENT MEASUREMENT APPARATUS INCLUDING SUCH DETECTOR

This invention relates to a current sensor intended for use in an electrical apparatus such as a residual current detection (RCD) device, a current meter or a power meter.

It is an object of the present invention to provide a current sensor in an economical form.

In accordance with the invention there is provided a current sensor comprising a metallic link member having two end portions of conductive material and an intermediate portion interconnecting the end portions, said intermediate portion being formed of a resistive material, and an integrated circuit analog to digital converter mounted on said link member, said converter having analog input terminals connected to respective ones of said two end portions and digital output terminals for connection to a processing apparatus.

Conveniently, the converter is attached to the intermediate portion by a layer of electrically insulative adhesive material and the analog input terminals of the converter are connected to the end portions by wire bonds.

The converter preferably includes a delta-sigma modulator which provides a high frequency one-bit digital data. One or more decimation filtering stages may be included in the converter.

- 2 -

The converter may also have a voltage reference terminal for connection to a reference voltage source, the converter operating to provide digital output signals respectively representing the current flowing through said intermediate portion and digital output signals representing the voltage on one of said end portions.

In the accompanying drawings:

Figure 1 is a perspective view of one example of a current detector in accordance with the invention,

Figure 2 is a sectional view of the detector,

Figure 3 is an elevation of the detector,

Figure 4 is a block diagram of a simple form of an electronic circuit for the detector, and

Figures 5 and 6 are block diagrams of more complex forms of electronic circuits.

The detector shown in Figures 1 to 3 includes a rigid composite conductor strip having two end portions 13 of copper and an intermediate portion 14 of a resistive material such as manganin. The strips are formed by slicing up a sandwich formed by electron beam welding of the copper bars to opposite sides of a manganin bar. The shunts formed by the resistive portions 14 manufactured by this method may have a nominal resistance

of $0.2\text{m}\Omega$ to a tolerance of less than 5%. The resistance of adjacent slices from the sandwich may differ by as little as 2%.

A signal pre-processing Application-Specific Integrated Circuit (ASIC) 15 is mounted on the manganin portion 14 by means of a layer of electrically insulating adhesive 16. Wire leads 17 connect two analog input terminals of the ASIC to respective ones of the copper end portions 13. Further leads connect terminals on the ASIC to conductors of a lead frame 18 parts of which are shown. As shown in Figure 3 the ASIC, the manganin portion, the wire leads and the lead frame conductors are all enclosed within a block 19 of electrically insulating encapsulation material for the protection thereof. Opposite ends of the copper end portions 13 project from the encapsulation block 19.

Turning now to Figure 4, it will be seen that the main block within the ASIC 15 consists of a single delta-sigma modulator 20. There is also an analog input circuit 21 which has its input terminals connected to the copper end portions 13. The output of the ASIC 15 in this case consists of a high frequency one-bit data signal train. In use, the ASIC output is connected via a transformer or other isolation barrier 22 to a processor 23. The processor in this arrangement is configured to carry out one or more decimation filtering operations to convert the one-bit signal stream into a multi-bit digital value at a lower frequency.

The processor 23 may typically be configured to receive signals from a plurality of the detectors and to sum these signals to ascertain whether the current flows through the detectors are balanced. Such an arrangement

can be used for residual current correction allowing an actuator to trip a switch if an unbalanced condition is found to exist.

The processor 23 may alternatively or additionally compare the instantaneous current level with a trip level so that overcurrent tripping can be controlled.

In the alternative embodiment shown in Figure 5, the ASIC is more complex and includes one or more of the decimation filtration stages 24 and a serial output driver 25 to transmit the bits of the multi-bit digital signal produced by the filtration stage 24 serially to the processor. With this arrangement, the configuration of the processor can be simplified as part or all of the decimation filtration operation is carried out in the ASIC.

In the arrangement shown in Figure 6 the ASIC has a further analog input which can be connected to a reference voltage source. Two analog input stages 21a and 21b are present and these feed signals to two independent delta-sigma modulators 20a, 20b. As shown, there are two independent decimation filtration stages 22a, 22b for the two one-bit digital signal streams. The outputs of the stages 22a, 22b may, as shown, be connected to a common serial output stage 25 or (not shown) separate serial output stages may be provided.

It will be appreciated that the arrangement of Figure 6 may be modified by the omission of the two filtration stages 22a, 22b where all filtration is to be carried out by the processor.

- 5 -

Where voltage as well as current is monitored by the processor, precise calibration of the shunts can be achieved. This allows more accurate determination of the current balance in RCD applications. Moreover, as voltage and current are both being monitored to a high level of precision, accurate power consumption metering can be obtained.

Where the devices of the invention are used in RCD and overcurrent trip systems, the processor can be programmed to recognise the transients which may occur when loads are switched in and out of circuit to avoid false tripping. Many other convenient functions can be programmed into the processor, made possible by the high precision of the current measurements capable of being carried out.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A current sensor comprising a metallic link member having two end portions of conductive material and an intermediate portion interconnecting the end portions, said intermediate portion being formed of a resistive material, and an integrated circuit analog to digital converter mounted on said link member, said converter having analog input terminals connected to respective ones of said two end portions and a digital output for connection to a processing apparatus.
2. A current sensor as claimed in claim 1, in which the converter is attached to the link member by means of a layer of electrically insulating adhesive.
3. A current sensor as claimed in claim 1 or 2, in which the converter is attached to the intermediate portion.
4. A current sensor as claimed in claim 1, 2 or 3, in which the analog input terminals of the converter are connected to the end portions by means of wire bonds.
5. A current sensor as claimed in any one of claims 1 to 4, in which the converter has a voltage reference terminal for connection to a reference voltage source and said converter operates to provide digital output signals representing

7

the current through said intermediate portion and digital output signals representing the voltage on one of the end portions.

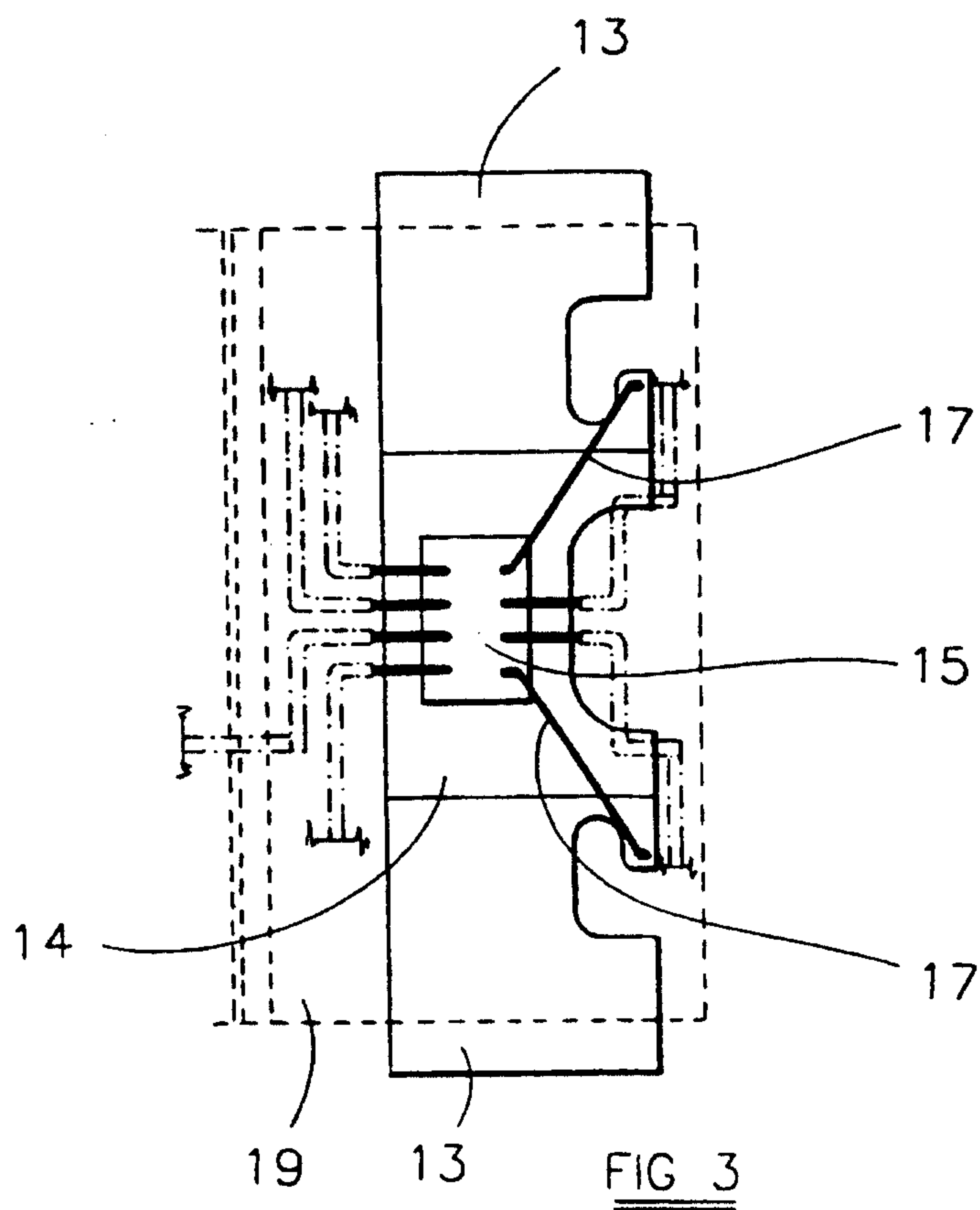
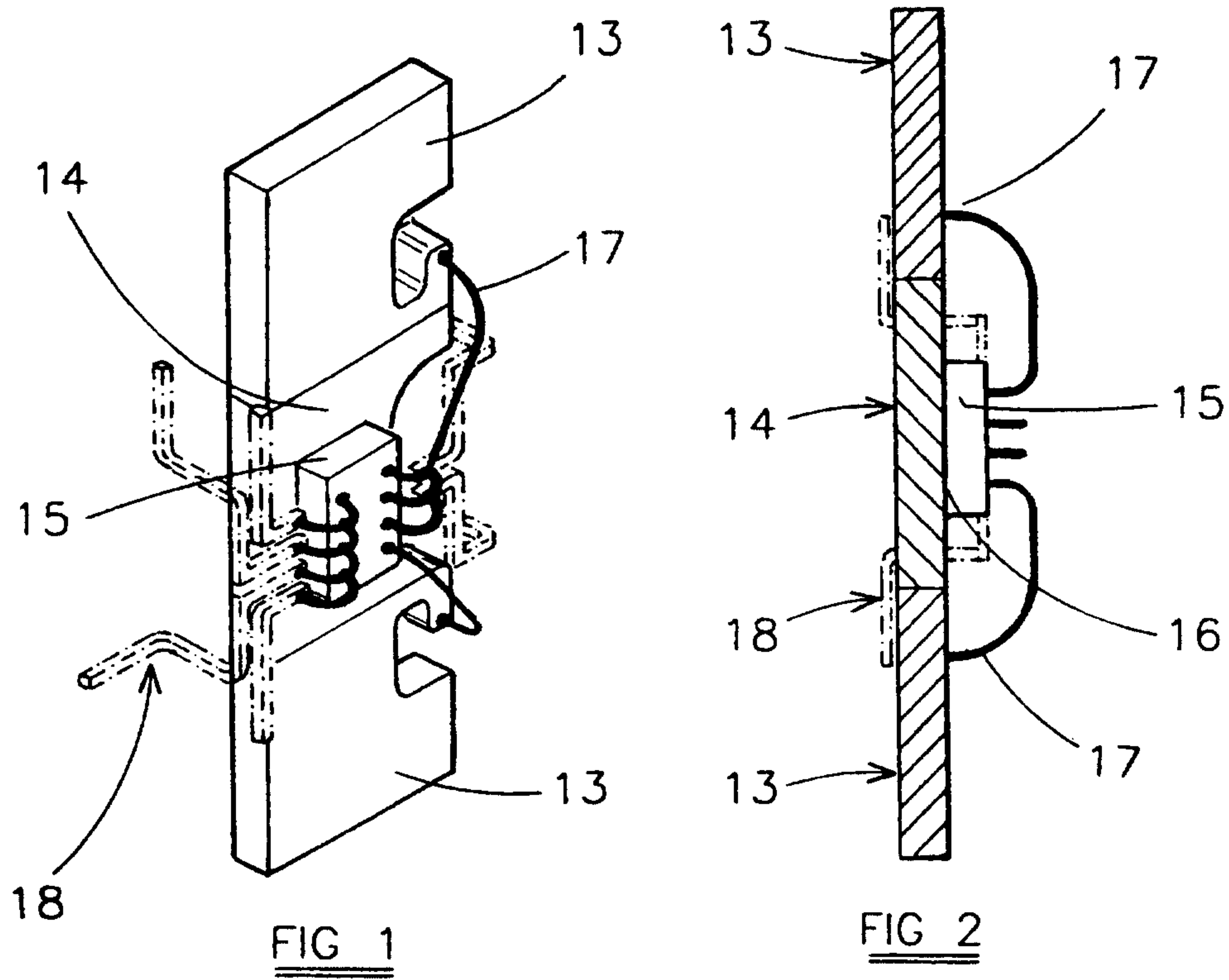
6. A current sensor as claimed in any one of claims 1 to 5, in which said converter includes a delta-sigma modulator which provides a high frequency one-bit digital data stream.

7. A current sensor as claimed in any one of claims 1 to 6, in which the converter also includes at least one decimation filter stage.

8. A current measurement apparatus including at least one current sensor as defined in any one of claims 1 to 7, and a processor circuit connected to receive and process digital signals received from said current sensor.

9. A current measurement apparatus as claimed in claim 8, in which the processor circuit is configured to carry out one or more decimation filtering operations on the received digital signals.

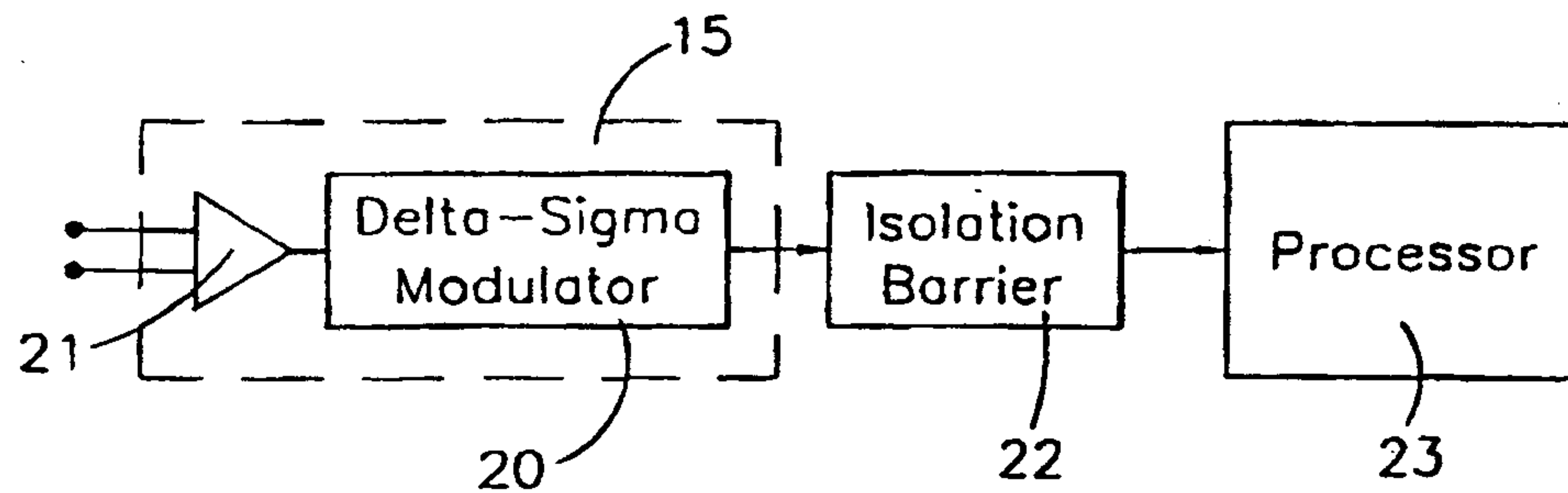
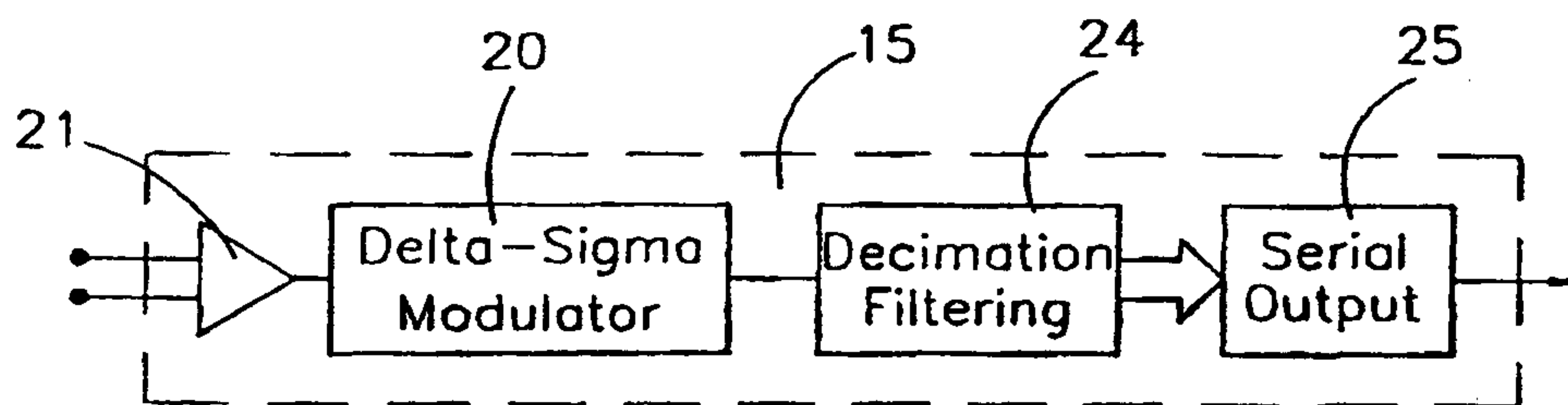
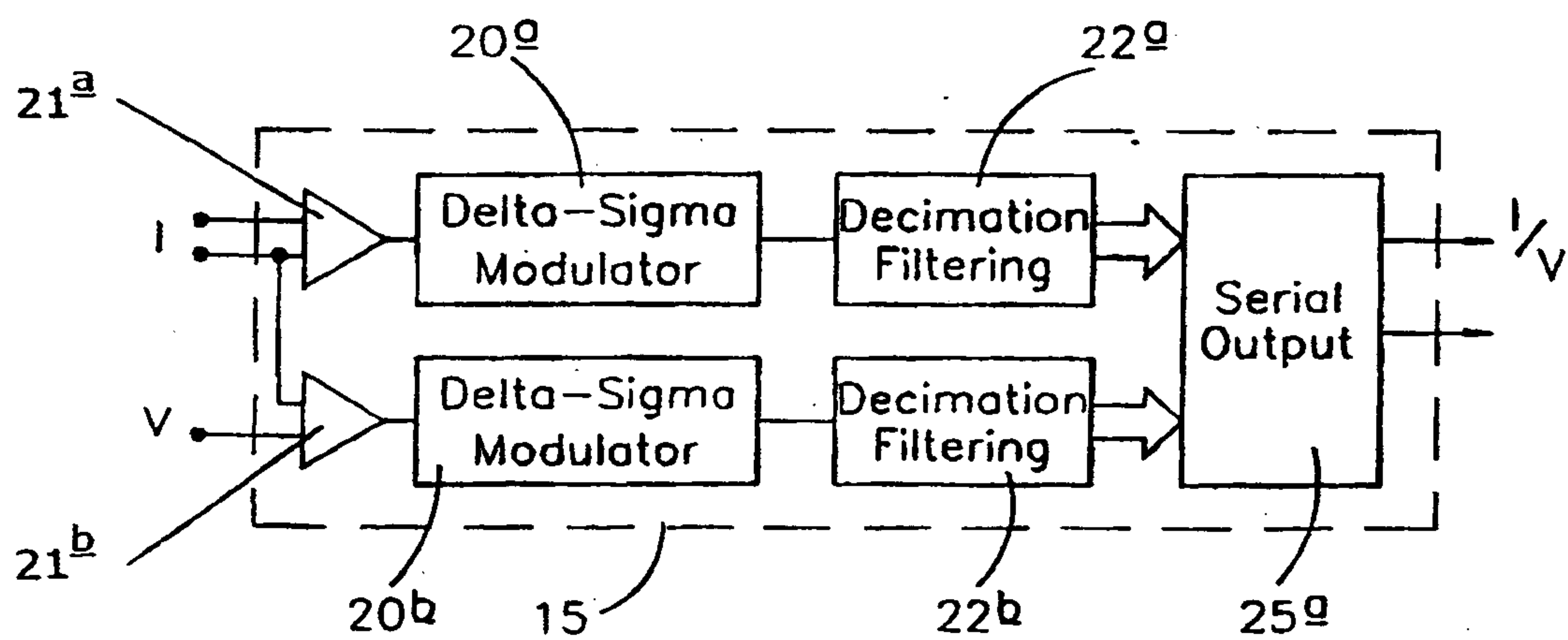
1 / 2



SUBSTITUTE SHEET (RULE 26)

Manuscript & Co.

2/2

FIG 4FIG 5FIG 6

