(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
11 January 2018 (11.01.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/009158 A1

(51) International Patent Classification:
H01L 21/28 (2006.01) *H01L 29/78* (2006.01)
H01L 21/02 (2006.01)

(21) International Application Number:
PCT/US2016/040894

(22) International Filing Date:
02 July 2016 (02.07.2016)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventors; and

(71) Applicants: **CLENDENNING, Scott B.** [CA/US]; 205 SW 97th Avenue, Portland, Oregon 97225 (US). **KIM, Kyoung H.** [KR/US]; 8414 NW Gilliam Lane, Portland, Oregon 97229 (US). **ROMERO, Patricio E.** [CL/US]; 219 SW Valeria View Drive, Portland, Oregon 97225 (US).

(74) Agent: **BRASK, Justin, K.** et al.; Schwabe, Williamson & Wyatt, 1211 SW 5th Ave., Suite 1900, Portland, OR 97204 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: CONFORMAL FILMS INCLUDING METAL GALLIUM CARBIDE AND METAL INDIUM CARBIDE FOR DEVICE APPLICATIONS AND THEIR FABRICATION

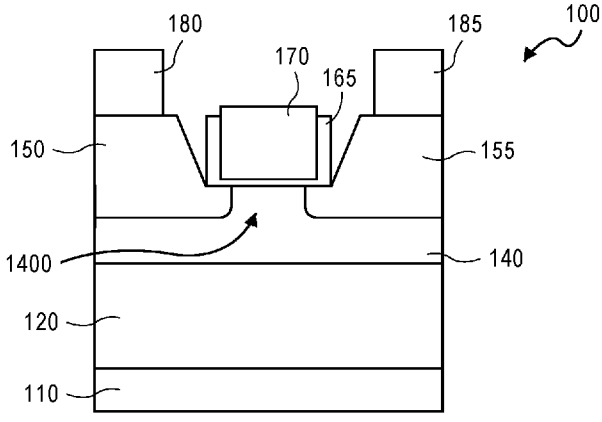


FIG. 1

(57) Abstract: An apparatus including an integrated circuit device structure including a metal layer including a composition of General Formula I: $M\text{-}Al_m\text{-}X^1{}_n\text{-}X^2{}_p\text{-}C_q\text{-}O_r$, wherein M includes a metal selected from one or more of titanium, zirconium, hafnium, tantalum, niobium and vanadium, wherein C includes carbon, wherein X^1 includes gallium, wherein X^2 includes indium, wherein m, n, p, q and r represent an atomic percent of an element in the metal layer that can be 0 percent, with the proviso that n and p cannot each be 0 percent. A method including introducing a first precursor including a metal halide into a chamber including an integrated circuit structure, introducing a second precursor of at least one of an organogallium compound and organoindium compound into the chamber; and depositing a metal including the metal cation of the halide and at least one of gallium and indium.

WO 2018/009158 A1

CONFORMAL FILMS INCLUDING METAL GALLIUM CARBIDE AND METAL INDIUM CARBIDE FOR DEVICE APPLICATIONS AND THEIR FABRICATION

BACKGROUND

Field

Integrated circuit devices.

Description of Related Art

Many conformal work function metal layers or films (e.g., N-type work function metal layers or films) are metal aluminum carbides having the chemical formula of M(Al)C, where M is titanium (Ti), zirconium (Zr), hafnium (Hf), tantalum (Ta), niobium (Nb) and vanadium (V). Such metal layers or films may be formed by an atomic layer deposition (ALD) like process where a metal halide, typically a metal chloride, is pulsed followed by a purge and a pulse of an alkylaluminum coreactant. Known N-type ALD or ALD-like metal aluminum carbide films typically suffer from relatively high resistance, on the order of several thousand micro-ohm-centimeters (μΩ cm) at a thickness of 5-10 nanometers (nm). When used as a gate work function metal or contact metal, such a high resistance can degrade device performance.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a cross-sectional side view of an embodiment of a field effect transistor (FET) device.

Figure 2 shows a perspective side view of a substrate having a sacrificial fin formed therein.

Figure 3 shows the structure of **Figure 2** having a trench dielectric layer on the substrate surrounding the sacrificial fin.

Figure 4 shows the structure of **Figure 3** following the removal of the sacrificial fin to form a trench of a controlled size and shape.

Figure 5 shows the structure of **Figure 4** following the introduction of a buffer material in the trench.

Figure 6 shows the structure of **Figure 5** following a removal of a portion of the buffer material in the trench and the introduction of an intrinsic material into the trench.

Figure 7 shows a cross-sectional side view of the structure of **Figure 6** through line 7-7'.

Figure 8 shows a top side perspective view of the structure of **Figure 6** following the formation of a sacrificial or dummy gate stack on the fin portion of an intrinsic layer extending above a dielectric layer.

Figure 9 shows the structure of **Figure 8** through line 9-9' showing the gate stack of a gate dielectric and a dummy gate on the fin defined by the intrinsic layer.

Figure 10 shows a view of the structure of **Figure 8** through line 10-10' after removing portions of the intrinsic layer corresponding to diffusion or junction regions (source and drain) in the fin.

Figure 11 shows the structure of **Figure 10** following the formation of a source and a drain of the device and a gate stack including a gate dielectric, a liner layer and a gate electrode.

Figure 12 shows a top side perspective view of the gate stack of **Figure 11**.

Figure 13 presents a flow chart of a process of forming the transistor device illustrated in **Figures 2-12**.

Figure 14 describes an embodiment of a flow process for forming a MAlGaC or MAlInC film.

Figure 15 describes an embodiment of a flow process for forming a MGaC or MInC film.

Figure 16 shows top side perspective view of a portion of a semiconductor substrate, such as a portion of a wafer having a sacrificial fin formed thereon and a dielectric material adjacent the sacrificial fin.

Figure 17 shows the structure of **Figure 16** following the removal of a sacrificial fin to form a trench in the dielectric material.

Figure 18 shows the structure of **Figure 17** following the epitaxial growth of alternative layers of nanowires and a sacrificial material according to an aspect ratio trapping (ART) method.

Figure 19 shows the structure of **Figure 18** following a recess of the dielectric material.

Figure 20 shows the structure of **Figure 19** following the introduction of spacers and a sacrificial or dummy gate electrode on the nanowire in a designated channel region of the structure and a dielectric material adjacent the spacers with an implementation of a source and a drain of nanowires on sacrificial material.

Figure 21 shows the structure of **Figure 19** following the introduction of spacers and a sacrificial or dummy gate electrode on the nanowire in a designated channel region of the

structure and a dielectric material adjacent the spacers with an implementation of a source and a drain as nanowires and the sacrificial material removed in designated junction regions.

Figure 22 shows the structure of **Figure 19** following the introduction of spacers and a sacrificial or dummy gate electrode on the nanowire in a designated channel region of the structure and a dielectric material adjacent the spacers with an implementation of a source and a drain as nanowires with a cladding material formed thereon.

Figure 23 shows the structure of **Figure 19** following the introduction of spacers and a sacrificial or dummy gate electrode on the nanowire in a designated channel region of the structure and a dielectric material adjacent the spacers with an implementation of a source and a drain as grown or deposited material replacing the nanowires and sacrificial material in designated junction regions.

Figure 24 shows the structure of **Figure 20** following the removal of a sacrificial gate electrode, leaving the spacers adjacent the junction regions.

Figure 25 shows the structure of **Figure 24** following a removal of sacrificial layer material in the channel region.

Figure 26 shows the structure of **Figure 25** following the introduction of a gate stack on the channel region.

Figure 27 shows a magnified view of the channel region of the structure of **Figure 26**.

Figure 28 is an interposer implementing one or more embodiments.

Figure 29 illustrates an embodiment of a computing device.

DETAILED DESCRIPTION

This disclosure describes an integrated circuit metal layer or film and a method for the deposition of metal layers or films offering tunable compositions and electronic properties such as work function and resistivity. Integrated circuit applications for the metal layer or film are also described.

In one embodiment, a metal layer or film (or metallic layer or film) includes a composition of General Formula I:

$$M\text{-}Al_m\text{-}X^1{}_n\text{-}X^2{}_p\text{-}C_q\text{-}O_r, \quad (I)$$

wherein M includes a metal selected from one or more of titanium (Ti), zirconium (Zr), hafnium (Hf), tantalum (Ta), niobium (Nb) and vanadium (V),

wherein C is carbon,

wherein O is oxygen,

wherein X^1 is gallium,

wherein X^2 is indium, and

wherein m, n, p, q and r represent an atomic percent of an element in the metal layer that can be zero percent, with the proviso that n and p cannot each be zero percent.

The described metal layers or films having the composition of General Formula I include metal gallium carbide (M(Ga)C); metal aluminum gallium carbide (M(Al)(Ga)C); metal gallium indium carbide (M(Ga)(In)C); metal aluminum gallium indium carbide (M(Al)(Ga)(In)C); metal aluminum indium carbide (M(Al)(In)C); and metal indium carbide (M(In)C) with the individual elements of the films being present in atomic percent ranges as defined below and optionally including oxygen at a level up to 5 atomic percent (0 to 5 atomic percent oxygen). Representative uses for such metal layers or films as an integrated circuit metal layer include, but are not limited to, as a gate electrode and as a contact to transistor devices (e.g., a contact to a source or drain). In terms of a gate electrode metal, a work function gate electrode metal based on a metallic film having the composition of General Formula I can be an order of magnitude less resistive than titanium aluminum carbide (TiAlC) layers or films and offer a range of tunability for flatband voltage.

In one embodiment, metal layers or films having the composition of General Formula I include constituents in the following ranges:

Carbon: 0.1 to 70 atomic percent;

Metal (one or more of Ti, Zr, Hf, Ta, Nb, V): 10 to 60 atomic percent;

Aluminum: 0 to 35 atomic percent;

Gallium: 0 to 70 atomic percent (only 0 atomic percent if indium present but can be present with indium);

Indium: 0 to 70 atomic percent (only 0 atomic percent if gallium present but can be present with gallium); and

Oxygen: 0 to 5 atomic percent.

In one embodiment, metal layers or films of having the composition of General Formula I including metal gallium carbide (M(Ga)C); metal aluminum gallium carbide (M(Al)(Ga)C); metal gallium indium carbide (M(Ga)(In)C); metal aluminum gallium indium carbide (M(Al)(Ga)(In)C); metal aluminum indium carbide (M(Al)(In)C); and metal indium carbide (M(In)C) where M may be one or more metals selected from Ti, Zr, Hf, Ta, Nb and V and the atomic percent of individual elements in the film are as specified above and optionally including oxygen at a level up to 5 atomic percent (0 to 5 atomic percent oxygen), may be formed by an atomic layer deposition (ALD) process. In one embodiment of a

process, a metal halide is pulsed onto a surface of a heated substrate in a chamber such as a wafer that has features thereon including possibly features that are relatively narrow and/or have relatively high aspect ratios. The metal halide pulse is followed by a purge then an option pulse of an organoaluminum co-reactant follwed by a purge and a pulse of an organogallium or organoindium coreactant and purge. In some embodiments, a final pulse of the other of an organogallium or organoindium coreactant followed by a purge may terminate the pulse sequence such that both gallium and indium may be incorporated into the film. In processes where both are used, the organogallium and organoindium coreactants may be introduced in any order but after the organoaluminum coreactant if it is used. The sequential pulsing of coreactants produce a film on the substrate resulting in the composition of General Formula I. The sequential pulsing of reactants continues until a layer or film of a desired thickness is formed on the substrate. Without wishing to be bound by theory, it is believed that the exposure of a film surface to organogallium and/or organoindium improves overall transmetallization, eliminating metal halide bonds and leading to an air stable, low resistivity film.

Figure 1 shows a cross-sectional side view of an embodiment of a field effect transistor (FET) device such as N-type metal oxide semiconductor FET (MOSFET) or P-type MOSFET. Referring to **Figure 1**, device 100 includes substrate 110 that is, for example, a single crystal silicon substrate. Disposed on substrate 110, in this embodiment, is buffer layer 120. Examples of a suitable material for buffer layer 120 include, but are not limited to, one or more of silicon germanium or a group III-V compound semiconductor material such as gallium arsenide (GaAs), indium aluminum arsenide (InAlAs), gallium antimony (GaSb), indium phosphide (InP), indium aluminum phosphide (InAlP) and gallium aluminum antimony (GaAlSb). A representative thickness of buffer layer 120 is on the order of 150 nanometers (nm) to 250 nm.

As illustrated in **Figure 1**, disposed on buffer layer 120 is intrinsic layer 140. Intrinsic layer 140, in one embodiment, is silicon, germanium (e.g., n-doped germanium, intrinsic germanium), silicon germanium or a group III-V compound semiconductor material such as but not limited to indium gallium arsenide (InGaAs), indium phosphide (InP), indium arsenide (InAs), and indium gallium antimony (InGaSb). Intrinsic layer 140, in one embodiment, is selected of a material desired for a channel of the transistor device as the intrinsic layer will include the channel of the device.

Formed in intrinsic layer 140 is diffusion or junction region or source 150 and diffusion or junction region or drain 155. In one embodiment, source 150 is an n^+ source of

an NMOSFET and drain 155 is an n^+ drain. In one embodiment, each of source 150 and drain 155 are, for example, a germanium (e.g., n-doped) or a group III-V compound semiconductor material. Representative examples of a group III-V compound semiconductor material for an NMOSFET include but are not limited to indium arsenide (InAs), indium antimony (InSb), and InGaAs. For an embodiment, where source 150 is a p+ source and drain 155 is a p+ drain of a PMOSFET, each of source 150 and drain 155 are, for example, boron-doped germanium. Disposed between source 150 and drain 155 is channel 1400 of intrinsic layer 140. In one embodiment, channel 1400 is undoped (electrically neutral or doped with less than 5E17 carriers of either type).

Overlying channel 1400 is gate dielectric layer 165 of, for example, a silicon dioxide or a dielectric material having a dielectric constant greater than silicon dioxide (a high k material) or a combination of silicon dioxide and high k material or multiple high k materials. Disposed on gate dielectric layer 165 is gate electrode 170. In one embodiment, gate electrode 170 is a layer or film represented by the composition of General Formula I. Respective metal layers or films for gate electrode 170 include metal gallium carbide (M(Ga)C); metal aluminum gallium carbide (M(Al)(Ga)C); metal gallium indium carbide (M(Ga)(In)C); metal aluminum gallium indium carbide (M(Al)(Ga)(In)C); metal aluminum indium carbide (M(Al)(In)C); and metal indium carbide (M(In)C), where M may be one or more metals selected from Ti, Zr, Hf, Ta, Nb and V and the atomic percent of individual elements in the film are as specified above and optionally including oxygen at a level up to 5 atomic percent (0 to 5 atomic percent oxygen), may be formed by an atomic layer deposition (ALD) process. In one optional embodiment, disposed between gate electrode 170 and gate dielectric layer 165 is a barrier layer (not shown) of a material that may provide an adhesive property for the gate electrode and/or inhibit interaction between gate electrode 170 and gate dielectric layer 165. Suitable materials for a barrier layer include, but are not limited to, titanium nitride (TiN), manganese nitride (MnN), niobium nitride (NbN), zirconium nitride (ZrN) or tantalum nitride (TaN). A representative thickness for a barrier layer is on the order of 0.1 nm to a few nanometers.

Figure 1 also shows contact 180 to source 150 and contact 185 to drain 155. In one embodiment, one or both of contact 180 and contact 175 is a layer or film represented by the composition of General Formula I. In another embodiment, one or both of contact 180 and contact 185 are titanium (Ti), tungsten, or a nitride of titanium or tungsten.

Figures 2-12 describe a process for forming an FET such as illustrated in **Figure 1**. **Figure 13** presents a flow chart of the process. **Figures 2-12** describe a three-dimensional

multi-gate FET including metal film of the composition of General Formula I as a gate electrode and optionally as a contact metal to one or both of a source and a drain of the transistor. The concept of including a metal film of, for example, metal gallium carbide (M(Ga)C); metal aluminum gallium carbide (M(Al)(Ga)C); metal gallium indium carbide (M(Ga)(In)C); metal aluminum gallium indium carbide (M(Al)(Ga)(In)C); metal aluminum indium carbide (M(Al)(In)C); and metal indium carbide (M(In)C) as a gate electrode material and/or as a contact structure can similarly be applied to planar transistors and gate all around transistors. Referring to **Figure 2** and with reference to the flow chart of **Figure 13**, the process begins by defining sacrificial fin structures in a substrate material (block 310, **Figure 13**). **Figure 2** shows a perspective side view of structure 200 of substrate 210 that may be any material that may serve as a foundation of which a multi-gate FET may be constructed. Representatively, substrate 210 is a portion of a larger substrate such as wafer. In one embodiment, substrate 210 is a semiconductor material such as single crystal silicon. Substrate 210 may be a bulk substrate or, in another embodiment, a semiconductor on insulator (SOI) structure. **Figure 2** shows substrate 210 following a patterning of the substrate to define sacrificial fin 2100. Sacrificial fin 2100 may be one of many sacrificial fins formed in the substrate. Sacrificial fin 2100 may be formed by a mask and etch process wherein a mask (e.g., a hard mask) is introduced on a surface (superior surface) of substrate 210 to protect areas of the substrate where the sacrificial fins will be defined and to provide openings in non-fin areas. Once the mask is patterned, substrate 210 may be etched to remove material in unprotected areas. A substrate of silicon may be etched with a wet or dry etch. Representatively, a suitable etchant is HF based chemistry. In one embodiment, sacrificial fin 2100 is etched to have a height, H, on the order of 100 nanometers (nm) to 400 nm.

Figure 3 shows structure 200 of **Figure 2** following a removal of the mask on the fin and following the deposition of a trench dielectric layer on the substrate (block 315, **Figure 13**). In one embodiment, dielectric layer 215 is silicon dioxide or a low-k dielectric material. Following deposition of dielectric layer 215, a surface of the structure (a superior surface as viewed) is polished to the level of the top of sacrificial fin 2100 so that the fin is exposed.

Figure 4 shows structure 200 of **Figure 3** following the removal of sacrificial fin 2100 to form a trench of a controlled size and shape (block 320, **Figure 13**). The sacrificial fin may be removed by a mask and etch process wherein a mask is patterned on a surface of dielectric layer 215 leaving sacrificial fin 2100 exposed followed by an etch process to remove the fin. Sacrificial fins of a silicon material may be etched by a dry or wet etch or a

combination of the two. Suitable etchants for etching sacrificial fins of a silicon material include potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH). The removal of the sacrificial fin forms trench 218. In one embodiment, the etching of the sacrificial fin may be performed to provide a {111} faceting at the bottom of trench 218 to facilitate a growth of a group III-V compound material in the trench which is done using TMAH-like or any equivalent chemistry. Alternative geometries are also contemplated.

Figure 5 shows structure 200 of **Figure 4** following the introduction of a buffer material in trench 218 (block 322, **Figure 13**). In one embodiment, buffer material 220 is silicon germanium, germanium or a group III-V compound semiconductor material such as, but not limited to, gallium arsenide (GaAs), indium phosphide (InP); germanium (Ge), gallium phosphide (GaP), gallium arsenide antimony (GaAsSb), indium aluminum arsenide (InAlAs) and gallium antimony (GaSb). The buffer material may be introduced by an epitaxial growth process. In another embodiment, the trenches may be filled with a first buffer material of one of the noted materials as, for example, a nucleation layer at a base of trench 218 followed by a second buffer material of another of the noted materials. The trench confined growth of a buffer material or materials offer an advantage of aspect ratio trapping (ART) whereby crystalline quality of the epitaxial layer(s) is enhanced through trapping of threading dislocations, stacking faults, twins, etc., at sidewalls of a trench where defects terminate such that overlying layers may be increasingly defect-free. **Figure 5** shows buffer material 220 in trench 218. The buffer material has a dimension measured in z direction on the order of 100 nm to 400 nm. **Figure 5** representatively shows buffer material 220 including {111} faceted overgrowth protruding off the superior plane defined by dielectric layer 215.

Figure 6 shows structure 200 of **Figure 5** following a removal of a portion of buffer material 220 in trench 218 and the introduction of an intrinsic material into the trench. In one embodiment, the removal of buffer material 220 is performed by an etch to recess the buffer material in the trench (block 324, **Figure 13**). A suitable etchant for buffer material 220 is TMAH or any equivalent chemistry.

Figure 6 shows intrinsic layer 240 formed on buffer material 220 (block 326, **Figure 13**). The intrinsic layer may be epitaxially grown. In one embodiment, intrinsic layer 240 is silicon, silicon germanium, intrinsic germanium, doped germanium, or a group III-V compound semiconductor material such as an indium-containing group III-V compound material (e.g., InGaAs). Intrinsic layer 240 has a representative height on the order of 40 nm to 100 nm. **Figure 6** shows the structure following a polish of the intrinsic layer to a plane

defined by dielectric layer 215 and after a recession of dielectric layer 215 such that the intrinsic layer is protruding above a plane defined by dielectric layer 215 as a fin structure (block 330, **Figure 13**). **Figure 7** shows a cross-sectional side view of the structure of **Figure 6** through line 7-7'. A representative height of the exposed fin is representatively on the order of 500 angstroms (Å).

Figure 8 shows a top side perspective view of structure 200 of **Figure 6** following the formation of a sacrificial or dummy gate stack on fin portion of intrinsic layer 240 extending above dielectric layer 215 (block 340, **Figure 13**). In one embodiment, a gate stack includes gate dielectric layer 260 of, for example, silicon dioxide or a high k dielectric material. Disposed on gate dielectric layer 260, in one embodiment, is dummy gate 265 of, for example, polysilicon deposited by, for example, a chemical vapor deposition method. In one embodiment, prior to forming the gate stack, a dielectric layer of silicon dioxide or a low k material is introduced on the structure (shown in dashed lines). To form the gate stack, a mask material is introduced over the structure on the dielectric layer and patterned to have an opening for the gate stack. The gate stack is then introduced in the opening. The gate stack may include a spacer dielectric layer defining spacers 285 on opposite sides thereof.

Figure 9 shows structure 200 of **Figure 8** through line 9-9' showing the gate stack of gate dielectric 260 and dummy gate 265 on the fin defined by intrinsic layer 240. **Figure 10** shows a view of the structure of **Figure 8** through line 10-10' after removing portions of intrinsic layer 240 corresponding to diffusion or junction regions (source and drain) in the fin. Representatively, areas of intrinsic layer 240 corresponding to the diffusion or junction regions of the fin are exposed in the dielectric layer and an etch of the exposed areas is performed (an etch under-cut (EUC)) to remove intrinsic layer material leaving voids (block 350, **Figure 13**).

Figure 11 shows structure 200 of **Figure 10** following the formation of a source and a drain of the device (block 360, **Figure 13**). Source 250 and drain 255, in one embodiment, are a silicon-doped group III-V compound material suitable for an NMOSFET. Examples include but are not limited to InAs, InSb and InGaAs. For a PMOSFET, source 250 and drain 255, in one embodiment, are a boron-doped germanium. Silicon germanium and germanium may also be used on silicon, silicon germanium and germanium channel devices. In one embodiment, a material for source 240 and drain 250 is epitaxial grown.

Following formation of source 250 and drain 255, a dielectric material is introduced on the structure (on a surface including junction regions 240 and 250 and sacrificial gate 265). In one embodiment, the dielectric material is silicon dioxide or a low k material or a

combination of materials (e.g., multiple low k materials or silicon dioxide and one or more low k materials). **Figure 11** shows dielectric material 245 in dashed lines. Sacrificial gate 265 and gate dielectric are then removed and replaced with a gate dielectric of silicon dioxide, a high-k material such as Al_2O_3, ZrO_2 or HfO_2 or a combination of silicon dioxide and a high-k material. This is followed by the introduction of an optional barrier layer of titanium nitride (TiN), manganese nitride (MnN), niobium nitride (NbN), zirconium nitride (ZrN) or tantalum nitride (TaN) and then a gate electrode such as a metal gate electrode (block 370, **Figure 13**). A barrier layer has a representative thickness of 0.5 nm to 10 nm and may be introduced by ALD or chemical vapor deposition techniques. **Figure 11** shows the structure including gate dielectric 270, barrier layer 272 and gate electrode 275. **Figure 12** shows a top side perspective magnified view of the gate stack between spacers 285. Representative materials for gate electrode 275 include metal films having the composition of General Formula I. The described metal layers or films include metal gallium carbide (M(Ga)C); metal aluminum gallium carbide (M(Al)(Ga)C); metal gallium indium carbide (M(Ga)(In)C); metal aluminum gallium indium carbide (M(Al)(Ga)(In)C); metal aluminum indium carbide (M(Al)(In)C); and metal indium carbide (M(In)(C), where M is one or more of Ti, Zr, Hf, Ta, Nb and V and the atomic percent of individual elements in the film are as specified above and optionally including oxygen at a level up to 5 atomic percent (0 to 5 atomic percent oxygen). A representative thickness of gate electrode 275 is on the order of 0.5 nm to 25 nm.

In one embodiment, gate electrode 275 of a metal film or layer having the composition of General Formula I is formed by an ALD process. **Figure 14** describes an embodiment of a flow process for forming a MAlGaC film or a MAlInC film by an ALD process. In order to accomplish the growth of an ALD MAlGaC film or an MAlInC film, the surface of a structure such as a structure 200 is heated to 300°C to 500°C (block 410, **Figure 14**). Once heated, the structure is exposed to a metal halide precursor such as $TiCl_4$, $HfCl_4$, $ZrCl_4$, $TaCl_5$, $NbCl_5$, VCl_4 or any of the related fluorides, bromides or iodides of the same metals with sufficient volatility to be delivered to a substrate surface (block 420, **Figure 14**). Excess precursor and by-products are then purged from the chamber using an inert gas such as nitrogen (N_2) or argon (Ar) (block 430, **Figure 14**). The surface of the substrate is then exposed to an organoaluminum precursor (e.g., an alkyl aluminum) such as trimethylaluminum ($AlMe_3$),triethylaluminum ($AlEt_3$), tripropylaluminum ($AlPr_3$) or tri-isobutylaluminum ($Al^{iso}Bu_3$) (block 440, **Figure 14**). Excess organoaluminum precursor and byproducts are then purged from the chamber using an inert gas (block 450, **Figure 14**). The

substrate surface is then exposed to an organogallium precursor such as trimethylgallium ($GaMe_3$), triethylgallium ($GaEt_3$) or tripropylgallium ($GaPr_3$) or to an organoindium precursor such as trimethylindium ($InMe_3$), triethylindium ($InEt_3$) or tripropylindium ($InPr_3$) (block 460, **Figure 14**). This is followed by an inert gas purge of excess precursor and by-products (block 470, **Figure 14**). The sequential exposure of the heated substrate to a metal halide precursor, an organoaluminum precursor and an organogallium or organoindium precursor forms a conformal film having the formula of MAlGaC or MAlInC. The sequential process may be repeated a number of times to deposit a film of a desired thickness (block 480, **Figure 14**). Through the exposure of the film surface to both the organoaluminum and organogallium or organoindium precursor, it is believed that more efficient overall transmetallation occurs to eliminate metal halide bonds leading to a more air stable and a lower resistivity film. In one embodiment, films deposited using the described method have the composition MAlGaC or MAlInC where there is 10 to 60 atomic percent metal M, where M is Ti, Zr, Hf, Ta, Nb or V; 0.5 to 35 atomic percent Al; 0.5 to 30 atomic percent Ga or In; 25 to 50 atomic percent C; and 0 to 5 atomic percent oxygen (O). In another embodiment, films deposited using the described method have the composition MAlGaC or MAlInC where there is 25-60 atomic percent metal M, where M is Ti, Zr, Hf, Ta, Nb or V; 0.5-25 atomic percent Al; 0.5-25 atomic percent Ga or In; 25-50 atomic percent C and 0-5 atomic percent O. It is also possible to further tune the composition and work function of the metal by combining subcycles using different metal halide precursors M^1X_n, M^2X_m and M^3X_p, etc. in larger supercycles such that films of composition $M^1M^2M^3AlGaC$ are deposited (M^1, M^2 and M^3 each representing different metals of the group Ti, Zr, Hf, Ta, Nb and V).

Following a similar process, ALD metal gallium carbide or metal indium carbide films of the form MGaC or MInC, respectively, where M is one or more of Ti, Zr, Hf, Ta, Nb and V, may be deposited. **Figure 15** presents a flow chart of a method. Referring to **Figure 15**, the surface of a substrate such as structure 200 is heated to 300°C to 500°C (block 510, **Figure 15**). This is followed by exposure of the heated substrate surface to a metal halide precursor (block 520, **Figure 15**). This is followed by a purge to remove any unreacted precursor and reaction by-products (block 530, **Figure 15**) and exposure to an organogallium or organoindium precursor (block 540, **Figure 15**) and a final purge. In one embodiment, films deposited using the described method have the composition MGaC or MInC where there is 10-60 atomic percent metal M, where M is Ti, Zr, Hf, Ta, Nb or V; 0.5-70 atomic percent Ga or In; 20-70 atomic percent C and 0-5 atomic percent O. In another embodiment, films deposited using this method have the composition MGaC or MInC where there is 30-70

atomic percent metal M, where M = Ti, Zr, Hf, Ta, Nb or V; 0.5-25 atomic percent Ga or In; 25-70 atomic percent C and 0-5 atomic percent O. It is also possible to further tune the composition and related film properties by combining subcycles using different metal halide precursors M^1Xn, M^2Xm and M^3Xp etc. into supercycles such that films of composition $M^1M^2M^3GaC$ or $M^1M^2M^3InC$ are deposited. In another embodiment, to form a film of MGaInC, the process described with reference to **Figure 15** may be modified after a pulsing and purge of an organogallium or organoindium to add a pulsing and purging of the other of organogallium or organoindium. In the case of both the MAlGaC or MAlInC and MGaC, MInC or MGaInC films, modification of the ALD process may be used to create a metallic film with a graded composition so as to achieve desired interfacial versus bulk film properties. For example, referring to **Figure 11** and **Figure 12**, a film of composition MAlGaC could be placed directly in contact with gate dielectric 270 of, for example, a high-k dielectric material or barrier layer 272 (if present) to set interfacial properties, then a film of a lower resistance ALD MGaC composition could be deposited on top to lower the overall resistance of the gate electrode. In other embodiments, more than two different compositions of General Formula I may be formed to describe a graded composition. Finally, the carbon content of the films may be decreased through the exposure of a metallic film to a remote or direct hydrogen plasma either every ALD cycle, intermittently during film growth or at the end of film deposition.

Table 1 provides examples of various ALD processes.

Example	Metal Halide	Coreactant #1	Coreactant #2	Coreactant #3	ALD Film Composition
1	MXn	GaR_3	none	none	MGaC
2	MXn	InR_3	none	none	MInC
3	MXn	GaR_3	InR_3	none	MGaInC
4	MXn	InR_3	GaR_3	none	MGaInC
5	MXn	AlR_3	GaR_3	none	MAlGaC
6	MXn	AlR_3	InR_3	none	MAlInC
7	MXn	AlR_3	GaR_3	InR_3	MAlGaInC
8	MXn	AlR_3	InR_3	GaR_3	MAlGaInC

In the above examples, MXn is a volatile metal halide where M is Ti, Zr, Hf, V, Nb or Ta and X is a halide such as F, Cl, Br or I and n is 4 or 5. Each example can be the unique ALD pulse sequence or can represent a subcycle in a larger supercycle process that allows for the incorporation of two or more different metals M or for finer tuning of the film composition and physical properties such as resistivity, roughness or work function. For example, one could run supercycles consisting of two subcycles of Example 1 where MXn is

$TaCl_5$ and GaR_3 is $GaPr_3$ followed by three subcycles of Example 6 where MXn is $TiCl_4$ and AlR_3 is $AlMe_3$ and InR_3 is $InEt_3$ to deposit a TaTiAlGaIn film. All ALD processes are run with a substrate temperature between 300°C and 500°C. Finally, any of the film composition of Examples 1-8 may include oxygen at a level up to 5 atomic percent.

Referring again to **Figure 11** and the process of **Figure 13**, following formation of gate electrode 275, contacts may be made to source 250 and drain 255 (and gate electrode 275) to form the device shown in **Figure 1** (block 380, **Figure 13**). As noted above, in one embodiment, one or both contacts may be a metal film or layer having the composition of General Formula I or a graded composition of more than one composition of General Formula I. An ALD process such as described with reference to **Figure 14** or **Figure 15** may be used to form the contacts.

Another embodiment of a non-planar semiconductor device (a three-dimensional device) including a channel region and junction regions disposed on opposite side of the channel region includes where the channel region includes multiple nanowires or nanoribbons. In one such embodiment, a gate stack of the device surrounds the channel region in a gate all around configuration.

Figures 16-26 describe a process of forming a device including a channel region of multiple nanowires or nanoribbons.

Figure 16 shows top side perspective view of structure 600 that is a portion of a semiconductor substrate, such as a portion of a wafer. Substrate 610, in one embodiment, is silicon or an SOF substrate. Formed in substrate 610 is sacrificial fin 6100 having a desired length, L, height, H and width, W, dimension for a desired nanowire or desired nanoribbon nanowire three-dimensional circuit device. In one embodiment, sacrificial fin 6100 is formed by etching substrate 610 to a depth equal to the desired height, H, of the sacrificial fin. Following the formation of sacrificial fin 6100, in the embodiment shown in **Figure 1**, dielectric material 615 is introduced around the fin (e.g., on opposing sides of sacrificial fin 6100). In one embodiment, dielectric material 615 is an oxide material.

Figure 17 shows structure 600 of **Figure 1** following the removal of sacrificial fin 6100 to form trench 618 in dielectric material 615. Sacrificial fin 6100 may be removed by a selective etch process.

Figure 18 shows structure 600 of **Figure 2** following the epitaxial growth of alternative layers of nanowires and a sacrificial material according to an aspect ratio trapping (ART) method. **Figure 18** shows nanowires 650A, 650B and 650C of a desired channel material such as silicon, silicon germanium, a group III-V compound semiconductor material

(e.g., InGaAs, InP, InAs, InGaSb) or a germanium material epitaxially grown on sacrificial layers 640A, 640B and 640C, respectively. The word nanowire as used herein is not limited to any particular shape (e.g., cylindrical, rectangular, etc.) and thus includes nanoribbons and nanostructures of various cross-sectional shapes. In one embodiment, sacrificial layers 640A-640C are each a material having a lattice constant similar to a lattice constant of a material of nanowires 650A-650C. In an embodiment where a material of nanowires 650A-650C are each germanium, sacrificial layers 640A-640C are each a group III-V compound structure, such as gallium arsenide (GaAs) epitaxially grown in trench 618. As illustrated in **Figure 18**, the epitaxial growth proceeds first with sacrificial layer 640A followed by nanowire 650A, followed by sacrificial layer 640B, nanowire 650B, sacrificial layer 640C and nanowire 650C. Thus, the sacrificial layer and nanowire layer alternate with each nanowire formed on a sacrificial layer. As illustrated in **Figure 18**, the alternating layers of sacrificial layers 640A-640C and nanowires 650A-650C fill trench 125. Although **Figure 18** illustrates three nanowires, the structure is not limited to three nanowires and may contain fewer or greater than three nanowires.

Figure 19 shows structure 600 of **Figure 18** following a recess of dielectric material 615. In one embodiment, dielectric material 615 of silicon dioxide is selectively etched as to remove the dielectric material and not remove the layers of nanowire and sacrificial material. As illustrated, the recess proceeds to a level that exposes each of nanowires 650A-650C.

Figure 20 shows structure 600 of **Figure 19** following the introduction of spacers and a sacrificial or dummy gate electrode on the nanowire in a designated channel region of the structure. **Figure 20** shows designated channel region 655, including spacers 660 and sacrificial material 665 deposited between spacers 660. In one embodiment, to form the structure of **Figure 20**, gate dielectric material 670 (e.g., silicon dioxide or a low-k dielectric material) is deposited as a blanket on the structure of **Figure 19** followed by a depositing of a sacrificial or dummy gate material (e.g., polycrystalline silicon) also as a blanket on the gate dielectric material. The sacrificial or dummy gate material and gate dielectric material are then patterned to a sacrificial or dummy gate 665 and gate dielectric in designated channel region 655. A spacer material film (e.g., a dielectric material having a dielectric constant less than a dielectric constant of silicon dioxide (a low k dielectric) such as carbon-doped silicon dioxide is then deposited and etched to form spacers 660. Next, a source and a drain are formed in designated junction regions 680A and 680B.

There are different possibilities for source and drain implementation. In one embodiment, nanowires 650A-650C in designated junction regions 680A and 680B may be

used as is with sacrificial material 640A-640C therebetween. Representatively, nanowires 650A-650C may be exposed in designated diffusion or junction regions 680A and 680B and doped with a suitable dopant followed by a blanket deposition of dielectric material 670 to form ILD0. This implementation is illustrated in **Figure 20**.

In another embodiment, illustrated in **Figure 21**, a source and drain implementation involves a removal of sacrificial material 640A-640C in designated junction regions 680A and 680B and nanowires 650A-650C are doped. Representatively, nanowires 650A-650C and sacrificial material 640A-640C would initially be exposed, then an etch process would follow that removed sacrificial material 640A-640C selectively relative to nanowires 650A-650C. Nanowires 650A-650C could then be doped followed by a blanket deposition of dielectric material 670.

In a further embodiment, illustrated in **Figure 22**, a source and drain implementation involves a removal of sacrificial material 640A-640C in designated junction regions 680A and 680B and an introduction of a cladding material on nanowires 650A-650C. Representatively, nanowires 650A-650C and sacrificial material 640A-640C would be exposed, followed by a selective removal of the sacrificial material as described in the implementation of **Figure 20**. Cladding material 652 such as a doped silicon germanium or a doped germanium for P-type would then be introduced by way of an epitaxial process around each of nanowires 650A-650C. A blanket deposition of dielectric material 670 would follow.

In a still further embodiment illustrated in **Figure 23**, a source and drain implementation involves a removal of nanowires 650A-650C and a removal of sacrificial material 640A-640C in designate diffusion or junction regions 680A and 680B and a replacement of the removed material with source and drain material. Representatively, a dielectric material may be formed in designated diffusion or junction regions 680A and 680B. Then, a masking and etching process can be used to remove nanowires 650A-650C and sacrificial material 640A-640C followed by an epitaxial process to introduce source and drain material such as doped silicon germanium or doped germanium for a P-type device or a combination of doped silicon germanium and doped germanium. **Figure 23** shows source 656 and drain 658 formed in designated diffusion or junction regions 680A and 680B in place of nanowires 650A-650C and sacrificial material 640A-640C.

Each of the implementations of **Figures 16-23** shows dielectric material 670 of, for example, a silicon dioxide or a low k dielectric material is deposited on designated diffusion or junction regions 680A and 680B adjacent spacers 660 and the dielectric material polished to expose sacrificial or dummy gate 665.

Using the source and drain implementation illustrated in **Figure 20, Figure 24** shows structure 600 of **Figure 20** following the removal of sacrificial gate electrode 665, leaving spacers 660 adjacent junction region 680A and junction 680B, respectively, and defining gate electrode region or channel region 655. In one embodiment, a dummy gate of, e.g., polycrystalline silicon, is removed by a selective etch process.

Figure 24 shows structure 600 of **Figure 23** following a removal of sacrificial layer material in channel region 655. In one embodiment, for a sacrificial layer material of gallium arsenide, such material may be selectively removed relative to germanium nanowires by a hydrochloric acid-based etch. In junction region 680A and junction region 680B, the material of sacrificial layers 640A-640C, if still present, is protected from any etch process by dielectric material 670. **Figure 25** representatively shows dielectric material 670 removed in junction region 680A to illustrate the retention of material of sacrificial layers 640A-640C in the junction regions and the removal of such material in channel region 655. In some embodiments, portions or structures of the sacrificial material may still remain within the spacers 660 after the sacrificial material is etched out of the channel region.

Figure 26 shows the structure of **Figure 25** following the introduction of a gate stack on channel region 655. **Figure 26** is a magnified, isolated view of channel region 655 of the structure of **Figure 24**. A gate stack, in one embodiment, includes gate dielectric 690, optional barrier layer 692 and gate electrode 695. In one embodiment, gate dielectric 690 is a silicon dioxide or a low-k dielectric material. Barrier layer 692 is a material such as TiN, MnN, NbN or TaN. Gate electrode 695 is a metal material of a metal film or layer having the formula of General Formula I. **Figure 27** illustrates an all-around gate configuration where dielectric layer 690 respectively surrounds each of nanowire 650A, 650B and nanowire 650C, and gate electrode 695 surrounds each gate dielectric. Each gate dielectric of, for example, a high-k material may be introduced by an ALD process. Barrier layer 692 may be introduced by an atomic layer deposition or chemical vapor deposition process. The gate metal may be introduced by an ALD process as described above with reference to **Figure 14** or **Figure 15**. Following the formation of the gate stack, contacts may be made to diffusion or junction regions 680A and 680B, as well as to gate electrode 695 to form electrical connections for structure 600. In one embodiment, the contacts may be a metal film or layer having the composition of General Formula I and formed by an ALD process such as described with reference to **Figure 14** and **Figure 15**.

Figure 28 illustrates interposer 700 that includes one or more embodiments. Interposer 700 is an intervening substrate used to bridge a first substrate 702 to second

substrate 704. First substrate 702 may be, for instance, an integrated circuit die. Second substrate 704 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of interposer 700 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 700 may couple an integrated circuit die to a ball grid array (BGA) 706 that can subsequently be coupled to the second substrate 704. In some embodiments, the first and second substrates 702/704 are attached to opposing sides of interposer 700. In other embodiments, the first and second substrates 702/704 are attached to the same side of interposer 700. In further embodiments, three or more substrates are interconnected by way of interposer 700.

The interposer 700 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer may include metal interconnects 708 and vias 710, including but not limited to through-silicon vias (TSVs) 712. The interposer 700 may further include embedded devices 714, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on interposer 700.

In accordance with embodiments, apparatuses or processes disclosed herein may be used in the fabrication of interposer 700.

Figure 29 illustrates a computing device 800 in accordance with one embodiment. The computing device 800 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, these components are fabricated onto a single system-on-a-chip (SoC) die rather than a motherboard. The components in the computing device 800 include, but are not limited to, an integrated circuit die 802 and at least one communication chip 808. In some implementations the communication chip 808 is fabricated as part of the integrated circuit die 802. The integrated circuit die 802 may include a CPU 804 as well as on-die memory 806, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STTM-RAM).

Computing device 800 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 810 (e.g., DRAM), non-volatile memory 812 (e.g., ROM or flash memory), a graphics processing unit 814 (GPU), a digital signal processor 816, a crypto processor 842 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 820, an antenna 822, a display or a touchscreen display 824, a touchscreen controller 826, a battery 828 or other power source, a power amplifier (not shown), a global positioning system (GPS) device 844, a compass 830, a motion coprocessor or sensors 832 (that may include an accelerometer, a gyroscope, and a compass), a speaker 834, a camera 836, user input devices 838 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 840 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communications chip 808 enables wireless communications for the transfer of data to and from the computing device 800. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 808 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 800 may include a plurality of communication chips 808. For instance, a first communication chip 808 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 808 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 804 of the computing device 800 includes one or more devices, such as transistors, that are formed in accordance with embodiments described above. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 808 may also include one or more devices, such as transistors, that are formed in accordance with embodiments.

In further embodiments, another component housed within the computing device 800 may contain one or more devices, such as transistors, that are formed in accordance with implementations.

In various embodiments, the computing device 800 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 800 may be any other electronic device that processes data.

EXAMPLES

The following examples pertain to embodiments:

Example 1 is an apparatus including an integrated circuit device structure including a metal layer including a composition of General Formula I: $M\text{-}Al_m\text{-}X^1{}_n\text{-}X^2{}_p\text{-}C_q\text{-}O_r$, wherein M includes a metal selected from one or more of titanium, zirconium, hafnium, tantalum, niobium and vanadium, wherein C includes carbon, wherein O includes oxygen, wherein X^1 includes gallium, wherein X^2 includes indium, and wherein m, n, p, q and r represent an atomic percent of an element in the metal layer that can be 0 percent, with the proviso that n and p cannot each be 0 percent.

In Example 2, m, n, p, q and r of the apparatus of Example 1 are as follows: m is 0 to 35 atomic percent, n is 0 to 70 atomic percent, p is 0 to 70 atomic percent, q is 0.1 to 60 atomic percent, and r is 0 to 5 atomic percent.

In Example 3, M of the apparatus of Example 1 is present in an amount of 10 to 60 atomic percent.

In Example 4, n of the apparatus of Example 1 is 0.1 to 70 atomic percent and p is 0 atomic percent.

In Example 5, p of the apparatus of Example 1 is 0.1 to 70 atomic percent and n is 0 atomic percent.

In Example 6, m of the apparatus of Example 1 is 5 to 35 atomic percent and only one of n and p is 0 atomic percent.

In Example 7, the integrated circuit device structure of the apparatus of any of Examples 1-6 includes a gate electrode of a transistor.

In Example 8, the metal layer of the apparatus of Example 7 includes a graded composition including a plurality of compositions of General Formula I.

In Example 9, the integrated circuit device structure of the apparatus of any of Examples 1-6 includes a contact coupled to a source or a drain of a transistor devices.

Example 10 is an apparatus including a transistor device including a gate electrode, the gate electrode including a metallic layer including at least one of metal gallium carbide (M(Ga)C); metal aluminum gallium carbide (M(Al)(Ga)C); metal gallium indium carbide (M(Ga)(In)C); metal aluminum gallium indium carbide (M(Al)(Ga)(In)C); metal aluminum indium carbide (M(Al)(In)C); and metal indium carbide (M(In)C), wherein M includes a metal selected from one or more of titanium (Ti), zirconium (Zr), hafnium (Hf), tantalum (Ta), niobium (Nb) and vanadium (V), and wherein the metallic layer may include oxygen.

In Example 11, the metallic layer of the apparatus of Example 10 includes at least one of metal gallium carbide (M(Ga)C); metal gallium indium carbide (M(Ga)(In)C); and metal indium carbide (M(In)C).

In Example 12, the metallic layer of the apparatus of Example 10 includes at least one of metal aluminum gallium carbide (M(Al)(Ga)(C); metal aluminum gallium indium carbide (M(Al)(Ga)(In)C); and metal aluminum indium carbide (M(Al)(In)C).

In Example 13, the apparatus of Example 10, wherein C is present in an amount of 0.1 to 60 atomic percent.

Example 14 is an apparatus including a transistor device including and a contact to the transistor device, the contract including a metallic layer including metal gallium carbide (M(Ga)C); metal aluminum gallium carbide (M(Al)(Ga)C); metal gallium indium carbide (M(Ga)(In)C); metal aluminum gallium indium carbide (M(Al)(Ga)(In)C); metal aluminum indium carbide (M(Al)(In)C); and metal indium carbide (M(In)C), wherein M includes a metal selected from one or more of titanium (Ti), zirconium (Zr), hafnium (Hf), tantalum (Ta), niobium (Nb) and vanadium (V), and wherein the metallic layer may include oxygen.

In Example 15, the metallic layer of the apparatus of Example 14 includes at least one of metal gallium carbide (M(Ga)C); metal gallium indium carbide (M(Ga)(In)C); and metal indium carbide (M(In)C).

In Example 16, the metallic layer of the apparatus of Example 14 includes at least one of metal aluminum gallium carbide (M(Al)(Ga)(C); metal aluminum gallium indium carbide (M(Al)(Ga)(In)C); and metal aluminum indium carbide (M(Al)(In)C).

In Example 17, the apparatus of Example 14, wherein C is present in an amount of 0.1 to 60 atomic percent.

Example 18 is a method including introducing a first precursor including a metal halide into a chamber including an integrated circuit structure, wherein a metal cation of the

first precursor is selected from the group consisting of titanium, zirconium, hafnium, tantalum, niobium and vanadium; introducing a second precursor of at least one of an organogallium compound and organoindium compound into the chamber; and depositing a metal including the metal cation of the halide and at least one of gallium and indium.

In Example 19, introducing the first precursor and introducing the second precursor of the method of Example 18 are performed sequentially in any order.

In Example 20, the method of Example 18 or 19 further includes introducing a third precursor including an organoaluminum into the chamber, wherein the third precursor is introduced after the first precursor and before the second precursor.

In Example 21, introducing a second precursor of the method of any of Examples 18-20 includes sequentially introducing each of the organogallium and organoindium into the chamber.

In Example 22, introducing a first precursor including a metal halide of the method of any of Examples 18-21 includes sequentially introducing a first precursor having a first metal cation and a first precursor having a second metal cation different from the first metal cation.

In Example 23, an integrated circuit device structure includes a metal layer formed by the method of any of Examples 18-22.

Example 24 is the integrated circuit device of Example 23 wherein the integrated circuit device structure is one of a gate electrode and a device contact.

The above description of illustrated implementations, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific implementations of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope, as those skilled in the relevant art will recognize.

These modifications may be made in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific implementations disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

CLAIMS

1. An apparatus comprising:

an integrated circuit device structure comprising a metal layer comprising a composition of General Formula I:

$$M\text{-}Al_m\text{-}X^1{}_n\text{-}X^2{}_p\text{-}C_q\text{-}O_r, \quad (I)$$

wherein M comprises a metal selected from one or more of titanium, zirconium, hafnium, tantalum, niobium and vanadium,

wherein C comprises carbon,

wherein O comprises oxygen,

wherein X^1 comprises gallium,

wherein X^2 comprises indium, and

wherein m, n, p, q and r represent an atomic percent of an element in the metal layer that can be 0 percent, with the proviso that n and p cannot each be 0 percent.

2. The apparatus of claim 1, wherein m is 0 to 35 atomic percent, n is 0 to 70 atomic percent, p is 0 to 70 atomic percent, q is 0.1 to 60 atomic percent, and r is 0 to 5 atomic percent.

3. The apparatus of claim 1, wherein M is present in an amount of 10 to 60 atomic percent.

4. The apparatus of claim 1, wherein n is 0.1 to 70 atomic percent and p is 0 atomic percent.

5. The apparatus of claim 1, wherein p is 0.1 to 70 atomic percent and n is 0 atomic percent.

6. The apparatus of claim 1, wherein m is 5 to 35 atomic percent and only one of n and p is 0 atomic percent.

7. The apparatus of claim 1, wherein the integrated circuit device structure comprises a gate electrode of a transistor.

8. The apparatus of claim 7, wherein the metal layer comprises a graded composition comprising a plurality of compositions of General Formula I.

9. The apparatus of claim 1, wherein the integrated circuit device structure comprises a contact coupled to a source or a drain of a transistor device.

10. An apparatus comprising:

a transistor device comprising a gate electrode, the gate electrode comprising a metallic layer comprising at least one of metal gallium carbide (M(Ga)C); metal aluminum gallium carbide (M(Al)(Ga)C); metal gallium indium carbide (M(Ga)(In)C); metal aluminum gallium indium carbide (M(Al)(Ga)(In)C); metal aluminum indium carbide (M(Al)(In)C); and metal indium carbide (M(In)C),

wherein M includes a metal selected from one or more of titanium (Ti), zirconium (Zr), hafnium (Hf), tantalum (Ta), niobium (Nb) and vanadium (V), and

wherein the metallic layer may comprise oxygen.

11. The apparatus of claim 10, wherein the metallic layer comprises at least one of metal gallium carbide (M(Ga)C); metal gallium indium carbide (M(Ga)(In)C); and metal indium carbide (M(In)C).

12. The apparatus of claim 10, wherein the metallic layer comprises at least one of metal aluminum gallium carbide (M(Al)(Ga)(C); metal aluminum gallium indium carbide (M(Al)(Ga)(In)C); and metal aluminum indium carbide (M(Al)(In)C).

13. The apparatus of claim 10, wherein C is present in an amount of 0.1 to 60 atomic percent.

14. An apparatus comprising:

a transistor device comprising and a contact to the transistor device, the contract comprising a metallic layer comprising metal gallium carbide (M(Ga)C); metal aluminum gallium carbide (M(Al)(Ga)C); metal gallium indium carbide (M(Ga)(In)C); metal aluminum gallium indium carbide (M(Al)(Ga)(In)C); metal aluminum indium carbide (M(Al)(In)C); and metal indium carbide (M(In)C),

wherein M includes a metal selected from one or more of titanium (Ti), zirconium (Zr), hafnium (Hf), tantalum (Ta), niobium (Nb) and vanadium (V), and

wherein the metallic layer may comprise oxygen.

15. The apparatus of claim 14, wherein the metallic layer comprises at least one of metal gallium carbide (M(Ga)C); metal gallium indium carbide (M(Ga)(In)C); and metal indium carbide (M(In)C).

16. The apparatus of claim 14, wherein the metallic layer comprises at least one of metal aluminum gallium carbide (M(Al)(Ga)(C); metal aluminum gallium indium carbide (M(Al)(Ga)(In)C); and metal aluminum indium carbide (M(Al)(In)C).

17. The apparatus of claim 14, wherein C is present in an amount of 0.1 to 60 atomic percent.

18. A method comprising:

introducing a first precursor comprising a metal halide into a chamber comprising an integrated circuit structure, wherein a metal cation of the first precursor is selected from the group consisting of titanium, zirconium, hafnium, tantalum, niobium and vanadium;

introducing a second precursor of at least one of an organogallium compound and organoindium compound into the chamber; and

depositing a metal comprising the metal cation of the halide and at least one of gallium and indium.

19. The method of claim 18, wherein introducing the first precursor and introducing the second precursor are performed sequentially in any order.

20. The method of claim 18, further comprising introducing a third precursor comprising an organoaluminum into the chamber, wherein the third precursor is introduced after the first precursor and before the second precursor.

21. The method of claim 18, wherein introducing a second precursor comprises sequentially introducing each of the organogallium and organoindium into the chamber.

22. The method of claim 18, wherein introducing a first precursor comprising a metal halide comprises sequentially introducing a first precursor having a first metal cation and a first precursor having a second metal cation different from the first metal cation.

5

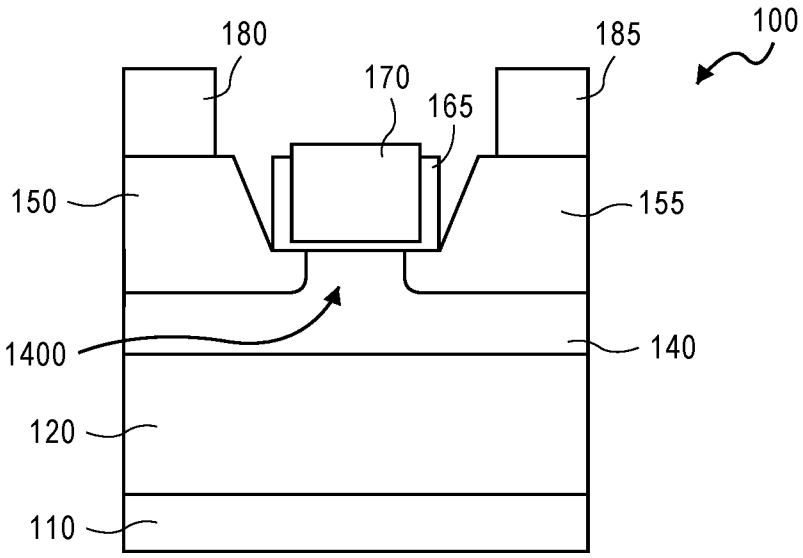


FIG. 1

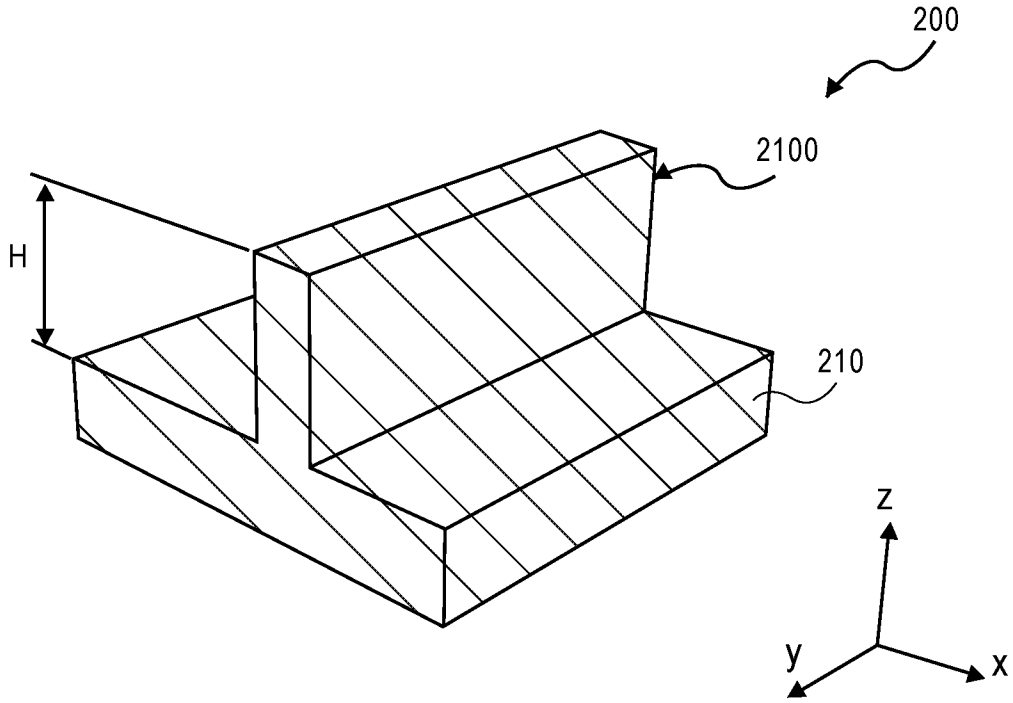


FIG. 2

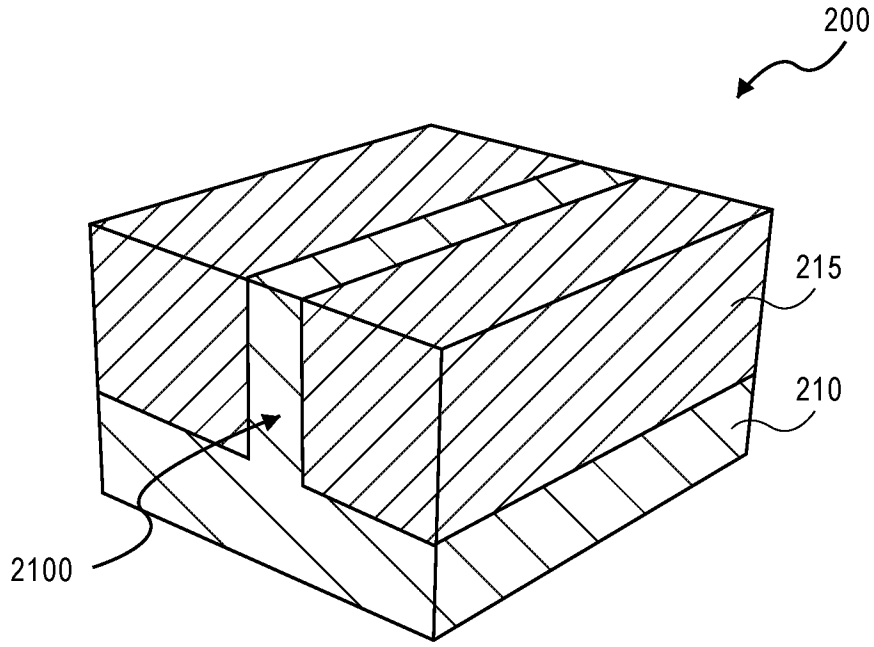


FIG. 3

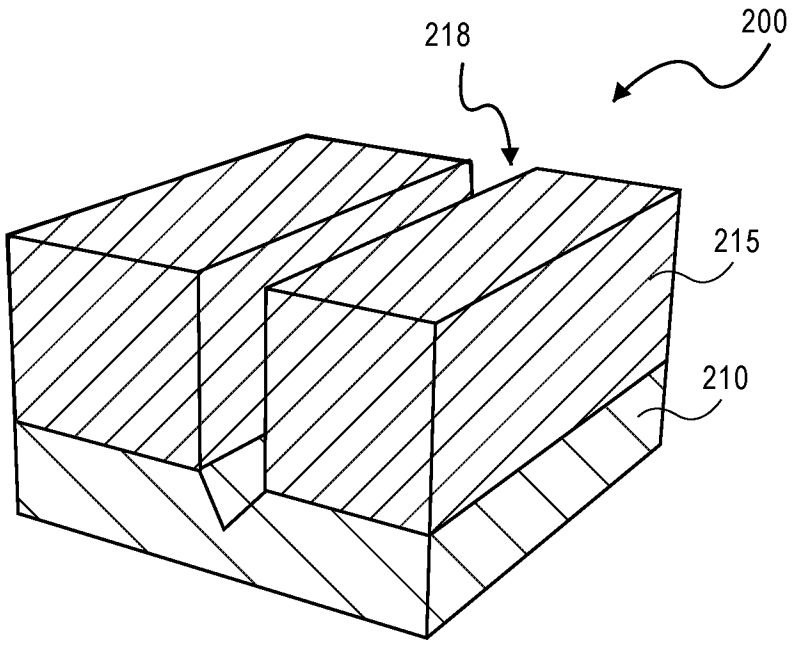


FIG. 4

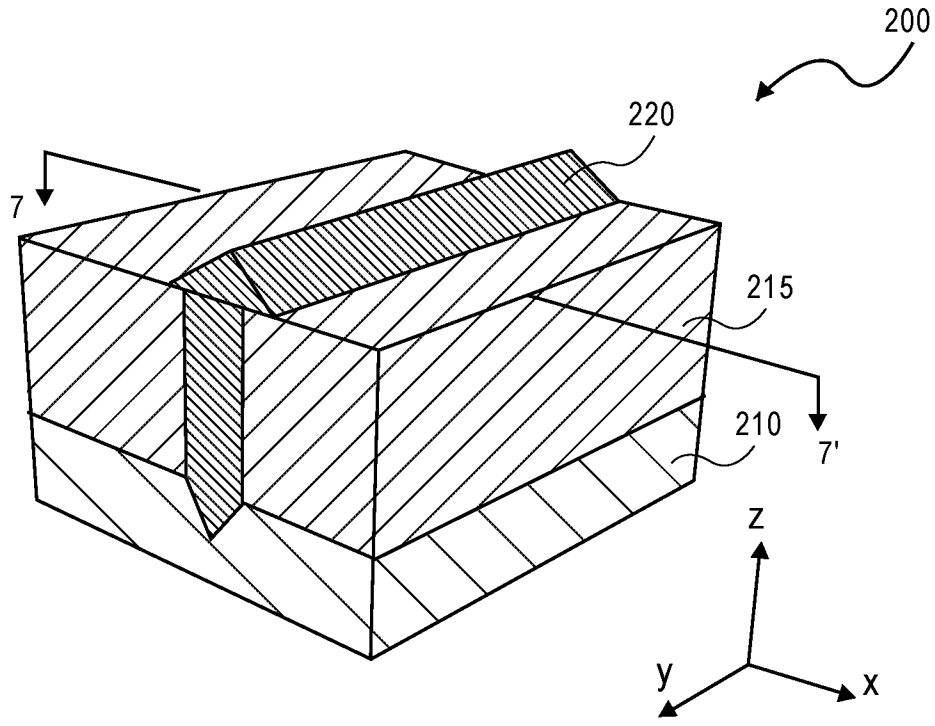


FIG. 5

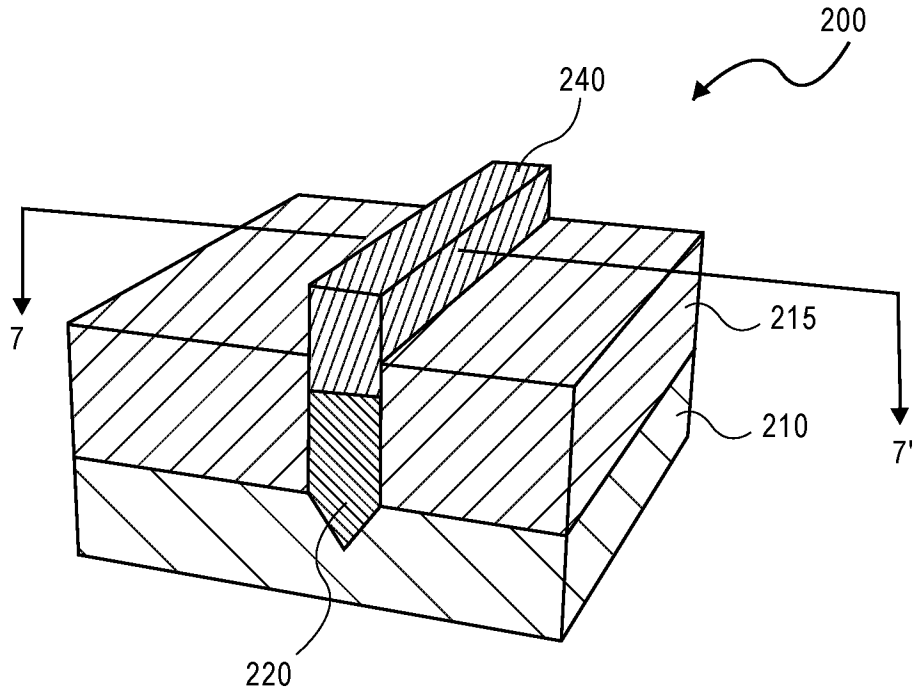


FIG. 6

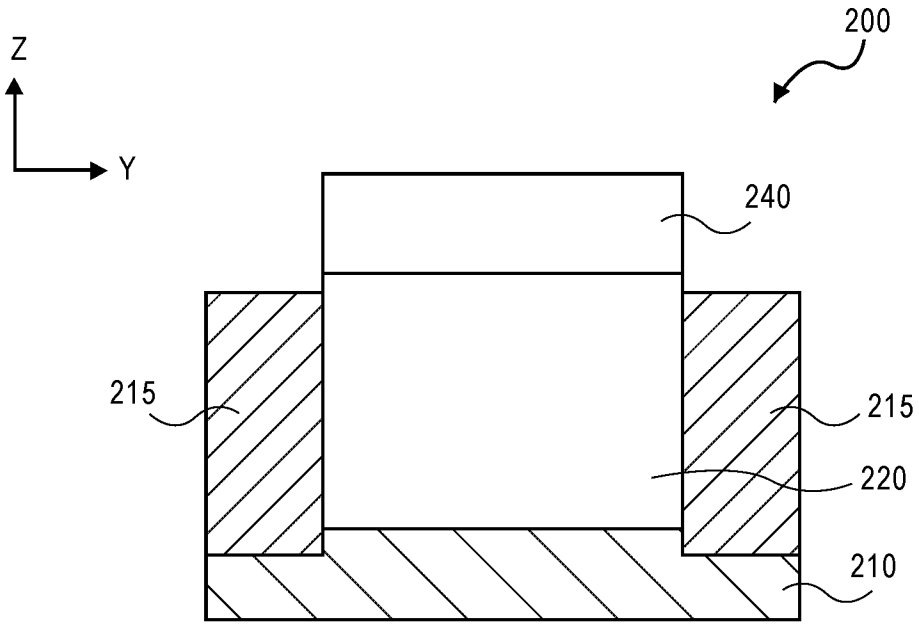

200
Z
Y
240
215
215
220
210

FIG. 7

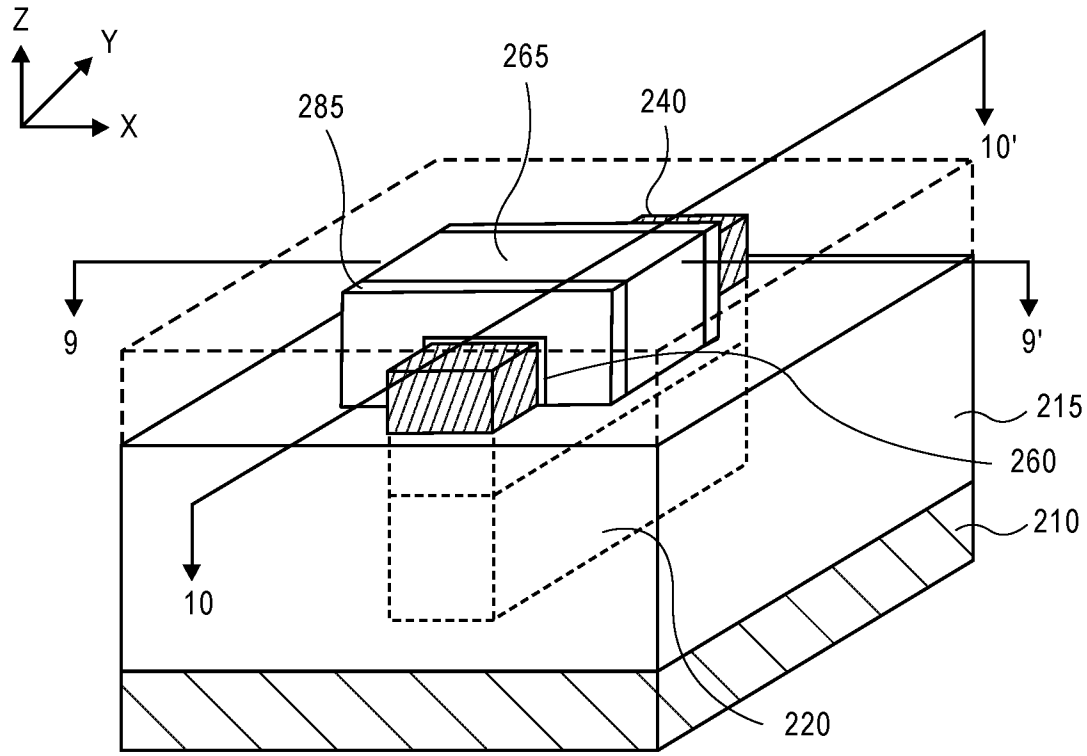

Z
Y
X
265
285
240
10'
9
9'
215
260
210
10
220

FIG. 8

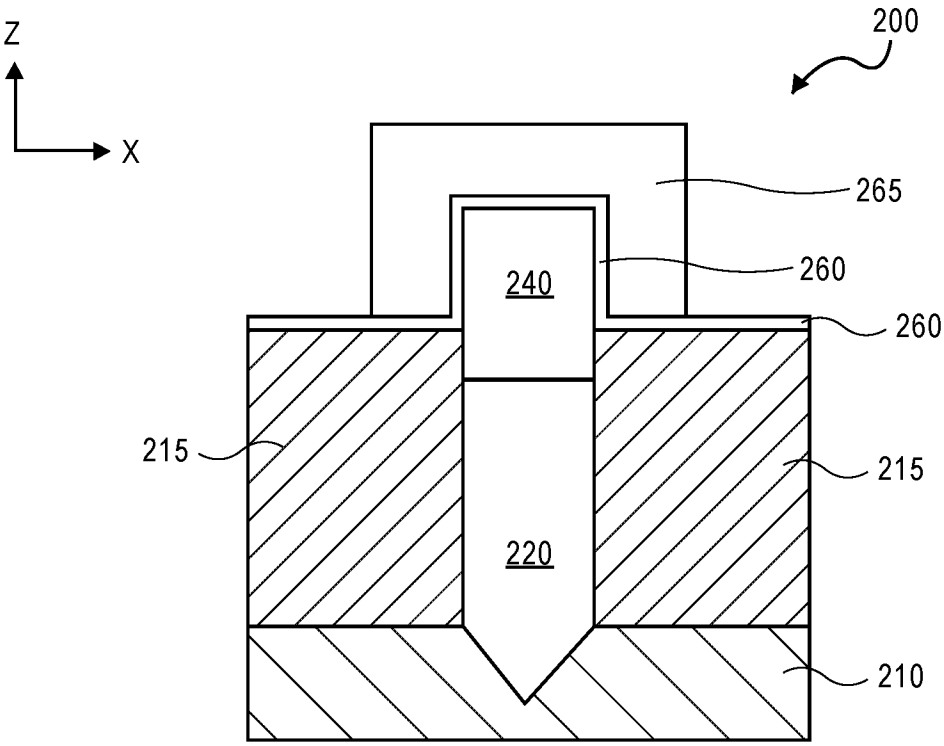

Z
X
200
265
260
240
260
215
215
220
210

FIG. 9

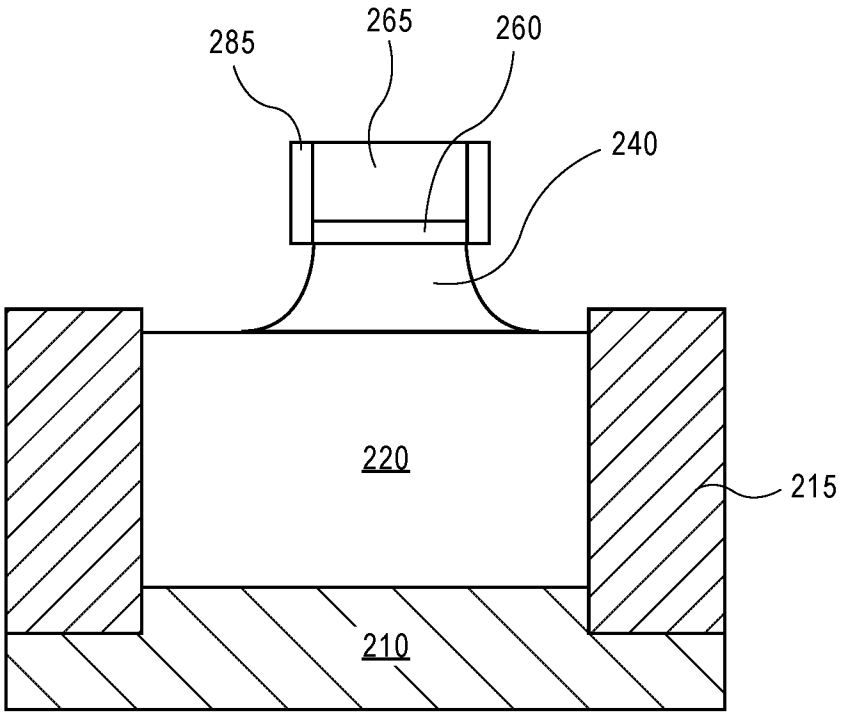

285
265
260
240
220
215
210

FIG. 10

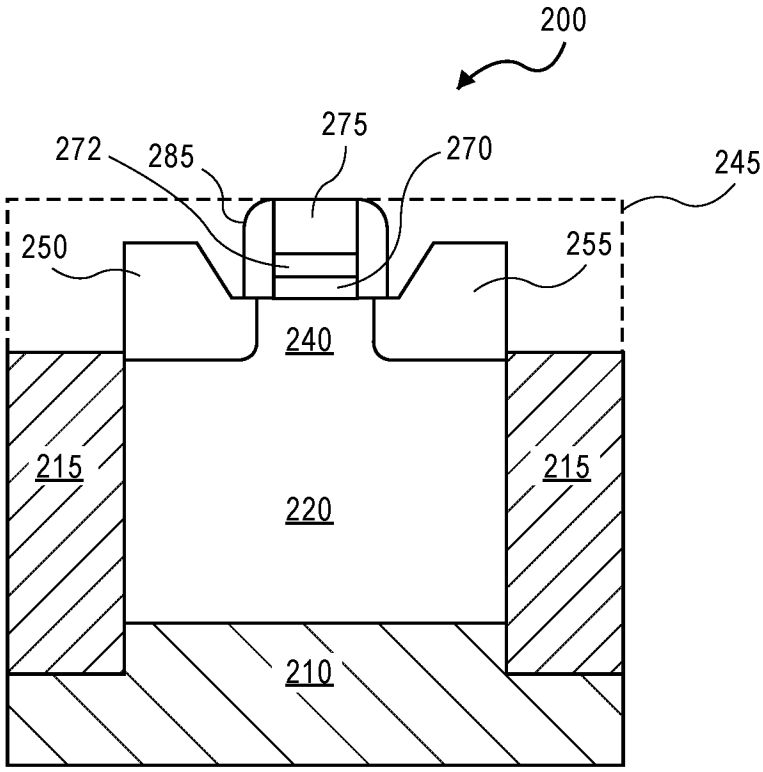


FIG. 11

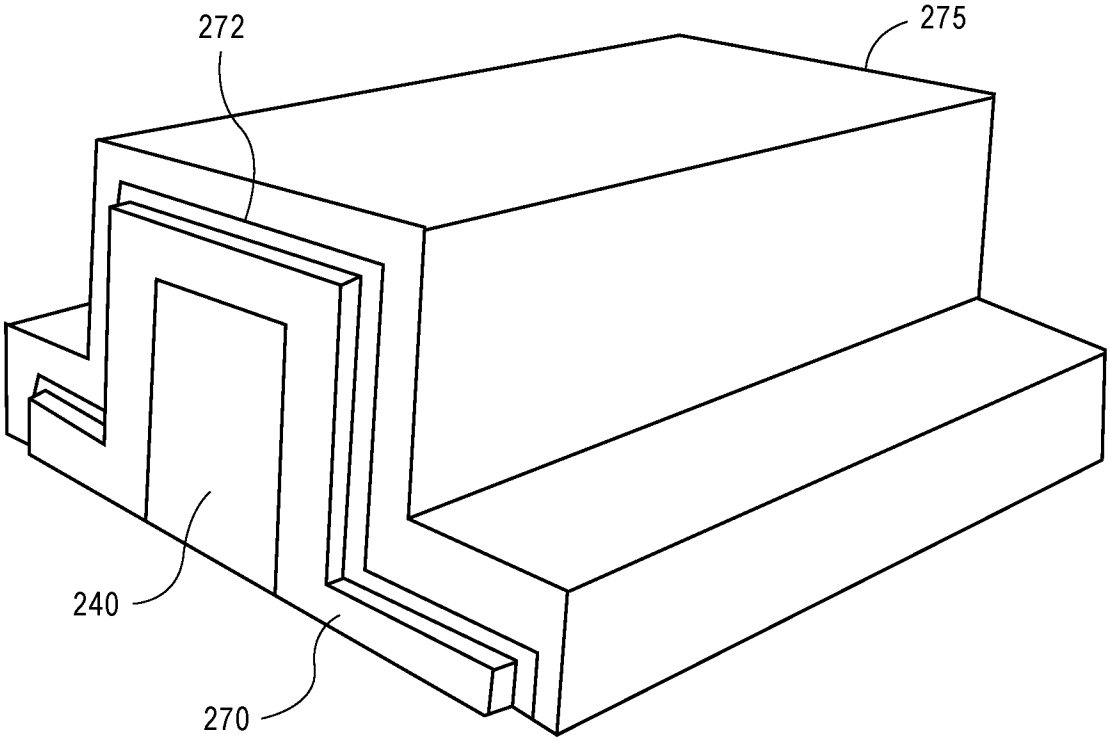


FIG. 12

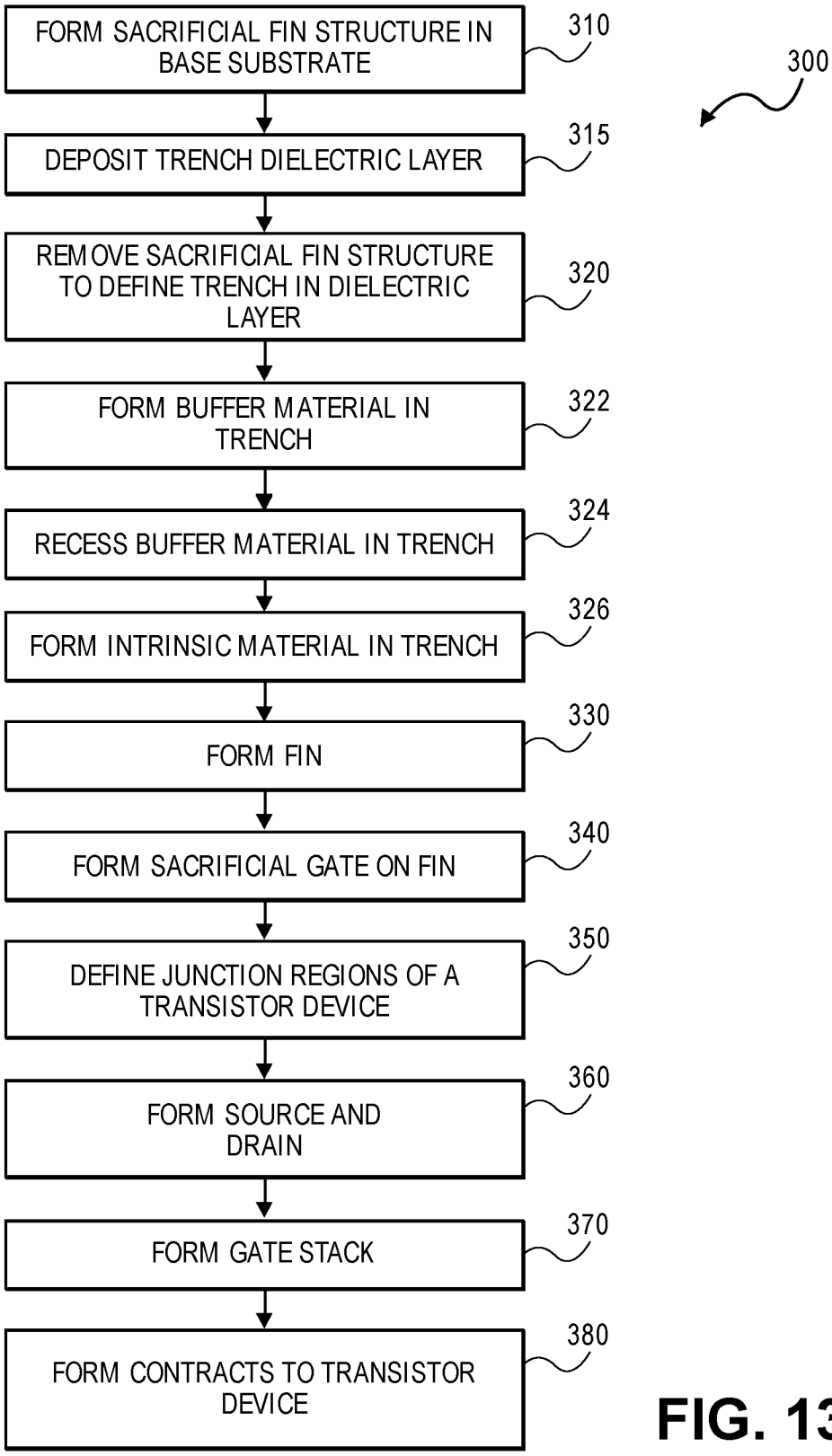

FORM SACRIFICIAL FIN STRUCTURE IN BASE SUBSTRATE
310
300
DEPOSIT TRENCH DIELECTRIC LAYER
315
REMOVE SACRIFICIAL FIN STRUCTURE TO DEFINE TRENCH IN DIELECTRIC LAYER
320
FORM BUFFER MATERIAL IN TRENCH
322
RECESS BUFFER MATERIAL IN TRENCH
324
FORM INTRINSIC MATERIAL IN TRENCH
326
FORM FIN
330
FORM SACRIFICIAL GATE ON FIN
340
DEFINE JUNCTION REGIONS OF A TRANSISTOR DEVICE
350
FORM SOURCE AND DRAIN
360
FORM GATE STACK
370
FORM CONTRACTS TO TRANSISTOR DEVICE
380

FIG. 13

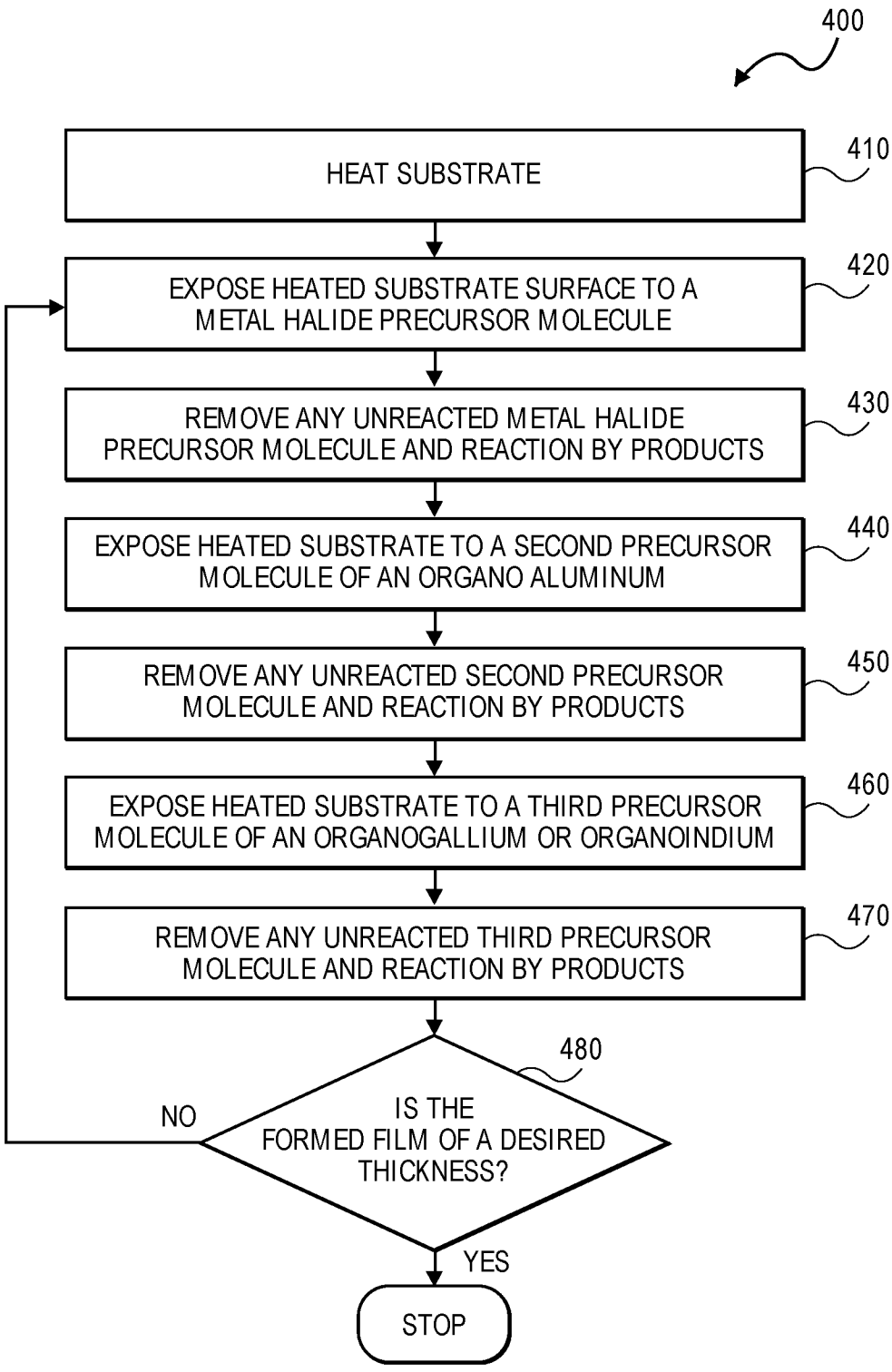

400
HEAT SUBSTRATE
410
EXPOSE HEATED SUBSTRATE SURFACE TO A METAL HALIDE PRECURSOR MOLECULE
420
REMOVE ANY UNREACTED METAL HALIDE PRECURSOR MOLECULE AND REACTION BY PRODUCTS
430
EXPOSE HEATED SUBSTRATE TO A SECOND PRECURSOR MOLECULE OF AN ORGANO ALUMINUM
440
REMOVE ANY UNREACTED SECOND PRECURSOR MOLECULE AND REACTION BY PRODUCTS
450
EXPOSE HEATED SUBSTRATE TO A THIRD PRECURSOR MOLECULE OF AN ORGANOGALLIUM OR ORGANOINDIUM
460
REMOVE ANY UNREACTED THIRD PRECURSOR MOLECULE AND REACTION BY PRODUCTS
470
480
IS THE FORMED FILM OF A DESIRED THICKNESS?
NO
YES
STOP

FIG. 14

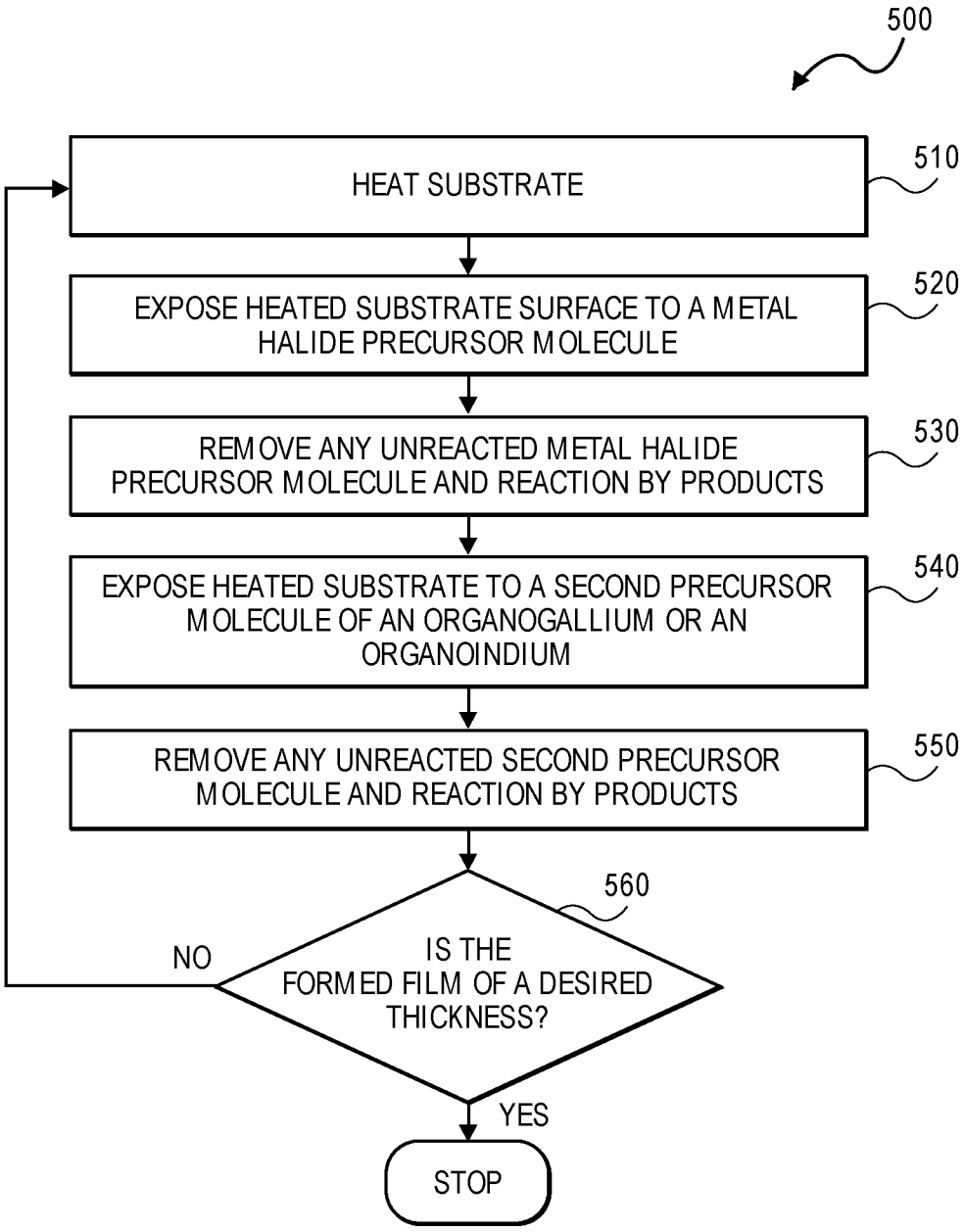

500
HEAT SUBSTRATE
510
EXPOSE HEATED SUBSTRATE SURFACE TO A METAL HALIDE PRECURSOR MOLECULE
520
REMOVE ANY UNREACTED METAL HALIDE PRECURSOR MOLECULE AND REACTION BY PRODUCTS
530
EXPOSE HEATED SUBSTRATE TO A SECOND PRECURSOR MOLECULE OF AN ORGANOGALLIUM OR AN ORGANOINDIUM
540
REMOVE ANY UNREACTED SECOND PRECURSOR MOLECULE AND REACTION BY PRODUCTS
550
560
IS THE FORMED FILM OF A DESIRED THICKNESS?
NO
YES
STOP

FIG. 15

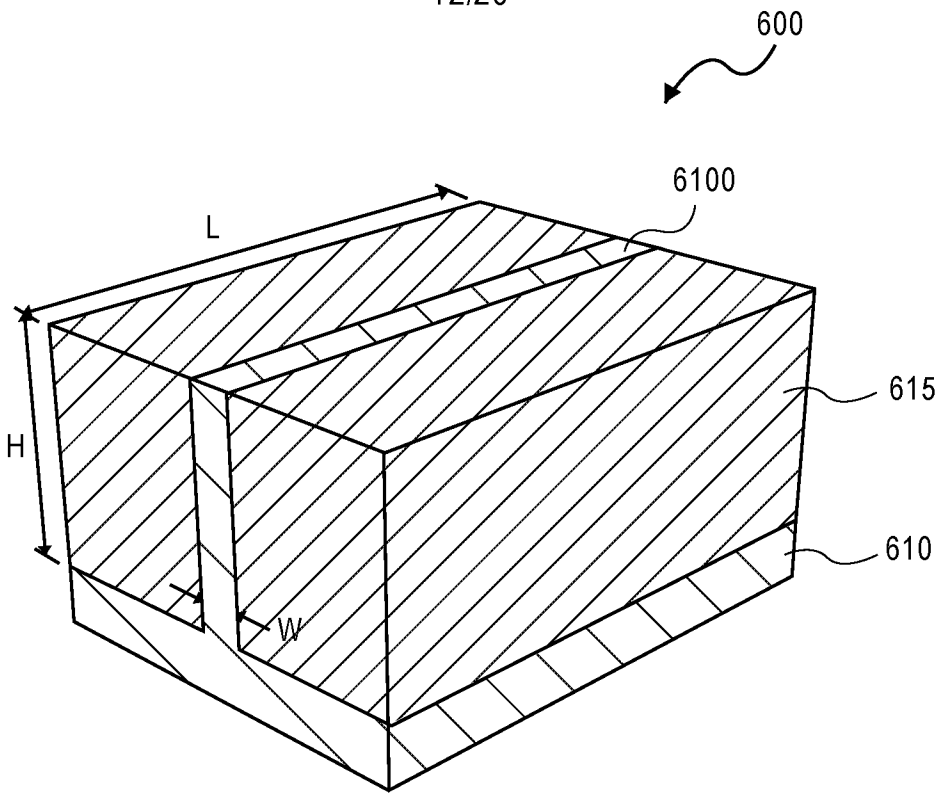


FIG. 16

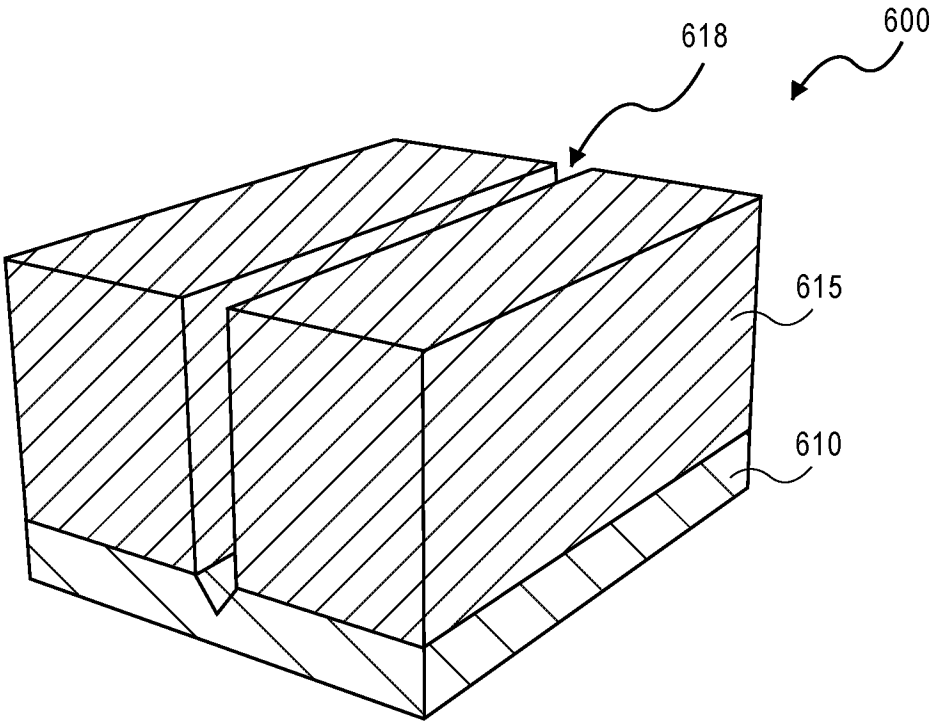


FIG. 17

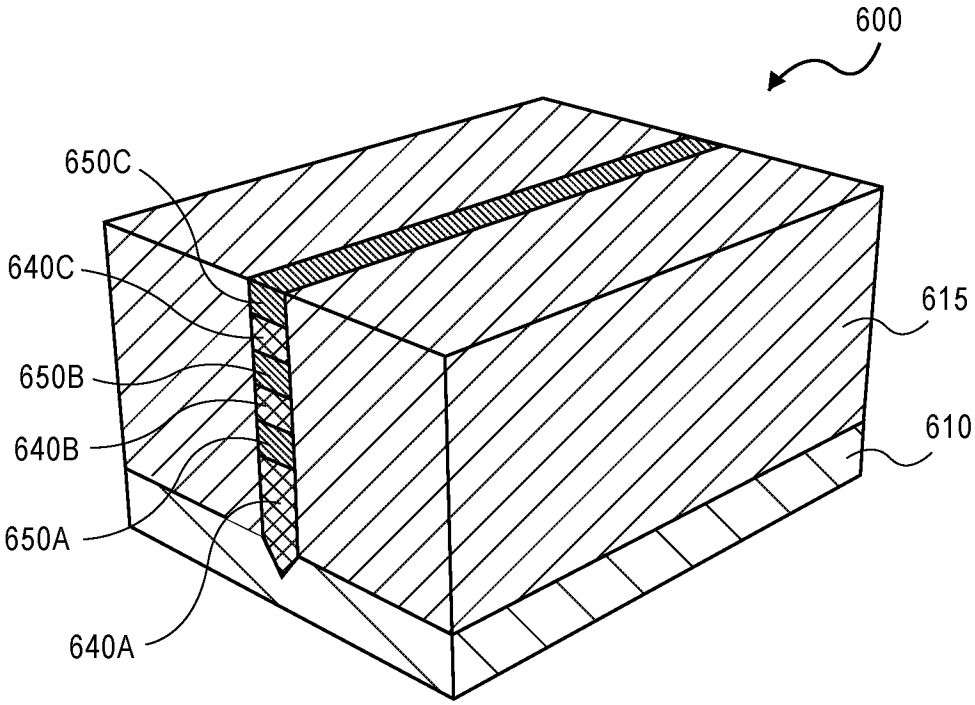

600
650C
640C
650B
640B
650A
640A
615
610

FIG. 18

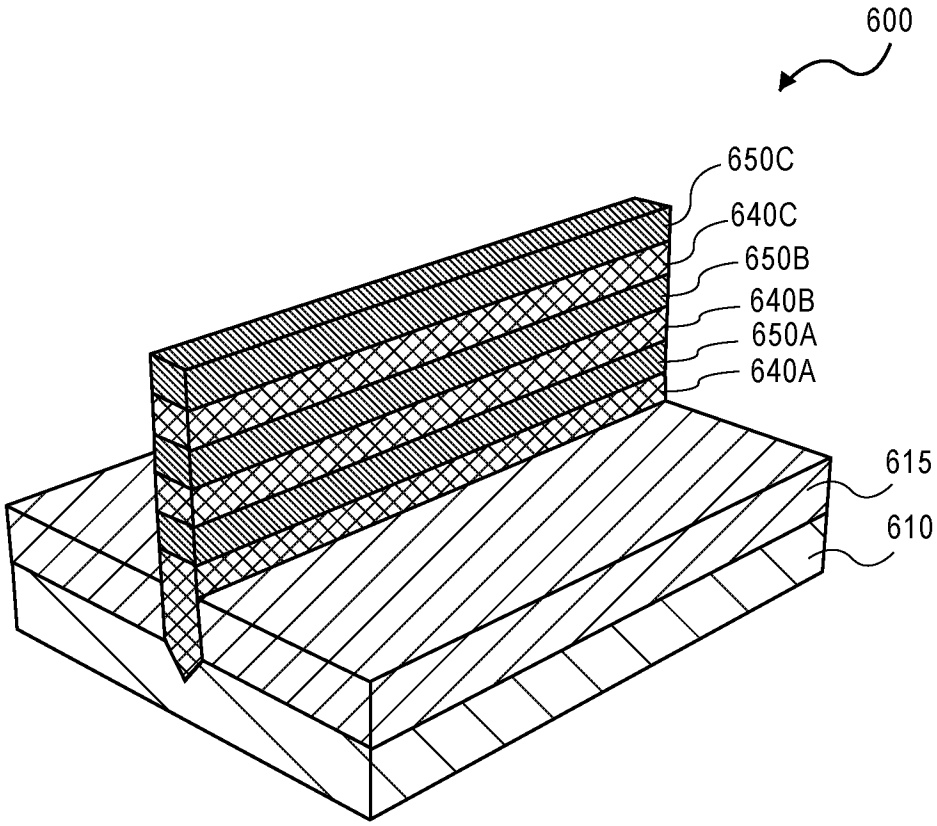

600
650C
640C
650B
640B
650A
640A
615
610

FIG. 19

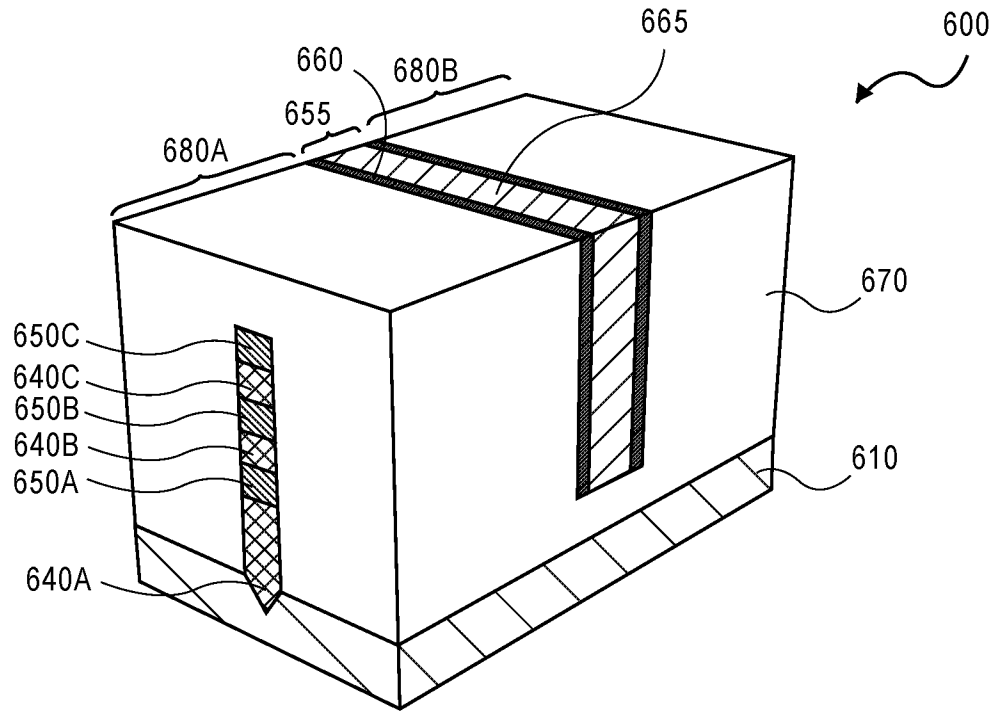

665
600
660
680B
655
680A
670
650C
640C
650B
640B
650A
610
640A

FIG. 20

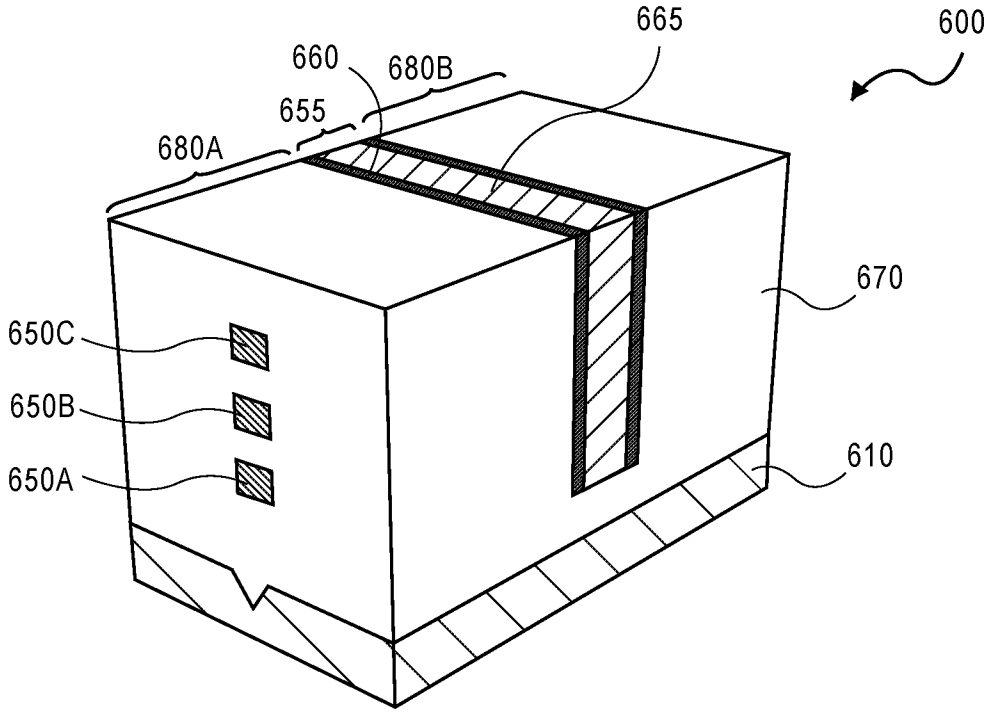

665
600
660
680B
655
680A
670
650C
650B
650A
610

FIG. 21

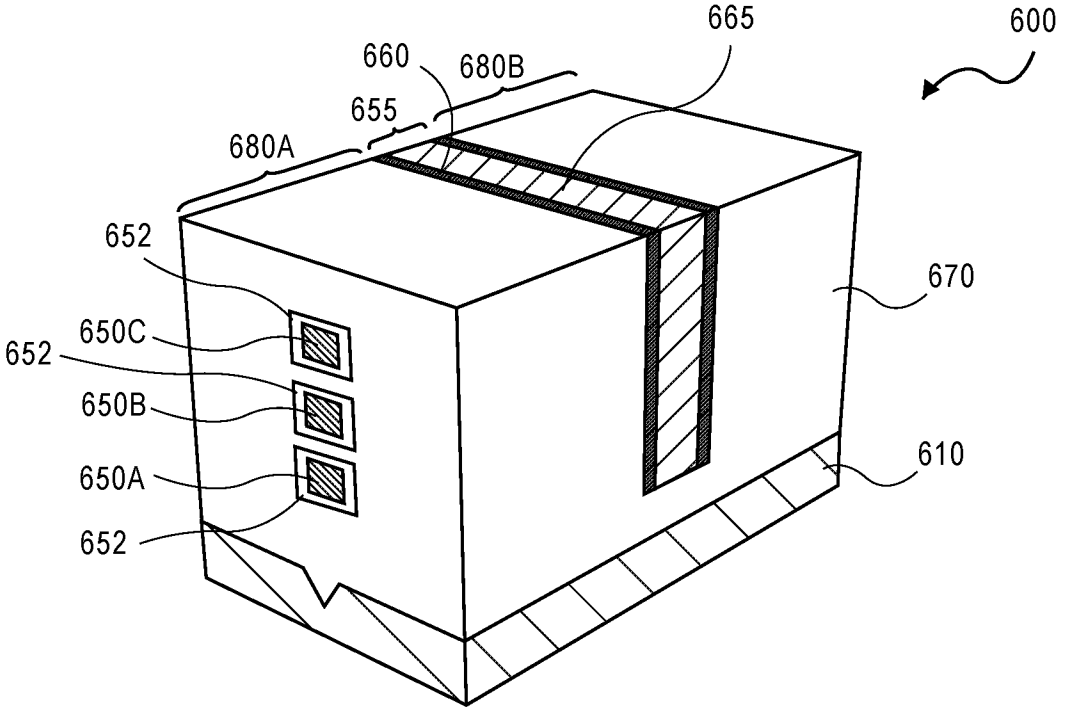

665
600
660
680B
655
680A
652
670
650C
652
650B
650A
610
652

FIG. 22

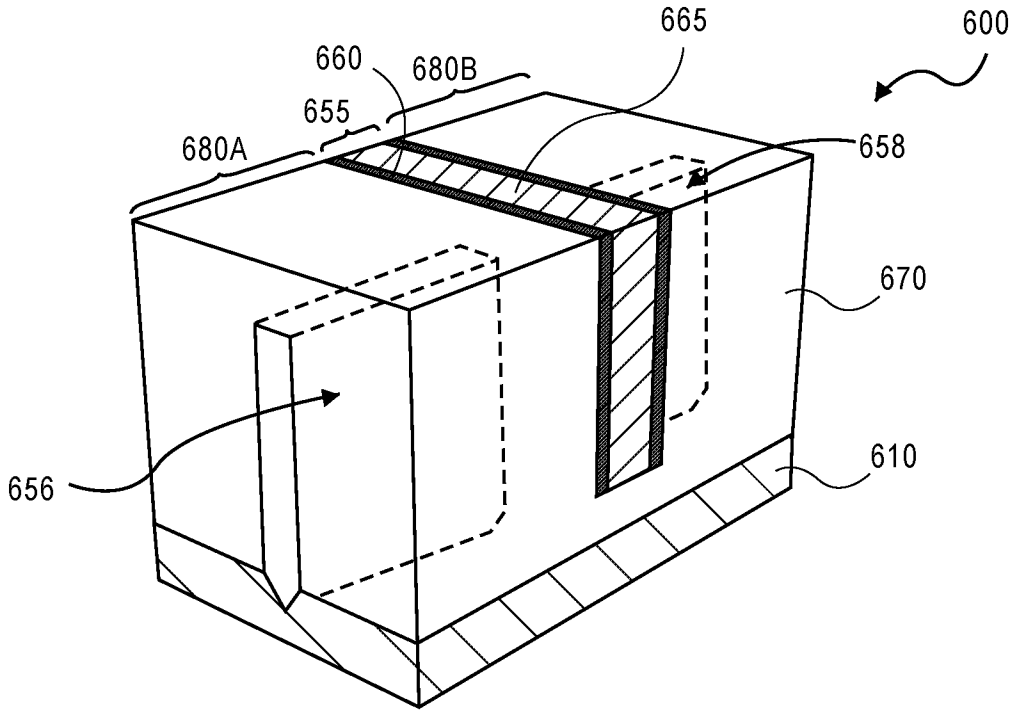

665
600
660
680B
655
680A
658
670
656
610

FIG. 23

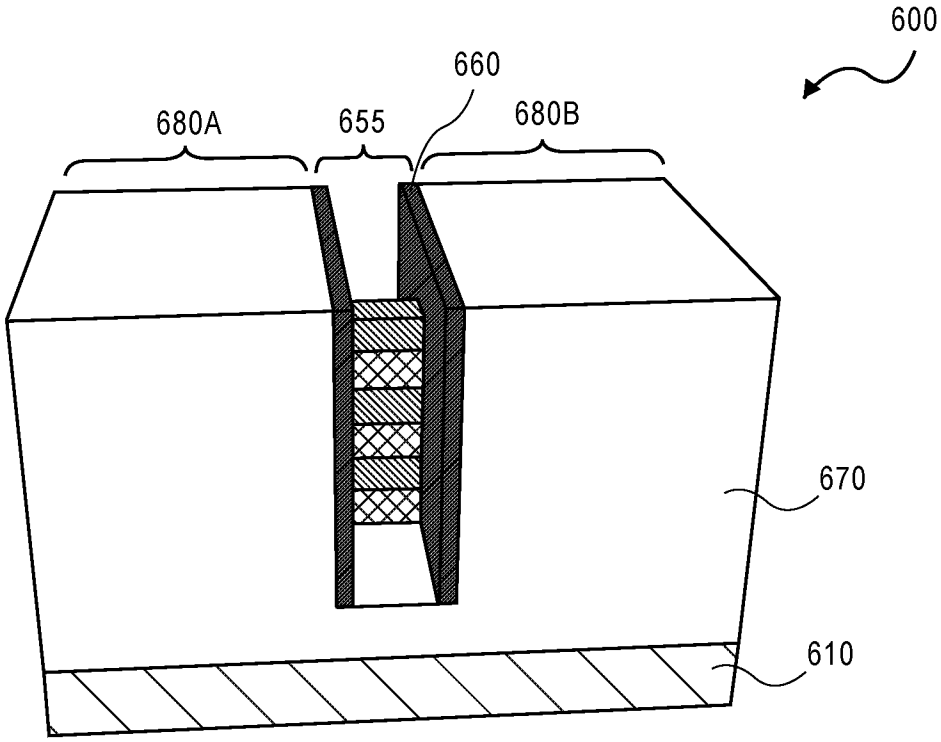


FIG. 24

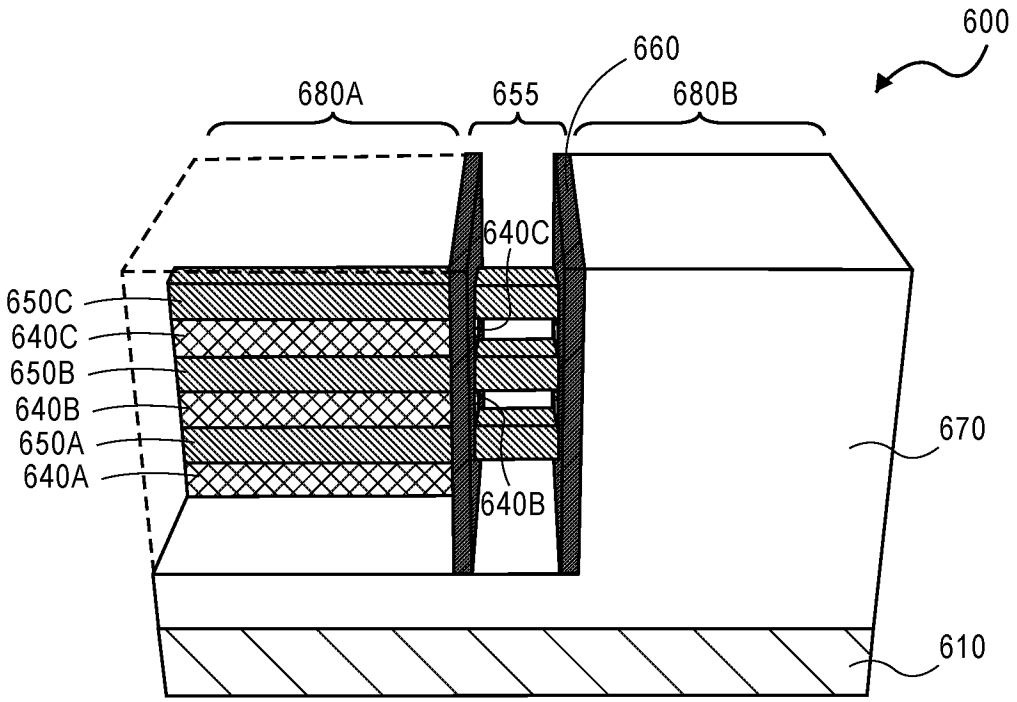

600
660
680A
655
680B
640C
650C
640C
650B
640B
650A
640A
640B
670
610

FIG. 25

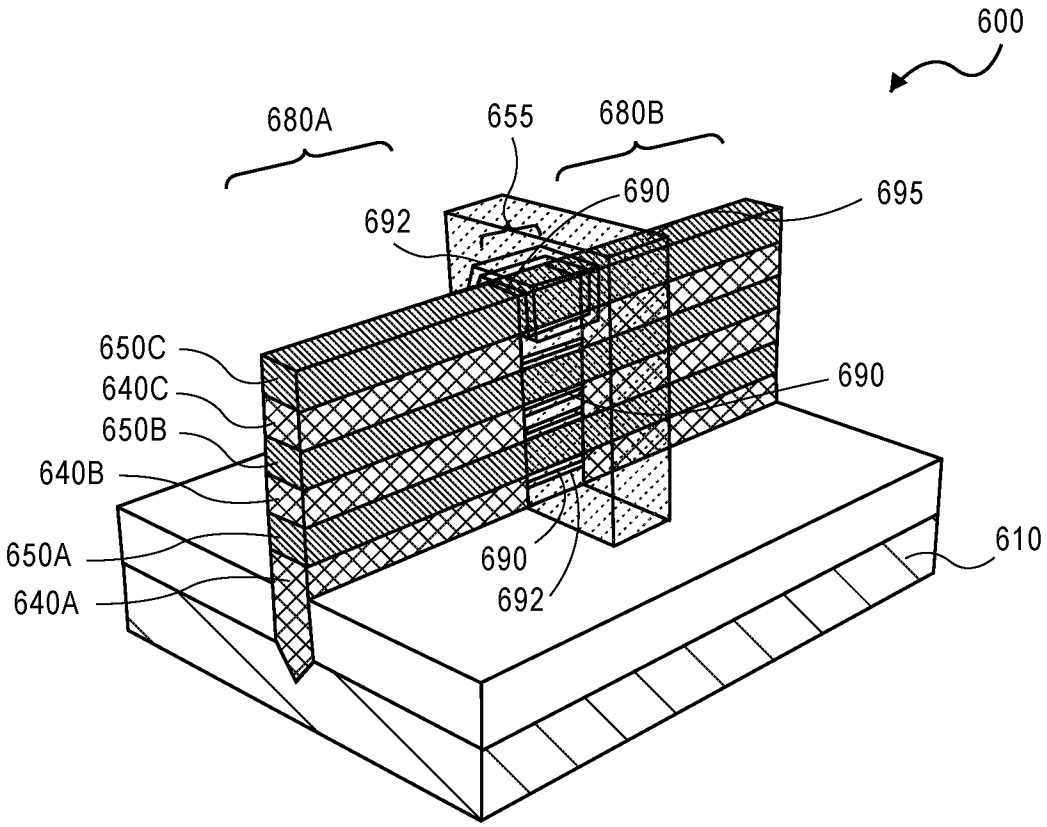

600
680A
655
680B
690
695
692
650C
640C
650B
640B
650A
640A
690
690
692
610

FIG. 26

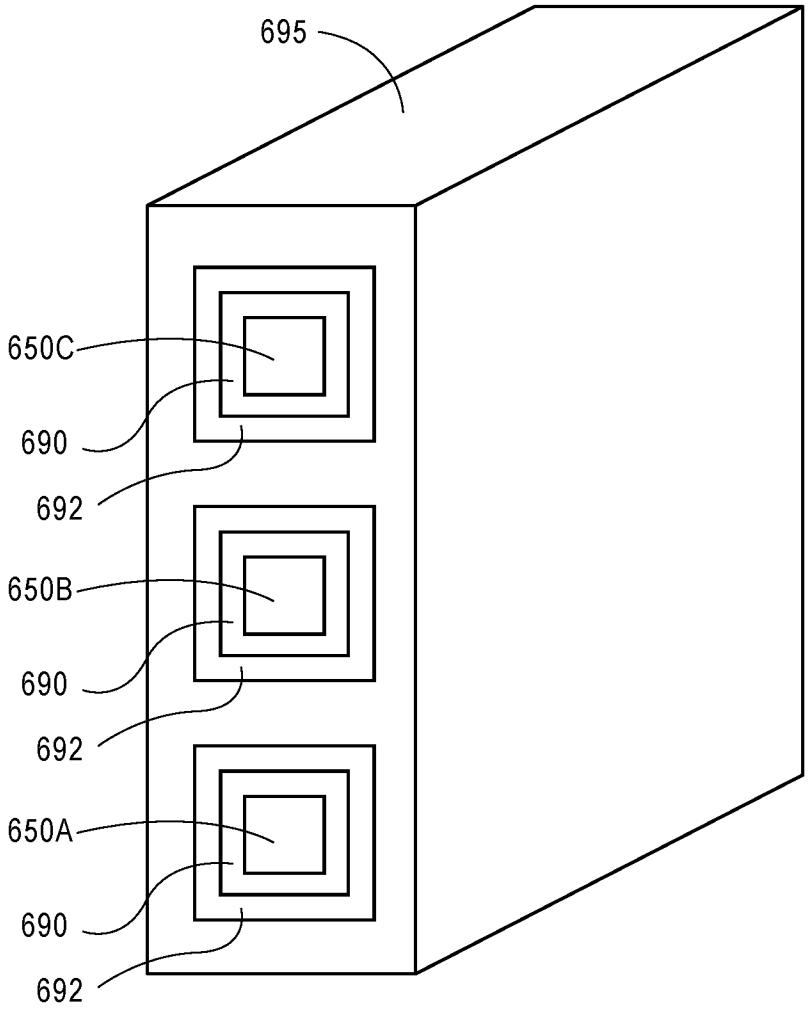


FIG. 27

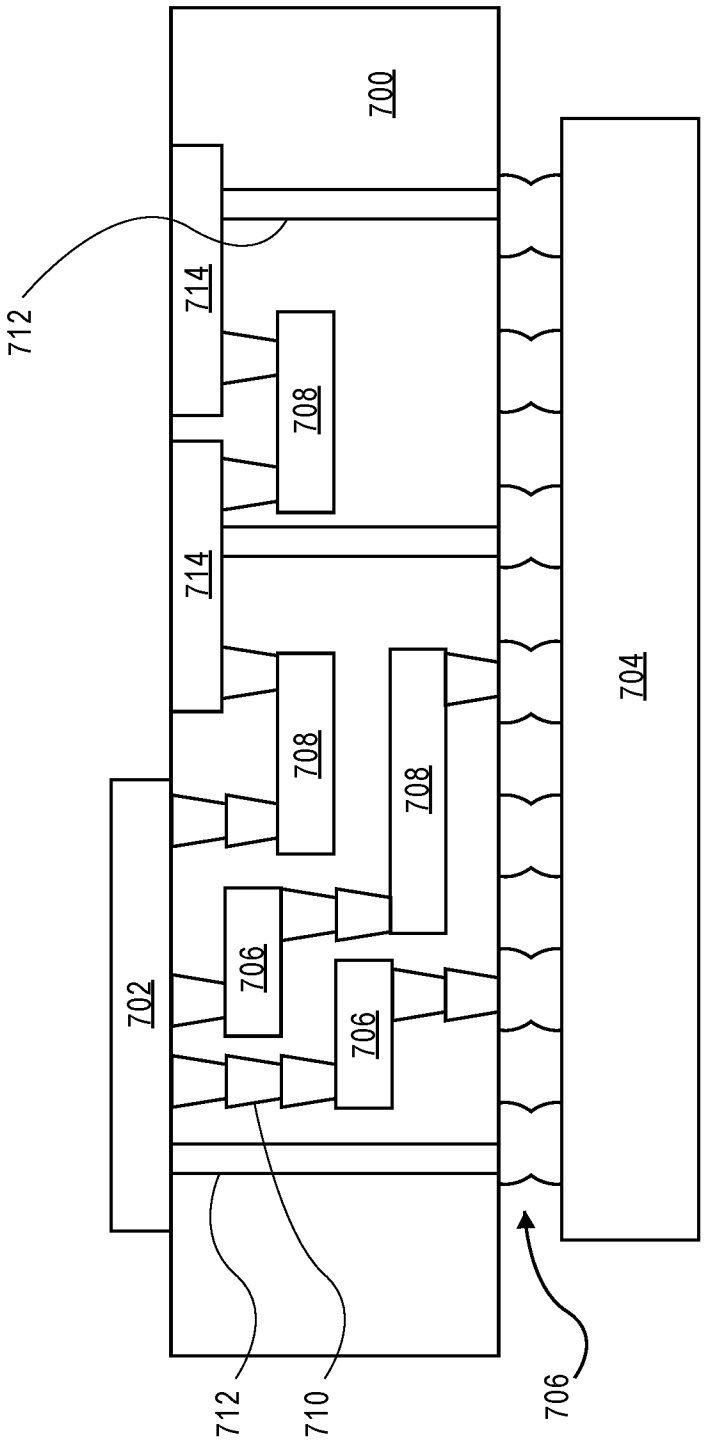


FIG. 28

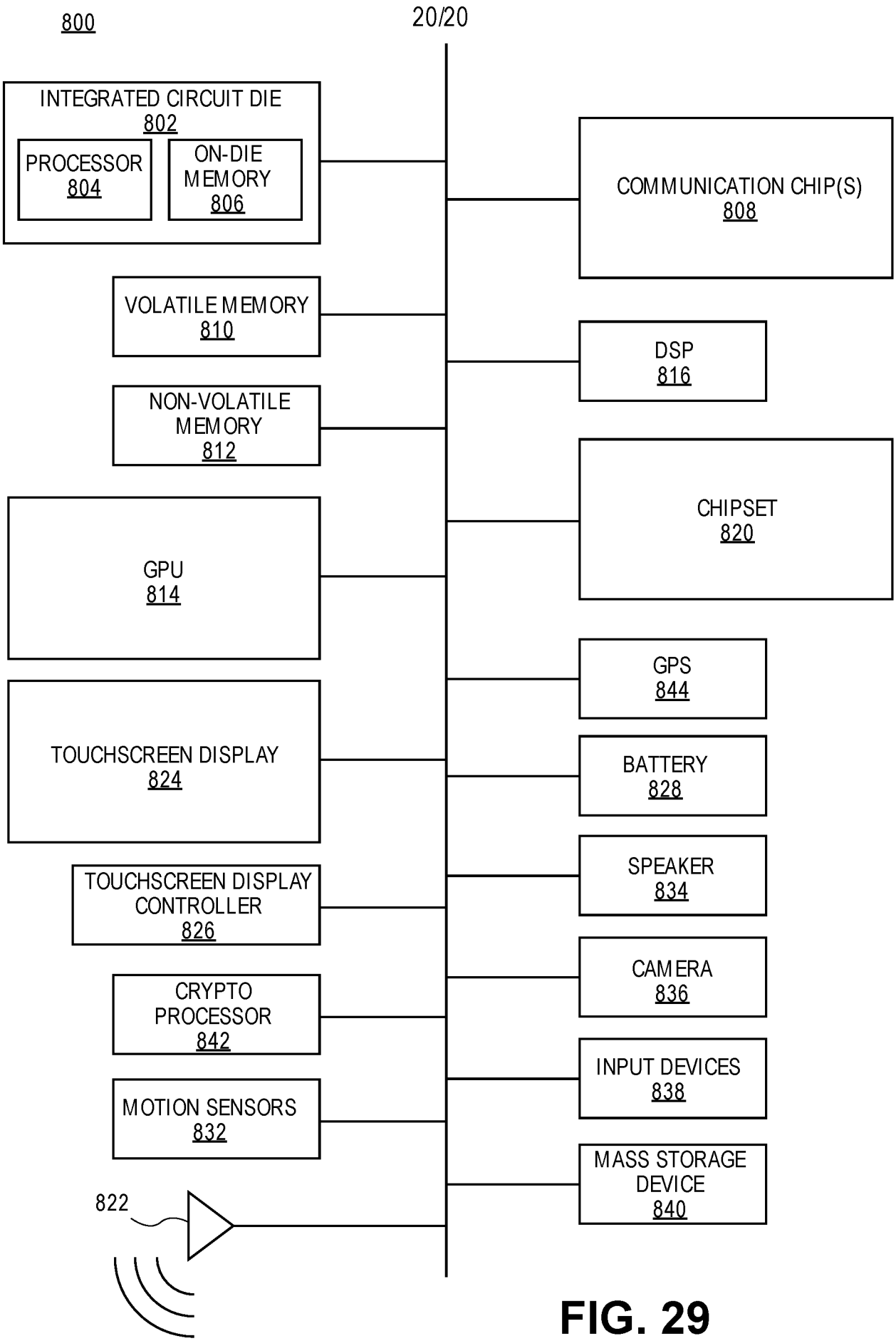

800
20/20
INTEGRATED CIRCUIT DIE
802
PROCESSOR
804
ON-DIE
MEMORY
806
VOLATILE MEMORY
810
NON-VOLATILE
MEMORY
812
GPU
814
TOUCHSCREEN DISPLAY
824
TOUCHSCREEN DISPLAY
CONTROLLER
826
CRYPTO
PROCESSOR
842
MOTION SENSORS
832
822
COMMUNICATION CHIP(S)
808
DSP
816
CHIPSET
820
GPS
844
BATTERY
828
SPEAKER
834
CAMERA
836
INPUT DEVICES
838
MASS STORAGE
DEVICE
840

FIG. 29

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/040894

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/28(2006.01)i, H01L 21/02(2006.01)i, H01L 29/78(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/28; H01L 29/778; H01L 21/336; H01L 29/78; H01L 21/338; H01L 29/786; H01L 29/423; H01L 21/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: transistor, gallium carbide, indium carbide, resistivity, gate electrode

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2016-043769 A1 (INTEL CORPORATION et al.) 24 March 2016 See page 6, lines 26-34 and figure 10.	1-22
A	JP 5906004 B2 (RENESAS ELECTRONICS CORP.) 20 April 2016 See paragraphs [0003]-[0012] and figure 6.	1-22
A	US 2011-0298060 A1 (TZE-CHIANG CHEN et al.) 08 December 2011 See paragraphs [0014]-[0017] and figures 1(a)-1(d)	1-22
A	WO 2016-068935 A1 (INTEL CORPORATION et al.) 06 May 2016 See page 6, lines 29-33 and figure 1.	1-22
A	US 2016-0056298 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 25 February 2016 See paragraphs [0145]-[0149] and figures 8A-8C.	1-22

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 March 2017 (20.03.2017)	**20 March 2017 (20.03.2017)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/040894

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2016-043769 A1	24/03/2016	TW 201631668 A	01/09/2016
JP 5906004 B2	20/04/2016	US 2010-0270559 A1	28/10/2010
		US 8680580 B2	25/03/2014
		WO 2009-066434 A1	28/05/2009
US 2011-0298060 A1	08/12/2011	CN 102893375 A	23/01/2013
		CN 102893375 B	25/11/2015
		DE 112011101215 B4	11/12/2014
		DE 112011101215 T5	07/02/2013
		GB 2493463 A	06/02/2013
		GB 2493463 B	25/06/2014
		TW 201208078 A	16/02/2012
		TW I515897 B	01/01/2016
		US 8492852 B2	23/07/2013
		WO 2011-151183 A1	08/12/2011
WO 2016-068935 A1	06/05/2016	TW 201628092 A	01/08/2016
US 2016-0056298 A1	25/02/2016	JP 2013-219327 A	24/10/2013
		US 2013-0200368 A1	08/08/2013
		US 9196741 B2	24/11/2015
		US 9484467 B2	01/11/2016