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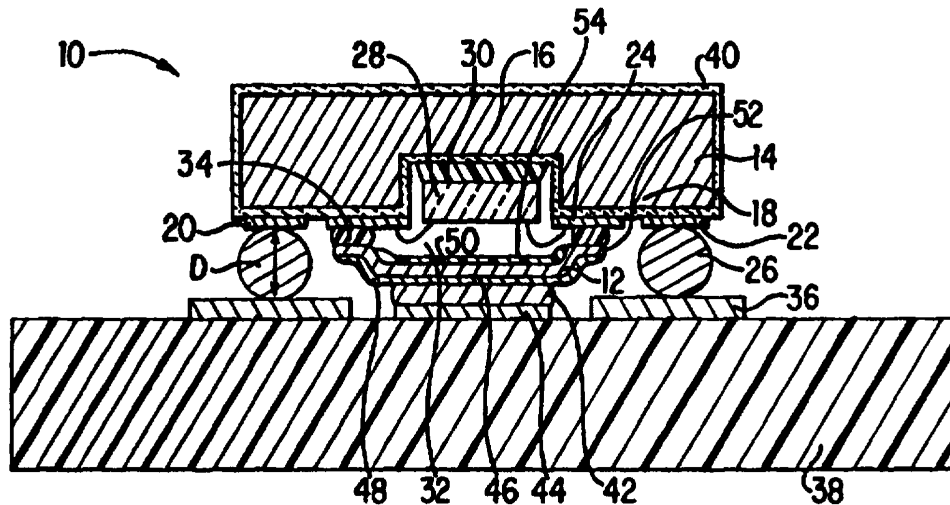

(57) Abstract

A surface mount package (10) to encapsulate one or more semiconductor devices (28) has a standoff (12) that maintains the thickness (D) of solder columns (26) bonding the package (10) to an external circuit (38). The standoff (12) either extends over or circumscribes a central portion (16) of the package base (14). To enhance the thermal performance of the standoff (12), a solderable layer (48) enhances soldering of the standoff (12) to the external circuit (38). In alternative embodiments, the standoff (12) contains a flange (58) having a plurality of apertures (62) useful for either mechanically locking an adhesive (34) or for enabling irradiation of an adhesive (34) by a light source. The standoff (12) may contain protrusions (64, 65) for alignment, strength or circuit (66) routing.

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BALL GRID ARRAY ELECTRONIC PACKAGE STANDOFF DESIGN

This invention relates to a standoff for a ball grid array electronic package. More
5 particularly, the amount of solder ball collapse is determined by a standoff attached to a central portion of the package base.

Electronic packages provide environmental and mechanical protection to an integrated circuit
10 device. Additionally, the electronic package provides a conduit for electrical signals to travel between external circuitry and the integrated circuit device. One type of electronic package is referred to as a surface mount package. With a
15 surface mount package, electrically conductive sites on the package body are soldered directly to bond pads on an external circuit, such as a printed circuit board. A surface mount package does not require external leads and therefore, requires less
20 space for mounting on the external circuit. One type of surface mount package is a ball grid array electronic package.

Ball grid array electronic packages are used to house one or more integrated circuit devices,
25 such as silicon based semiconductor chips. The ball grid array electronic packages have a base component containing a plurality of metallized circuit traces. A semiconductor device is bonded to a central portion of the base component and is

electrically interconnected to one end of the circuit traces.

The opposing ends of the circuit traces form an array about a peripheral portion of the base 5 component. Solder balls are then attached to each point of this array.

A covering encapsulates a central portion of the base component, the semiconductor device and the inner ends of the circuit traces. The solder 10 balls then bond the ball grid array electronic package to an external structure, such as a printed circuit board.

One type of a ball grid array electronic package has a metallic base component that is 15 typically an aluminum alloy. An anodization layer coats portions of the base component to provide electrical isolation between the circuit traces and the metallic base component. This type of ball grid array is disclosed in PCT Publication WO 20 96/03020 that was published on February 1, 1996.

When the solder balls melt and become liquid, surface tension attraction of the liquid solder to the array on the package base and to a matching array of metallized pads on a printed circuit board 25 causes the ball grid array package to self center, facilitating alignment of the package. However, the weight of the package compresses the liquid solder prior to solidification into a solder joint.

The thinner the solder joint, once solidified, 30 the more prone that joint is to fatigue fracture. Fatigue fracture occurs because the coefficients of thermal expansion of the electronic package base and of the external structure are different. As the package base is cyclically heated and cooled, 35 during operation of the semiconductor device,

stresses are applied to the solder joints. These stresses propagate stress cracks through the solder joints. When a stress crack extends across the diameter of the solder joint, package failure occurs.

One way to minimize fracture of the solder joints is to maintain a relatively thick solder joint following soldering. PCT Publication WO 96/03020 discloses a standoff, polymer protrusions at the peripheral corners of the package base, that maintains the height of the solder joint. Other standoffs are disclosed in U.S. Patent No. 4,816,896 to Owens and 5,045,921 to Lin et al. In the Owens patent, an apertured standoff is designed to fit over the corner pins of a pin grid array electronic package. In the Lin et al. patent, a centrally disposed cover component determines the height of the solder joints.

While the prior art standoffs are effective, there remains a need for a centrally disposed standoff that facilitates package assembly and alignment.

Accordingly, it is an object of the present invention to provide a standoff for a ball grid array electronic package. It is a feature of the invention that this standoff is bonded to a central portion of the package base and either encapsulates or circumscribes the central portion of the base.

In one embodiment of the invention, the standoff has a solderable first major surface and an electrically insulating second major surface. Alternatively, the standoff has a central portion and a parallel running, non-planar, peripheral flange. A plurality of apertures may extend through the flange. In another embodiment, a

plurality of extensions protrude from either the central portion or from the flange.

Among the advantages of the standoffs of the invention are that the amount of solder ball squeeze-out is controlled, minimizing fatigue fracture. In some embodiments, the standoff is bonded to an external structure to reduce stresses applied to the solder balls and to provide a conduction path for enhanced thermal dissipation. In alternative embodiments, a gap is provided under a portion of the standoff to permit circuit traces to extend beneath the standoff.

In accordance with the invention, there is provided a cover for an electronic package. The cover has a substrate with a first major surface that is generally parallel to a second major surface and sidewalls that extend from the first major surface to the second major surface. A solderable layer coats a central portion of the first major surface.

Optionally, an electrically insulating layer may coat a central portion of the second major surface.

In accordance with another embodiment of the invention, the cover for the electronic package has a substrate with a central portion and a parallel running, non-planar, peripheral flange. The flange may contain a plurality of apertures extending therethrough. Optionally, a plurality of extensions may protrude from either the central portion of the cover or from the flange.

The above stated objects, features and advantages will become more apparent from the specification and drawings that follow.

Figure 1 shows in cross-sectional representation a ball grid array package, including a standoff in accordance with an embodiment of the invention.

5 Figure 2 illustrates in cross-sectional representation a standoff in accordance with a second embodiment of the invention.

Figure 3 illustrates in top planar view the standoff of Figure 2.

10 Figure 4 shows in top planar view a standoff in accordance with another embodiment of the invention.

Figure 5 shows in top planar view a standoff in accordance with another embodiment of the

15 invention.

Figure 6 illustrates in partial perspective view circuit traces extending under the standoff of either Figure 4 or Figure 5.

Figure 7 shows in cross-sectional

20 representation a standoff in accordance with another embodiment of the invention.

Figure 8 illustrates in top planar view the standoff of Figure 7.

Figure 9 illustrates in top planar view a

25 standoff in accordance with another embodiment of the invention.

Figure 10 illustrates in cross-sectional representation a ball grid array electronic package utilizing the standoff of Figure 9.

30 Figure 1 illustrates in cross-sectional representation a ball grid array electronic package 10 utilizing a standoff 12 in accordance with an embodiment of the invention. The ball grid array package 10 includes a base 14 having a central

35 portion 16 and a peripheral portion 18. A

plurality of circuit traces 20 are formed on the peripheral portion 18 of the base. Each circuit trace 20 has an external end 22 and an inner end 24. The external ends 22 of the circuit traces form an array. Solder balls 26 having a diameter "D" prior to melting are bonded to the external ends 22. A semiconductor device 28 is bonded, by die attach 30, to the central portion 16 of the base 14. Small bond wires 32, or optionally, thin strips of copper foil as utilized in tape automated bonding, electrically interconnect the semiconductor device 28 to the inner ends 24 of the circuit traces 20.

The standoff 12, extends across the central portion 16, forming a cover to encapsulate the semiconductor device 28, bond wires 32 and inner ends 24 of the circuit traces 20. The standoff 12 is bonded to the base 14 by a bonding agent 34 that is any suitable polymer, solder or sealing glass. Preferably, the bonding agent 34 is thermosetting adhesive such as an epoxy.

The combined height of the bonding agent 34 and the standoff 12 relative to the base 14 is less than the diameter "D" of the solder balls 26. Preferably, the difference between the combined height and the diameter is between 0.13 mm (0.005 inch) and 0.76 mm (0.030 inch), and most preferably, the difference is between 0.51 mm (0.020 inch) and 0.64 mm (0.025 inch). As a result, on bonding the solder balls 26 to an electrically conductive array 36 formed on an external structure, such as a printed circuit board 38, the solder joints formed by the melting and re-solidification of the solder balls 26 are defined

by the combined height of the bonding agent 34 and standoff 12.

The package base 14 is typically formed from a metal or a metal alloy such as copper, copper alloys, aluminum and aluminum alloys. The metallic base 14 is coated with a dielectric layer 40 that electrically isolates the circuit traces 20 from the metallic base 14. When the base 14 is aluminum or an aluminum alloy, the dielectric layer 40 may be an anodic film having a thickness between 0.013 mm and 0.025 mm (0.0005 and 0.001 inch).

During operation, the semiconductor device 28 generates heat. Efficient operation of the semiconductor device 28 requires that this heat be dissipated to avoid excessively raising the temperature of the semiconductor device. The heat readily flows into the metallic base 14 and, by providing a direct thermal link between the standoff 12 and the printed circuit board 38, efficient dissipation of heat is achieved. This direct thermal link is formed by bonding the standoff 12 to the printed circuit board 38 through a cover solder 42. The cover solder 42 is any material that efficiently conducts heat and bonds to both the standoff 12 and to a bonding pad 44 formed on the printed circuit board. Preferably, the cover bonding agent 42 is a low-melting solder such as a lead/tin alloy. To enhance bonding of the cover solder 42 to the standoff 12, a first major surface 46 of the standoff 12 is coated with a solderable layer 48.

One suitable solderable layer 48 is a nickel coating having a thickness between 1 micron and 10 microns. Other suitable materials for the

solderable layer 48 include gold, palladium, copper, tin and alloys thereof.

By bonding the standoff to the external structure 38, the joint reliability of the inner row of solder joints is improved. This is because flexing of the package in a vertical direction is reduced. Soldering is preferred over other methods of attachment, such as a thermosetting adhesive, because soldering is an inherently reworkable process and soldering is readily adaptable to convection, vapor phase and infrared heating that is typically used in electronic package assembly.

Running generally parallel to the first major surface 46 of the standoff 12 is a second major surface 50. The first major surface 46 and second major surface 50 are joined together by sidewalls 52. If the standoff 12 is formed from a metal or a metal alloy, such as copper, aluminum or an alloy thereof, it is preferable for at least a central portion of the second major surface 50 to be coated with an electrically insulating layer 54. The electrically insulating layer 54 prevents electrical short circuits in the event that a bond wire 32 contacts the standoff 12 and facilitates a lower package profile by not requiring a significant gap between the apex of the bond wires 32 and the second major surface 50 of the standoff 12.

The electrically insulating layer 54 may be an anodic film when the standoff 12 is aluminum or an aluminum alloy. Alternatively, the electrically insulating layer 54 is a thin, on the order of 0.0025 mm (0.0001 inch) to 0.051 mm (0.002 inch) polymer coating. Suitable polymer coatings include epoxies, thermoplastics and polyimides. These

polymeric coatings are preferred because they also enhance the adhesion of the bonding agent 34 to the standoff 12 and prevent corrosion. Additionally, when the electrically insulating layer 54 is a polymeric coating that extends under the bonding agent 34, the coating functions as a stress buffer to compensate for coefficient of thermal expansion differences between the standoff 12 and the base 14 of the ball grid array package 10.

Alternative standoffs are illustrated in Figures 2 through 10. In the embodiment illustrated in cross-sectional representation in Figure 2 and top planar view in Figure 3, the standoff 12 has a central portion 56 and a parallel running peripheral flange 58 that, while generally parallel with, is non-planar with the central portion 56. The combination of the central portion 36 and flange 58 defines a central cavity 60 underlying the second major surface 50 of the central portion 56. A plurality of apertures 62 extend through the flange 58.

As illustrated in Figure 3, the apertures preferably form a uniform array of holes through the flange 58, circumscribing the central portion 56. While the height of the central portion 56 relative to a package base defines the standoff height, the apertures 62 are useful for improving the adhesion of the standoff 12 to a package substrate. A bonding agent flows into the apertures 62 during cure, forming a mechanical lock that increases the strength of the adhesive bond.

The apertures 62 enable the use of photo-curable adhesives that facilitate attachment of the standoff 12 to a package substrate without heat. An underlying adhesive is irradiated with a

suitable energy source such as infrared light or ultraviolet light through the apertures 62. One exemplary adhesive is a UV-curable epoxy.

5 As illustrated in Figures 4 and 5, the standoff height may be defined by dimples 64 or ridges 65 that protrude from the central portion 56 in a direction outward from the flange 58. The dimples preferably have a height of from 0.13 mm (0.005 inch) to 0.25 mm (0.010 inch) above the
10 central portion 56.

The advantage of this embodiment is illustrated in Figure 6. Circuitry 66 formed on the printed circuit board 38 can travel under the standoff 12 in the space defined by the dimples 64
15 or ridges. By minimizing the contact area with the printed circuit board 38, greater space is available for the routing of circuitry 66.

With reference to Figures 7 and 8, the standoff 12 may include alignment features 68 such
20 as dimples that mate with holes or other features in the package base. The dimples preferably have a height of from 0.13 mm (0.005 inch) to 0.25 mm (0.010 inch) above the surface of the flange 58.

Alternatively, ribs or a pattern of
25 reinforcing dimples 70 may be provided in non-critical portions of the standoff, such as along a diagonal or disposed about the center of the standoff to increase the stiffness of the central portion 56.

30 In all embodiments, the flange 58 may have a width effective to provide a longer seal path to prevent moisture or contamination ingress. The larger width flange also provides greater mechanical strength adhesion between the standoff
35 and the bonding adhesive. Typically, the flange 58

width is equal to or greater than 1 mm (0.040 inch). Preferably, the flange 58 extends to the perimeter of the package base.

5 Rather than encasing the central portion of an electronic package base, the standoff may circumscribe this portion as illustrated in Figure 9. In Figure 9, the standoff 72 is a frame having a first side 74 and an opposing second side. The frame circumscribes a central aperture 76 and
10 contains a plurality of extensions 78 protruding from the first surface 74. These protrusions typically extend for a height of from 0.13 mm (0.005 inch) to 0.25 mm (0.010 inch) above the first surface 74. The use of the standoff 72 is
15 illustrated in Figure 10.

In Figure 10, the ball grid array electronic package 80 has many features similar to those described in the ball grid array package of Figure 1. These common components are identified by like
20 reference numerals and not fully described herein.

The package base 14 contains circuit traces 20 formed on a peripheral portion 18 thereof. In the event that the base 14 is formed from an electrically conductive material, a dielectric
25 layer 40 coats at least those surfaces of the base 14 underlying the circuit traces 20. Solder balls 26 are bonded to external ends of the circuit traces 20.

A semiconductor device 28 is bonded to a
30 central portion 16 of the base 14 through die attach 30. The central portion is recessed to form a cavity 82. A portion of this cavity is occupied by the semiconductor device 28 and die attach 30.

The standoff 72 is adhesively bonded to the
35 base 14 to circumscribe the cavity 82. That

portion of the cavity 82 not occupied by the semiconductor device 28 or die attach 30, as well as the central aperture 76 of the standoff are filled with a polymer resin 84. One suitable 5 polymer resin is a thermosetting epoxy adhesive. The resin generally fills the cavity 82 and central aperture 76 up to the first surface 74 of the standoff 72.

When the solder balls become molten, the 10 extensions 78 define the height of the solder columns.

While the invention has been described in terms of ball grid array electronic packages, it is equally applicable to other types of surface mount 15 packages such as leadless chip carriers.

It is apparent that there has been provided in accordance with this invention a standoff for a surface mount electronic package that fully satisfies the objects, features and advantages set 20 forth hereinabove. While the invention has been described in combination with specific embodiments thereof, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art in light of the foregoing 25 description. Accordingly, it is intended to embrace all such alternatives, modifications and variations as fall within the spirit and broad scope of the appended claims.

IN THE CLAIMS:

1. A cover (12) for an electronic package (10), characterized by:

a substrate having a first major surface (46)
5 that is generally parallel running to a second major surface (50) and sidewalls (52) extending from said first major surface (46) to said second major surface (50); and

a solderable layer (48) coating a central
10 portion (56) of said first major surface (46).

2. The cover (12) of claim 1 characterized in that said solderable layer (48) is selected from the group consisting of nickel, gold, palladium, copper, tin, and alloys thereof.

15 3. The cover (12) of claim 2 characterized in that an electrically insulating layer (54) coats a central portion (56) of said second major surface (50).

4. A cover (12) for an electronic package (10),
20 characterized by:

an electrically conductive substrate having a first major surface (46) that is generally parallel running to a second major surface (50) and sidewalls (52) extending from said first major
25 surface (46) to said second major surface (50); and

an electrically insulating layer (54) coating a central portion (56) of said second major surface (50).

5. The cover (12) of either claim 3 or claim 4 characterized in that said electrically insulating layer (54) is selected from the group consisting of anodic films, polyimides, thermoplastics and
5 epoxies.

6. The cover (12) of claim 5 characterized in that said electrically insulating layer (54) is an epoxy having a thickness of between 0.0025 mm and 0.51 mm.

10 7. A cover (12) for an electronic package (10), characterized by:

a substrate having a central portion (56) and a parallel running, non-planar peripheral flange (58); and

15 said flange (58) containing a plurality of apertures (62) extending therethrough.

8. A cover (12) for an electronic package (10), characterized by:

a substrate having a central portion (56) and
20 a parallel running, non-planar peripheral flange (58); and

a plurality of extensions (64, 65) protruding from said central portion (56).

9. The cover (12) of claim 8 characterized in
25 that said extensions (64, 65) extend diagonally across said central portion (56).

10. A cover (12) for an electronic package, characterized by:

a substrate having a central portion (56) and a parallel running, non-planar peripheral flange
5 (58); and

a plurality of extensions (64, 65) protruding outward from said flange (58) in a direction away from said central portion (56).

11. The cover (12) of any one of claims 8-10
10 characterized in that said extensions (64, 65) protrude for a height of from 0.13 mm to 0.25 mm above said flange (56).

12. A cover for an electronic package (80), characterized by:
15 a frame (72) having first (74) and second opposing sides circumscribing a central aperture (76); and

a plurality of extensions (78) protruding outward from said first side (74).

20 13. The cover of claim 12 characterized in that said plurality of extensions (78) have a height of from 0.13 mm to 0.25 mm above said first side (74).

14. A ball grid array electronic package (10), characterized by:

a base (14) having a central portion (16) and a peripheral portion (18);

5 a plurality of circuit traces (20) formed on the peripheral portion (18) of said base (14), said of each circuit traces (20) having an inner end (24) adjacent the central portion (16) of said base (14) and an external end (22) forming a point on an 10 array formed on said peripheral portion (18) of said base (14);

solder balls (26) having a diameter bonded to points of said array;

a semiconductor device (28) bonded (30) to 15 said central portion (16) and electrically interconnected (32) to said inner ends (24) of said circuit traces (20); and

a standoff (12) joined to said base (14) by a first adhesive (34), said standoff (12) having a 20 first major surface (46) that is generally parallel running to a second major surface (50) and sidewalls (52) extending from said first major surface (46) to said second major surface (50), the combined height of said first adhesive (34) and 25 said standoff (12) being less than the diameter of said solder balls (26).

15. The ball grid array electronic package (10) of claim 14 characterized in that a central portion (56) of said first major surface (46) is coated 30 with a solderable layer (48).

16. The ball grid array electronic package (10) of either claim 14 or claim 15 characterized in that a central portion (56) of said second major surface (50) is coated with electrically insulating layer
5 (54).

17. The ball grid array electronic package (10) of claim 16 characterized in that said electrically insulating layer (54) is selected from the group consisting of anodic films, thermoplastics,
10 polyimides and epoxy.

18. The ball grid array electronic package (10) of claim 14 characterized in that said standoff (12) has a centrally disposed central portion (50) and a peripheral flange (58) with said flange (58) having
15 a width effective to prevent moisture ingress and to provide greater mechanical strength adhesion to a bonding agent (34).

19. The ball grid array electronic package (10) of claim 14 characterized in that said standoff (12)
20 has a centrally disposed central portion (56) and a peripheral flange (58) with said flange (58) having a plurality of apertures (62).

20. The ball grid array electronic package (10) of claim 14 characterized in that said standoff (12)
25 has a centrally disposed central portion (56) and a peripheral flange (58) with protrusions (64, 65) extending outwardly from at least one of said flange (58) and said central portion (56).

21. A ball grid array electronic package (80), characterized by:

a base (14) having a central portion (16) and a peripheral portion (18);

5 a plurality of circuit traces (20) formed on the peripheral portion (18) of said base (14), said each of circuit traces (20) having an inner end (24) adjacent to the central portion (16) of said base (14) and an external end (22) forming a point 10 on an array formed on said peripheral portion (18) of said base (14);

solder balls (26) having a diameter bonded to points of said array;

a semiconductor device (28) bonded (30) to 15 said central portion (16) and electrically interconnected (32) to said inner ends (24) of said circuit traces (20); and

a standoff (72) having first (74) and second opposing sides with a height less than the diameter 20 of said solder balls (26) having said second side bonded to said base (14) circumscribing a perimeter of said central portion (16) thereof.

22. The ball grid array electronic package (80) of claim 21 characterized in that said first side (74) 25 of said standoff (72) has protrusions (78) extending therefrom.

23. The ball grid array electronic package (80) of claim 22 characterized in that a polymer resin (84) fills said central portion (16) of said base (80) 30 and said standoff (72) up to said first side (74).

AMENDED CLAIMS

[received by the International Bureau on 28 July 1997 (28.07.97); original claims 7-9, 14 and 21 amended; original claims 1-6, 12 and 13 cancelled; new claim 24 added; remaining claims unchanged (5 pages)]

7. A cover (12) for an electronic package (10), characterized by:

a substrate having a central portion (56) and a parallel running, non-planar peripheral flange (58); and

said flange (58) containing a plurality of apertures (62) extending
5 therethrough, said apertures (62) uniformly arranged and circumscribing said central portion (56).

8. A cover (12) for an electronic package (10), characterized by:

a substrate having a central portion (56) and a parallel running, non-planar peripheral flange (58); and

10 a plurality of extensions (64) protruding from said central portion (56), said extensions being dimples.

9. The cover (12) of either claim 8 or claim 24 characterized in that said extensions (64, 65) extend diagonally across said central portion (56).

10. A cover (12) for an electronic package, characterized by:

a substrate having a central portion (56) and a parallel running, non-planar peripheral flange (58); and

a plurality of extensions (64, 65) protruding outward from said flange
5 (58) in a direction away from said central portion (56).

11. The cover (12) of any one of claims 8-10 characterized in that said extensions (64, 65) protrude for a height of from 0.13 mm to 0.25 mm above said flange (56).

14. A ball grid array electronic package (10), characterized by:
a base (14) having a central portion (16) and a peripheral portion (18);
a plurality of circuit traces (20) formed on the peripheral portion (18)
5 of said base (14), each of said circuit traces (20) having an inner end (24) adjacent the central portion (16) of said base (14) and an external end (22) forming a point on an array formed on said peripheral portion (18) of said base (14);
solder balls (26) having a diameter bonded to points of said array;
a semiconductor device (28) bonded (30) to said central portion (16)
10 and electrically interconnected (32) to said inner ends (24) of said circuit traces (20); and
a standoff (12) having a central portion (56) and a generally parallel, non-planar flange portion (58) joined to said base (14) by a first adhesive (34), said standoff (12) having a first major surface (46) that is generally parallel running to a
15 second major surface (50) and sidewalls (52) extending from said first major surface (46) to said second major surface (50), the combined height of said first adhesive (34) and said standoff (12) being less than the diameter of said solder balls (26).

15. The ball grid array electronic package (10) of claim 14 characterized
20 in that a central portion (56) of said first major surface (46) is coated with a solderable layer (48).

21. A ball grid array electronic package (80), characterized by:
a base (14) having a central portion (16) and a peripheral portion (18);
a plurality of circuit traces (20) formed on the peripheral portion (18)
5 of said base (14) each of said circuit traces (20) having an inner end (24) adjacent to the central portion (16) of said base (14) and an external end (22) forming a point on an array formed on said peripheral portion (18) of said base (14);
solder balls (26) having a diameter bonded to points of said array;
a semiconductor device (28) bonded (30) to said central portion (16)
10 and electrically interconnected (32) to said inner ends (24) of said circuit traces (20); and
a standoff frame (72) having first (74) and second opposing sides with a height less than the diameter of said solder balls (26) having said second side bonded to said base (14) circumscribing a perimeter of said central portion (16)
15 thereof.

22. The ball grid array electronic package (80) of claim 21 characterized in that said first side (74) of said standoff (72) has protrusions (78) extending therefrom.

23. The ball grid array electronic package (80) of claim 22 characterized
20 in that a polymer resin (84) fills said central portion (16) of said base (80) and said standoff (72) up to said first side (74).

24. A cover (12) for an electronic package (10), characterized by:

a substrate having a central portion (56) and a parallel running, non-planar peripheral flange (58); and

5 a plurality of extensions (65) protruding from said central portion (56), said extensions being ridges.

STATEMENT UNDER ARTICLE 19

In reference to the above-identified International patent application, this is the response to the PCT International Search Report (Form PCT/ISA/210) mailed 02 June, 1997 having a statutory period for response set to expire on 02 August, 1997. Applicant encloses herewith replacement pages 14, 15, 16, 18/1 and 18/2 to replace pages 13-16 and 18 as originally filed with the International Application. As the result of this amendment, claims 1-6 and 12-13 have been canceled. Claims 7-9, 14 and 21 have been amended. New claim 24 is added. Claims 10, 11, 15-19, 22 and 23 are unchanged.

Claim 7 has been amended to recite that the apertures extending around the flange of the electronic package cover are in the form of a uniform array that circumscribes a central portion of that cover. Such an array is illustrated in Applicant's Figure 3. This is different than two mounting holes positioned on opposing sides of a flange of an electronic package cover as disclosed in U.S. 4,731,644 and also different than apertures formed through the insulating polymer layer of a tape automative bonding tape as illustrated in U.S. 5,083,191.

Regarding claim 14, a grammatical error has been corrected in claims 6 and 7 to more precisely claim the invention. The standoff is identifid as having a central portion and a generally parallel, non-planar flange portion in accordance with Applicant's specification at page 9, lines 13-17. The flange enhances the bond between the electronic package and the standoff. Such a flange for a standoff is neither taught nor suggested by any of the references of record in the present application.

Claim 21 has been amended to correct a grammatical error in line 6-7, similar to the error corrected in line 14. The standoff is identified as a frame in accordance with Applicant's specification at page 11, lines 7-8 and Applicant's Figures 9 and 10. A frame-like standoff is neither taught nor suggested by any of the references of record in the present application.

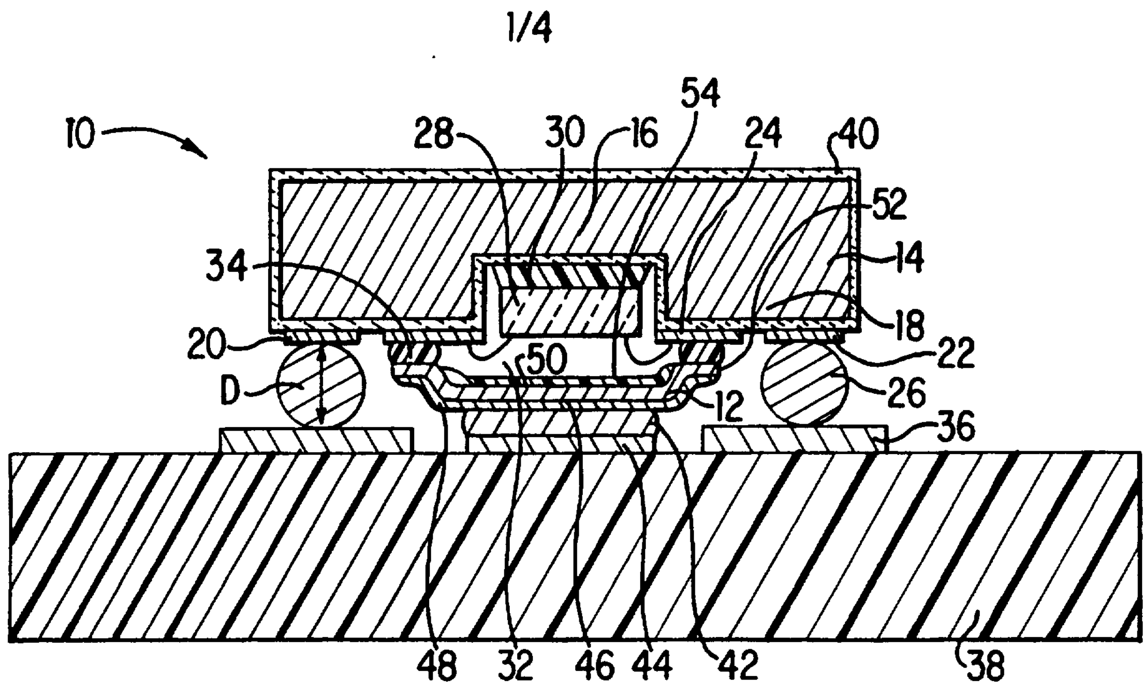

FIG. 1

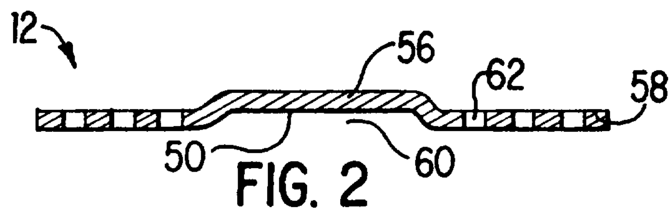

FIG. 2

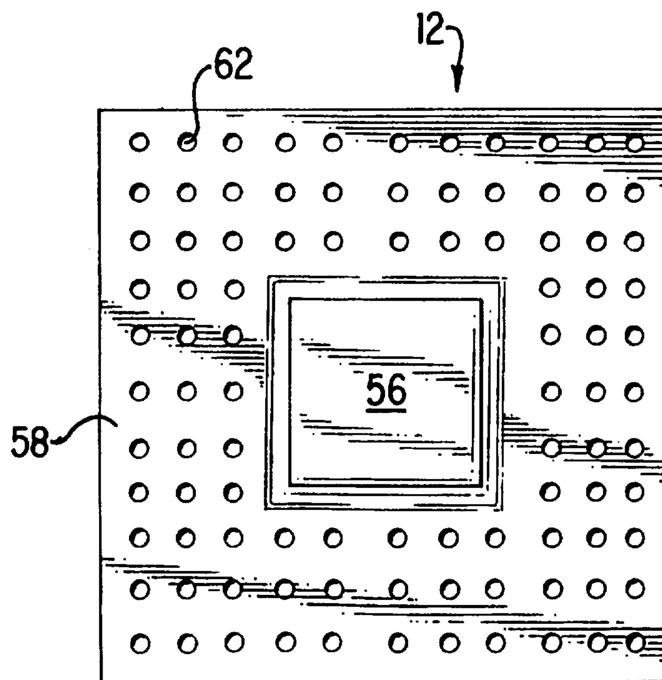

FIG. 3

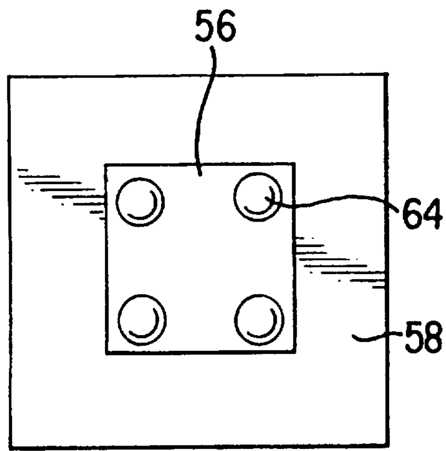

FIG. 4

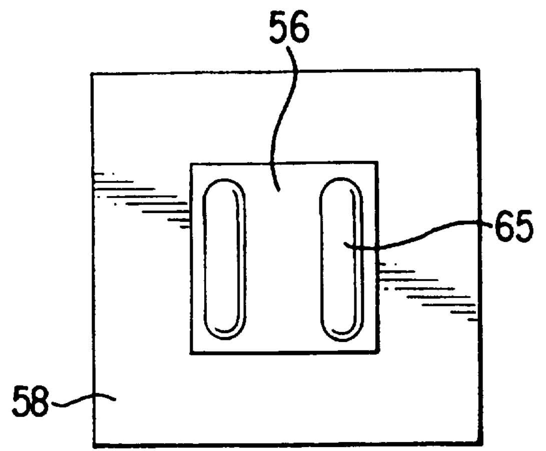

FIG. 5

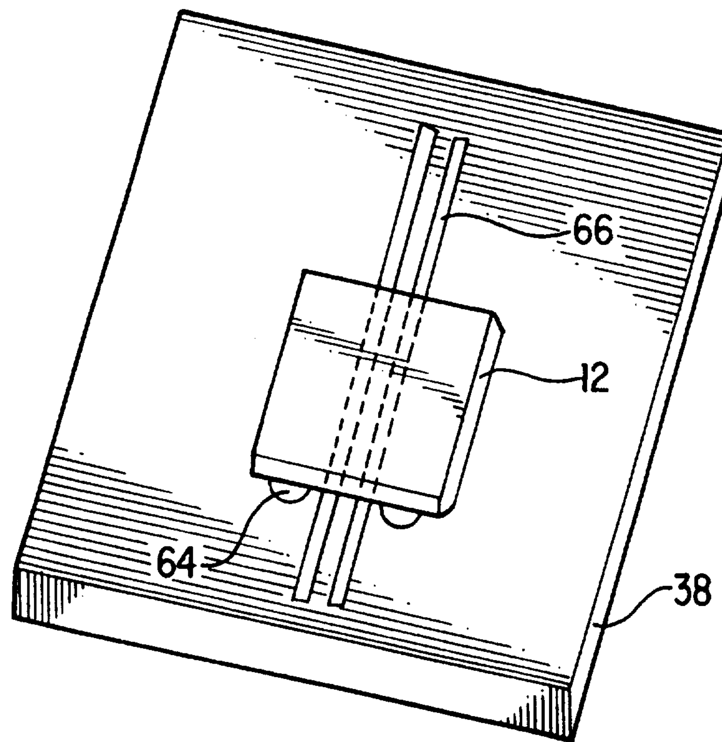

FIG. 6

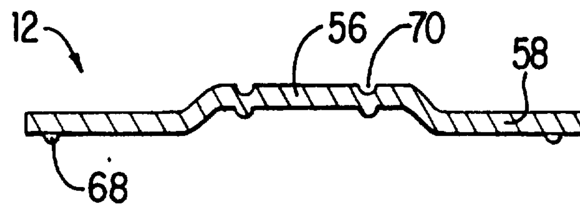

FIG. 7

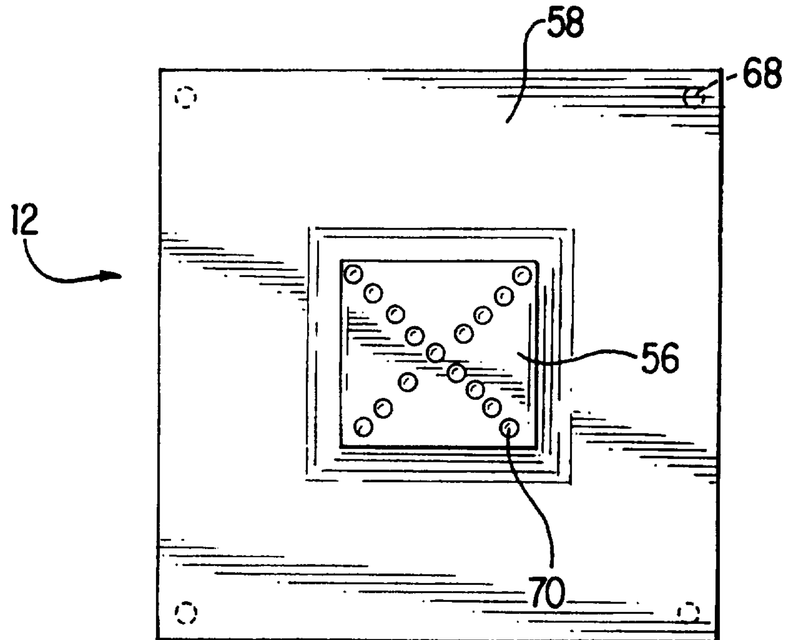

FIG. 8

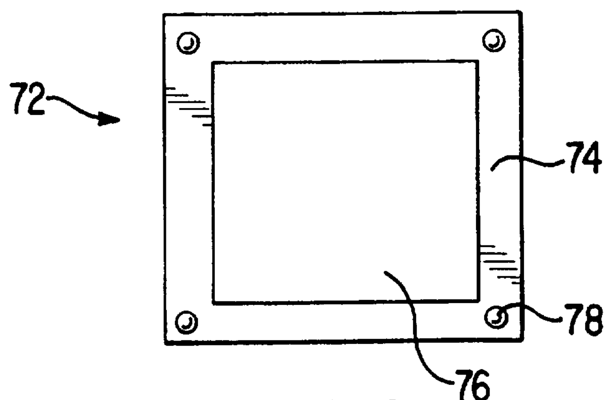

FIG. 9

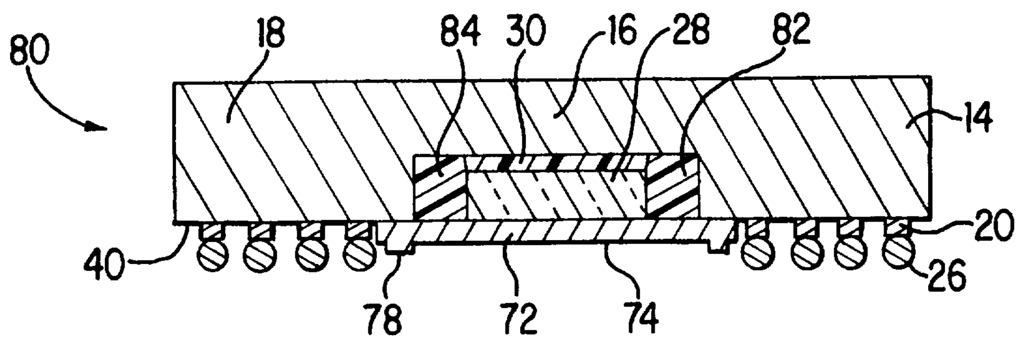

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/01873

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 23/12, 23/14, 23/48, 23/488
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/697, 704, 706, 737, 738, 778, 779, 780, 786; 437/183; 228/180.22; 174/52.4; 361/761, 762, 763, 764, 770, 820

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS
search terms: solder bump, solder ball, bump electrode, ball electrode, lid, cap, spacer, standoff

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,E	US 5,583,377 A (HIGGINS III) 10 December 1996 (10/12/96), see entire document, especially col. 4, line 8-col. 5, line 63	1, 3-5, 14
X,P	US 5,541,450 A (JONES et al) 30 July 1996 (30/07/96), see entire document, especially col. 3, lines 18-23, 31-52; col. 4, lines 20-40.	12, 14, 15, 16
X	US 5,045,921 A (LIN et al) 03 September 1991 (3/09/91), col. 6, lines 29-58.	1, 12, 14, 21
X	US 5,222,014 A (LIN) 22 June 1993, (22/06/93), col. 6, lines 13-21.	14
X	US 4,577,398 A (Sliwa et al) 25 March 1986 (25/03/86), Figs. 6 and 9; col. 3, lines 64-68.	12, 13

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 APRIL 1997	02 JUN 1997

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/01873

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,092,034 A (ALTENDORF et al) 03 March 1992 (03/03/92), Figs. 5 and 6	12
X	US 3,893,156 A (RISEMAN) 01 July 1975 (01/07/75), Fig. 2J.	8
X	US 5,394,009 A (LOO) 02 February 1995 (02/02/95), Figs. 3 and 4; col. 3, lines 28-31.	12, 13
X	US 5,102,829 A (COHN) 07 April 1992 (07/04/92), col. 2, lines 45-63; col. 4, lines 10-12, 55-57; col. 5, lines 2-11	1, 4
X	US 4,703,339 A (MATSUO) 27 October 1987 (27/10/87), Figs. 1 and 2; col. 2, lines 13-24.	14
X	US 4,731,644 A (NEIDIG) 15 March 1988 (15/03/88), Fig. 2.	7
X	US 5,083,191 (UEDA) 21 January 1992 (21/01/92), Figs. 8A,B.	7
X	US 5,446,316 A (TEMPLE et al) 29 August 1995 (29/08/95), Fig. 1; col. 2, lines 46-52.	1

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

257/697, 704, 706, 737, 738, 778, 779, 780, 786; 437/183; 228/180.22; 174/52.4; 361/761, 762, 763, 764, 770, 820