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(54) Title: CURRENT MODE BLIXER WITH NOISE CANCELLATION

FIG. 2

(57) Abstract: A blixer is provided that improves linearity and reduces noise over other conventional blixer designs. To accomplish this, the blixer provided here uses a differential amplifier and/or a dummy path within its mixing circuit to perform noise reduction (and improve linearity). In a described example, an apparatus includes a transconductance circuit (202) generates amplified signals from an input signal (VIN). A mixing circuit (204-1) mixes the amplified signals with a mixing signal (LOF1) having a duty cycle that is a fraction (generally 50% or 25%) of a local oscillator signal so that a differential amplifier (214) and impedance networks (e.g., resistors R7, R8 and switch S2, or resistors R9, RIO and switch SI) can perform noise reduction. The mixing is performed by mixers (210, 212) which are typically passive mixers (e.g., Gilbert cell passive mixers).

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CURRENT MODE BLIXER WITH NOISE CANCELLATION

[0001]   The invention relates generally to radio frequency (RF) circuitry and, more particularly, to a blixer.

BACKGROUND

[0002]   FIG. 1 illustrates an example of a conventional blixer 100. A blixer (i.e., 100) is a circuit that combines a balun, low-noise amplifier (LNA) and an I/Q mixer. As shown, blixer 100 generally comprises a balun-LNA core (which generally comprises NMOS transistors Q1 and Q2, inductor L, capacitor C1, and resistor R1) coupled to a switching quad or switching core (which generally comprises NMOS transistors Q3 through Q6 and resistor-capacitor (RC) networks 102-1 and 102-2). In operation, an RF input signal is provided to the balun-LNA core (which also receives bias voltages VBIAS1 and VBIAS2). Since transistors Q2 is n-times the size of transistor Q1, the transconductance g_{m2} of transistor Q2 is n-times the transconductance g_{m1} of transistor Q1 (or $g_{m2}=n*g_{m1}$). The signals from balun-LNA core (which are $g_{m1}*V_{IN}$ and $g_{m2}*V_{IN}$) are applied to low impedance nodes of the switching core so as to be mixed with a differential local oscillator signal LOP and LOM. In order to achieve the desired intermediate frequency signals IFP and IFM, transistors Q4 and Q5 are n-times the side of transistors Q3 and Q6. Additionally, each RC network 104-1 through 104-4 has an impedance Z_2 that is 1-nth the impedance Z_1 of each of RC networks 102-1 and 102-2 (or $Z_2=Z_1/n$). This blixer 100, however, can be noisy, and due to the stacking of the transistors Q1-Q6, the amount of head room available for signal swing can be severely limited, limiting achievable gain. Additionally, this headroom limitation due to the supply voltage also limits the linearity blixer 100. Thus, there is however a desire to improve the linearity and reduce the noise of this blixer 100.

[0003]   An example of a conventional blixer is described in Blaakmeer et al., "The BLIXER, a wideband balun-LNA-I/Q-mixer topology," IEEE J. Solid-State Circuits, vol. 43, No. 12, pp. 2706–2715, Dec. 2008.

SUMMARY

[0004] A disclosed embodiment of the present invention provides an apparatus. The apparatus comprises a transconductance circuit that receives an input signal and that generates a first amplified signal and a second amplified signal; and a mixing circuit having: a first mixer that is coupled to the transconductance circuit so as to receive the first amplified signal, wherein the first mixer mixes the first amplified signal with a mixing signal, wherein the mixing signal has a duty cycle that is a fraction of a local oscillator duty cycle; a second mixer that is coupled to the transconductance circuit so as to receive the second amplified signal, wherein the second mixer mixes the second amplified signal with the mixing signal; an first impedance network that is coupled each of the first and second mixers, wherein the first impedance network is adapted to have an feedback impedance; a second impedance network that is coupled each of the first and second mixers, wherein the second impedance network is adapted to have the feedback impedance; and a differential amplifier that is coupled to each impedance network.

[0005] In an embodiment, the mixing circuit further comprises a first capacitor that is coupled between the transconductance circuit and the first mixer; and a second capacitor that is coupled between the transconductance circuit and the second mixer.

[0006] In an embodiment, the first impedance network further comprises: a first resistor that is coupled to the first mixer; a second resistor that is coupled in series with the first resistor, wherein a collective impedance of the first and second resistors is approximately equal to the feedback impedance, and wherein the second mixer is coupled to a node between the first and second resistors; and a first switch that is coupled in parallel to the first resistor.

[0007] In an embodiment, the first impedance network further comprises: a third resistor that is coupled to the first mixer; a fourth resistor that is coupled in series with the third resistor, wherein a collective impedance of the third and fourth resistors is approximately equal to the feedback impedance, and wherein the second mixer is coupled to a node between the first and second resistors; and a second switch that is coupled in parallel to the first resistor.

[0008] In an embodiment, the first impedance network further comprises a first resistor having the feedback impedance and wherein the second impedance network further comprises a second resistor having the feedback impedance.

[0009] In an embodiment, the mixing circuit further comprises a dummy path that is coupled to second capacitor.

[0010]   In an embodiment, the differential amplifier further comprises a first differential amplifier, and wherein the dummy path further comprises: a third mixer that is coupled to the second capacitor; and a second differential amplifier that is coupled to the third mixer.

[0011]   In an embodiment, the fraction further comprises a first fraction, and wherein the mixing signal further comprises a first mixing signal, and wherein the third mixer mixes the second amplified signal with a second mixing signal having a duty cycle that is a second fraction of the local oscillator duty cycle.

[0012]   In an embodiment, the transistors from each of first and second mixers have a first size, and wherein the transistors from the third mixer have a second size.

[0013]   In an embodiment, an apparatus comprises: a transconductance circuit that generates a first amplified signal and a second amplified signal, wherein the transconductance circuit includes: a first current source having a first current; a second current source having a second current, wherein the second current is K-times larger than the first current; a first transistor that is coupled to the first current source and that receives a first bias voltage; a second transistor that is coupled to the first transistor and that receives an input signal and a second bias voltage; a third transistor that is coupled to the second current source and that receives first bias voltage; and a fourth transistor that is coupled to the third transistor and that receives the input signal and the second bias voltage; and a mixing circuit having: a first mixer that is coupled to the transconductance circuit so as to receive the first amplified signal, wherein the first mixer mixes the first amplified signal with a mixing signal, wherein the mixing signal has a duty cycle that is a fraction of a local oscillator duty cycle; a second mixer that is coupled to the transconductance circuit so as to receive the second amplified signal, wherein the second mixer mixes the second amplified signal with the mixing signal; an first impedance network that is coupled each of the first and second mixers, wherein the first impedance network is adapted to have an feedback impedance; a second impedance network that is coupled each of the first and second mixers, wherein the second impedance network is adapted to have the feedback impedance; and a differential amplifier that is coupled to each impedance network.

[0014]   In an embodiment, the transconductance circuit further comprises: a resistor that is coupled to the fourth transistor and that receives the second bias voltage; and a capacitor that is coupled to the fourth transistor and that receives the input signal.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0015]   Example embodiments are described with reference to accompanying drawings, in which:

[0016]   FIG. 1 is a circuit diagram of a conventional blixer; and

[0017]   FIGS. 2 through 4 are circuit diagrams of examples of blixers In an embodiment.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0018]   FIG. 2 illustrates an example blixer 200-1 implementing principles of the invention. Blixer 200-1 generally comprises a transconductance circuit 202 and a mixing circuit 204-1. In operation, the tranconductance circuit 202 generally receives the input signal VIN and generates amplified signals from the input signal VIN. Mixing circuit 204-1 then can mix these amplified signals with a mixing signal LOF1 having a duty cycle that is a fraction (generally 50% or 25%) of a local oscillator signal so that differential amplifier 214 and impedance networks (generally resistors R7 and R8 and switch S2 or resistors R9 and R10 and switch S1) can generally perform noise cancellation or noise reduction. The mixing is generally performed by mixers 210 and 212, which are typically passive mixers (which can, for example, be Gilbert cell mixers).

[0019]   To generate the amplified signal, the transconductance circuit 202 generally uses two branches that each generate one of the amplified signals. The input signal VIN is generally received at the source of NMOS transistor Q9 (which can biased by bias voltage VBIAS3 and generally has a transconductance g_{m3}), and, in combination with current source 206 (which can generate a current I0) and NMOS transistor Q7 (which can bias by bias voltage VBIAS4), transistor Q9 generates an amplified signal (which is generally VIN* g_{m3}). Additionally, NMOS transistor Q10 generally receives the input voltage VIN through capacitor C6 (which is also biased by bias voltage VBIAS3 through resistor R6). This transistor Q10 generally has a transconductance of K* g_{m3} and, in combination with transistor Q8 (which is generally biased by bias voltage VBIAS4) and current source 208 (which generates a current of K*I0), generates an amplified signal (which is generally VIN*K*g_{m3}). These amplified signals can then be provided to AC-coupling capacitors C7 and C8.

[0020]   To provide noise cancellation, switches S1 and S2 can be actuated to vary the impedance of the impedance networks. Typically, resistor R8 and R10 have resistances of K*RL, and resistors R7 and R9 typically have resistances of (K-1)RL/K. When the switches S1

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and S2 are actuated, the total resistance (or impedance for the circuit shown) for each impedance network is RL. Thus, when switches S1 and S2 are actuated, the differential amplifier 214 is used to perform noise reduction using the total impedance of the impedance network, whereas in normal operation (when switches S1 and S2 are open), a resistance of K*RL is used.

[0021]   FIG. 3 illustrates another example blixer 200-2. In this configuration the impedance networks of blixer 200-1 have been replaced by resistors R11 and R12 (which generally have a resistance of RL) and a dummy path 216-1 has been included. The dummy path 216-1 generally comprises a mixer 220-1 (which is typically a passive mixer having transistors that are about the same size or aspect ratio (channel width to channel length) as the transistors used for mixers 210 and 220), differential amplifier 218, and resistors R13 and R14 (which each typically have a resistance of RL). Typically, mixer 220-1 mixes an amplified output signal from capacitor C7 with a mixing signal LOF2 having a duty cycle that is a fraction or multiple (i.e., K-2 times) the local oscillator duty cycle. This dummy path 216-1 generally "siphons" the extra signal current from the main path. Additionally, the dummy path 216-1 can be used for RF filtering by appropriately sizing the filter around amplifier 218.

[0022]   In another alternative, shown in FIG. 4, blixer 200-3 generally uses a dummy path 216-2 instead of dummy path 216-1. A difference between dummy paths 216-1 and 216-2 lies in difference between mixers 220-1 and 220-2. Namely, mixer 220-2 uses mixing signal LOF1, but the transistors used within mixer 220-2 are K-1 times the size of the transistors used for mixers 210 and 212. This arrangement for blixer 200-3 generally provides substantially similar functionality to the arrangement for blixer 200-2 but may provide an advantageous layout.

[0023]   As a result of using the blixer 200-1, 200-2, or 200-3, several advantages can be realized. Namely, the linearity is improved over blixer 100 due to the low signal swing at the output of transconductance circuit 202. There is also a much larger intermediate frequency gain due to the available signal swing. Additionally, there is generally little to no flicker noise because of the passive nature of the mixing circuits 204-1, 204-2, and 204-3. To demonstrate the improved performance, Table 1 is provided below, which compares blixer 100 to blixer 200-1, 200-2, and 200-3.

Table 1

	Blixer 100	Blixer 200-1, 200-2, or 200-3
Noise	4.3dB	2.1dB
IP$_3$	+10dBm	+14.5dBm
Signal swing after mixer	+15dB (voltage output)	+5dB (current output)
DC current	3+12+16mA	2+8mA

[0024]   Those skilled in the art to which this relates will appreciate that modifications may be made to the described example embodiments, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS

1.   An apparatus comprising:

a transconductance circuit that receives an input signal and that generates a first amplified signal and a second amplified signal; and

a mixing circuit having:

a first mixer that is coupled to the transconductance circuit so as to receive the first amplified signal, wherein the first mixer mixes the first amplified signal with a mixing signal, wherein the mixing signal has a duty cycle that is a fraction of a local oscillator duty cycle;

a second mixer that is coupled to the transconductance circuit so as to receive the second amplified signal, wherein the second mixer mixes the second amplified signal with the mixing signal;

a first impedance network that is coupled each of the first and second mixers, wherein the first impedance network is adapted to have an feedback impedance;

a second impedance network that is coupled each of the first and second mixers, wherein the second impedance network is adapted to have the feedback impedance; and

a differential amplifier that is coupled to each impedance network.

2.   The apparatus of Claim 1, wherein the mixing circuit further comprises   a   first capacitor that is coupled between the transconductance circuit and the first mixer; and   a second capacitor that is coupled between the transconductance circuit and the second mixer.

3.   The apparatus of Claim 2, wherein the first impedance network further comprises a first resistor that is coupled to the first mixer; a second resistor that is coupled in series with the first resistor, wherein a collective impedance of the first and second resistors is approximately equal to the feedback impedance, and wherein the second mixer is coupled to a node between the first and second resistors; and a first switch that is coupled in parallel to the first resistor.

4.   The apparatus of Claim 3, wherein the first impedance network further comprises a third resistor that is coupled to the first mixer; a fourth resistor that is coupled in series with the third resistor, wherein a collective impedance of the third and fourth resistors is approximately

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equal to the feedback impedance, and wherein the second mixer is coupled to a node between the first and second resistors; and a second switch that is coupled in parallel to the first resistor.

5.   The apparatus of Claim 2, wherein the first impedance network further comprises a first resistor having the feedback impedance and wherein the second impedance network further comprises a second resistor having the feedback impedance.

6.   The apparatus of Claim 5, wherein the mixing circuit further comprises a dummy path that is coupled to second capacitor.

7.   The apparatus of Claim 5, wherein the differential amplifier further comprises a first differential amplifier, and wherein the dummy path further comprises a third mixer that is coupled to the second capacitor; and a second differential amplifier that is coupled to the third mixer.

8.   The apparatus of Claim 7, wherein the fraction further comprises a first fraction, and wherein the mixing signal further comprises a first mixing signal, and wherein the third mixer mixes the second amplified signal with a second mixing signal having a duty cycle that is a second fraction of the local oscillator duty cycle.

9.   The apparatus of Claim 7, wherein the transistors from each of first and second mixers have a first size, and wherein the transistors from the third mixer have a second size.

10.   The apparatus of Claim 1, wherein the transconductance circuit includes:
        a first current source having a first current;
        a second current source having a second current, wherein the second current is K- times larger than the first current;
        a first transistor that is coupled to the first current source and that receives a first bias voltage;
        a second transistor that is coupled to the first transistor and that receives an input signal and a second bias voltage;

a third transistor that is coupled to the second current source and that receives first bias voltage; and

a fourth transistor that is coupled to the third transistor and that receives the input signal and the second bias voltage.

11. The apparatus of Claim 10, wherein the transconductance circuit further comprises a resistor that is coupled to the fourth transistor and that receives the second bias voltage; and a capacitor that is coupled to the fourth transistor and that receives the input signal.

12. The apparatus of Claim 10, wherein the mixing circuit further comprises a first capacitor that is coupled between the transconductance circuit and the first mixer; and a second capacitor that is coupled between the transconductance circuit and the second mixer.

13. The apparatus of Claim 12, wherein the first impedance network further comprises:

a first resistor that is coupled to the first mixer;

a second resistor that is coupled in series with the first resistor, wherein a collective impedance of the first and second resistors is approximately equal to the feedback impedance, and wherein the second mixer is coupled to a node between the first and second resistors; and

a first switch that is coupled in parallel to the first resistor.

14. The apparatus of Claim 13, wherein the first impedance network further comprises:
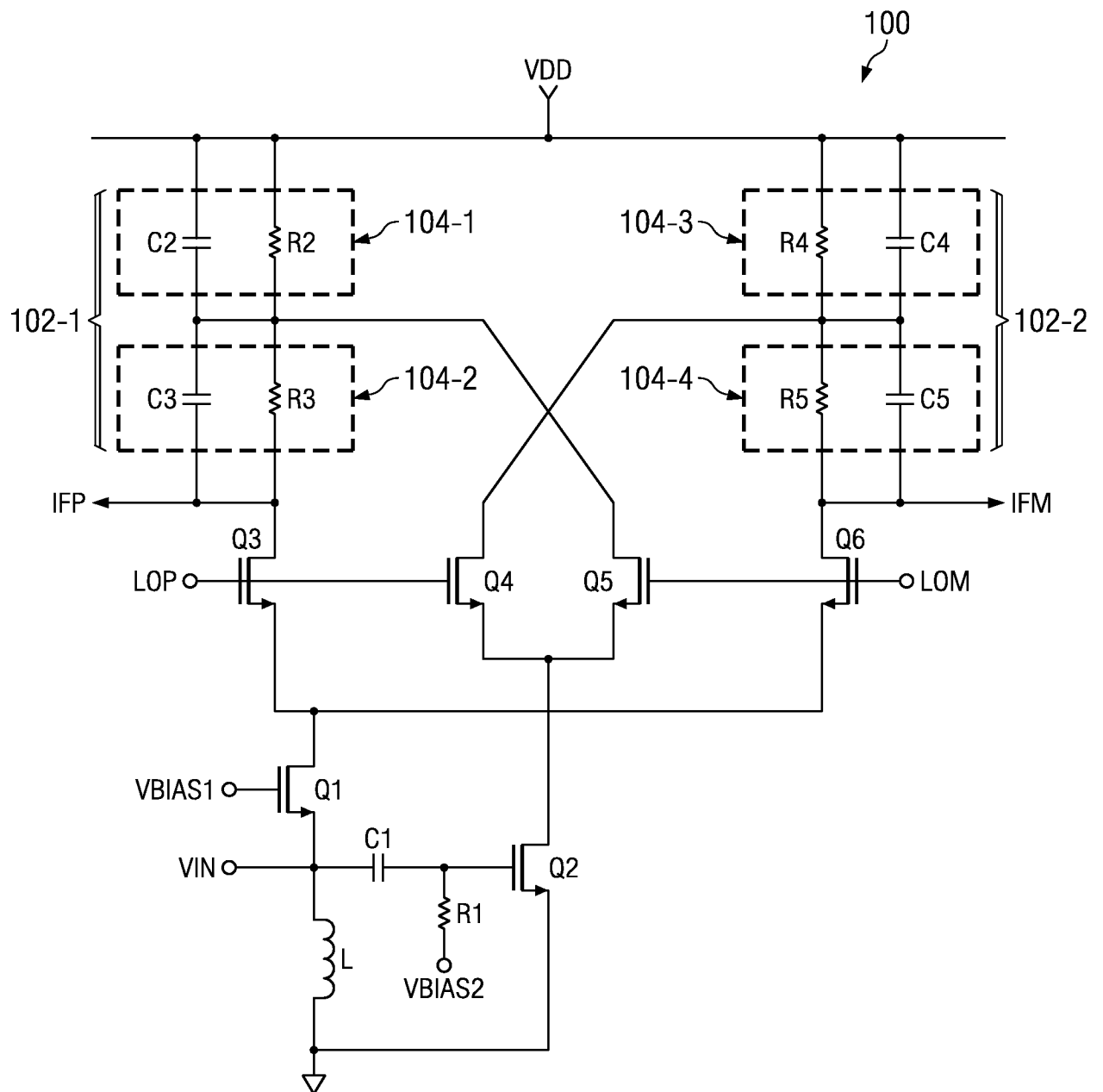
a third resistor that is coupled to the first mixer;

a fourth resistor that is coupled in series with the third resistor, wherein a collective impedance of the third and fourth resistors is approximately equal to the feedback impedance, and wherein the second mixer is coupled to a node between the first and second resistors; and
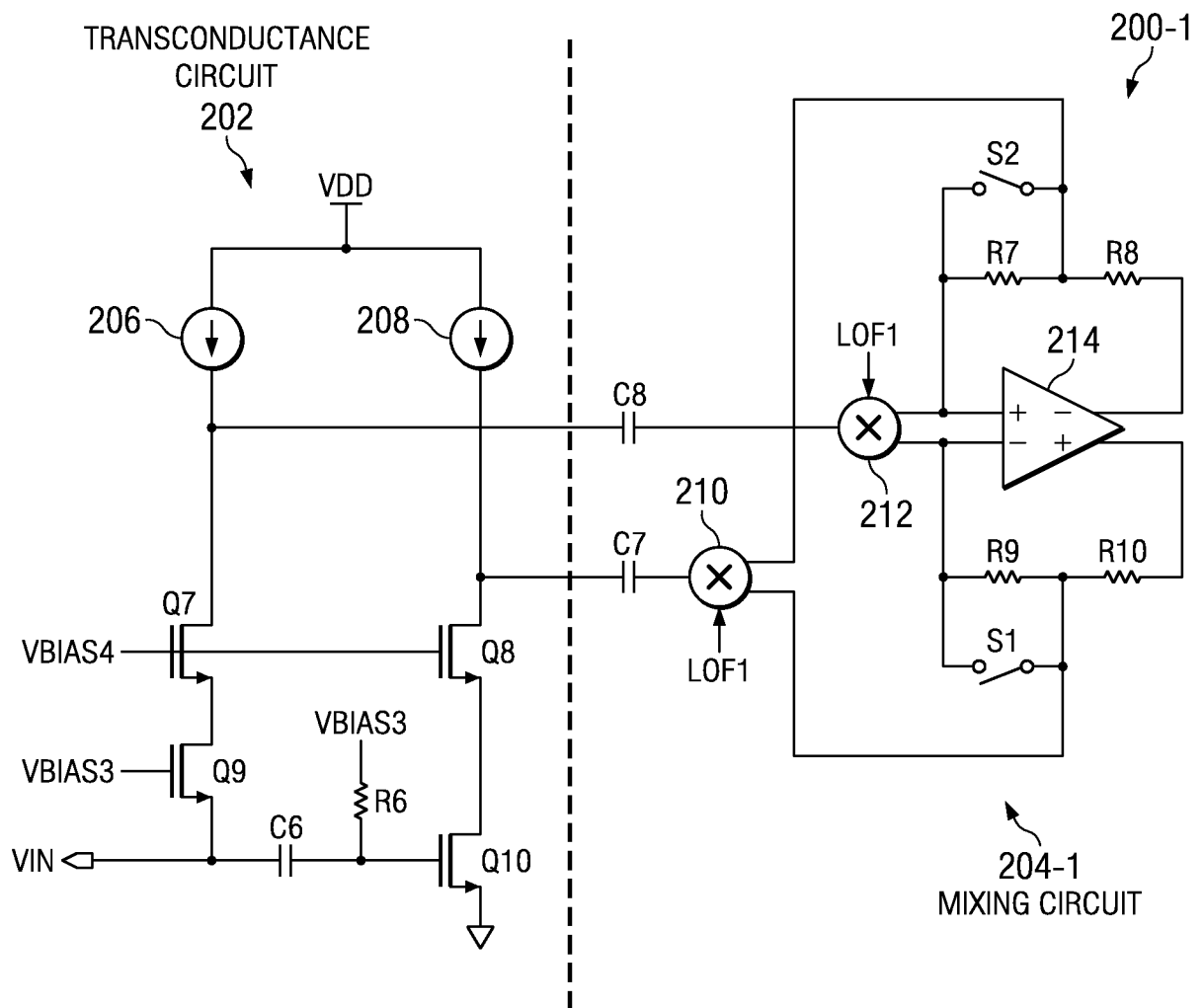
a second switch that is coupled in parallel to the first resistor.

15. The apparatus of Claim 12, wherein the first impedance network further comprises a first resistor having the feedback impedance and wherein the second impedance network further comprises a second resistor having the feedback impedance.

16. The apparatus of Claim 15, wherein the mixing circuit further comprises a dummy path that is coupled to second capacitor.
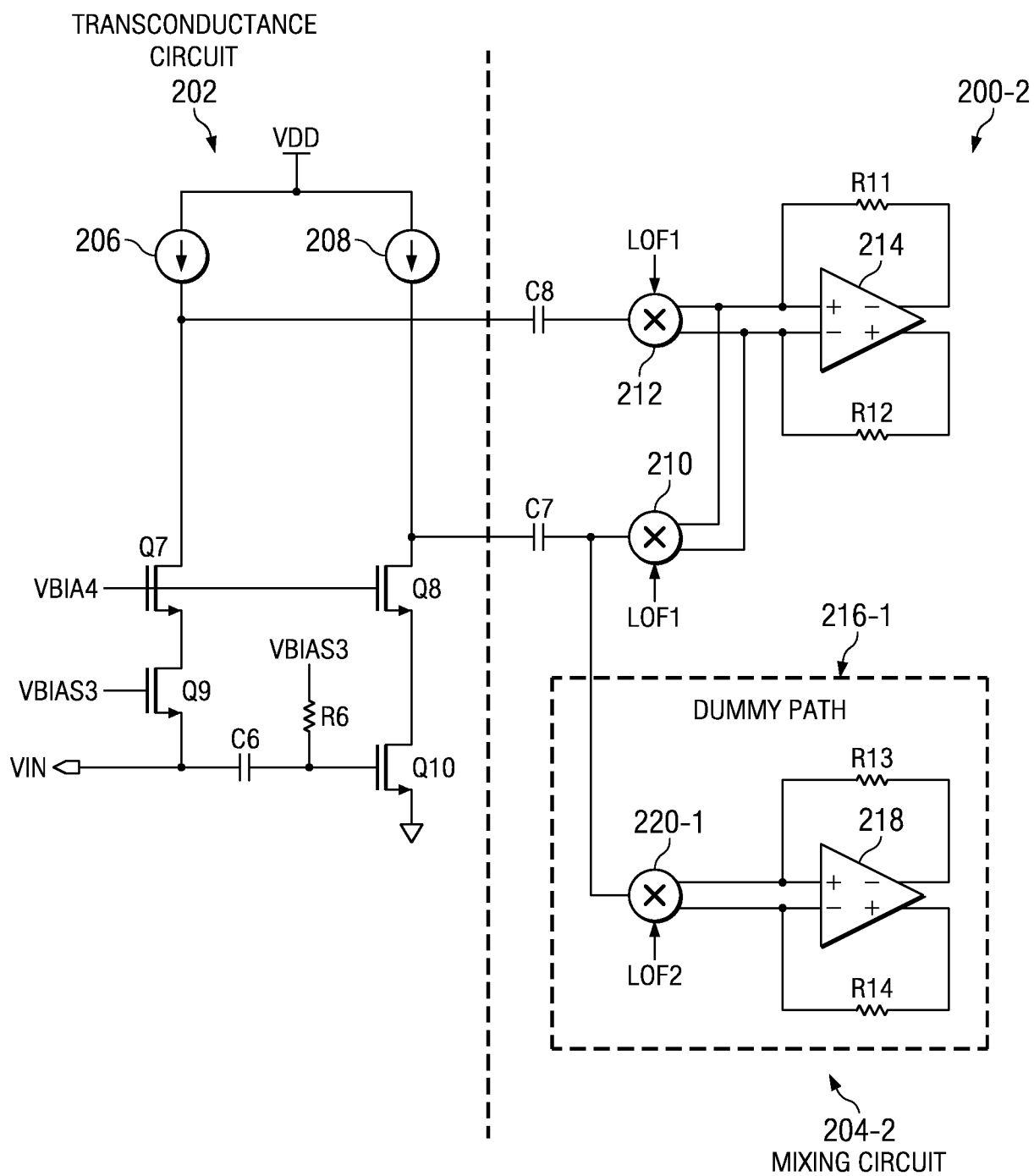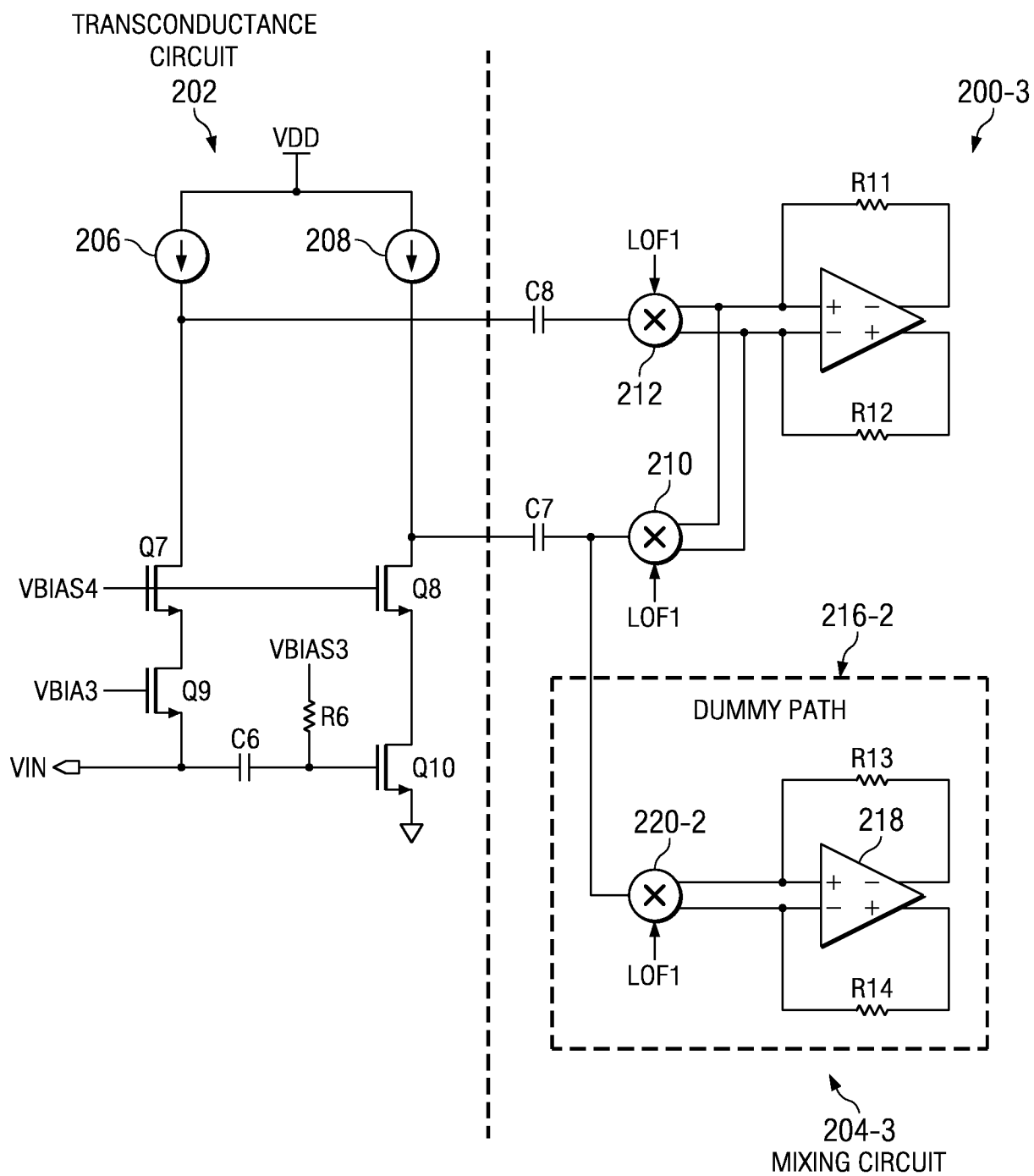
FIG. 1
(PRIOR ART)

FIG. 2

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FIG. 3

FIG. 4