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Plummer

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[54] **MONOLITHIC SEMICONDUCTOR SWITCHING DEVICE**

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[73] Assignee: **Board of Trustees of the Leland Stanford Jr. Univ.**, Stanford, Ill.

[21] Appl. No.: **539,111**

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Related U.S. Patent Documents

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Appl. No.: **943,200**
Filed: **Sep. 18, 1978**

[51] **Int. Cl.**[5] **H01L 29/78**

[52] **U.S. Cl.** **357/23.4**; 357/23.9; 357/39; 357/48; 357/55; 357/41

[58] **Field of Search** 357/23.4, 23.9, 55, 357/48, 41, 39

[56] **References Cited**

U.S. PATENT DOCUMENTS

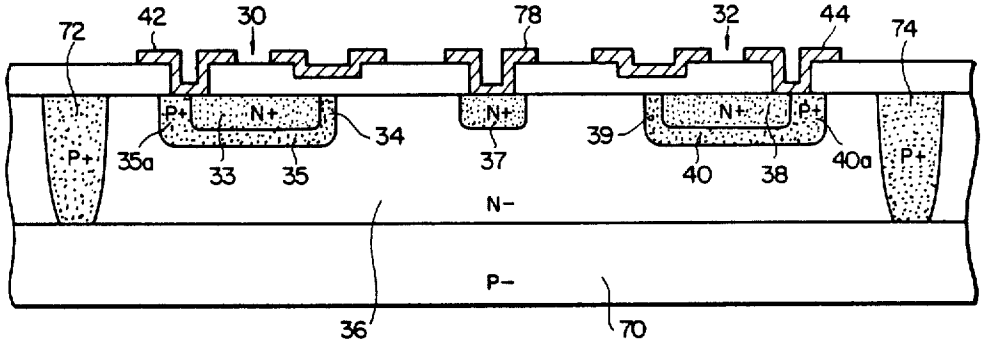
3,845,495	10/1974	Cauge	357/23.4
3,909,320	9/1975	Cauge	357/23.4 X
3,926,694	12/1975	Cauge	340/173 R
3,974,486	8/1976	Curtis	340/173 R
3,996,655	12/1976	Cunningham	29/571
4,072,975	2/1978	Ishitami	357/23.4
4,119,996	10/1978	Jhabrola	357/23
4,145,703	3/1979	Blanchard	357/23.4 X

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Flehr, Hohbach, Test, Albritton & Herbert

[57] **ABSTRACT**

An electrical circuit device made in integrated monolithic form has low level operating characteristics of a MOS device and high level operating characteristics of a Triac. The structure includes two double diffused MOS transistors which have merged drain regions. At higher voltage and current levels a lateral Triac structure is triggered by the MOS devices. Alternatively, separate terminal contacts can be made to the P and N regions comprising the MOS transistor source and channel regions with the Triac triggered conventionally by an externally applied control voltage.

20 Claims, 4 Drawing Sheets



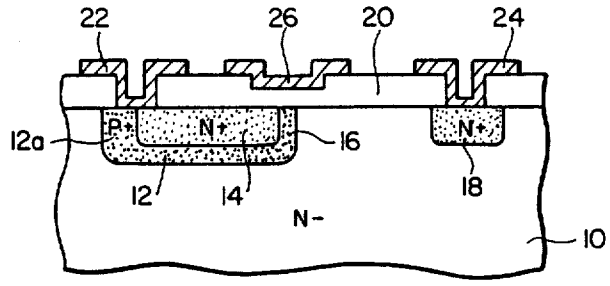


FIG__1

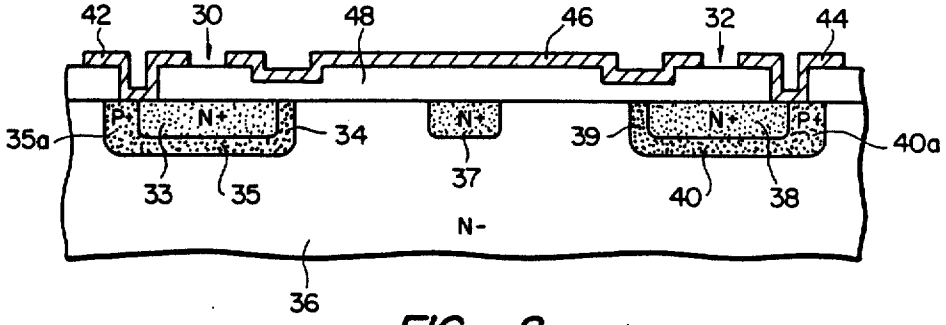


FIG__2

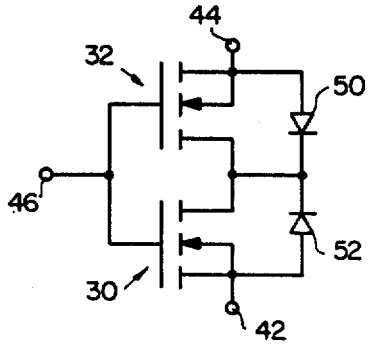


FIG__3A

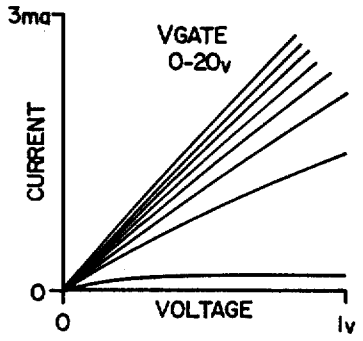


FIG__3B

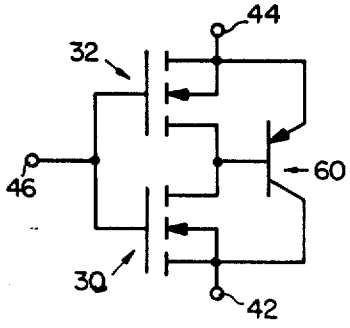


FIG__4A

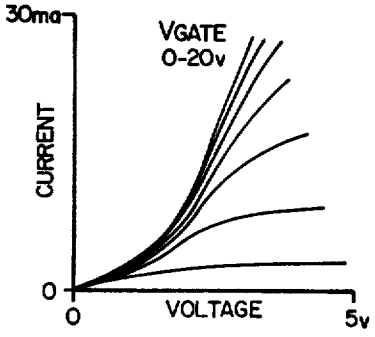


FIG__4B

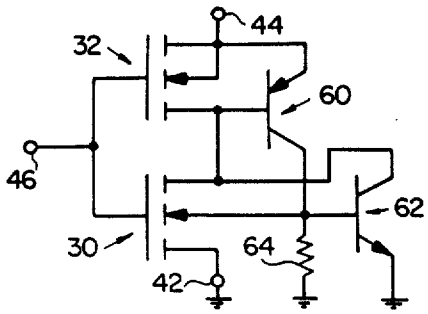


FIG_5A

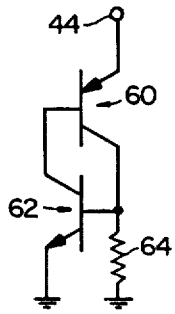


FIG_5B

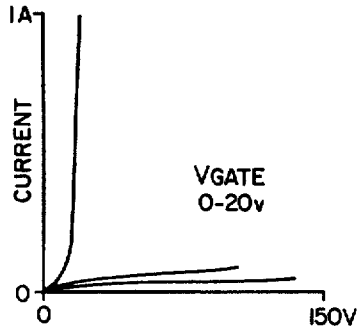


FIG_5C

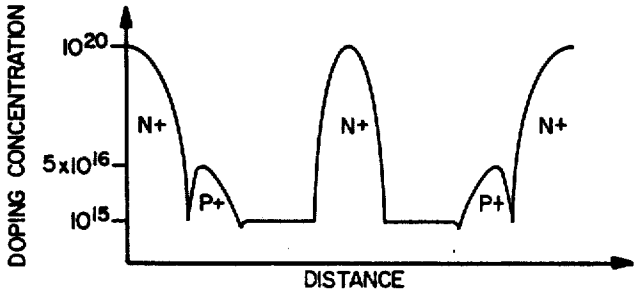


FIG_6

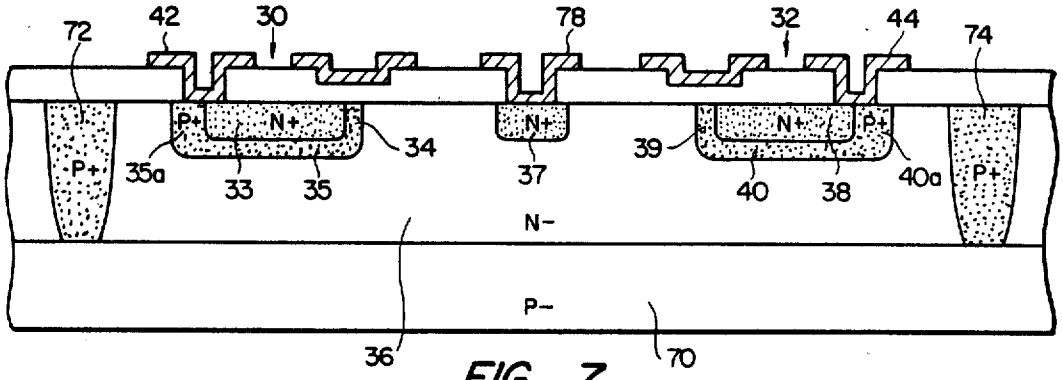


FIG_7

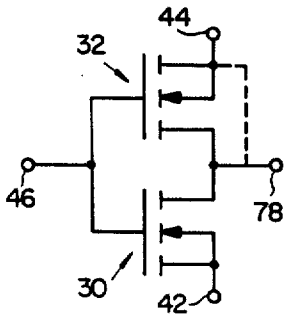


FIG_8A

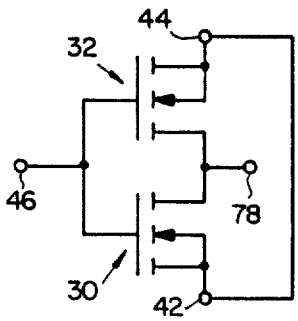


FIG_8B

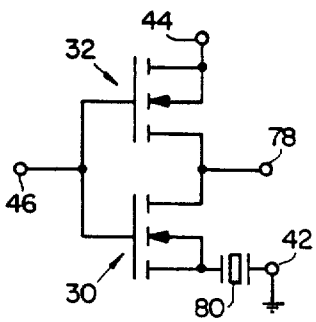


FIG_8C

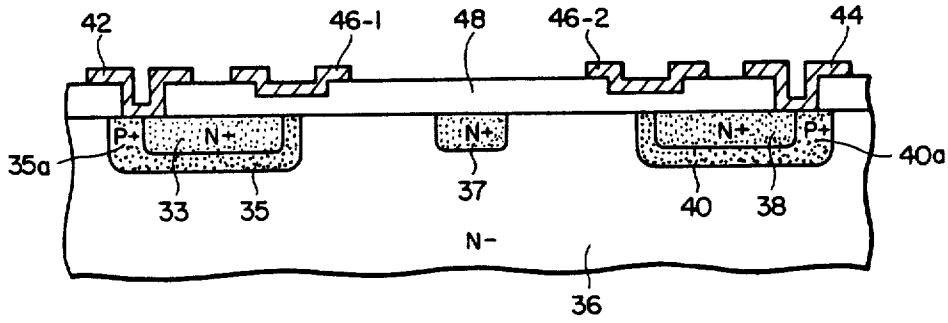


FIG__9

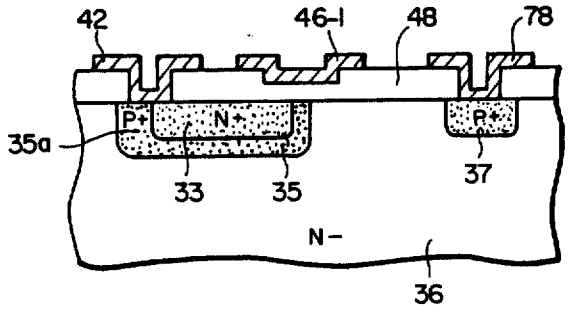


FIG__10

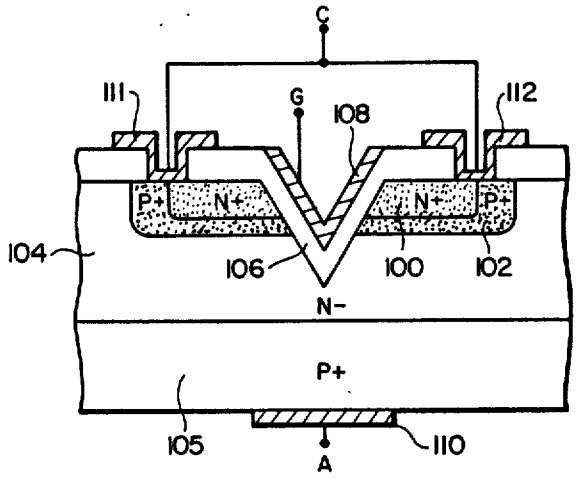


FIG__11

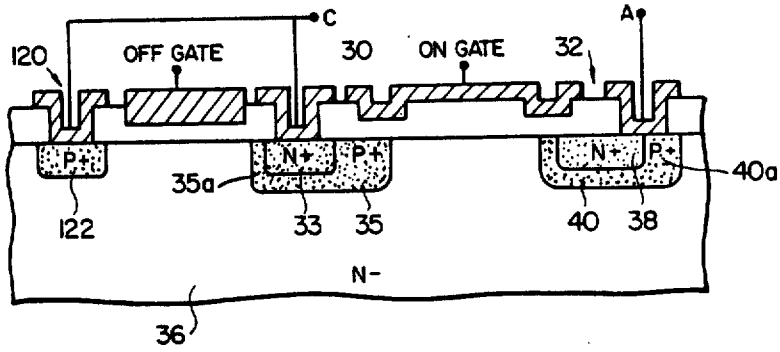


FIG_12

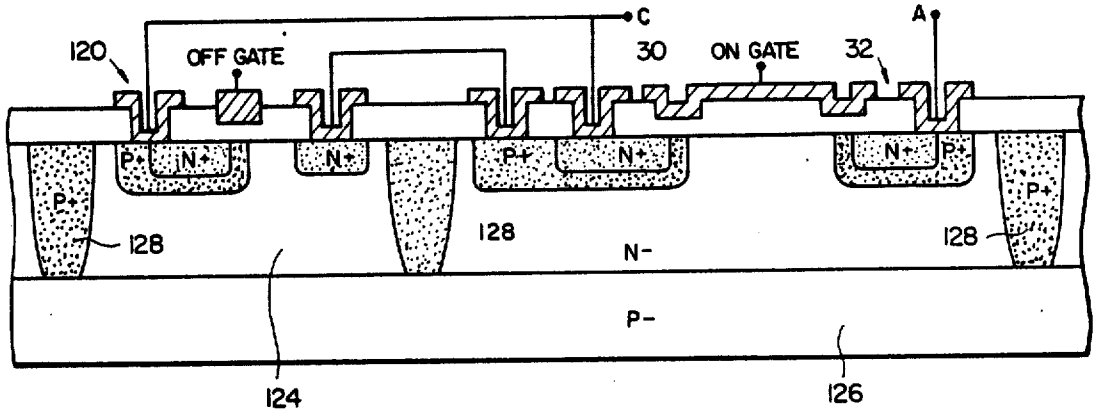


FIG_13

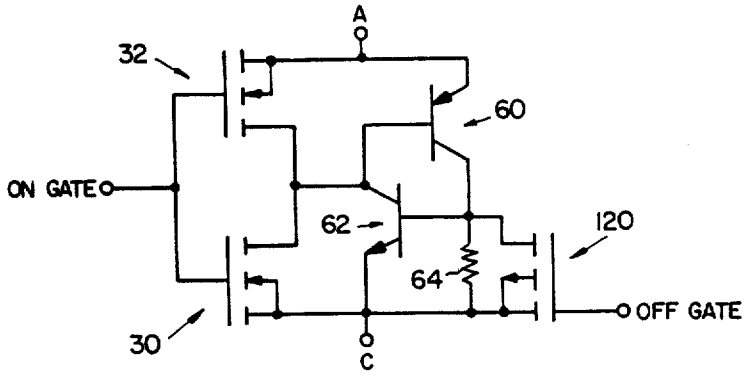


FIG_14

MONOLITHIC SEMICONDUCTOR SWITCHING DEVICE

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

BACKGROUND OF THE INVENTION

This invention relates generally to semiconductor circuits and devices, and more particularly the invention relates to an integrated circuit device having current dependent properties.

The metal oxide silicon (MOS) field effect transistor and the multijunction silicon controlled rectifier and Triac are known semiconductor devices which have current switching applications. The MOS transistor generally operates at lower voltages and current levels and can be used in linear applications. One form of MOS transistor is the double diffused device in which a very short channel region is defined by diffusing a region of one conductivity type in a substrate of opposite conductivity type and then diffusing a region of opposite conductivity type in the first region. The silicon controlled rectifier (SCR) or Triac is normally employed for higher voltage and current switching applications. The MOS transistor employs a field effect channel created by the application of a gate voltage, while the SCR typically is turned on by forward biasing a PN junction which renders the device conductive. The Triac is similar to the SCR but provides full wave switching.

SUMMARY OF THE INVENTION

An object of this invention is a new and improved current switching device.

Another object of the invention is an electrical circuit device which has the characteristics of an MOS transistor and of a full wave silicon switch.

Still another object of the invention is a monolithic semiconductor device having operational characteristics which are current dependent.

A feature of the invention is a monolithic semiconductor device including two merged double diffused MOS transistors.

Briefly, a device in accordance with the invention comprises a semiconductor body having at least one major surface and a region adjacent to the surface of one conductivity. First and second spaced regions of opposite conductivity type are formed in the body region and abutting the major surface. Third and fourth regions of the one conductivity type are formed in the first and second regions, respectively, abutting the major surface and defining first and second channel regions in the first and second regions, respectively. A layer of insulation is formed on the major surface and an ohmic contact is formed on the layer of insulation and adjacent to the first and second gate regions. An ohmic contact is made to the first and third regions, and an ohmic contact is made to the second and fourth regions. An ohmic contact between the first and third regions and between the second and fourth regions may be facilitated by a separate diffusion of the same conductivity type as regions one and two adjacent to regions one and two. This diffusion is normally performed prior to diffusion of regions one and two, with a separate masking operation.

The first and third regions cooperatively function with the body region as a first double diffused MOS transistor, and the second and fourth regions cooperatively function with the body region as a second double diffused MOS transistor. The body region functions as a merged drain of the two transistors. A fifth diffused region of the same conductivity type as the body region can be formed in the body region between the first and second diffused regions.

At lower operating voltages and currents, the device functions as serially connected MOS transistors having merged drain regions, while at higher voltages and operating currents the device functions as a full wave silicon switch.

The invention and objects and features thereof will be more readily apparent from the following detailed description and appended claims when taken with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross section view of a conventional double diffused MOS transistor.

FIG. **2** is a cross section view of one embodiment of a switching device in accordance with the present invention.

FIG. **3A** and FIG. **3B** are an electrical schematic and voltage-current characteristics, respectively, of the device of FIG. **2** at lower operating voltages.

FIGS. **4A** and **4B** are an electrical schematic and voltage-current characteristics, respectively, of the device of FIG. **2** operated at higher voltage level.

FIG. **5A** [and], FIG. **5B**, *and FIG. 5C* are an electrical schematic and voltage-current characteristics, respectively, of the device of FIG. **2** operated at still higher voltages.

FIG. **6** is the doping profile along the silicon surface of one embodiment of the device of FIG. **2**.

FIG. **7** is a cross section view of another embodiment of a switch device in accordance with the present invention.

FIGS. **8A**, **8B**, **8C** illustrate schematically several applications of the device of FIG. **7**.

FIGS. **9–13** are cross section views of other embodiments of devices in accordance with the invention.

FIG. **14** is an electrical schematic of the device shown in FIGS. **12** and **13**.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

Referring now to the drawings, FIG. **1** is a cross section view of a conventional double diffused MOS transistor (DMOS) formed in a lightly doped (N−) semiconductor body **10**. The device includes a first P+ diffused region **12a**, a second P diffused region **12** overlapping a portion of region **12a**, a third N+ diffused region **14** formed in the P region **12** with all three regions being adjacent to a major surface of the semiconductor body **10**. The N+ region **14** comprises the source of the transistor, and the portion **16** of P region **12** adjacent to the major surface and between the N+ region **14** and the N− body **10** comprises the transistor channel. An N+ diffused region **18** spaced from the first two regions along with the adjacent N− body region comprises the transistor drain. A silicon oxide layer **20** is formed on the major surface of the semiconductor body **10** with a metallic ohmic contact **22** made

to regions **12**, **12a** and **14**, a metallic ohmic contact **24** made to the drain region **18**, and a metallic layer for the gate electrode **26** formed on the layer of insulation **20** above the channel region **16**.

The device functions as a typical MOS transistor with a short channel region provided by the double diffused structure. However, due to the PN junction between region **12** and the body **10**, the DMOS device is inherently asymmetrical; that is, the source and drain terminals are not interchangeable. This asymmetry can be a problem in many circuit applications, and a device in accordance with the present invention overcomes this limitation.

Referring now to FIG. **2**, one embodiment of a device in accordance with the present invention is illustrated in cross section. The device is effectively two DMOS devices shown generally at **30** and **32** integrated in a monolithic semiconductor body **36** with merged drain regions. The DMOS transistor **30** comprises a source N+ region **33**, a channel region **34** formed in P region **35** and a drain comprising the N− semiconductor body **36** and the N+ diffused region **37**. DMOS transistor **32** comprises an N+ source **38**, a P channel region **39** formed in P region **40**, and a drain comprising the N− body **36** and the N+ diffused region **37**. Regions **35a** and **40a** again are P+ diffused regions designed to facilitate ohmic contact to the P channel regions **35** and **40**. One input-output (I/O) contact **42** is made to regions **33**, **35** and **35a**, a second I/O contact **44** is made to regions **38**, **40** and **40a**, and a gate electrode **46** is formed on the silicon oxide layer **48** above the channel regions **34**, **39**.

Due to the symmetrical construction of the device as shown in FIG. **2**, the device has symmetry of operation, i.e. the two I/O contacts are interchangeable. Importantly, the operational characteristics of this device change with the operating voltage and current levels.

FIG. **3A** is an electrical schematic of the device in FIG. **2** operated at low voltage and current levels (e.g. less than one volt across the device, gate voltage of a few volts above the threshold voltage), and FIG. **3B** is the current-voltage operating characteristics of the device of FIG. **3A**. In FIG. **3A** the two DMOS transistors **30** and **32** are shown serially connected with the I/O terminals **42**, **44** connected to the source regions of transistors **30** and **32**, respectively, and gate terminal **46** controlling the gates of both transistors. Diode **52** formed by P region **35** and the N− body **36** is connected in parallel with transistor **30**, and diode **50** formed by P region **40** and the N− body **36** is connected in parallel with transistor **32**. Thus, since the two diodes are provided in series opposition, the device in accordance with the present invention is symmetrical at lower voltage and current operation. FIG. **3B** is a plot of current vs. voltage for low-level operation wherein the device function in accordance with the circuit illustrated in FIG. **3A**.

For applied voltages greater than approximately 1.5 volts (gate voltage of a few volts above the threshold voltage), holes are injected into semiconductor body **36** by the plus voltage on P regions **40** and **40a**, with P regions **40** and **40a** and **35** and **35a** functioning with the N− semiconductor body **36** as a PNP transistor **60** connected as shown in FIG. **4A**. Referring to the plot of voltage vs. current in FIG. **4B**, the transconductance or gain of the device shows a sharp increase. However, the device remains symmetrical. The increase in transconductance or device gain can be attributed to the injected holes from regions **40** and **40a** which pass through body **36** and are collected at regions **35** and **35a**. These collected holes contribute to the total device current (which is measured externally) and thus increase the transconductance or device gain. Some of the injected holes recombine with majority carriers in the N− region while the remaining injected holes are collected at regions **35** and **35a**. Thus, applied voltages greater than approximately 1.5 volts cause the lateral PNP transistor to turn on. The current contributed by this device explains the increase in overall device gain as demonstrated by the plot in FIG. **4B**. In this mode of operation two parallel conduction paths are provided in the device, electron flow through the surface DMOS devices and hole current through the lateral PNP transistor. The overall device current is the sum of the DMOS electron current and the injected hole current.

By increasing current flow through the device by increasing gate voltage, for example, an applied voltage of +2 volts on one I/O terminal and a +10 volt gate potential, the device assumes an electrical and equivalent electrical schematic as demonstrated in FIGS. **5A** and **5B**, with the other I/O terminal grounded. In this mode of operation the device assumes the characteristics of a Triac with switching action to a low resistance device, similar to that observed in PNPN four layer structures. The structure shown in FIG. **2** can be viewed as a lateral NPNPN structure, or a symmetrical PNPN arrangement, between the two I/O terminals. As illustrated in FIG. **5A**, an NPN transistor **62** formed by regions **33**, **35** and **36** of the structure in FIG. **2**, is added to the circuit of FIG. **[4B]** *4A* with transistor **62** shunting DMOS transistor **30**. Both electrons and holes continue to contribute to the overall device current, however, the holes collected by the P region **35** (FIG. **2**) flow through a relatively high resistance before reaching the I/O contact **42**. This resistance is denoted **64** in the schematic of FIG. **5A**, and is physically analogous to the base resistance in a bipolar transistor and is an inherent part of the DMOS structure. The resistance is a distributed resistor and holes are collected all along its length. The voltage drop along the resistor will tend to forward bias the PN+ junction (region **35**, **33**) which is the base-emitter junction of the NPN transistor whose collector is the N− body **36**. Once the voltage differential turns the NPN transistor on (at approximately 0.7 volts) a regenerative switching causes the four layer structure comprising the two bipolar transistors to switch to a low resistance state, which is illustrated in FIG. **[5B]** *5C*. Transistors **60** and **62** are equivalent to the arrangement of PNP and NPN devices used in conventional Triacs and SCRs.

It should be noted that the Triac or SCR is switched by applying a trigger voltage from an external source. While the device as illustrated in FIG. **2** is triggered to a low resistance state when the current through the device is increased by increasing the gate voltage, the device can be made to operate as a conventional SCR by forward biasing a junction. If separate ohmic contacts are formed to regions **35a** and **33**, externally forward biasing the P+N+ junction between regions **35a** and **33** will switch the device to its low resistance state. However, the device illustrated in FIG. **2** is switched to a low resistance mode by an MOS device in parallel with the Triac and not by forward biasing the junction externally, as is found with the conventional Triacs and SCRs. At low current levels before the Triac fires, the MOS characteristics of the structure dominate.

After firing the Triac, the device becomes a low resistance device.

FIG. 6 illustrates the surface doping profile for one switch device in accordance with the present invention. Absolute surface doping concentration is illustrated along the ordinate and distance across the device is illustrated along the abscissa. Relating the doping concentration to the device illustrated in cross section in FIG. 2, the N+ regions 33, 37 and 38 have a dopant concentration on the order of 10^{20} impurities per cubic centimeter. The P regions which comprise the channel regions of the two DMOS transistors 34, 39 have a peak dopant concentration on the order of 5×10^{16} impurities per cubic centimeter. The dopant concentration of the N− semiconductor body is on the order of 10^{15} impurities per cubic centimeter.

In fabricating the device, P+ diffusions are first formed to facilitate ohmic contact to the DMOS transistor channel regions. Then sequential diffusions of boron (P type) and phosphorus or arsenic (N type) are made employing conventional diffusion techniques to form the P and N+ regions. Ion implantation may also be advantageously used to introduce the boron (P type) impurity for the channel region of the devices. The gate oxidation is then formed over the channel regions, contact holes are made for the I/O contacts, metal is formed over the surface of the device and the metal pattern is defined by conventional photoresist masking and etching techniques.

The maximum doping in the P region at the surface under the gate along with the gate oxide thickness and the oxide charge density determine the DMOS threshold voltage. The channel width largely determines the DMOS transconductance and on resistance. The channel width also affects the Triac trigger current because the Triac is triggered by a specific current density flowing through the device. The DMOS properties are largely independent of the channel length.

The channel doping profile determines directly the DMOS threshold voltage. In addition, the current density at which switching to the low resistance mode of operation occurs is affected by this profile.

The doping level in the N− semiconductor body affects the device breakdown voltage, the DMOS on resistance and the lateral PNP transport efficiency.

The N+ drain region in the middle of the device is important in order to increase the breakdown voltage. If this diffused region is not included a parasitic P channel MOS transistor across the surface will reduce the breakdown voltage to the field oxide threshold voltage which is typically 20 to 40 volts. In addition, this N+ region increases the lateral PNP transport efficiency. The lateral dimension of the N+ region should be minimized as it degrades the PNP transport efficiency.

Referring now to FIG. 7, several modifications to the device shown in cross section in FIG. 2 are made. The same numerals are given to like elements. The semiconductor body region 36 in this embodiment comprises an epitaxial layer formed on a P− substrate 70. The structure may comprise a plurality of switching devices with each device isolated by means of diffused P+ regions 72 and 74 which extend through the epitaxial layer 36 to the underlying substrate 70 and surround the device. However, it is noted that a P+ substrate collects injected holes thus delaying the turn-on of the Triac lateral structure. Experimental results indicate that depending upon device geometry 10% to 50% of the injected holes are collected by the substrate before the Triac fires. While this does affect the efficiency of the device at higher voltage and current levels, the efficiency of the device is not affected at low voltage and current levels when all of the device current is carried by the MOS transistors. By adding an N+ buried layer between the N− epitaxial layer and the P− substrate, a reduction in injected holes captured by the substrate would be effected. Such buried layers are commonly employed in commercial integrated circuits and are readily acapted in standard production techniques. Additionally, dielectric isolation techniques can be employed instead of diffused isolation as shown in FIG. 7. By employing dielectric isolation the P− substrate of FIG. 7 can be replaced with an insulator, and consequently injected holes are not collected by the substrate. Alternatively, the P+ diffused regions, 72, 74 can be replaced by a dielectric such as silicon oxide.

The N+ region 37 spaced from the two double diffused regions is not necessary for low voltage. Triac operation and it can be eliminated if the device is not operated at high voltages. By eliminating this N+ region, the base width of the lateral PNP transistor can be reduced, resulting in lower triggering currents for the Triac and lower on resistance for the DMOS device. However, as indicated above the elimination of the N+ regoin creates a parasitic PMOS transistor between the two P diffused regions thus limiting the device breakdown voltage.

The separate ohmic contact made to the N+ region 37 as illustrated in FIG. 7 allows more versatility in operation of the device. The device can still be operated as a switching device as above described and as illustrated schematically in FIG. 8A. The N+ connection 78 can be left floating or can be connected to the +V potential applied to terminal [42] *44*. By connecting the terminal to the +V potential, the DMOS characteristics will dominate up to a higher voltage and current level before the device becomes a low resistance switch.

Alternatively, as shown schematically in FIG. 8B the device can be used as a standard DMOS transistor over its full operating range by connecting terminals 42 and 44 together as the source, and the N+ contact 78 becomes the drain.

In FIG. 8C, the device is used as a high level analog switch wherein a transducer 80 is driven at a high voltage with the transducer also used as part of a receiver. In this application the Triac capability is used with the transmitter, and the single DMOS capability is used with a receiver. Such a circuit would have application in an ultrasonic imaging system, or other applications involving transmit-receive switching.

FIG. 9 is a cross section view of another embodiment of a device in accordance with the present invention. In this embodiment the gate metallization is split into two separate gate contacts 46-1 and 46-2. This structure allows separate control of the firing of the device in the first and third quadrants of the device I-V characteristics. When the terminal 44 is positive (the anode) gate 46-1 is used to trigger the device. When the terminal 42 is positive (the anode), gate 46-2 is used to trigger the device. This configuration is useful in minimizing high oxide electric fields between the anode and the gate.

FIG. 10 is a cross section view of another embodiment of the device in accordance with the present invention. In this embodiment a single double diffused region comprising the N+ region 33 and P region 35 is provided along with a P+ diffused region 37. Contact 42 is made to regions 33 and 35, usually with the addi-

tion of P+ region **35a**, a gate contact **46-1** is made over oxide **48**, and an ohmic contact **78** is made to the P+ region **37**. This structure forms an MOS controlled silicon controlled rectifier and operates in the same mode as the device of FIG. **2** except that it is not symmetrical. Contact **78** must always be the anode and contact **42** must always be the cathode. The device has high input impedance on the control electrode **46-1**, and good isolation is provided between the control and signal paths.

FIG. **11** is a cross section view of another device in accordance with the present invention which also functions as an MOS controlled silicon controlled rectifier. Double diffused region **100** and **102** are formed in N− epitaxial layer **104**, and anisotropic silicon etching is employed to form a V groove through the regions **100** and **102** into the epitaxial layer **104**. An oxide layer **106** is thermally grown or deposited in the V groove and a gate contact **108** is formed thereover. An anode contact **110** is made to the P+ substrate **105**, the contacts **111** and **112** to the double diffused regions are connected in parallel as the cathode, and contact **108** is the gate. In this device current flows vertically.

FIG. **12** and FIG. **13** are cross section views of a device similar to the device of FIG. **2** and in which an additional MOS transistor is added to achieve a turnoff capability. In FIG. **12** the added MOS transistor is provided by a diffused P+ region **122** which is spaced from the P+ region **35a** with the N− substrate region therebetween functioning as a channel region of an MOS transistor. The gate electrode to transistor **120** is the off gate, and the gate electrode to the merged transistor **30** and **32** is the on gate.

FIG. **13** is a similar structure in which the device is formed in an N− epitaxial layer **124** on a P− substrate **126** with P+ isolation regions **128** diffused through the epitaxial layer **124**. In this embodiment the added transistor **120** is isolated from the merged transistor structure and comprises a double diffused MOS transistor (DMOS).

FIG. **14** is the equivalent electrical schematic of the devices illustrated in FIG. **12** and FIG. **13** and is similar to the electrical schematic of FIG. **5A** with the addition of the transistor **120** and off gate. When the off gate is turned on, the MOS transistor **120** effectively shorts out the base-emitter junction of the NPN transistor **62** thus bringing the transistor out of saturation. This causes the overall device to transfer from its low impedance regenerative condition and, provided the on gate is not turned on, will shut the device completely off thereby stopping anode current. This is a unique capability for a Triac type structure and is especially attractive because a high impedance MOS input is used to turn the device off. In addition, an off switch may be included on the anode (A) side of the device to enable it to be switched off when the anode and the cathode are reversed. This makes the overall device symmetric. Additionally, the transistor **120** may be used as a variable resistor to electronically vary the current at which the device switches to a low impedance regenerative condition. It will be appreciated that in a junction isolated or dielectrically isolated structure, the device in accordance with the present invention may be fabricated along side other components as technology in fabricating the device is compatible with the fabrication of other semiconductor devices.

The switching device in accordance with the present invention has a number of applications including analog multiplexers with high current "boost" capability, high voltage display driving, telephone cross point switches, and in power control applications.

Thus, while the invention has been described with reference to specific embodiments and applications, the description is illustrative of the invention and is not to be construed as limiting the invention. It will be appreciated that various manufacturing techniques are known for fabricating the devices and equivalent structures can be fabricated. For example, while the ohmic contacts are described as metallic, other contacts such as doped polysilicon can be employed. Thus, various applications, changes, and modifications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A monolithic semiconductor *SCR* device comprising:

a semiconductor [body] *substrate of one conductivity type and an epitaxial layer of opposite conductivity type, said epitaxial layer* having at least one major surface, and

[a body region adjacent to said surface of one conductivity type,] first and second spaced regions of [opposite] *said one* conductivity type formed in said [body region] *epitaxial layer* and abutting said major surface, third and fourth regions of said [one conductivity] *opposite conductivity* type formed in said first and second regions, respectively, abutting said major surface and defining first and second channel regions in said first and second regions, respectively,

a layer of insulation on said major surface,

a gate electrode formed on said layer of insulation and above said first and second channel regions, an ohmic contact to said first and third regions, and an ohmic contact to said second and fourth regions, *and*

an ohmic contact to said semiconductor substrate.

[**2**. A monolithic semiconductor device as defined by claim **1** and further including a fifth region of said one conductivity type formed in said semiconductor body between and spaced from said first and second regions.]

3. A monolithic semiconductor device as defined by claim [**2**] *1* wherein said one conductivity type is [N] *P* type and said opposite conductivity type is [P] *N* type.

[**4**. A monolithic semiconductor device as defined by claim **2** and including an ohmic contact to said fifth region.]

[**5**. A monolithic semiconductor device as defined by claim **1** wherein said body region of said semiconductor body comprises an epitaxial layer.]

6. A monolithic semiconductor device as defined by claim [**5**] *1* wherein said semiconductor device is electrically isolated by an isolation region through said epitaxial layer and surrounding said device.

7. A monolithic semiconductor device as defined by claim **6** wherein said isolation region comprises a diffused region.

8. A monolithic semiconductor device as defined by claim **6** wherein said isolation region comprises a dielectric material.

9. A monolithic semiconductor device as defined by claim **6** [wherein said semiconductor body includes] *and including a* plurality of like semiconductor devices

which are spaced and isolated from said one device by said isolation region.

10. A monolithic semiconductor device as defined by claim 1 wherein [said semiconductor body comprises a semiconductor substrate of said opposite conductivity type, said body region comprises an epitaxial layer of said one conductivity type formed on said substrate,] said first and second regions are spaced apart by a V-groove formed in said major surface and further including a layer of insulation over the surface of said V-groove and [a] *said* gate electrode *is* formed over said layer of insulation and spaced from said surface of said V-groove.

[11. A monolithic semiconductor device as defined by claim 1 and further including a fifth region of said opposite conductivity type abutting said major surface and spaced from said first region, an insulating layer overlying said major surface between said first and fifth regions, and a gate electrode formed on said insulative layer.]

12. An electrical *triac* circuit device comprising:

a first double diffused field effect transistor having source, gate, and drain regions,

a second double diffused field effect transistor having source, gate, and drain regions,

means ohmically connecting said drain regions, contact means for said gate regions,

[an] *a first anode* ohmic contact to said source region of said first field effect transistor, and

[an] *a second anode* ohmic contact to said source region of said second field effect transistor,

said first and second field effect transistors being formed in a semiconductor body and said means ohmically connecting said drain regions comprises a region of said semiconductor body.

[13. An electrical circuit device as defined by claim 12 wherein said first and second field effect transistors are formed in a semiconductor body and said means ohmically connecting said drain regions comprises a region of said semiconductor body.]

14. An electrical circuit device as defined by claim 12 wherein said source and drain regions are N type, and said channel regions are P type.

15. An electrical circuit device as defined by claim 12 wherein said semiconductor body includes an epitaxial layer and said first and second field effect transistors are formed in said epitaxial layer.

16. An electrical circuit device as defined by claim 15 and including an isolation region extending through said epitaxial layer and surrounding said first and second field effect transistors.

17. A monolithic semiconductor device as defined by claim 16 wherein said isolation region comprises a diffused region.

18. A monolithic semiconductor device as defined by claim 16 wherein said isolation region comprises a dielectric material.

19. A monolithic body having a plurality of isolated semiconductor regions of one conductivity type abutting a major surface of said body, each region including an electrical *triac* device comprising

first and second spaced regions of opposite conductivity type,

third and fourth regions of said one conductivity type formed in said first and second regions, respectively, and defining first and second channel regions in said first and second regions, respectively,

a layer of insulation on the surface of said semiconductor region,

a gate electrode formed on said layer of insulation and adjacent to said first and second channel regions,

[an] *a first anode* ohmic contact to said first and third regions, and

[an] *a second anode* ohmic contact to said second and fourth regions.

20. A monolithic body as defined by claim 19 wherein said insulation layer comprises silicon oxide and said monolithic body comprises a silicon substrate.

21. A monolithic body as defined by claim 20 wherein said monolithic body further includes an epitaxial layer and said electrical device is formed in said epitaxial layer.

22. A monolithic body as defined by claim 21 wherein said isolation is provided by diffused regions through said epitaxial layer of said opposite conductivity type.

23. A monolithic body as defined by claim 21 wherein said isolation is formed by dielectric material extending through said epitaxial layer.

24. A monolithic body as defined by claim 23 wherein said dielectric material is silicon oxide.

25. A monolithic semiconductor device comprising:

a semiconductor substrate of one conductivity type,

an epitaxial layer of opposite conductivity type, said epitaxial layer having a major surface, isolation means extending through said epitaxial layer and defined at least two isolated regions in said epitaxial layer,

one of said isolated regions including

a first double diffused field effect transistor having source, gate, and drain regions,

a second double diffused field effect transistor having source, gate, and drain regions,

means ohmically connecting said drain regions,

contact means for said gate regions,

an ohmic contact to said source region of said first field effect transistor, and

an ohmic contact to said source region of said second field effect transistor,

another of said isolated regions including

a third field effect transistor having source, gate, and drain regions, and

means electrically connecting said source region of said third transistor and said source region of said second transistor, said source region of said first transistor functions as an anode, said connected source regions of said second and third transistor function as a cathode, said gate regions of said first and second transistors function as an on gate, and said gate of said third field effect transistor functions as an off gate.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : Re. 33,209

DATED : May 1, 1990

INVENTOR(S) : JAMES D. PLUMMER

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On page 1, after the title, insert the following paragraph:

--This invention was made with Government support under National Institutes of Health (NIH) grant number 1PO1GM1 17940-5. The Government has certain rights in this invention.--

Signed and Sealed this

Eleventh Day of April, 1995

Bruce Lehman

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

US001033209A

REEXAMINATION CERTIFICATE (2666th)

United States Patent [19]

[11] B1 Re. 33,209

Plummer

[45] Certificate Issued Sep. 12, 1995

[54] **MONOLITHIC SEMICONDUCTOR SWITCHING DEVICE**

[75] Inventor: **James D. Plummer**, Mt. View, Calif.

[73] Assignee: **The Board of Trustees of the Leland Stanford Junior University**, Stanford, Calif.

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Reexamination Certificate for:

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Related U.S. Patent Documents

Reissue of:

[64] Patent No.:	**4,199,774**
Issued:	**Apr. 22, 1980**
Appl. No.:	**943,200**
Filed:	**Sep. 18, 1978**

Certificate of Correction issued Apr. 11, 1995.

[51] **Int. Cl.**[6] **H01L 29/78**
[52] **U.S. Cl.** **257/124**; 257/335
[58] **Field of Search** 257/378

[56] **References Cited**

U.S. PATENT DOCUMENTS

Re. 30,282	5/1980	Hunt et al.	437/47
1,745,175	1/1930	Lilienfeld	257/43
1,877,140	9/1932	Lilienfeld	257/43
1,900,018	3/1933	Lilienfeld	257/43
2,994,811	8/1961	Senitzky	257/367
3,025,589	3/1962	Hoerni	437/157
3,056,888	10/1962	Atalla	257/288
3,102,230	8/1963	Kahng	257/288
3,264,493	8/1966	Price	257/378
3,271,640	9/1966	Moore	257/378
3,283,170	11/1966	Buie	257/560
3,319,311	5/1967	Mutter	257/577
3,365,629	1/1968	Bouchard	257/563
3,398,337	8/1968	So	257/266
3,401,319	9/1968	Watkins	257/378
3,414,781	12/1968	Dill	257/401
3,417,299	12/1968	Dixon et al.	257/606
3,419,766	12/1968	Ono	257/404
3,437,891	4/1969	Yamashita	257/125
3,440,502	4/1969	Lin et al.	257/394
3,458,781	7/1969	Simon	257/171
3,461,360	8/1969	Barson et al.	257/337
3,484,865	12/1969	Nienhuis	257/343
3,500,368	3/1970	Abe	327/399
3,509,375	4/1970	Gormley	257/392
3,518,494	6/1970	James	257/539
3,521,141	6/1970	Walton	327/389
3,534,235	10/1970	Bower et al.	257/409
3,553,541	1/1971	King	257/378
3,566,518	3/1971	Brown et al.	257/369
3,590,345	6/1971	Brewer et al.	257/547
3,594,241	7/1971	Bresee	257/273
3,600,647	8/1971	Gray	257/339
3,600,651	8/1971	Duncan	257/263

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

2110326	8/1972	France .
1639373	12/1971	Germany .

(List continued on next page.)

OTHER PUBLICATIONS

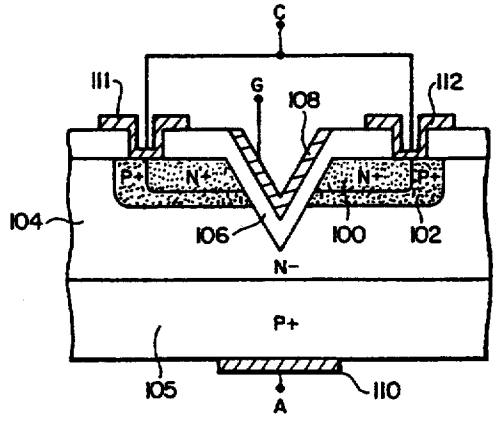
S. Y. Yu et al, "New V-Groove Double Diffused MOS (VDMOS)", Electronic Letters, vol. 12, No. 23, 11 Nov. 1976, p. 605.

(List continued on next page.)

Primary Examiner—William D. Larkins

[57] **ABSTRACT**

An electrical circuit device made in integrated monolithic form has low level operating characteristics of a MOS device and high level operating characteristics of a Triac. The structure includes two double diffused MOS transistors which have merged drain regions. At higher voltage and current levels a lateral Triac structure is triggered by the MOS devices. Alternatively, separate terminal contacts can be made to the P and N regions comprising the MOS transistor source and channel regions with the Triac triggered conventionally by an externally applied control voltage.



U.S. PATENT DOCUMENTS

3,609,473	9/1971	Bittmann et al.	257/664
3,619,740	11/1971	Nakanuma et al.	257/262
3,622,841	11/1971	Zoroglu	257/127
3,631,312	12/1971	Moyle et al.	257/409
3,650,019	3/1972	Robinson	437/40
3,665,266	5/1972	Drozdowicz et al.	257/552
3,667,115	6/1972	Barson et al.	257/378
3,675,092	7/1972	Kocsis et al.	257/367
3,702,947	11/1972	Schilling	257/552
3,719,535	3/1973	Zoroglu	257/279
3,731,164	5/1973	Cheney	257/378
3,733,597	5/1973	Healey et al.	327/421
3,739,237	6/1973	Shannon	257/387
3,742,318	6/1973	Yamashita	257/122
3,749,985	7/1973	Dawson	257/587
3,753,055	8/1973	Yamashita et al.	257/122
3,764,396	10/1973	Tarui et al.	257/593
3,786,319	1/1974	Tomisaburo	257/365
3,811,076	5/1974	Smith, Jr.	257/296
3,812,521	5/1974	Davis et al.	257/546
3,814,992	6/1974	Kump et al.	257/403
3,821,776	6/1974	Hayashi et al.	357/337
3,831,187	8/1974	Neilson	257/137
3,845,495	10/1974	Cauge et al.	257/336
3,846,259	11/1974	Duncan et al.	257/77
3,849,216	11/1974	Salters	257/365
3,863,330	2/1975	Kraybill et al.	257/336
3,871,067	3/1975	Bogardus et al.	257/655
3,873,989	3/1975	Schnilla et al.	257/162
3,891,468	6/1975	Ito et al.	257/403
3,895,978	7/1975	Tarui et al.	437/27
3,921,283	11/1975	Shappir	257/371
3,923,553	12/1975	Hayashi et al.	437/41
3,950,777	4/1976	Tarui et al.	257/330
3,977,017	8/1976	Ishitani	257/266
3,977,019	8/1976	Matsushita et al.	257/489
3,978,577	9/1976	Bhattacharyya et al.	257/324
3,986,195	10/1976	Arai	257/257
3,986,903	10/1976	Watrous, Jr.	437/153
4,001,860	1/1977	Cauge et al.	257/336
4,001,867	1/1977	Kravitz et al.	257/122
4,003,071	1/1977	Takagi	257/406
4,003,072	1/1977	Matsushita et al.	257/170
4,007,478	2/1977	Yagi	257/336
4,009,483	2/1977	Clark	257/489
4,015,278	3/1977	Fukuta	257/266
4,028,717	6/1977	Joy et al.	257/404
4,042,945	8/1977	Lin et al.	257/406
4,055,884	11/1977	Jambotkar	257/341
4,058,822	11/1977	Awane et al.	257/336
4,062,040	12/1977	Abbas et al.	257/394
4,070,690	1/1978	Wickstrom	257/331
4,078,947	3/1978	Johnson et al.	257/337
4,080,619	3/1978	Susuki	257/337
4,084,175	4/1978	Ouyang	257/336
4,092,661	5/1978	Watrous, Jr.	257/387
4,101,922	7/1978	Tihanyi et al.	257/360
4,112,455	9/1978	Seliger et al.	257/335
4,190,850	2/1980	Tihanyi et al.	257/343
4,206,469	6/1980	Hanes et al.	257/341
4,213,140	7/1980	Okabe et al.	257/357
4,219,834	8/1980	Esch et al.	257/296
4,224,634	9/1980	Svedberg	257/138
4,246,596	1/1981	Mori	257/659
4,396,932	8/1983	Alonas et al.	257/122
4,561,008	12/1985	Becke	257/152

FOREIGN PATENT DOCUMENTS

2040657	2/1972	Germany .
1564534	9/1972	Germany .
2136509	11/1972	Germany .
1489250	2/1974	Germany .
2511487	9/1975	Germany .
2754229	6/1978	Germany .
2705990	8/1978	Germany .
52-23277	8/1975	Japan .
51-48981	4/1976	Japan .
51-85381	7/1976	Japan .
52-106688	of 1977	Japan .
52-42080	4/1977	Japan .
52-104878	9/1977	Japan .
53-74385	7/1978	Japan .
53-74386	7/1978	Japan .
439457	12/1935	United Kingdom .
1153428	5/1969	United Kingdom .
1224335	3/1971	United Kingdom .
1367325	9/1971	United Kingdom .
1372086	11/1971	United Kingdom .
1390135	5/1972	United Kingdom .
1400574	8/1972	United Kingdom .
1455840	12/1973	United Kingdom .
1465244	3/1975	United Kingdom .

OTHER PUBLICATIONS

Zuleeg, R., "A Multichannel Field-effect Transistor", *Proceedings of the IEEE,* vol. 52, No. 10, pp. 1245–1246 (Oct. 1964).

Author unidentified, *Integrated Circuits<Design Principles and Manufacture>, Scientific Book Printing, published by Hosaku Kanai, (May 10, 1967), pp. 233–235.*

Zuleeg, R., "A Multi-Channel Field-Effect Transistor Theory and Experiment", *Solid-State Electronics,* vol. 10, pp. 559–576 (1967).

Kao, Y. C., et al., "High-Voltage Planar *p–n* Junctions", *Proceedings of the IEEE,* vol. 55, No. 8, pp. 1409–1414 (Aug. 1967).

Tarui, Y., et al., "Diffusion Self-aligned MOST: A New

(List continued on next page.)

OTHER PUBLICATIONS

Hamilton & Howard, Basic Integrated Circuit Engineering (McGraw-Hill, N.Y.), 1975, pp. 12-13, 24, 82-84.

Plummer et al, IEEE Journal of Solid State Circuits, vol. SC-11, No. 6, Dec. 1976, pp. 809-817.

Shockley, W., et al., "*p-n* Junction Transistors", *Physical Review*, vol. 83, No. 1, pp. 151-162 (Jul. 1, 1951).

Shockley, W., "A Unipolar 'Field-Effect' Transistor", *Proceedings of the I.R.E.*, vol. 40, No. 11, pp. 1365-1376 (Nov., 1952).

Hofstein et al, "The Silicon Insulated-Gate Field-Effect Transistor", *Proceedings of the IEEE*, vol. 51, No. 9, pp. 1190-1202 (Sep., 1963).

Approach for High Speed Device", Proceedings of the 1st Conference on Solid State Devices, Tokyo, 1969, Supplement to the *Journal of the Japan Society of Applied Physics*, vol. 39, pp. 105-110 (1970).

Lee, D. B., "Anisotropic Etching of Silicon", *Journal of Applied Physics*, vol. 40, No. 11, pp. 4569-4574 (Oct. 1969).

Dill, H., "A New Insulated Gate Tetrode with High Drain Breakdown Potential and Low Miller Feedback Capacitance", *IEEE Transactions on Electron Devices*, vol. ED-15, No. 10 (Oct. 1968).

Author unidentified, "Japanese Take Two Steps Forward in MOS-bipolar Compatibility", *Electronics International* (Oct. 13, 1969).

Faggin, F. et al., "Silicon Gate Technology", *Solid-State Electronics*, vol. 13, pp. 1125-1144 (1970).

Le Can, C., "Session VI: Digital Circuit Applications of IC Technology; WPM 6.4: A New Current-Mode Circuitry and Process for Fast Logic and Memory Applications", IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 66-67 (Feb. 1971).

Cauge, T. et al., "Double-diffused MOS Transistor Archieves Microwave Gain", *Electronics*, pp. 99-104 (Feb. 15, 1971).

Author unidentified, "Improvement in Breakdown Voltage of MOSFET to 200 V", *Nikkei Electronics*, p. 22 (1972).

Sigg, H. et al., "D-MOS Transistor for Microwave Applications", *Transactions on Electron Devices*, vol. ED-19, No. 1, pp. 45-53 (Jan. 1972).

McLintock, G. et al., "Forward and Reverse Characteristics of Self-Aligned Double-Diffused M.O.S. Transistors", *Electronic Letters*, vol. 8, No. 18, pp. 463-465 (Sep. 7, 1972).

Rao et al., "MOSFET Devices with Trapezoidal Gates: *I-V* Characteristics and Magnetic Sensitivity", *Solid-State Electronics*, vol. 16, pp. 483-490 (1973).

Rodges, T., et al., "Epitaxial V-Groove Bipolar Integrated Circuit Process", *IEEE Transactions on Electronic Devices*, vol. ED-20, No. 3, pp. 226-232 (Mar. 1973).

Holmes, F. E. et al., "V Groove M.O.S. Transistor Technology", *Electronic Letters*, vol. 9, No. 19, pp. 457-458 (Sep. 20, 1973).

Yagi, H. et al, "FET Application to Power Amplifiers", *JEI*, pp. 18-30, Jan. 1974.

Author unidentified, "Aus Japan: Ein Feldeffekt-Transistor für hohe Nf-Leistungen", *Funkschau*, pp. 3069-3070 (1974).

Hemmert, R., "Invariance of the Hall Effect MOSFET to Gate Geometry", *Solid-State Electronics*, vol. 17, pp. 1039-1043 (1974).

Holmes, F. E. et al., "VMOS—A New MOS Integrated Circuit Technology", *Solid-State Electronics*, vol. 17, pp. 791-797 (1974).

Plummer, J. et al., "Session XIV: New Applications of Integrated Electronics, THPM 14.2: An Utrasonic Imaging System for Realtime Cardiac Imaging", *IEEE* International Solid-State Circuits Conference, Digest of Technical Papers, pp. 162-163 (Feb. 1974).

Rodgers, T. et al., "VMOS: High Speed TTL Compatible MOS Logic", *IEEE Journal of Solid-State Circuits*, vol. SC-9, No. 5, pp. 239-249 (Oct. 1974).

Cady, R. et al., "Integration Technique for Closed Field-Effect Transistors", *IBM Technical Disclosure Bulletin*, vol. 16, No. 11, pp. 3519-3520 (Apr. 1974).

Dennard, R. et al., "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions", *IEEE Journal of Solid-State Circuits*, vol. SC-9, No. 5, pp. 256-268 (Oct. 1974).

Taylor, B., "Vertical M.O.S. Transistor Geometry for Power Amplification at Gigahertz Frequencies", *Electronic Letters*, vol. 10, No. 23, pp. 490-493 (Nov. 14, 1974).

(List continued on next page.)

OTHER PUBLICATIONS

Pocha, M. et al., "Threshold Voltage Controllability in Double-Diffused-MOS Transistors", *IEEE Transactions on Electron Devices*, vol. ED-21, No. 12, pp. 778-784 (Dec. 1974).

Ozawa, O. et al., "A Multi-Channel FET with a New Diffusion Type Structure", Proceedings of the 7th Conference on Solid State Devices, Tokyo, 1975: Supplement of *Japanese Journal of Applied Physics*, vol. 15, pp. 171-177 (1976).

Yoshida, I. et al., "A High Power MOSFET with a Vertical Drain Electrode and Meshed Gate Structure", International Electron Devices Meeting, Sponsored by IEEE Group on Electron Devices, Technical Digest, pp. 159-162 (1975).

Nishizawa, J. et al., "Field-Effect Transistor Versus Analog Transistor (Static Induction Transistor)", *IEEE Transactions on Electron Devices*, vol. ED-22, No. 4, pp. 185-197 (Apr. 1975).

Suwa, H. et al., "Vertical Field Effect Transistor and its Application to High Fidelity Audio Amplifiers", Presented at the 51st Convention, pp. 1-7 (May 13-16, 1975).

Saraswat, K. et al., "A High Voltage MOS Switch", *IEEE Journal of Solid-State Circuits*, vol. SC-10, No. 3, pp. 136-142 (Jun. 1975).

Rodgers, T. et al., "An Experimental and Theoretical Analysis of Double-Diffused MOS Transistors", *IEEE Journal of Solid-State Circuits*, vol. SC-10, No. 5, pp. 322-331 (Oct. 1975).

Author unidentified, "MOSFET Power Soars to 60 W with Currents up to 2 A", *Electronic Design*, vol. 21, pp. 103-104 (Oct. 11, 1975).

Hama, T., "Invited: Electronic Watches Using Quartz Crystal Oscillators", Proceedings of the 8th Conference (1976 International) on Solid-State Devices, Tokyo 1976: *Japanese Journal of Applied Physics*, vol. 16, Supplement 16-1, p. 185 (1977).

Ohkura, I. et al., "Fully Ion Implanted DSA MOS IC", Proceedings of the 8th Conference (1976 International) on Solid State Devices, Tokyo, 1976: *Japanese Journal of Applied Physics*, vol. 16, Supplement 16-1, pp. 167-171 (1977).

Hayashi, T. et al., "Invited: DSA MOS Transistor and Its Integrated Circuit", Proceedings of the 8th Conference (1976 International) on Solid State Devices, Tokyo, 1976: *Japanese Journal of Applied Physics*, vol. 16, Supplement 16-1, pp. 163-166 (1977).

Nagata, M., "Invited: Power Handling Capability of MOSFET", Proceedings of the 8th Conference (1976 International) on Solid State Devices, Tokyo, 1976: *Japanese Journal of Applied Physics*, vol. 16, Supplement 16-1, pp. 217-222 (1977).

Nishimatsu, S. et al., "Grooved Gate MOSFET", Proceedings of the 8th Conference (1976 International) on Solid State Devices, Tokyo, 1976: *Japanese Journal of Applied Physics*, vol. 16, Supplement 16-1, pp. 179-183 (1977).

Masuhru, T. et al., "Analytical Technique for the Design of DMOS Transistors", Proceedings of the 8th Conferernce (1976 International) on Solid State Devices, Tokyo, 1976: *Japanese of Applied Physics*, vol. 16, Supplement 16-1, pp. 173-178 (1977).

Declercq, M. et al., "Avalanche Breakdown in High--Voltage D-MOS Devices", *IEEE Transactions on Electron Devices*, vol. ED-23, No. 1, pp. 1-4 (Jan. 1976).

Stone, J. et al., "Recent Advances in Ion Implantation—A State of the Art Review", *Solid State Technology*, pp. 35-44 (Jul. 1976).

Oakes, J. et al., "A Power Silicon Microwave MOS Transistor", *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-24, No. 6, pp. 305-311 (Jun. 1976).

Vander Kooi, M. et al., "MOS Moves into High-Power Applications", *Electronics*, pp. 98-103 (Jun. 24, 1976).

REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **2, 4, 5, 11** and **13** were previously cancelled.

Claims **6–9** are cancelled.

Claims **1, 12, 19** and **25** are determined to be patentable as amended.

Claims **3, 10, 14–18** and **20–24**, dependent on an amended claim, are determined to be patentable.

1. A monolithic semiconductor SCR device *having a bipolar mode of operation,* comprising:

a semiconductor substrate of one conductivity type and an epitaxial layer of opposite conductivity type, said epitaxial layer having at least one major surface, and

first and second spaced regions of said one conductivity type formed in said epitaxial layer and abutting said major surface, third and fourth regions of said opposite conductivity type formed in said first and second regions, respectively, abutting said major surface and defining first and second channel regions in said first and second regions, respectively,

a layer of insulation of said major surface,

a gate electrode formed on said layer of insulation and above said first and second channel regions, an ohmic contact to said first and third regions, and an ohmic contact to said second and fourth regions,

means for electrically connecting said ohmic contact to said first and third regions to said ohmic contact to said second and fourth regions,

said first and second regions, said epitaxial layer, and said substrate defining a first bipolar transistor whose conduction is controlled by current supplied through said first and second channel regions under control of the voltage applied to said gate electrode, said first, second, third, and fourth regions and said epitaxial layer defining a second bipolar transistor whose conduction is controlled by current supplied by the conduction of said first bipolar transistor, and

an ohmic contact to said semiconductor substrate,

first means for applying a first voltage to said gate electrode with respect to said ohmic contacts to said first, second, third, and fourth regions,

second means for applying a second voltage to said ohmic contact to said semiconductor substrate with respect to said ohmic contacts to said first, second, third, and fourth regions,

said first and second voltages being such as to cause said first bipolar transistor to conduct without resulting in the turn-on of said second bipolar transistor, such that said SCR is operated as an MOS controlled bipolar transistor.

12. An electrical triac circuit device *having a bipolar mode of operation,* comprising:

a first double diffused field effect transistor having source, gate, and drain regions,

a second double diffused field effect transistor having source, gate, and drain regions,

means ohmically connecting said drain regions,

contact means for *providing a gate electrode for* said gate regions,

a first anode ohmic contact to said source [region] *and gate regions* of said first field effect transistor, and

a second anode ohmic contact to said source [region] *and gate regions* of said second field effect transistor,

said first and second field effect transistors being formed in a semiconductor body and said means ohmically connecting said drain regions comprises a region of said semiconductor [body] *body,*

each said gate region having a channel region and each being of opposite conductivity type to said body,

said first and second field effect transistor gate regions and said body defining a first bipolar transistor whose conduction is controlled by current supplied through said channel regions under control of the voltage applied to said gate electrode,

said body and said first field effect transistor gate and source regions defining a second bipolar transistor whose conduction is controlled by current supplied by the conduction of said first bipolar transistor,

first means for applying a first voltage to said gate electrode with respect to said first anode ohmic contact,

second means for applying a second voltage to said second anode ohmic contact with respect to said first anode ohmic contact,

said first and second voltages being such as to cause said first bipolar transistor to conduct without resulting in the turn-on of said second bipolar transistor, such that said device is operated as an MOS controlled bipolar transistor.

19. A monolithic body having a plurality of isolated semiconductor regions of one conductivity type abutting a major surface of said body, each region including an electrical triac device *having a bipolar mode of operation,* comprising

first and second spaced regions of opposite conductivity type,

third and fourth regions of said one conductivity type formed in said first and second regions, respectively, and defining first and second channel regions in said first and second regions, respectively,

a layer of insulation on the surface of said semiconductor region,

a gate electrode formed on said layer of insulation and adjacent to said first and second channel regions,

a first anode ohmic contact to said first and third regions, and

a second anode ohmic contact to said second and fourth [regions] *regions,*

said first and second regions and said body defining a first bipolar transistor whose conduction is controlled by current supplied through said channel regions under control of the voltage applied to said gate electrode,

said body and said first and third regions defining a second bipolar transistor whose conduction is controlled by current supplied by the conduction of said first bipolar transistor,

first means for applying a first voltage to said gate electrode with respect to said first anode ohmic contact,

second means for applying a second voltage to said second anode ohmic contact with respect to said first anode ohmic contact,

said first and second voltages being such as to cause said first bipolar transistor to conduct without resulting in the turn-on of said second bipolar transistor, such that said device is operated as an MOS controlled bipolar transistor.

25. A monolithic semiconductor device *having a bipolar mode of operation,* comprising:

a semiconductor substrate of one conductivity type,

an epitaxial layer of opposite conductivity type, said epitaxial layer having a major surface, isolation means extending through said epitaxial layer and [defined] *defining* at least two isolated regions in said epitaxial layer,

one of said isolated regions including

a first double diffused field effect transistor having source, gate, and drain regions, *said first double diffused field effect transistor being defined by said epitaxial layer, a first region of said one conductivity type formed in said epitaxial layer and a second region of said opposite conductivity type formed in said first region, said second region defining said source of said first double diffused field effect transistor, said first and second regions defining said gate region of said first field effect transistor, said gate region having a first channel region,*

a second double diffused field effect transistor having source, gate, and drain regions, *said second double diffused field effect transistor being defined by said epitaxial layer, a third region of said one conductivity type formed in said epitaxial layer and a fourth region of said opposite conductivity type formed in said third region, said fourth region defining said source of said second double diffused field effect transistor, said third and fourth regions defining said gate region of said second field effect transistor, said gate region having a second channel region,*

means ohmically connecting said drain regions,

contact means for *providing a gate electrode for* said *first and second field effect transistor* gate regions,

an ohmic contact to said source region *and to said first region* of said first field effect transistor, and

an ohmic contact to said source region of said second field effect transistor,

another of said isolated regions including

a third field effect transistor having source, gate, and drain regions, *said third double diffused field effect transistor being defined by said epitaxial layer, a fifth region of said one conductivity type formed in said epitaxial layer and a sixth region of said opposite conductivity type formed in said fifth region, said sixth region defining the source of said third double diffused field effect transistor,*

an ohmic contact to said source region and said fifth region of said third field effect transistor,

means electrically connecting said drain region of said third field effect transistor and said third region, and

means electrically connecting said *ohmic contact to said* source region of said third transistor and said source region of said second transistor, said source region of said first transistor functions as an anode, said connected source regions of said second and third transistor function as a cathode, said gate regions of said first and second transistors function as an on gate, and said gate *region* of said third field effect transistor functions as an off [gate] *gate,*

said first region, said epitaxial layer and said third region defining a first bipolar transistor whose conduction is controlled by current supplied through said first and second channel regions under control of the voltage applied to said electrode gate, said epitaxial layer, said third region and said fourth region defining a second bipolar transistor whose conduction is controlled by the current supplied by the conduction of said first bipolar transistor,

first means for applying a first voltage to said gate electrode with respect to said ohmic contact to said source region of said second field effect transistor,

second means for applying a second voltage to said ohmic contact to said source region of said first field effect transistor with respect to said ohmic contact to said source region of said second field effect transistor,

said first and second voltages being such as to cause said first bipolar transistor to conduct without resulting in the turn-on of said second bipolar transistor, such that said device is operated as an MOS controlled bipolar transistor.

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REEXAMINATION CERTIFICATE (2773th)

United States Patent [19]

Plummer

[11] **B2 Re. 33,209**

[45] Certificate Issued **Jan. 16, 1996**

[54] **MONOLITHIC SEMICONDUCTOR SWITCHING DEVICE**

[75] Inventor: **James D. Plummer**, Mt. View, Calif.

[73] Assignee: **The Board of Trustees of the Leland Stanford Junior University**, Stanford, Calif.

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No. 90/003,603, Oct. 17, 1994
No. 90/003,934, Sep. 15, 1995

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Appl. No.: **943,200**
Filed: **Sep. 18, 1978**

Reexamination Certificate B1 1,033,209 issued Sep. 12, 1995

Certificate of Correction issued Apr. 11, 1995.

Related U.S. Patent Documents

Reissue of:
[64] Patent No.: **3,209,**
Issued: **May 1, 1990**
Appl. No.: **539,111**
Filed: **Dec. 5, 1983**

Which Is a Reissue of:
[64] Patent No.: **4,199,774**
Issued: **Apr. 22, 1980**
Appl. No.: **943,200**
Filed: **Sep. 18, 1978**

[51] **Int. Cl.**[6] **H01L 29/78**
[52] **U.S. Cl.** **257/124**; 257/335

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,239,362	3/1966	Sadler	148/177
3,337,783	8/1967	Stehney	317/235
3,437,891	4/1969	Yamashita	317/235
3,476,993	11/1994	Aldrich et al.	317/235
3,831,187	8/1974	Neilson	357/38
4,224,634	9/1980	Svedberg	357/38

FOREIGN PATENT DOCUMENTS

52-104878 9/1977 Japan .

OTHER PUBLICATIONS

Hung L. D. Eng., "The Field Effect Controlled Switch," Microelectronics, vol. 3, No. 7, Jul. 1970, pp. 36–38.

R. W. Aldrich and N. Holonyak, Jr., "Two-terminal asymmetrical and symmetrical silicon negative resistance switches," J. Appl. Physics vol. 30 pp. 1819–1824, Nov., 1959.

Adolph Blicher, Thyristor Physics, Springer-Verlag, New York: 1976, pp. 1–13.

P. S. Raderecht, "A Review of the 'Shorted Emitter' Principle as Applied to P–N–P–N Silicon Controlled Rectifiers," Inc. J. Electronics, 1971, vol. 31, No. 6, pp. 541–564.

L. L. Rosier, "Semiconductor Crosspoints," IBM J. Research Development, Jul. 1969, pp. 439–446.

Chang K. Chu, "Geometry of Thyristor Cathode Shunts," Trans. on Electron Devices, vol. ED–17, No. 9, Sep. 1970, pp. 68–690.

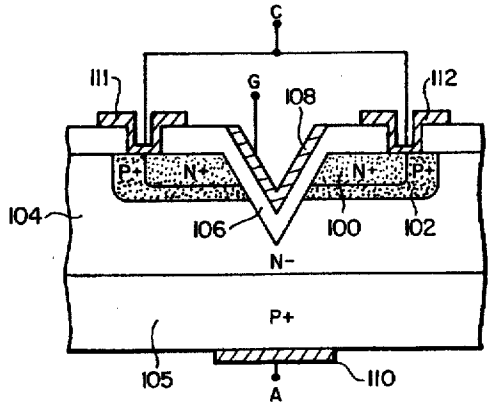
A. Munoz-Yague, et al., "Optimum Design of Thyristor Gate–Emitter Geometry," IEEE Trans. on Electron Devices, vol. ED–23, No. 8, Aug., 1976, pp. 917–924.

(List continued on next page.)

Primary Examiner—William D. Larkins

[57] **ABSTRACT**

An electrical circuit device made in integrated monolithic form has low level operating characteristics of a MOS device and high level operating characteristics of a Triac. The structure includes two double diffused MOS transistors which have merged drain regions. At higher voltage and current levels a lateral Triac structure is triggered by the MOS devices. Alternatively, separate terminal contacts can be made to the P and N regions comprising the MOS transistor source and channel regions with the Triac triggered conventionally by an externally applied control voltage.



OTHER PUBLICATIONS

F. E. Gentry, et al, "Bidirectional Triode P–N–P–N Switches," Proceedings of the IEEE, vol. 53, No. 4, Apr. 1965, pp. 355–369.

W. Kapallo, et al., "On–Characteristics of Planar SCR's with Regard to the Use of These Devices in Monolithic Circuits," Solid–State Electronics, Pergamon Press 1968, vol. 11, pp. 347–444.

F. E. Gentry, Semiconductor Controlled Rectifiers: Principles and Applications of P.N.P.N. Devices, Prentice–Hall, Englewood Cliffs, N.J. 1964, pp. 138–139.

Brad W. Scharf, "An Insulated–Gate Thyristor Structure: Principles of Operation and Design,"Ph.d Dissertation, Dec., 1979. Terman Engineering Library, Stanford University.

James D. Plummer, et al, "Insulated–Gate Planar Thyristors: I–Structure and Basic Operation," IEEE Transactions on Electron Devices, vol. ED–27, No. 2, Feb. 1980, pp. 380–387.

Brad W. Scharf, et al., "Insulated–Gate Planar Thyristors: II—Quantitative Modeling," IEEE Transactions on Electron Devices, vol. ED–27, No. 2, Feb. 1980, pp. 387–394.

Power Integrated Circuits: Physics, Design, and Application, R. Krajewski, et al. editor, Ch. 3, J. D. Plummer, et al., McGraw–Hill, 1986, pp. 3.1–3.58.

B. Jayant Baliga, "Enhancement—and Depletion–Mode Vertical–Channel M.O.S. Gated Thyristors," IEEE Electronics Letters, Sep. 27, 1979, vol. 15, No. 20, pp. 645–647.

B. Jayant Baliga, Modern Power Devices, Krieger Publishing Company, Malabar, Fla., 1992, Ch. 7, pp. 344–406.

R. W. Aldrich, "Silicon–Controlled Rectifiers from Oxide–Masked Duffused Structures," Transaction of IEEE (Communications and Electronics) vol. 77, Jan., 1959, pp. 952–954.

W. Fulop, "Three Terminal Measurements of Current Amplification Factors of Controlled Rectifiers," IEEE Transactions on Electron Devices, vol. ED–10, May, 1963, pp. 120–133.

I. M. Mackintosh, "The Electrical Characteristics of Silicon P–N–P–N Triodes," Proceedings of the IRE, Jun., 1958, pp. 1229–1235.

C. W. Mueller, et al., "The 'Thyristor'—A New High–Speed Switching Transistor,"IRE Transactions on Electron Devices, Jan., 1958, pp. 2–5.

Yu, et al., "New V–Groove Double Diffused MOS (VDMOS)", Electronics Letters, Nov. 11, 1976, vol. 12, No. 23, pp. 605.

Plumer, et al., "Monolithic 200V CMOS Analog Switch," IEEE Journal of Solid State Circuit, ISL. SC–11, No. 6, Dec. 1976, pp. 809–817.

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NO AMENDMENTS HAVE BEEN MADE TO THE PATENT

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **1**, **3**, **10**, **12** and **14–25** is confirmed.

Claims **2**, **4–9**, **11** and **13** were previously cancelled.

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