

United States Patent

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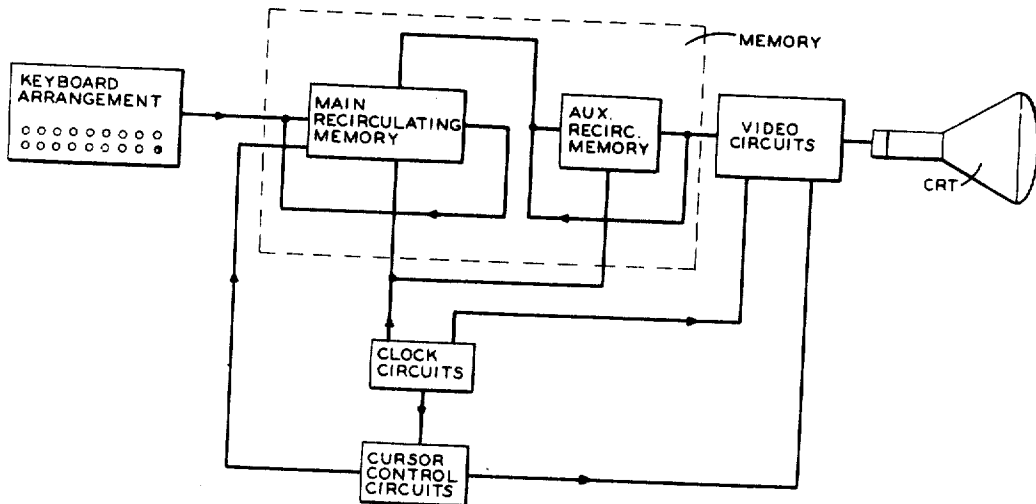
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[54] **INFORMATION DISPLAY SYSTEM**
31 Claims, 9 Drawing Figs.

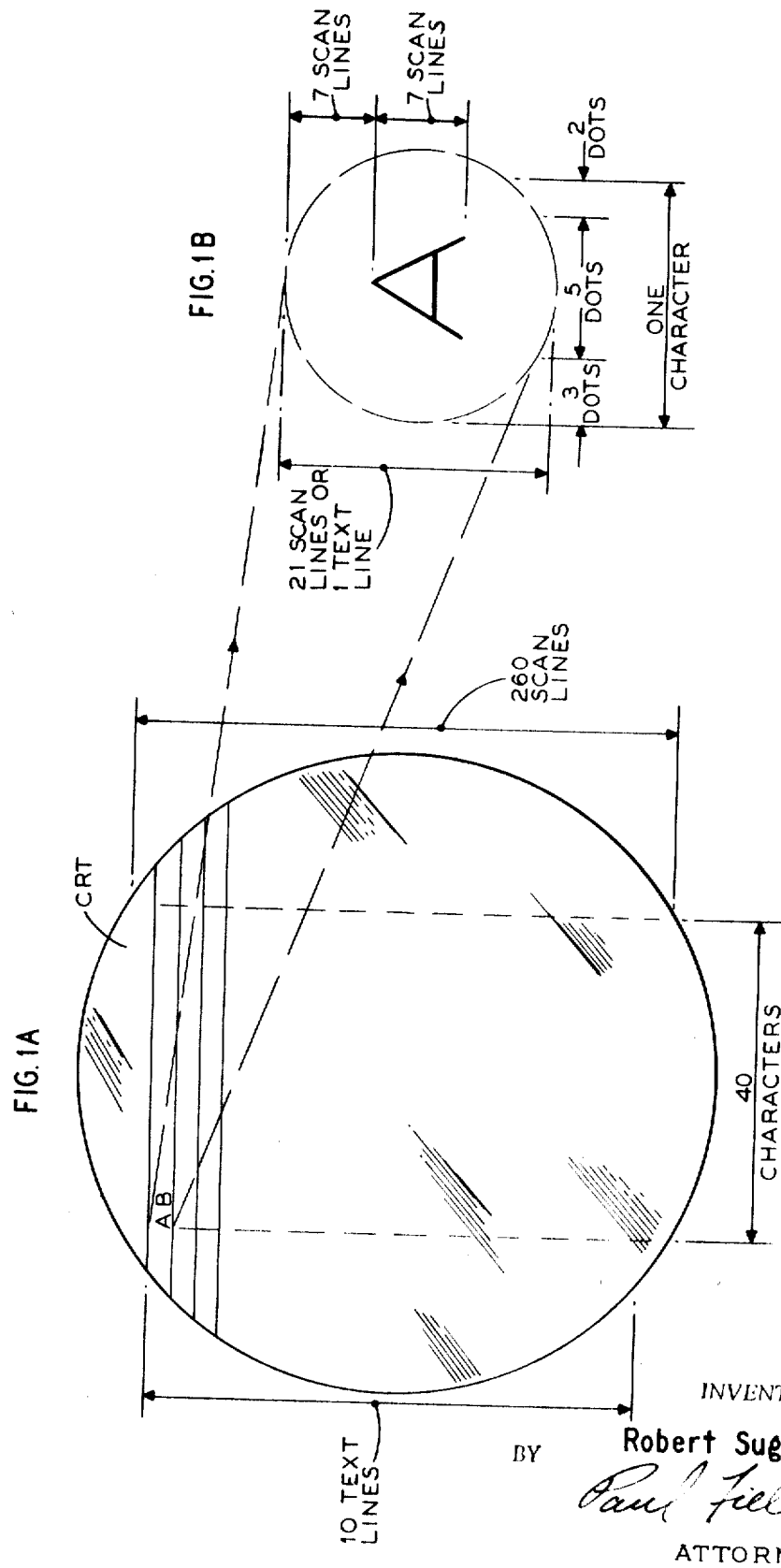
[52] U.S. Cl. **340/172.5**
[51] Int. Cl. **G06f 3/14**
[50] Field of Search **340/172.5,**
324; 235/157

[56] **References Cited**
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ABSTRACT: A system for the display of information on a cathode-ray tube or the like wherein the information comprises a plurality of lines of text comprising a number of characters and wherein each text line is formed by a plurality of scans. The system comprises a main memory for storing sets of bits wherein each set of bits represents a different one of all the characters to be displayed and an auxiliary memory for storing the sets of bits comprising the particular text line being formed on the screen of the cathode-ray tube. The auxiliary memory is operable to sequentially present each set of bits stored therein at its output during each scan comprising the particular text line. Decoding means responsive to the set of bits of the output of the auxiliary memory is provided to modulate the electron beam to form areas of the character represented by the set of bits during a particular scan.



GENERALIZED SYSTEM DIAGRAM



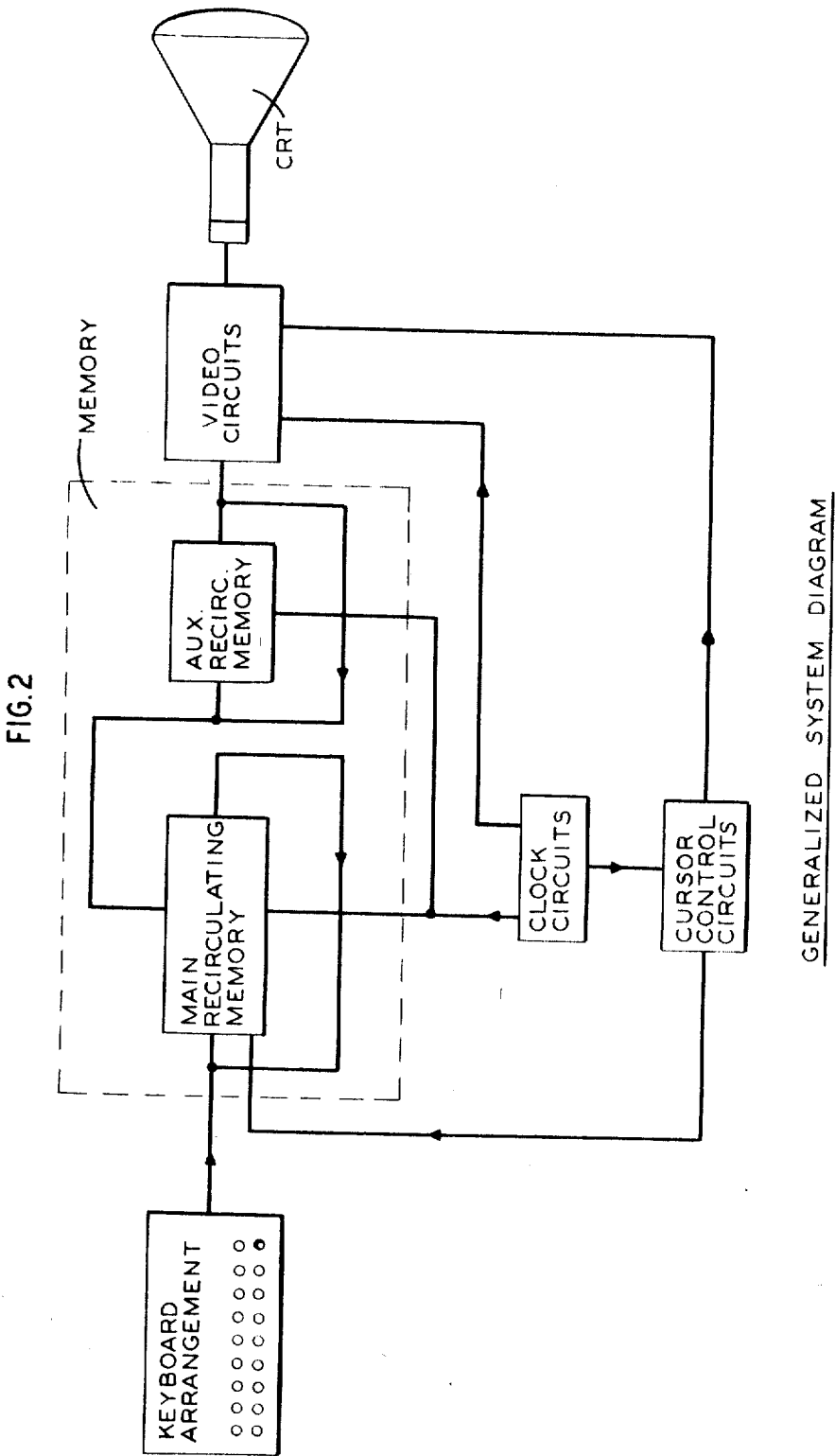
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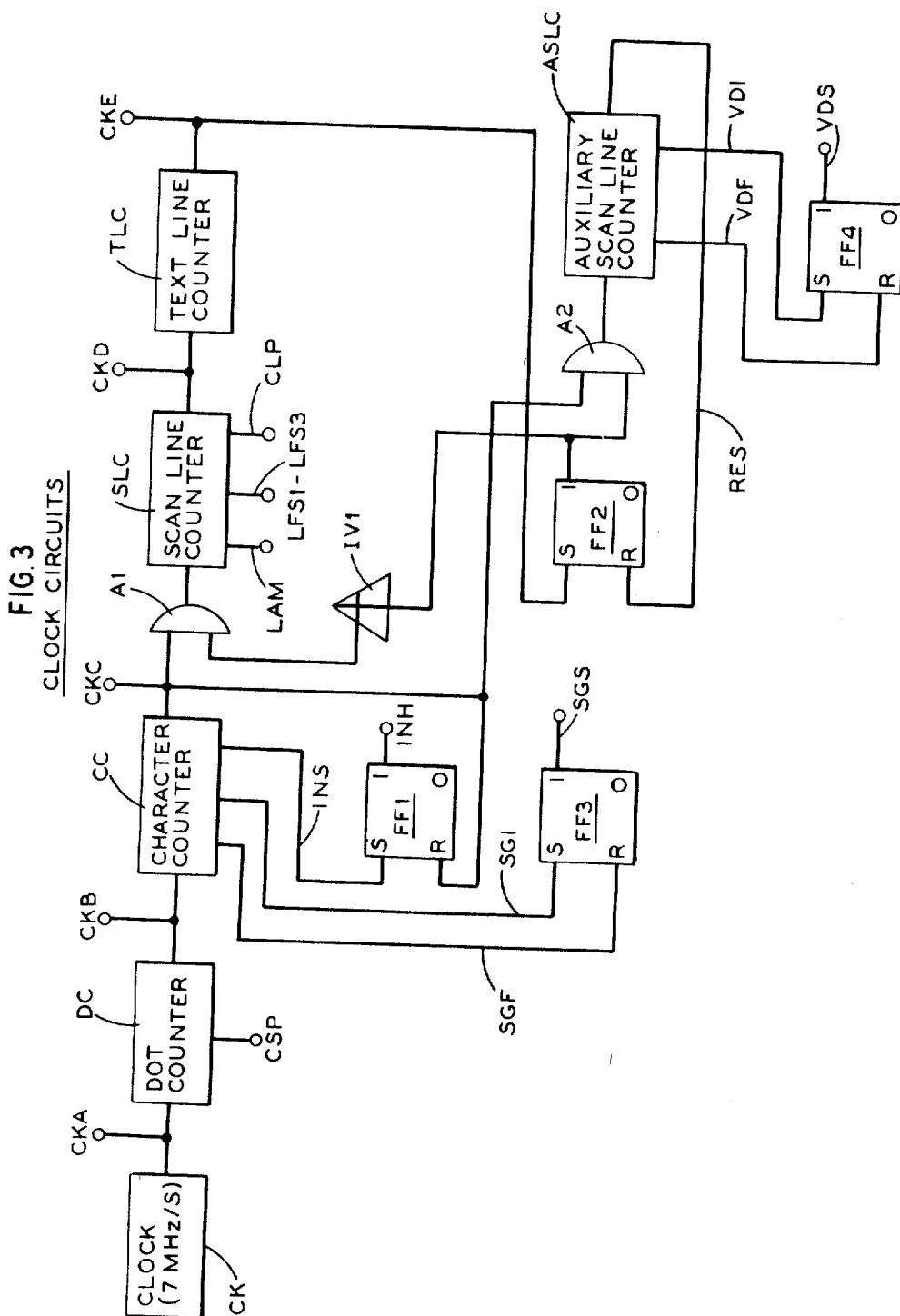


FIG. 4

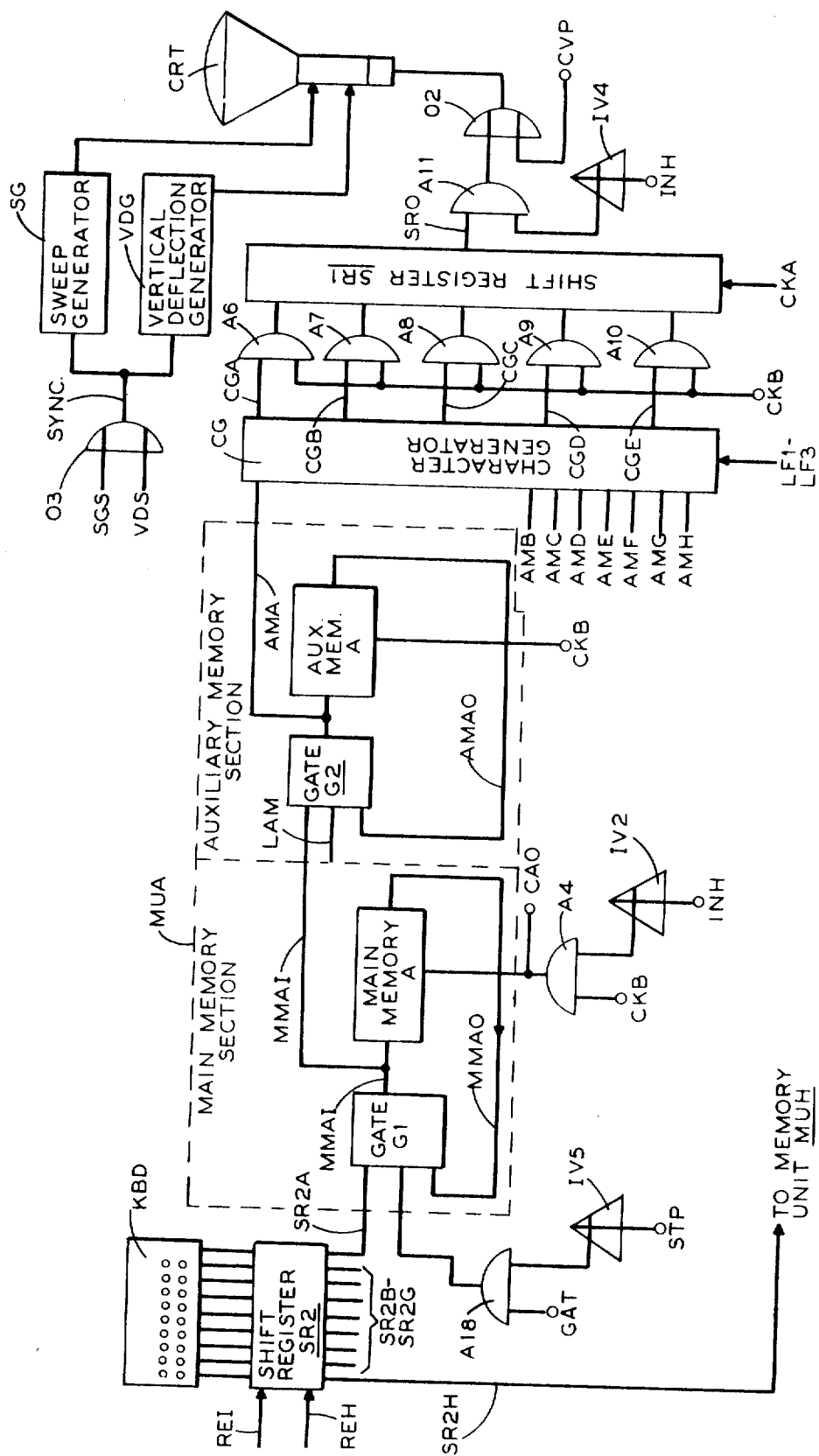


FIG. 5
GATE G2

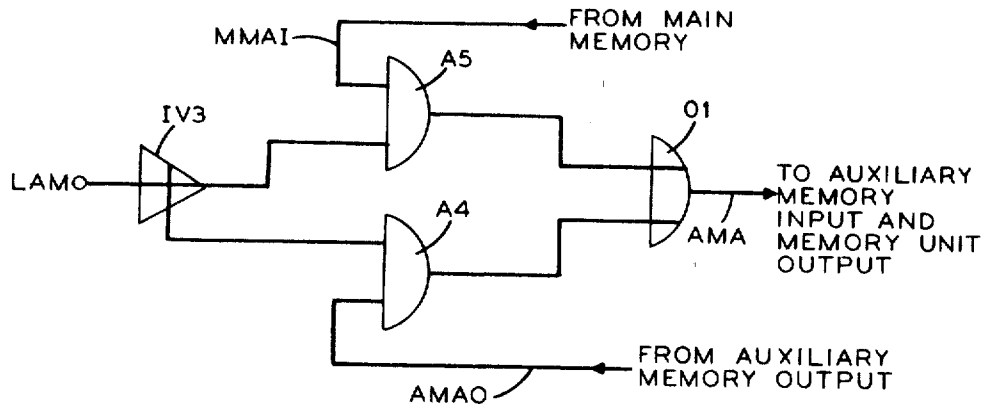


FIG. 6
CURSOR CONTROL CIRCUITS

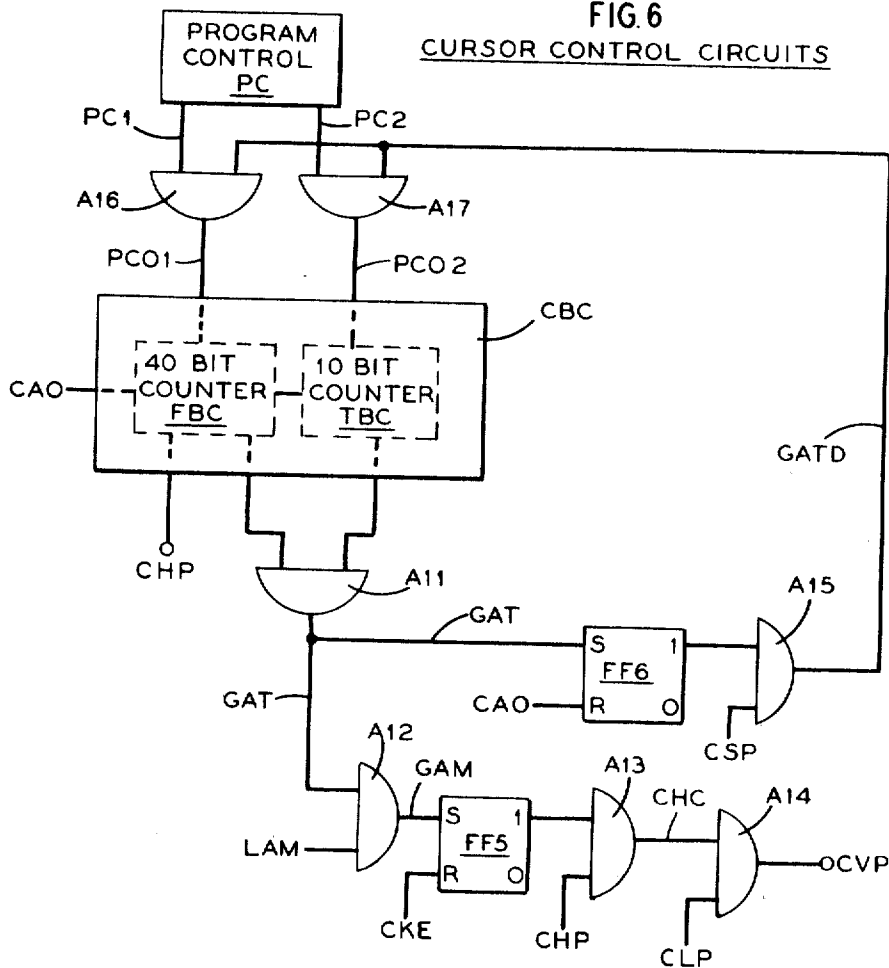


FIG. 7
FOR REMOTE TRANSMISSION OF MATERIAL

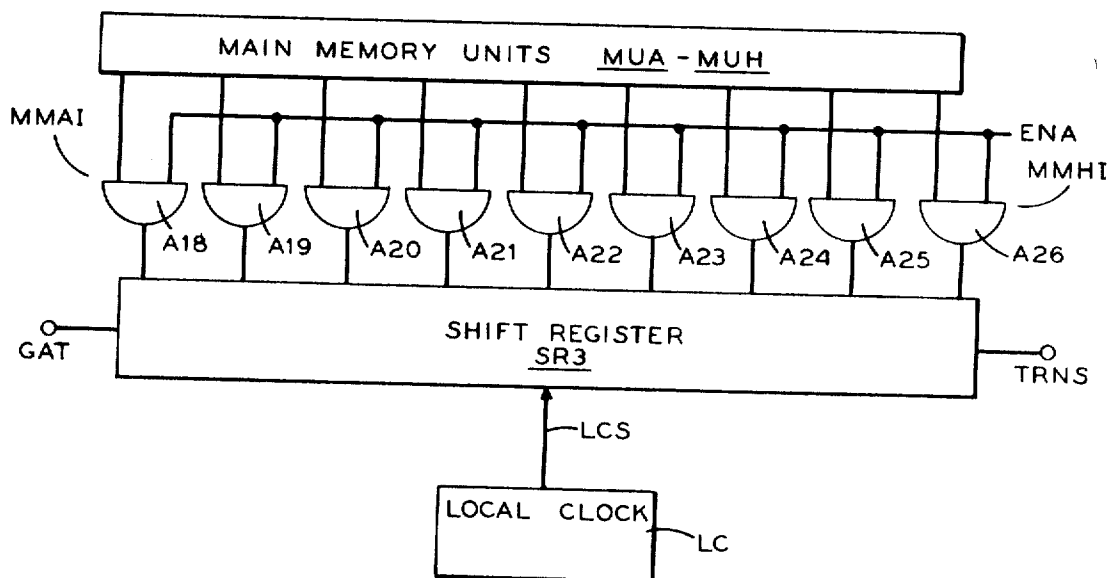
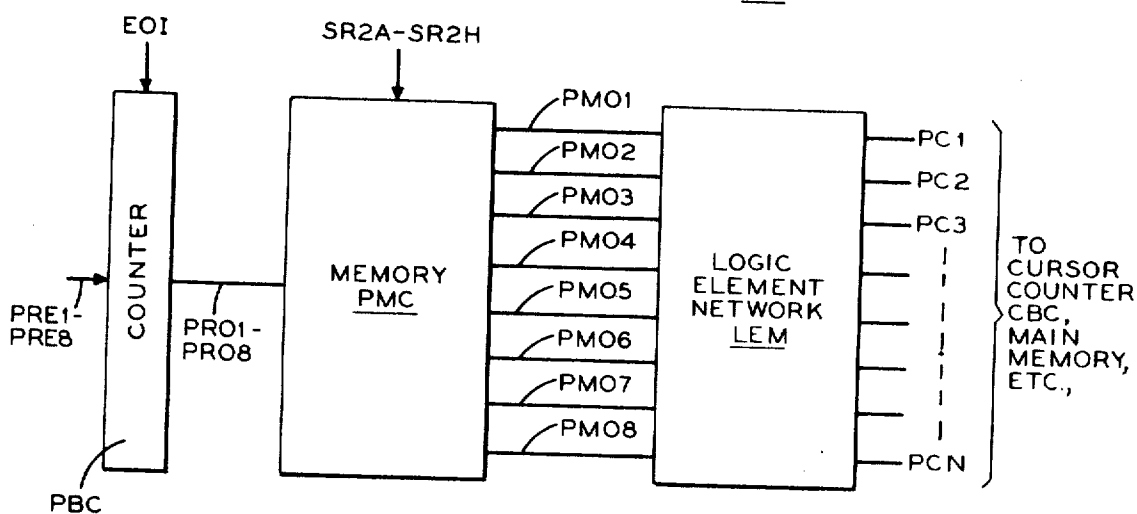


FIG. 8
PROGRAM CONTROL PC



INFORMATION DISPLAY SYSTEM

This invention relates generally to a display system and, more particularly, pertains to visual display terminal equipment which may be associated with data processing systems.

An information display system of the type under consideration receives coded information, usually in digitally or binary encoded form, from an information source such as a computer, a keyboard, a recording or the like, and presents the same in human readable form on a display device which may comprise the screen of a cathode-ray tube. Such display systems are gaining widespread use because, for example, an operator can view a message and correct any errors before transmitting the information to a remote receiver. At present, there are a number of such display systems available; however, these systems usually have a number of disadvantages associated with their use.

To be more specific, in display systems employing a cathode-ray tube each individual scan of the electron beam across the face of the tube produces a slice of each character in a text line. Hence, the signals representing the characters comprising a text line must be presented to a video decoder sequentially. Additionally, since each text line comprises a number of such scans, the sequential character signals must be repeated cyclically until the electron beam has traced out a complete text line. Present techniques include the use of a recirculating delay line memory to effect the sequential and cyclical presentation of such character signals to the video decoder. However, delay line memory units of the type described are costly and complex. Of more import is the fact that they require the use of sophisticated external circuits for proper operation.

In order to ameliorate the above situation, it has been proposed to replace such delay line memory units with core or random access memories. However the use of such devices becomes prohibitively expensive.

Accordingly, a primary object of the present invention is to provide an improved information display system.

A more specific object of this aspect of the invention resides in the novel details of the elements which provide an information display system of the type described wherein a plurality of shift registers comprise the circulating memory unit. The shift registers provide a reliable and inexpensive memory in which data may be stored.

A further object of this aspect of the invention is the provision of an information display system which includes a memory unit which is easily fabricated and is specifically adapted for modern mass production techniques.

As noted above, in information display systems of the type under consideration, the signals representing the characters in the memory unit must be presented to the video decoder sequentially and cyclically for a number of scans of the electron beam of the cathode-ray tube which are required to produce a text line. Where only one text line is to be produced, a single memory unit is used to recirculate the signals representing the characters for the requisite number of scans. However, a problem is presented when it is desired to simultaneously display more than one text line. Proposals have been made to simply provide a memory unit for each text line. Thus, if a text line comprises 32 characters of 6-bits per character and it is intended that 10 text lines be displayed, then the complete memory would include 10 individual memory subunits each comprising six storage devices of 32 character lengths. It is obvious that such a system is unwieldy and expensive.

Accordingly, an object of another aspect of the invention is to provide a system of the type under consideration which includes a main memory for storing all the signals representing the characters to be displayed and an auxiliary memory for storing the signals representing the characters comprising the text line being scanned, thereby providing a relatively inexpensive, reliable and easily produced memory unit.

In order to control and/or synchronize the electron beam of the cathode-ray tube in the subject information display

systems, it has been proposed to include command signals in the memory unit. This procedure, of necessity, requires high capacity memory units to record both character and control signals and, in addition, requires complex circuits to decode the control signals and convert them into signals compatible for use with the cathode-ray tube control circuits.

Accordingly, an object of a further aspect of this invention is to provide an information display system wherein the memory unit stores signals representing only the characters to be displayed thereby substantially decreasing the need for high capacity memory units.

Another object of this aspect of the invention is to provide an information display system in which an electron beam synchronizing signal is derived from the clock circuits which control the memory unit thereby eliminating the need for sophisticated and expensive circuitry to decode stored command signals.

Accordingly, an information display system constructed according to the present invention is adapted to display information by the cyclic scanning of a writing means. The system comprises storage means for storing characters divided into sets of information bits wherein the storage means includes a main storage means for storing all of the sets of bits representing all of the characters to be displayed and auxiliary storage means for storing the sets of bits representing the characters to be displayed during a scan of the writing means and for sequentially presenting each set of bits at an output. Modulating means is connected to the output of the auxiliary storage means responsive to the set of bits appearing at said output for modulating the writing means to form areas of a character represented by the set of bits during the scanning of the writing means.

Additionally, a feature of this invention is the provision of microprogramming techniques to further increase the flexibility of the system.

Another feature of this invention is to provide an information display system which includes a display device having a moving cursor and a memory unit accessible in synchronism with the pattern of movement of the cursor wherein the cursor indicates the location at which information will change on the display device when applied to the memory unit from an input source such as a keyboard or a computer and the like.

Other features and advantages of the present invention will become more apparent from a consideration of the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIGS. 1A and 1B are illustrations showing the manner in which the character patterns are displayed on the display device forming a part of the present invention;

FIG. 2 is a general block diagram of an information display system constructed according to the present invention;

FIG. 3 is a detailed schematic block diagram of the clock circuits of the present invention;

FIG. 4 is a detailed schematic block diagram of the memory and video portion of the present invention;

FIG. 5 is a detailed logic diagram of the gate arrangement shown in FIG. 4;

FIG. 6 is a schematic block diagram of the cursor control circuits shown in FIG. 2;

FIG. 7 is a schematic block diagram of an arrangement for the transmission of information to a remote station; and

FIG. 8 is a detailed block diagram of the program control shown in FIG. 6.

INTRODUCTION

In general, an information display system constructed in accordance with the present invention includes a display device such as a conventional cathode-ray tube having an electron beam which is adapted to move across the face or screen of the tube in the conventional manner and to illuminate various portions of the tube face or screen in accordance with an input modulating signal. Each horizontal movement of the electron

beam across the tube face, which is referred to as a scan line or scan, will produce a slice of the characters to be generated in a text line. For example, referring to FIG. 1B, which illustrates an enlarged section of a cathode-ray tube CRT face, it is noted that the electron beam must make 21 vertically displaced scans across the face of the tube CRT to produce a single line of text. The first seven lines of the scan are usually blank, portions of the next seven scan lines are illuminated in accordance with the character to be generated, and the remaining seven scan lines are also blank. The blank scan lines are provided to space one text line from the succeeding or preceding text line. The characters comprising a text line are produced by causing the electron beam to make a plurality of dots on the face of the tube. Each character in the text line is 10 dots or units wide. The first three dots are blank. The next five dots are illuminated in accordance with the character to be generated, and the next two dots are blank. The three blank dots and the two blank dots are utilized to space one character from the preceding and succeeding characters so each is spaced from an adjacent character by five dots.

As shown in FIG. 1A, the display system of the present invention is adapted to generate 10 lines of text across the screen of the tube CRT. Additionally, each line of text comprises 40 characters of the type shown in FIG. 1B. Moreover, the electron beam is adapted to sweep out 260 scan lines across the face of the tube.

It is emphasized that the quantities noted above (i.e., the number of scan lines per text line, the total number of text lines, etc.) are for illustrative purposes only and are not to be interpreted as being a limitation of the present invention. That is, the different quantities may be varied so that, for example, each text line comprises 42 scan lines of 10 characters per text line. Alternatively, the scan lines may be generated in the vertical direction rather than in the horizontal direction.

DESCRIPTION OF THE SYSTEM

In the description of the system the following conventions will be employed:

1. Each signal line has a reference character equal to the signal designation; i.e., the CKA signal line carries the CKA signal;
2. When a signal is being generated it is considered present and equivalent to logical 1 or +. On the other hand, when a signal is not being generated, it is considered absent and equivalent to logical 0 or -;
3. The signals transmitted throughout the system fall into two classes:
 - a. pulses such as the CKB pulses of short duration, and
 - b. signals such as INH signal of long duration, generally generated by a bistable device;
4. Throughout the description terminology such as "words or digits are transferred" is employed; it should be understood that binary coded combinations of signals or sets of bits representing the words or digits are actually transferred;
5. Words are usually transferred through the system with their bits in parallel. For example, a word is transferred from scan line counter SLC on the LFS1, LFS2, and LFS3 signal lines. However, to simplify the block diagrams, these three signal lines are generalized into a single line LFS1-LFS3 which implies a cable of at least three signal lines. From the range of numbers in the signal character it is immediately known what the minimum number of signal lines are in the cable;
6. Terminology such as "setting a flip-flop" means switching or triggering it to its on or 1 state wherein it generates a signal such as INH; and "unsetting" or "resetting a flip-flop" means switching it to its off or 0 state;
7. The terminology "character" is used to indicate a letter, a numeral, or a symbol such as an ampersand and the like.

GENERAL SYSTEM DESCRIPTION

FIG. 2 illustrates, in generalized form, an information display system constructed according to the present invention. Accordingly, the display system includes a memory having a main recirculating memory which stores, in sequential order, the words or sets of bits representing all of the characters which are to be produced on the screen of the tube CRT during any one picture frame. The words are recirculated through the main memory so that any one word is presented at the output of the main memory once during each cycle. Additionally, the memory includes an auxiliary recirculating memory which is adapted to store and recirculate the words representing the characters to be produced in any one text line. Similarly to the main recirculating memory, the words in the auxiliary recirculating memory are cyclically available at the output thereof. The output of the auxiliary recirculating memory is connected to the video circuits which operate upon the words representing the characters which are presented at the output of the auxiliary recirculating memory and converts these words into control signals for the cathode-ray tube CRT to reproduce the character on the face of the screen. In practice, the main recirculating memory and the auxiliary recirculating memory comprise shift registers which are adapted to store the words representing the characters or character words in individual cells and to move the words from cell to cell under the control of the clock circuits.

In the present embodiment, the auxiliary recirculating memory recirculates 40 words comprising a text line of characters for a total of 21 cycles corresponding to the 21 scan lines per text line of the display device or cathode-ray tube CRT. At the end of the 21 cycles, the clock circuits cause the next 40 words or sets of bits representing the following text line of characters to be loaded from the main recirculating memory into the auxiliary recirculating memory. Thus, these newly entered words recirculate in the auxiliary recirculating memory for a total of 21 cycles and the procedure is again repeated to load into the auxiliary recirculating memory, from the main recirculating memory, the next succeeding 40 words representing the characters comprising the next succeeding line of text.

A moving cursor or trace is also produced on the face of the tube CRT to indicate the character location at which new information will appear when it is introduced into the memory. The cursor is controlled by the cursor control circuits. Thus, if it is desired to introduce a new character from a source such as the keyboard arrangement or a magnetic tape source (not shown) or the like, the cursor control circuits enable the main recirculating memory to receive the new word at a point in the cycle of the main recirculating memory corresponding to the particular character location on the face of the tube CRT which is flagged by the cursor.

Additionally, a program control (not shown in FIG. 2) is provided to cause various portions of the system to perform various functions.

DETAILED DESCRIPTION OF THE CLOCK CIRCUITS (FIG. 3)

The clock circuits shown in FIG. 2 are illustrated in detail in FIG. 3. Where a particular counter is to produce a pulse, such as the CSP pulse, when the counter has reached a predetermined count, it is to be understood that the appropriate outputs of the individual registers in the counter are connected to an AND gate so that when the particular count is reached, all inputs to the AND gate will be energized whereby the AND gate produces the particular output pulse.

The clock circuits include a clock CK which may be a crystal controlled oscillator and, in the particular example under consideration, produces a 7 MHz./s signal. The clock CK produces an output signal CKA which is applied to the input of a dot counter DC. The dot counter is a conventional counter and produces one output pulse CKB in response to 10 input CKA pulses. The dot counter determines the width of a

particular character on the screen of the tube CRT which, as noted in the description of FIG. 1, is 10 dots wide.

Additionally, the dot counter DC produces a cursor strobe pulse CSP when the counter reaches a count of five.

The output pulses CKB of the dot counter DC are applied to the input of a character counter CC. For every 50 input CKB pulses the character counter CC produces one output pulse CKC. The character counter CC determines the number of characters appearing in a text line. The first 40 CKB pulses applied to character counter CC represent the 40 characters appearing in a text line. The remaining 10 pulses required to reach a count of 50 occupy a time interval which is equal to the time interval required for the retrace of the electron beam between scan lines in the tube CRT. Thus, a pulse CKC will be produced at the completion of each scan line or scan including the retrace time. However, as used herein, the word scan includes retrace time unless otherwise noted.

The character counter CC produces a pulse INS when the counter reaches a count of 40, representing completion of the sweep of the electron beam through the 40 characters comprising a text line. The pulse INS is applied to the set terminal S of a bistable device or flip-flop FF1 to set the flip-flop. Accordingly, the flip-flop produces an INH signal at its 1 output terminal when it is moved to the set state. The flip-flop is reset by the CKC pulse so that the INH signal is present only during the last ten CKB pulses.

The output of the character counter CC is connected to one input terminal of an AND gate A1. The output terminal of the gate A1 is connected to the input terminal of a scan line counter SLC. The scan line counter SLC produces one output pulse CKD in response to 21 input pulses CKC. (For the present, it is assumed that the other input terminal of the AND gate A1 is energized or enabled so that that CKC pulses pass through the gate A1 to the counter SLC.) The scan line counter SLC essentially counts the number of scans of the electron beam in the tube CRT and produces a pulse CKD after a text line comprising 21 such scans has been completed. (For ease of reference, a scan line is assumed to include the retrace time, as noted above).

Additionally, the scan line counter SLC is adapted to produce a load auxiliary memory pulse LAM when the first CKC pulse during a counting cycle is received by the counter. The scan line counter also produces line finder signals LFS1—LFS3. The signals LFS represent a 3-bit code to designate which particular slice of the characters are being scanned through by the electron beam. To be more specific, the characters occupy scan lines 8—15 in the text line as shown in FIG. 1B. The signals LFS1—LFS3 indicate which one of the scan lines 8—15 the electron beam is tracing through at that particular moment.

The scan line counter SLC also produces a pulse CLP representing the cursor line position pulse. This pulse is produced when a count of 17 has been reached so that the cursor is produced in the seventeenth scan line of the text line or, in other words, the cursor trace appears two scan lines below the particular character with which it is associated.

The output of the scan line counter SLC is connected to the input of a text line counter TLC. The text line counter is a conventional counter and is adapted to produce one output pulse CKE in response to 12 input CKD pulses. Although only 10 text lines are produced on the screen of the tube CRT the text line counter TLC counts 12 CKD pulses to compensate for the blanking period during the retrace of the electron beam. The reason for this operation will become apparent from a consideration of the description of the memory circuits of the present invention hereinbelow.

As noted hereinabove, the information display system of the present invention is adapted to be utilized in conjunction with a conventional cathode-ray tube CRT. In practice, 260 scan lines are produced across the face of the tube for each picture frame. However, it is to be noted that the pulse CKE is produced after 12 times 21 or 252 scan lines have been counted.

To have the first line of characters properly displayed at the initiation of each scan, it is necessary that the main memory recirculate an integral number of cycles for each complete scan of the cathode-ray tube CRT. In the example under consideration, the main memory completely recirculates or completes a cycle every 10 scan lines. Assuming that vertical blanking at the top and bottom of the scan occupies an additional 5 times 10 text lines, then there are $10 \times 21 + 5 \times 10$ or 260 scan lines produced during one picture frame. Thus, to synchronize the clock circuits with the electron beam and the memory unit, an additional eight scan lines are counted after the CKE pulse is produced so that the total scan line count is $252 + 8$ or 260.

To be more specific, in order to synchronize the operation of the clock circuits with the electron beam of the CRT, an auxiliary scan line counter is utilized to count an additional eight scan lines after the pulse CKE has appeared. More particularly, the output terminal of text line counter TLC is connected to the set terminals of a flip-flop FF2. The 1 output terminal of the flip-flop FF2 is connected to one input terminal of an AND gate A2. The other input terminal of the AND gate A2 is connected to the output terminal of the character counter CC so that the CKC pulses representing the completion of scan lines are applied to the AND gate A2. Accordingly, when the CKE pulse is produced, the flip-flop FF2 is set to energize one terminal of the AND gate A2. Thereafter, as the pulses CKC appear at the other terminal of AND gate A2, they are applied to an auxiliary scan line counter ASLC which is connected to the output of the gate A2. The counter ASLC is a conventional counter and produces an output pulse RES when eight pulses have been counted. Additionally, the 1 output terminal of the flip-flop FF2 is connected to the input terminal of an inverting or paraphase amplifier IV1, the inverting output terminal of which is connected to the other terminal of the AND gate A1. Thus, when the flip-flop FF2 is set, the AND gate A1 will be disabled and no further pulses will pass through to the scan line counter SLC.

When eight scan lines have been counted by the counter ASLC, the output pulse RES produced by this counter will be applied to the reset terminal R of the flip-flop FF2 to reset the flip-flop so that the 1 output signal is removed. Accordingly, the terminal of AND GATE A1 which is connected to the inverting amplifier IV1 will again be energized so that pulses CKC will pass through to scan line counter SLC.

A synchronizing pulse SYNC is applied to the vertical deflection generator and the sweep signal generator to synchronize the movement of the CRT electron beam with the operation of the clock circuits in the conventional manner. The SYNC pulse is derived from the character counter CC and the auxiliary scan line counter ASLC. More specifically, a pulse SGI, which may be produced during the last 10 counts of the character count CC (i.e., during the electron beam retrace period) is applied to the S terminal of a flip-flop FF3 to produce the SGS signal at the 1 output thereof. Additionally, the character counter CC produces an SGF pulse after the SGI pulse but before the next occurring CKC pulse which is applied to the R terminal of flip-flop FF3 to reset flip-flop FF3.

Similarly to the character counter CC, the auxiliary scan line counter ASLC produces a VDI pulse during the eight scan line count which is applied to the S terminal of a flip-flop FF4 whereby a VDS signal is produced at the 1 output. The auxiliary scan line counter ASLC also produces a VDF pulse after the VDI pulse but before the RES pulse which is applied to the R terminal of FF4 to reset flip-flop FF4.

As shown in FIG. 4, the VDS and the SGS signals are applied to respective terminals of an OR gate 03, the output of which is the synchronizing pulse SYNC, thereby to synchronize the operation of the tube CRT with the other elements of the system.

DETAILED DESCRIPTION OF THE MEMORY (FIG. 4)

In the present embodiment, each character is represented by an 8-bit word or set of eight information bits. The first 6 bits are utilized to designate the particular character which is to be produced on the face of the tube CRT. The seventh bit may be used for parity purposes and the eighth bit in the word may be used as a command signal, for example, to produce a reverse field effect on the screen of the cathode-ray tube or to denote that the character is not to be erased. Accordingly, there is provided eight identical memory units MUA—MUH which produce the signals AMA—AMH at their respective outputs. Each one of the signals AMA—AMH represents a bit in the 8-bit word noted above so that the signals AMA—AMH taken in parallel form one word. Since each of the memory units MUA—MUH is identical, only the memory unit MUA is shown and described in detail.

The memory unit MUA comprises a Main Memory Section and an Auxiliary Memory Section. The Main Memory Section includes Main Memory A which, in practice, comprises a shift register having provision to store 400 bits of information, each bit comprising one bit of the word representing the characters which are to be produced across the face of the tube CRT during any one picture frame. That is, as noted above, each line of text displayed comprises 40 characters and, since there are 10 lines of text which are displayed during a picture frame, the tube CRT can display 400 characters at any one time. Hence, Main Memory A stores 1 bit of the words representing all of the characters which may be displayed at any one time. It is to be noted that if the capacity of the tube CRT is changed, then the capacity of the Main Memory A will likewise be changed so that the Main Memory A stores as many word bits as the number of characters which may be displayed during a picture frame.

The output terminals of the Main Memory A is connected to the input of gate G1 via an MMAO signal lead. The output of gate G1 is connected to the input terminals of Main Memory A via an MMAI signal lead. The shift terminal of Main Memory A is connected to the output of an AND gate A4 which produces a shift pulse CAO when the input terminals of the gate are enabled. One input terminal of the AND gate A4 is connected to receive the pulse CKB. The other terminal of AND gate A4 receives an inverted INH signal via an inverting or paraphase amplifier IV2. Thus, when the INH signal is absent and a CKB pulse is received, a shift pulse CAO will be gated to the shift terminal of Main Memory A thereby causing the shift registers in Main Memory A to shift the information therein on position. Under normal conditions, the lead MMAO is connected to the lead MMAI through the gate G1. Thus, the output signal MMAO is applied directly to the input of the Main Memory A via the lead MMAI to provide a recirculating memory.

That is, when the signal leads MMAO and MMAI are connected together through the gate G1, the signal appearing at the output of Main Memory A is applied directly to the input of the Main Memory. When the next shift pulse CAO occurs, the next signal appearing at the output of Main Memory A is similarly applied to the input thereof so that the signals recirculate through the main memory. Moreover, since the AND gate A4 produces a shift pulse only during the time that characters are presented on the face of the CRT and not during retrace, it will be obvious that each word bit representing a character will be produced at the output (input) of the Main Memory in synchronism with the information producing movement of the electron beam.

The Auxiliary Memory Section includes an Auxiliary Memory A which comprises a 50-bit shift register. The Auxiliary Memory A is adapted to store the 40 word bits associated with the characters in a line of text and, in addition, contains 10 blank cells. The output of the Auxiliary Memory A is connected to the input terminal of a gate G2 via the signal lead AMAO. The output of gate G2 is connected to the input terminals of Auxiliary Memory A via the lead AMA.

Under normal operating conditions, the signal AMAO is connected through to the signal lead AMA via the gate G2. Accordingly, the output signal appearing at the output terminals of Auxiliary Memory A will be applied to the input thereof in a manner similar to the operation of Main Memory A. The shift pulse CKB is applied to the shift terminal of Auxiliary Memory A so that for each shift pulse received, the word bit appearing at the output will be applied to the input of Auxiliary Memory A thereby to provide a recirculating auxiliary memory. Additionally, this same output-input signal will appear at the output of memory unit MUA via the AMA lead.

It is to be noted that the Auxiliary Memory A is shifted by the CKB pulses and that 50 CKB pulses are required to produce a CKC pulse representing the completion of a scan line. Thus, the reason for providing 10 blank positions in the auxiliary memory will not become apparent. That is, during the first 40 CKB pulses the word bits associated with the characters appear on the lead AMA. However, during the last 10 CKB pulses, which occur during retrace of the electron beam, the 10 blank positions appear on the output lead AMA. Thus, when the next scan line begins, the Auxiliary Memory A will produce the word bit associated with the first character to be reproduced on the screen of the tube CRT so that the Auxiliary Memory is maintained in synchronism with the electron beam.

Additionally, it is to be noted that the Main Memory A does not include any blank positions but the Main Memory is not shifted during the occurrence of the last 10 CKC pulses. Thus, the Main Memory will be maintained in synchronism with the auxiliary memory. Furthermore, since the respective shift pulses CAO and CKB are applied to the respective main and auxiliary memory portions of each of the memory units MUA—MUH simultaneously, it will be obvious that each memory unit will be stepped or shifted in synchronism with each other memory unit so that all eight bits representing a character will be presented in parallel to a character generator CG via the signal leads AMA—AMH.

Summarizing the above, the auxiliary memory stores 40 characters and the main memory stores 400 characters. To put this another way, the auxiliary memory may be thought of as storing M (N) characters whereby the main memory therefore may be thought of as storing M (N+X) characters where M is greater than one and N and X are greater than zero.

A feature of the present invention is to fabricate the main and auxiliary memories of each of the memory units MUA—MUH from shift registers thereby to provide a device which is ideally adapted for large scale integration techniques. Hence, the memory units may be manufactured relatively easily and cheaply. Additionally, these memory units are flexible in operation.

As noted in the description of the clock circuits, the LAM pulse is produced at the initiation of the first scan line by the scan line counter SLC and has a duration which is equal to the time that is required for the electron beam to trace through the first scan line of a text line plus the retrace time. During the time interval that the LAM pulse is present and applied to gate G2, the connection between the AMAO lead and the AMA lead is broken and a connection is made between the MMAI and the AMA lead. Thus, as the shift pulses CAO and CKB occur, the word bit entering the Main Memory A will also enter Auxiliary Memory A and will appear on the output lead AMA.

To be more specific, FIG. 5 illustrates an embodiment which the gate G2 may take. Accordingly, there is provided an inverting or paraphase amplifier IV3 which receives the pulse LAM at the input terminals thereof. The inverting output terminal of the amplifier IV3 is applied to one input terminal of AND gate A4. The other terminal of AND gate A4 receives the AMAO signals from the output of Auxiliary Memory A. The output terminal of gate A4 is connected to one input terminal of OR gate O1, the output terminal of which is connected to the input terminal of Auxiliary Memory A via the signal lead AMA. The noninverting output terminal of ampli-

er IV3 is connected to one input terminal of an AND gate A5. The other input terminal of the gate A5 is connected to the Main Memory A signal lead MMAI. The output terminal of the AND gate A5 is connected to another input terminal of OR gate 01.

In operation, when the LAM pulse is absent, signals will be passed to the input terminal of the Auxiliary Memory A from the lead AMAO, gates A4 and 01 to produce the recirculating auxiliary memory noted above. However, when the LAM signal is present, thereby signifying that the Auxiliary Memory A is to be loaded from the Main Memory A, the MMAI signals will be passed through the AND gate A5 and OR gate 01 to the input terminal of the Auxiliary Memory A thereby to load the same. Simultaneously therewith, the same signal will appear at the output of memory unit MUA via the AMA lead.

The LAM pulse occurs once during every 21 scans of the electron beam. During the presence of the LAM pulse 40 CAO shift pulses will occur so that the 40 bits associated with the characters to be produced in the text line will be loaded into Auxiliary Memory A. Moreover, these data bits will recirculate through Auxiliary Memory A for 21 cycles. Hence, the data bits associated with the characters comprising a text line will be available on the AMA signal lead sequentially and cyclically for a total of 21 cycles.

After the electron beam has traced through the 21 scan lines comprising a text line, the LAM pulse again will be present so that the Auxiliary Memory A may again be loaded from the Main Memory A.

Since the Auxiliary Memory A stores 40 bits of information or data and the LAM pulse is present during only 40 CAO shift pulses, the full text line of word bits will be introduced into the Auxiliary Memory A. Any one particular bit in Auxiliary Memory A will be shifted a total of 50 times during any one scan line while a bit in the Main Memory A will be shifted a total of 40 times. Since the memories go through 21 cycles, a bit in Main Memory A will be shifted a total of 21×40 or 840 times during the generation of a text line on the face of the tube CRT. Since the Main Memory A stores only 400 bits of data, it will be obvious that when the LAM pulse again appears after the twenty-one scan lines, the information which is now loaded into the Auxiliary Memory A will correspond to the next line of text to be displayed.

Accordingly, another feature of the invention is the provision of an auxiliary memory section which recirculates the information required for the generation of a text line during the scanning of the text line thereby to eliminate the need for repetitive main memory sections for each line of text and to produce an extremely fine display without substantially increasing the storage capacity of the memory units.

VIDEO CIRCUITS (FIG. 4)

The video circuits include the character generator CG. The character generator CG may be a read-only memory which coordinates the parallel input signals AMA—AMH at its input terminals with the LFS1—LFS3 signals indicating the particular line being scanned and produces parallel output signals on the signal leads CGA—CGE, respectively, representing, in binary form, the portions of the scan line which are to be illuminated by the electron beam. To be more specific, the signals AMA—AMH indicate the particular character to be reproduced on the face of the tube CRT. The LFS1—LFS3 signals indicate the particular line being scanned. These signals cause the memory to read out on the leads CGA—CGE signals representing the slice of the character to be produced on the screen of CRT in binary form. Moreover, these CGA—CGE signals will change 40 times during each scan line in accordance with the signals AMA—AMH associated with the memory units MUA—MUH so that all 40 characters will be produced on the screen of the tube CRT during the generation of a text line. It is to be noted, however, that the character generator CG will not produce output signals during the first seven and last seven scan lines as noted above in the discus-

sion of FIG. 1B since the signals on leads LFS1—LFS3 will be interpreted to indicate that no signals are to be produced during these scans.

The leads CGA—CGE are individually connected to an input terminal of the respective AND gates A6—A10. The other input terminal of the AND gates A6—A10 are adapted to receive the CKB pulses. The output terminals of the AND gates A6—A10 are connected to particular registers in a 10-bit shift register SR1 having a parallel preset input and a serial output.

More specifically, the output terminals of the respective AND gates A6—A10 are connected to the registers of the shift register SR1 so that the signals appearing at the output terminals of A6—A10 will be applied to the fourth through eighth cells in the shift register. The first three cells and the last two cells of the shift register SR1 are always left blank. Pulses CKA are applied to the shift terminal of the shift register SR1 to serially shift the information in the register to the output lead SRO. The output lead SRO is connected to one terminal of an AND gate A11. The other terminal of the gate A11 is connected to the inverting terminal of an inverting amplifier IV4, the input terminal of which is adapted to receive the INH signal. Thus, if the INH signal is absent, the SRO signal will be gated to the cathode or grid of the cathode-ray tube CRT through an OR gate 02. When the INH signal is present, as during the blanking or retrace period, the AND gate A11 is disabled thereby preventing the passage of any SRO signals.

Each CKA signal represents a dot or unit of a character, a character being ten dots wide. Thus, since the first three cells in shift register SR1 are empty, the first three SRO signals during the generation of a character will be blank. The next five SRO signals will represent the slice of the character being generated and will modulate the electron beam to produce an area of the character. Thus, if a 1 signal appears on the lead SRO, the electron beam will produce a dot. However, if a 0 signal appears on the lead SRO during these next five CKA shift pulses, the electron beam will not illuminate the screen of the CRT. The remaining two blank cells will be shifted out by the last two CKA pulses to produce the space of two dots on the screen, as noted above in conjunction with the description of FIG. 1B.

DETAILED DESCRIPTION OF KEYBOARD ARRANGEMENT

The keyboard arrangement includes a standard keyboard KBD which is adapted to produce signals representing the particular characters to be entered into the memory units MUR—MUH or command signals for the program control. In practice, the keyboard KBD is adapted to represent the character in binary form utilizing the standard ASCII code (the latter referring to the American Standard Code for Interchange of Information recommended by the IEEE). The ASCII code represents a character by a 7-bit word. However, as noted above, in the present system the video portion of the character is represented by a 6-bit code with the two other bits of the word representing other information. Thus, the first bit is removed in the word representing the character struck on the keyboard KBD and two other bits of information are added by the keyboard. The output of the keyboard is applied to a parallel or serial-input parallel-output 8-bit shift register SR2. That is, information may be introduced into the shift register SR2 in either parallel form or serial form depending upon the source of information.

For example, when information is entered into the shift register SR2 from the keyboard KBD, the information is entered in parallel. However, the serial input of the shift register SR2 may be connected to a remote line so that information may be transmitted in serial form from a remote computer, magnetic tape, or the like, to the information display system of the present invention. Thus, the REF pulses which are applied to the serial input of shift register SR2 represent such serial infor-

mation. A shift pulse REH, which may be produced from a local clock or the like is used to shift the information pulses REI in shift register SR2.

The output terminals of the shift register SR2 are individually connected to respective gates G1 of each of the memory units MUA—MUH via the respective leads SR2A—SR2H.

The gate G1 is similar in construction to the gate G2 shown in detail in FIG. 5. However, the input lead of the gate G1 is connected to the output of an AND gate A18, an input terminal of which receives a GAT pulse from the cursor control circuits shown in FIG. 6. The other input terminal of the gate A18 is connected to the inverting terminal of an inverting amplifier IV5, the input terminal of which receives an STP signal from the program control.

During normal operation, in the absence of the GAT pulse and the STP signal, the signals appearing at the output of Main Memory A are circulated back to the input of the Main Memory A. However, when the GAT pulse is present and the STP signal is absent, the gate G1 passes the signal on lead SR2A to the input of Main Memory A so that the information in Main Memory A is updated.

The STP signal is generated by the program control, in the manner noted below, so that when the STP signal is present, the AND gate A18 is disabled. Hence, no character recorded in the memory can be erased or changed even though the GAT pulse is applied to the gate A18. Alternatively, the STP signal may be generated by setting a flip-flop by manually operating a switch on the keyboard KBD to protect the words or sets of bits in the memory.

DETAILED DESCRIPTION OF THE CURSOR CONTROL CIRCUITS (FIG. 6)

The cursor control circuits are illustrated in FIG. 6 and function to produce a trace or cursor on the face of the screen of the CRT at the point that new information will appear on the screen. The particular form of the cursor is a line which is spaced below the character occupying the position at which the new information will appear or is simply an underline if no character occupies that particular position.

The cursor control circuits include a 400-bit binary counter CBC which counts the CAO pulses applied to its count input. Additionally, the counters may be preset to a specific count or may be incremented or decremented in accordance with signals appearing on the leads PCO1 and PCO2. Since the counter CBC is driven by the CAO pulses, it will be obvious that the cursor counter will be stepped in synchronism with the Main Memory A and, therefore, the Auxiliary Memory A.

More particularly, the 400-bit counter CBC comprises a 40-bit binary counter FBC and a 10-bit binary counter TBC. The counters FBC and TBC are connected to the respective input terminals of an AND gate A11. Accordingly, when the counter CBC reaches a particular count both inputs of the AND gate A11 will be energized so that the gate will pass a GAT pulse. This GAT pulse will be produced once every 10 scan lines since the counter will have gone through a full cycle of operation during the 10 scan lines (i.e., 40 CAO pulses per scan line [representing the 40 characters per scan line] $\times$ 10 scan lines equals 400 CAO pulses). Additionally, when a particular count is reached by the 40-bit counter FBC, the counter FBC produces a CHP pulse. Moreover, the CHP pulse will be produced once during each cycle of the counter FBC so that the cursor counter CBC produces 10 CHP pulses for every GAT pulse produced since the 40-bit counter FBC goes through 10 cycles of operation during a 400-bit count of the counter CBC.

The GAT pulse is carried by the GAT signal lead which is connected to one input terminal of an AND gate A12, the other input terminal of which receives the LAM pulse. Since the LAM pulse is available only during the first scan line in a text line and the GAT pulse is produced once every 10 scan lines, the GAT and LAM pulses will coincide only during the

generation of the text line which includes the position to be identified by the cursor. The foregoing may best be understood by an example.

Thus, assuming that the cursor is to be displayed in the third text line, the LAM pulse will be available during scan lines 1, 22, 43, 54, etc. If it is assumed that the GAT pulse is produced during the third scan line on the face of the tube CRT, it will occur during scan lines 3, 13, 23, 33, 43, 53, etc. Thus, coincidence of the pulses GAT and LAM will occur during the generation of the first scan or scan line of the third text line and the gate A12 will pass a GAM pulse to the S terminal of a flip-flop FF5. The flip-flop FF5 is reset by the next occurring CKE pulse which is applied to its reset terminal R.

The particular position of the cursor once the text line has been selected by the GAT and LAM pulses is determined by the CHP and CLP pulses. Thus, when flip-flop FF5 has been set, a signal will appear at the 1 output to enable one input terminal of an AND gate A13 connected thereto. The gate A13 will pass a pulse CHC upon the occurrence of the CHP pulse which is applied to its other input terminal. As noted above, the CHP pulse is produced once every 40 CAO pulses and corresponds to the character position to be underlined by the cursor trace.

The CHC pulse is applied to one input of an AND gate A14, the other input of which receives the CLP pulse which is available during the generation of the seventeenth scan line. Thus, when the AND gate A14 is enabled by the CHC and CLP pulses, it passes the CVP pulse which is applied to the tube CRT through the OR gate O2 to modulate the electron beam whereby the cursor trace is produced on the screen.

As noted above, the GAT pulse is applied to the gate G1 (FIG. 4) of the memory so that the memory will be updated upon the occurrence of the GAT pulse. Since the Main Memory A is shifted by the CAO pulses which are counted by the cursor counter CBC, it will be obvious that the cursor will appear at the point at which new information will be entered into the memory.

The movement of the cursor on the face of the tube CRT is controlled by a program control PC which controls the state of the elements comprising the counter CBC. Thus, if it is desired to move the cursor one character position to the right on the screen after information has been entered into the memory, the counter CBC is decremented one count after the GAT pulse has been produced. For example, if the first GAT pulse is produced after 10 CAO pulses have been counted and the counter is decremented one count, the next GAT pulse will be produced after 400 plus 11 CAO pulses have been counted. This has the effect of moving the cursor one position to the right on the screen. If it is desired to move the cursor to the left, the counter CBC is incremented one bit by the program control PC.

More specifically, the GAT pulse is applied to the S terminal of a flip-flop FF6 to set the same. The flip-flop is reset by the next CAO pulse applied to its R terminal. The 1 output of FF6 is connected to one input terminal of an AND gate A15, the other input terminal of which receives the cursor strobe pulse CSP. When the gate A15 is enabled it passes an enabling pulse GATD to respective inputs of AND gates A16 and A17. The other input terminals of the respective AND gates A16 and A17 are connected to the program control PC via the respective leads PC1 and PC2. The output of the gates A16 and A17 are connected to the respective counters FBC and TBC via leads PCO1 and PCO2, respectively, so that these counters may be updated when the gates A16, A17 are enabled.

Thus, if the cursor is to move to the right one position when new information is introduced into the memory, the program control will produce signals which will cause the counter CBC to decrement 1 bit when the control PC is connected through to the counter CBC upon occurrence of the enabling pulse GATD.

Alternatively, the leads PCO1 and PCO2 may comprise cables of leads so that signals appearing on the leads will preset a

will be serially applied to the output terminal via the lead TRNS which, in turn, may be connected to the local telephone lines via a data phone or the like so that the information may be transmitted to a remote point.

APPENDIX

AND gates used throughout the system are of the coincidence type, which may, for example, comprise a crystal diode network which functions to receive input signals via a plurality of input terminals and to pass an output signal when, and only when, input signals are present at each one of its input terminals.

The OR gate for circuits used throughout the system may be crystal diode networks which function to pass a signal received at any one of its input terminals to its output terminal. Although it is not always shown that the output of the AND gates and the OR circuits are fed through amplifiers, it is possible that noninverting conventional direct-current amplifiers may be connected to the output of these units whenever power amplification is required. In some cases, when both the signal and its inverse are simultaneously required, it is then desirable to employ conventional paraphase direct-current amplifiers to perform the required operation. In some instances, throughout the system, only the inverse of signals are required. Accordingly, the amplifiers would be conventional signal inverters for inverting direct-current signals.

The flip-flops employed throughout the system are conventional flip-flops having a set input S, a reset input R, a one's output 1 and a zero's output 0. When the flip-flop receives a signal at the set input S, it transmits a signal from its one's output 1. When the flip-flop receives a signal at its reset input R it is cleared and transmits a signal from its zero's output 0.

The counters employed throughout the system are conventional binary counters having a count input, a clear input R, a one's output 1 and a zero's output 0. Each time the counter receives a signal at its count input, it changes states. For example, if the counter is initially cleared by a signal at its clear input R, its zero's output 0 transmits a signal and its one's output 1 transmits no signal. When the first signal is received at its count input, the counter changes states wherein a signal is transmitted from its one's output 1 and no signal is transmitted from its zero's output 0. When the counter then receives another signal at its count input, it again changes stable states wherein the zero's output 0 transmits a signal and the one's output 1 also transmits a signal. For the sake of clarity throughout the disclosure, it should be noted that all of the counters and all of the flip-flops have an input (not shown) which is connected to an initial clear line so that at the start of operation all of the flip-flops and the counters are switched to their clear states; that is, all of their zero's outputs 0 are transmitting signals.

Further, since the various elements shown in system are made up of standard components, and standard assemblies, reference may be had to "High Speed Computing Devices," by the Staff of Engineering Research Associates, Inc. (McGraw-Hill Book Co., Inc. 1950); and appropriate chapters in "Computer Handbook" (McGraw-Hill, 1962) edited by Harvey D. Huskey and Granino A. Corn, and for detailed circuitry, to the examples in "Principles of Transistor Circuits," edited by Richard F. Shea, published by John Wiley and Sons, Inc. New York and Chapman and Hall, Ltd., London, 1953 and 1957. In addition, other references are: for system organization and components: "Logic Design of Digital Computers," by M. Phister, Jr., (John Wiley and Sons, New York); "Arithmetic Operations in Digital Computers," by R. K. Richards (D. Van Nostrand Co., Inc., New York). For circuits and details: "Digital Computer Components and Circuits," by R. K. Richards (D. Van Nostrand Co., Inc., New York).

While a preferred embodiment of the present invention has been shown and described herein it will become obvious that numerous omissions, changes and additions may be made in such embodiment without departing from the spirit and scope of the present invention.

I claim:

1. A display system for displaying at least two lines of characters on a medium which requires a plurality of scans of a writing means to produce each one of said lines of characters comprising, in combination, storing means for storing said characters as respective sets of information bits, and decoding means for converting the information bits in any one of said sets into signals for modulating said writing means to produce the character represented by said one set of information bits during said plurality of scans, said storing means comprising a first storage device having output terminals for storing the sets of bits representing the characters to be displayed and for producing said sets of bits at recurrent intervals at said output terminals, and a second storage device connected to said output terminals of said first storage device for storing the sets of bits representing the characters to be displayed in one of said lines and for sequentially applying the stored sets of bits in said second storage device to said decoding means during each one of said plurality of scans.

2. A display system as in claim 1, in which said second storage device includes input terminals and output terminals and is operable to recirculate the sets of bits stored therein and sequentially present each one of said sets of bits at said output terminals in response to a shift pulse, and shift pulse generating means for applying shift pulses to said second storage device.

3. A display system as in claim 2, in which said first storage device includes input terminals and is operable to recirculate the sets of bits stored therein and sequentially present each one of said sets of bits at said output terminals in response to a shift pulse, and connecting means for connecting said shift pulse generating means to said first storage device to apply said shift pulses to said first storage device.

4. A display systems in claim 3, in which said second storage device includes second storage gate means for normally connecting said second storage device output terminals with said input terminals and for connecting said second storage device input with said first storage device output terminals in response to a second storage load signal, and second storage load signal generating means responsive to the completion of said plurality of scans of the writing means for applying said second storage load signal to said second storage gate means.

5. A display system as in claim 3, in which said first and second storage devices comprise shift registers.

6. A display system as in claim 4, in which each of said lines comprises MN characters where M is greater than one and N is greater than zero, said second storage device being operable to store MN sets of bits, said first storage device being operable to store at least $M(N+X)$ sets of bits where X is greater than zero, said plurality of scans of said writing means being an odd integer, whereby a different set of bits are transferred from said first to said second storage devices at the completion of said plurality of scans.

7. A display system as in claim 4, in which one scan of said writing means occupies an interval equal to a preselected number of said shift pulses, said second storage load signal generating means including counting means for counting said shift pulses and for terminating said second storage load signal after a count has been reached which is equal to said preselected number.

8. A display system as in claim 3, and input means for producing and applying sets of bits representing respective new characters to said first storage device, said first storage device comprising first storage gate means for normally connecting said first storage device output with said input and for connecting said input means with said first storage device input in response to a first storage load signal, and first storage load signal generating means responsive to the movement of said sets of bits around said first storage device for generating said first storage load signal to enter a set of bits from said input means at a desired location relative to the other sets of bits recirculating through said first storage device.

9. A display system as in claim 8, and indicating means responsive to said first storage load signal for controlling said

count to cause the GAT pulse and cursor to appear at a particular desired located on the screen.

It is also to be noted that the above functions may be performed manually rather than utilize the program control PC. For example, if it is desired to move the cursor control backwards (to the left), a signal may be placed on the PC01 lead by the operation of a switch on the keyboard KBD such that the counter FBC is incremented one count when the pulse GATD is produced.

DESCRIPTION OF THE PROGRAM CONTROL (FIG. 8)

As noted above, the system of the present invention is specifically adapted for the use of microprogramming techniques thereby to provide an extremely flexible display terminal. More specifically, the program control Pc, which utilizes such microprogramming designs, is shown in FIG. 8 and comprises a counter PBC which may be a conventional 8-bit binary counter having a count input which receives EO1 signals and a preset input which receives PRE1—PRE8 signals to preset the count therein to produce a reselected coded combination of signals at the output. The output of the counter PBC comprises the parallel coded signals PRO1—PRO8.

Connected to the counter PBC is a conventional read-only memory PMC, which may be a core memory. In the example under consideration, the memory PMC stores 256 words each one of which is 8-bits long. The memory PMC includes a decoder which decodes the signals appearing on the leads PRO1—PRO8 to select one of the 256 words in the memory. The selected word appears on the output leads PMO1—PMO8 as parallel signals. As noted above, the memory PMC and the counter PBC are conventional in construction and are commercially available.

The output leads PMO1—PMO8 are connected to the input of a logic element network LEM which contains conventional logic elements, such as decoders and the like, which are responsive to the coded combinations of signals appearing on the leads PMO1—PMO8 to perform various functions, such as the following. It is to be noted that after each function has been performed the network LEM produces an EO1 pulse to increment the counter PBC to cause the program to go on to the next instruction.

EDIT GROUP

1. Move cursor forward one character position.
2. Move cursor backward one character position.
3. Move cursor up one text line.
4. Move cursor down one text line.
5. Move cursor to left-hand character position of text line.
6. Move cursor vertically to top of screen.

The above functions are easily performed simply by changing the count in the cursor counter CBC. For example, if it is desired to move the cursor forward one position each time a new word is entered into the main memory, the PC1 lead is energized so that the counter CBC is decremented one count when the AND gate A16 is enabled by sensing a word in register SR2 and producing the appropriate signal on leads PC1 and PC2.

The microprogramming can also perform the following additional functions:

7. Skip an instruction on finding a preselected flag in a desired state. Typical flags to be checked are:
 - A. Whether the word in input register SR2 represents a character or a command;
 - B. Whether the loading of input register SR2 is completed;
 - C. Whether the character at the current cursor position is not to be erased. Accordingly, the LEM produces an STP signal, as noted above;
 - D. Whether the tab is at the current cursor position;
 - E. Whether the unloading of the output register has been completed;
- etc.

8. Jump to the next address in the program memory. This instruction transfers the contents of the next address into the program counter and simultaneously disables the decoder in memory PMC during the operation.

9. Jump to a command from the input register SR2 via the leads SR2A—SR2H. This instruction jumps to a subroutine at the address specified by the contents of the input register SR2. This is accomplished by storing the next to present memory address on top of the subroutine stack, incrementing the same and transferring the address to the program counter PBC via the PRE1—PRE8 signal leads.

10. Jump to a subroutine starting at an address contained in the location next to the present address. This instruction causes the LEM to store the address of the next location on the subroutine stack, increment the stack and transfer the address of the next location to the counter PBC via the PRE1—PRE8 signal lines.

11. Jump back from a subroutine. This instruction is used at the end of a subroutine which is entered by means of instructions 9 or 10, above.

The following instructions are used to either add or delete a character word to the main memory or a tab memory contained in the logic element network LEM:

12. Load main memory from the input register SR2, in which case the STP signal is absent.

13. Load an output register SR3 from the main memories by generating the ENA signal, as noted below.

14. Set tab. This instruction enters a binary 1 in the tab memory at the current cursor position.

15. Clear tab. This instruction enters a binary 0 in the tab memory at the current cursor position. In practice, the tab memory may comprise a 40-bit circulating memory which is synchronized with the main memory.

Additionally, the microprogram may be adapted to transmit pulses to appropriate logic for setting or clearing flags, initiating routines, and the like to perform one or more of the following functions: enable the keyboard KBD; disable the keyboard; clear the input register SR2 or the output register SR3, and the like.

Additionally, as noted above, commands may come from the input register SR2 via the lines SR2A—SR2H, which commands may originate from the keyboard KBD, from a remote computer via the signal lead RE1, and the like. The command words may be distinguished from the words or sets of bits representing a character by placing a binary zero in the two highest order positions of the word. On the other hand, a word representing a character may have a binary one in one of the two highest order positions.

While the above commands are illustrative of the type of program which may be associated with the system of the present invention, they are not to be interpreted as being a limitation thereof.

DETAILED DESCRIPTION OF APPARATUS FOR REMOTE TRANSMISSION OF MATERIAL (FIG. 7)

The information contained in the main memory sections of the memory units MUA—MUH may be transmitted to a remote station utilizing the apparatus illustrated in FIG. 7. Thus, the leads MMA1—MMH1 of the main memory units MUA—MUH are connected to a parallel-input serial-output shift register SR3 through the respective AND gates A18—A26, which are enabled by the ENA signal from program control PC. The GAT pulse is applied to the load terminal of shift register SR3 so that the output signals appearing on the leads MMA1—MMH1 during the occurrence of the GAT signal and the ENA signal will cause the information appearing on these leads to be entered into the shift register SR3. A signal LCS derived from a local clock CL is applied to the shift terminal of the shift register SR3. The local clock LC may produce shift pulses which are compatible for use in conjunction with the transmission of information on conventional telephone lines. Thus, the information in the shift register SR3

writing means to indicate on said medium the location at which the next new character will appear.

10. A display system as in claim 1, in which said decoding means includes inhibit means for preventing modulation of said writing means during a portion of said plurality of scans to provide a space between said lines of characters.

11. A display system as in claim 1, in which said decoding means includes a decoder for decoding the set of bits applied thereto into modulation signals for the writing means which are available at a number of decoder outputs, a shift register having inputs greater in number than said decoder outputs, means for connecting said decoder outputs individually to respective ones of a portion of said shift register inputs, means for connecting said shift register output to said writing means whereby the unconnected inputs of said shift register do not cause modulation of the writing means.

12. A system for displaying characters by the cyclic scanning of a writing means comprising, storage means for storing characters divided into sets of information bits, said storage means comprising a main storage means having output terminals for storing all of the sets of bits representing all of the characters to be displayed and for producing said sets of bits at said output terminals at recurrent intervals, and auxiliary storage means connected to said output terminals of said main storage means for storing the sets of bits representing the characters to be displayed during a scan of the writing means and for sequentially presenting each set of bits at an output, and modulating means connected to the output of said auxiliary storage means responsive to the set of bits appearing at the output for modulating the writing means to form areas of a character represented by said set of bits during the scanning of the writing means.

13. A system for displaying characters as in claim 12, in which said main and auxiliary storage means comprise circulating registers which operate in synchronism.

14. A system for displaying characters as in claim 12, and a clock circuit for controlling the operation of said system, said clock circuit including shift signal means responsive to said writing means scanning through a character to produce a shift signal, said auxiliary storage means being responsive to said shift pulse for presenting a new set of bits representing the next character at said output.

15. A system for displaying characters as in claim 14, in which said characters are formed by a plurality of scans of the writing means, said clock circuit further comprising line signal means responsive to the last scan of the writing means in said plurality of scans for generating a line signal, and gate means responsive to said line signal for connecting said main and auxiliary storage means together whereby sets of bits are transferred from said main to said auxiliary storage means.

16. A system for displaying characters as in claim 14, and synchronizing means connected with and responsive to said clock circuits for synchronizing the operation of said writing means with said main and auxiliary storage means.

17. A system for displaying characters as in claim 14, and counting means for counting said shift signals and for producing an indicating signal at a preselected count, input means for producing sets of bits representing new characters to be displayed, and connecting means responsive to said indicating means for connecting together said input means and said main storage means whereby the sets of bits produced by said input means are entered into said main storage means.

18. A display system as in claim 17, and indicating means responsive to said indicating signal for modulating said writing means to indicate the character position at which the character represented by the sets of bits produced by said input means will be displayed.

19. A display system as in claim 18, and moving means connected to said counting means for varying the count therein to change the indicated character to a new location.

20. A display system as in claim 18, and control means responsive to said indicating signal and the operation of said input means for moving the indicated character position one

character when said set of bits produced by said input means is entered into said main storage means.

21. A system for the display of information on a cathode-ray tube having an electron beam or the like wherein the information comprises a first plurality of text lines wherein each text line comprises a second plurality of characters which are formed by a third plurality of scans of the electron beam, said system comprising memory means for storing the characters to be displayed as respective sets of information bits, said memory means comprising a main memory having an input and an output for storing the sets of bits representing all of the characters to be displayed, and auxiliary memory connected to said main memory and having an input and an output for storing all of the sets of bits representing the second plurality of characters comprising a text line and being operable to sequentially present said sets of bits stored in said auxiliary memory at the output thereof during each of said third plurality of scans, scan counting means having a scan count output corresponding to each scan in a text line, and character generating means responsive to the particular set of bits at the output of said auxiliary memory and said scan count output to modulate the electron beam to form areas of the character represented by the particular set of bits during the scan represented by the scan count output.

22. A system for the display of information as in claim 21, and character signal means synchronized with the movement of the electron beam for producing a character signal after a character area has been formed, said auxiliary memory being responsive to said character signal to present the set of bits representing the next character to be displayed at the output thereof.

23. A system for the display of information as in claim 21, in which said scan counting means produces a load auxiliary memory signal at a particular count, and auxiliary gate means responsive to said load auxiliary memory signal for connecting said main memory output with said auxiliary memory input, and shift means operable to transfer sets of bits from said main memory to said auxiliary memory.

24. A system for the display of information as in claim 21, in which said main memory is operable to sequentially produce said sets of bits at the output thereof, cursor means including storage counter means synchronized with the sequential sets of bits output from said main memory for producing a load main memory signal at a particular count, input means for producing a set of bits representing a new character, and main gate means responsive to said load main memory signal for applying said sets of bits produced by said input means to said main memory input.

25. A system for the display of information as in claim 24, and inhibit means for disabling said main gate means to prevent the application of said set of bits produced by said input means to said main memory input.

26. A system for the display of information as in claim 24, in which said cursor means is operable to produce a trace on the cathode-ray tube at the location at which the new character will appear, said storage counter means including character counting means for producing a character signal when a particular character count is reached, said scan counting means producing a load auxiliary memory signal at a particular count and a cursor signal at a predetermined count, said cursor means including means responsive to said load main memory signal, load auxiliary memory signal, character signal and said cursor signal for modulating the electron beam to produce said trace.

27. A system for the display of information as in claim 26, in which said character counting means has a capacity equal to said second plurality of characters.

28. A system for the display of information as in claim 21, including transmission means for transmitting the sets of bits in said memory means to a remote location.

29. Position indicating means for a display system of the type having a writing means for forming elemental areas of characters comprising a line of characters during successive

scans of the writing means and wherein said line of characters is formed by a plurality of such successive scans, said position indicating means including character counting means for generating a character signal after a preselected count is reached corresponding to the horizontal position of the character to be indicated, scan counting means for producing a scan signal after a predetermined count has been reached corresponding to the horizontal position of the character to be indicated, scan counting means for producing a scan signal after a predetermined count has been reached corresponding to the vertical position at which said indication is to appear, and modulating means responsive to said character and scan signals for causing said writing means to form a trace at the

desired position.

30. Position indicating means as in claim 29, in which said writing means is adapted to produce a plurality of lines of characters, and line counting means for counting the lines of said characters and for producing a line signal corresponding to the line in which the character is to be indicated, said modulating means being further responsive to said line signal for producing said trace in the desired line.

31. Position indicating means as in claim 30, and count varying means for varying the count in said character counting means and said line counting means to change the position of said trace.

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