**Title:** NON-VOLATILE SINGLE-EVENT UPSET TOLERANT LATCH CIRCUIT

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PRIORITY CLAIM

The present application claims priority under 35 U.S.C. § 119(e)(1) to provisional application number 60/991,390 filed on November 30, 2007, the contents of which are incorporated herein by reference.

STATEMENT OF GOVERNMENT INTEREST

The present invention was made with United States Government assistance under Contract No. FA9453-04-C-0052. The United States Government has certain rights in the present invention.

BACKGROUND OF THE INVENTION

1. Technical Field

The present invention relates to memory devices in general, and in particular to chalcogenide memory devices. Still more particularly, the present invention relates to a non-volatile single-event upset tolerant latch circuit.

2. Description of Related Art

In certain environments, such as satellite orbital space, in which the level of radiation is relatively intense, memory devices, such as static random access memories (SRAMs), are more susceptible to single-event upsets (SEUs) or soft errors than they would have in terrestrial environments. These SEUs are typically caused by electron-hole pairs created by, and travelling along the path of, a single energetic particle as it passes through
within a storage node of an SRAM cell, the logic state of the SRAM cell will be upset.
By the same token, other circuits used in conjunction with SRAMs are also susceptible to
SEUs.

In the existing re-programmable SRAM-based field programmable gate
arrays (FPGAs), a device configuration is typically stored in the volatile SRAM cells and
must be reloaded at each power-up. Non-volatile FPGAs having flash memories can be
utilized to store device configurations, but the flash memory cells are not radiation tolerant
either, and there are reliability limitations for flash memory cells.
SUMMARY OF THE INVENTION

In accordance with a preferred embodiment of the present invention, a non-volatile single-event upset (SEU) tolerant latch is utilized to store device configurations. The non-volatile SEU tolerant latch includes a first and second inverters connected to each other in a cross-coupled manner. The gates of transistors within the first inverter are connected to the drains of transistors within the second inverter via a first feedback resistor. Similarly, the gates of transistors within the second inverter are connected to the drains of transistors within the first inverter via a second feedback resistor. The non-volatile SEU tolerant latch also includes a pair of chalcogenide memory elements connected to the inverters for storing information.

AU features and advantages of the present invention will become apparent in the following detailed written description.
BRIEF DESCRIPTION OF THE DRAWINGS

The invention itself, as well as a preferred mode of use, further objects, and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figure 1 is a block diagram of a field programmable gate array system, in accordance with a preferred embodiment of the present invention;

Figure 2 is a circuit diagram of a non-volatile single-event upset tolerant latch circuit for the field programmable gate array system of Figure 1, in accordance with a preferred embodiment of the present invention; and

Figure 3 is a circuit diagram of a non-volatile single-event upset tolerant latch circuit for the field programmable gate array system of Figure 1, in accordance with an alternative embodiment of the present invention.
DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Referring now to the drawings and in particular to Figure 1, there is illustrated a block diagram of a field programmable gate array (FPGA) system, in accordance with a preferred embodiment of the present invention. As shown, a FPGA system 10 includes a FPGA unit 11 coupled to a non-volatile single-event upset (SEU) tolerant latch 12. Device configurations from FPGA unit 11 can be stored in non-volatile SEU tolerant latch 12 before system shut down, and can be reloaded from non-volatile SEU tolerant latch 12 back to FPGA unit 11 at each power-up.

With reference now to Figure 2, there is depicted a circuit diagram of non-volatile SEU tolerant latch 12, in accordance with a preferred embodiment of the present invention. As shown, non-volatile SEU tolerant latch 12 includes two cross-coupled complementary metal oxide semiconductor (CMOS) inverters. The first inverter includes a p-channel transistor 21 connected in series with an n-channel transistor 22. The second inverter includes a p-channel transistor 23 connected in series with an n-channel transistor 24. The gates of transistors 21 and 22 are connected to the drains of transistors 23 and 24 via a feedback resistor 25, and the gates of transistors 23 and 24 are connected to the drains of transistors 21 and 22 via a feedback resistor 26. The resistances of feedback resistors 25 and 26 are greater than zero ohm. The higher the resistance values, the more tolerant non-volatile SEU tolerant latch 12 towards SEU.

The first inverter is connected to ground via a chalcogenide memory element 13a. Similarly, the second inverter is connected to ground via a chalcogenide memory element 13b. Chalcogenide, which preferably includes germanium, antimony and tellurium, can be made to have phase transformation properties at a relatively low voltage. Thus, each of chalcogenide memory elements 13a and 13b can be placed in an amorphous state or a crystalline state, which is utilized to represent a logical "0" and a logical "1," respectively. The state of each of chalcogenide memory elements 13a and 13b can be
changed from one to another via the application of an electrical field accordingly. For the
present application, the logical states of chalcogenide memory elements 13a and 13b are
always complementary to each other.

The device configuration information can be loaded from FPGA units 11a and lib into chalcogenide memory elements 13a and 13b, respectively, for the purpose of storage. During system start-up, the stored device configuration information can be reloaded from chalcogenide memory elements 13a and 13b back to FPGA units 11a and lib, respectively.

State set up modules 14a and 14b determine the initial state of non-volatile SEU tolerant latch 12. For example, the initial state of non-volatile SEU tolerant latch 12 can be reset by utilizing state set up modules 14a and 14b before the device configuration information is loaded from FPGA units 11a and lib.

Referring now to Figure 3, there is depicted a circuit diagram of a non-volatile SEU latch circuit 12', in accordance with an alternative embodiment of the present invention. As shown, chalcogenide memory element 13a along with state set up module 14a are connected between V_{DD} and p-channel transistor 21. Similarly, chalcogenide memory element 13b along with state set up module 14b are connected between V_{DD} and p-channel transistor 23. The functionalities of non-volatile SEU latch circuit 12' are identical to those of non-volatile SEU latch circuit 12 in Figure 2.

As has been described, the present invention provides a non-volatile SEU tolerant latch for storing device configurations. Since the cross-coupled CMOS inverters are SEU tolerant and chalcogenide memory elements are immune to SEU, the entire FPGA system is SEU tolerant.
While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.
What is claimed is:

1. A non-volatile single-event upset tolerant latch comprising:

   a first and second inverters connected to each other in a cross-coupled manner, wherein the gates of transistors within said first inverter are connected to the drains of transistors within said second inverter via a first feedback resistor, and the gates of transistors within said second inverter are connected to the drains of transistors within said first inverter via a second feedback resistor; and

   a pair of chalcogenide memory elements connected to said first and second inverters for storing information.
2. The latch of Claim 1, wherein said first inverter includes a p-channel transistor connected in series with an n-channel transistor.

3. The latch of Claim 1, wherein said second inverter includes a p-channel transistor connected in series with an n-channel transistor.

4. The latch of Claim 1, wherein said first inverter is connected to ground via a first one of said chalcogenide memory elements.

5. The latch of Claim 4, wherein said second inverter is connected to ground via a second one of said chalcogenide memory elements.

6. The latch of Claim 1, wherein said first inverter is connected to \( V_{DD} \) via a first one of said chalcogenide memory elements.

7. The latch of Claim 6, wherein said second inverter is connected to \( V_{DD} \) via a second one of said chalcogenide memory elements.

8. The latch of Claim 1, wherein said chalcogenide includes germanium, antimony and tellurium.
FIG. 3
INTERNATIONAL SEARCH REPORT

International application No
PCT/US 08/84714

A CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G11C 11/00 (2009.01)
USPC - 365/154

According to International Patent Classification (IPC) or to both national classification and IPC

B FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC 365/154

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
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USPC 365/72, 365/155, 365/156

Electronic data base consulted during the international search (name of data base and where practicable, search terms used)
PubWest (USPT, USOC, EPAB, JPAB), DialogPro, Google Scholar, non-volatile single-event upset (SEU) tolerant latch first second inverters cross-coupled gates transistors gates drains transistors feedback resistor pair chalcogenide memory element storing p-channel series n-channel ground VDD germanium antimony tellurium

C DOCUMENTS CONSIDERED TO BE RELEVANT

Category* Citation of document, with indication, where appropriate, of the relevant passages Relevant to claim No

Y US 2007/0165446 A1 (Ohya et al.), 19 July 2007 (19 07 2007), Fig 2, para [0012]-[0014], [0030], [0034]-[0036], [0038]-[0042], [0044], [0049]-[0052] 1-8


Y US 2004/0105301 A1 (Toyoda et al.), 03 June 2004 (03 06 2004), para [0041], [0044], [0063], [0066]-[0071], [0076] 4-7

A US 2006/0171 194 A1 (Lawley et al.), 03 August 2006 (03 08 2006), entire document 1-8


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Further documents are listed in the continuation of Box C

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y" document of particular relevance, the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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