



(51) International Patent Classification:

H04N 5/374 (2011.01) H01L 31/0264 (2006.01)

H01L 29/786 (2006.01)

(21) International Application Number:

PCT/EP2020/052468

(22) International Filing Date:

31 January 2020 (31.01.2020)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

19382066.9 31 January 2019 (31.01.2019) EP

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(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,

(54) **Title:** CHARGE SENSING DEVICE WITH GATE VOLTAGE SELECTED TO OPERATE AROUND THE CHARGE NEUTRALITY POINT AND TUNE THE QUANTUM CAPACITANCE

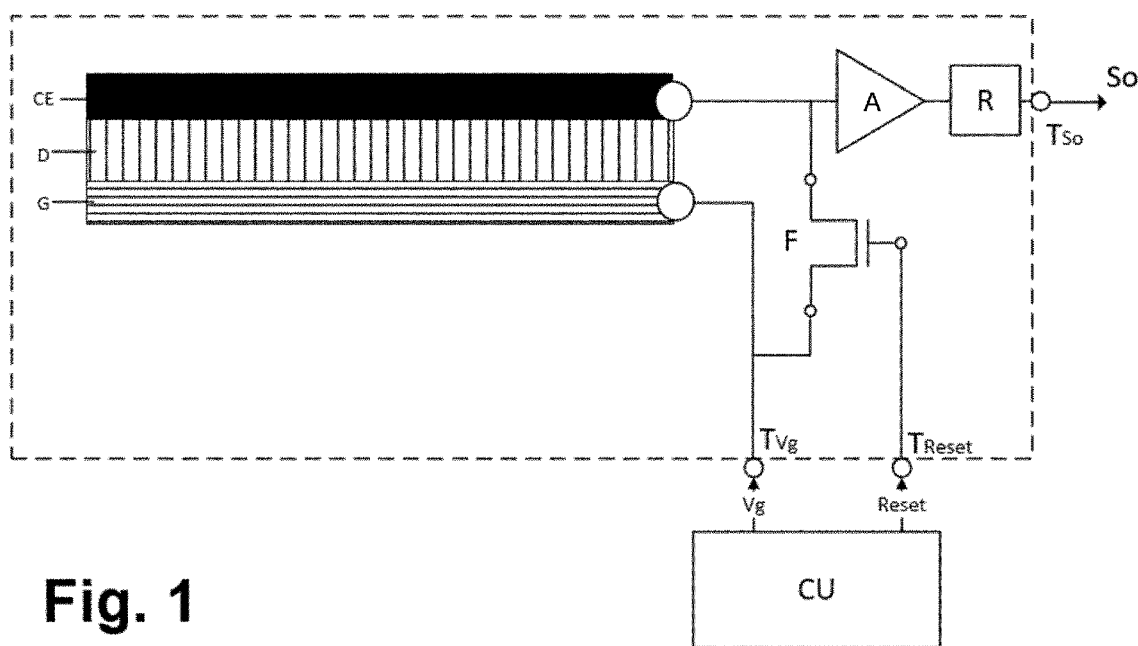


Fig. 1

(57) **Abstract:** The present invention relates to a system comprising an electronic apparatus which comprises: - an electronic device comprising: - a gate electrode (G, BE); - a dielectric (D) arranged over the gate electrode (G, BE); and - a charge sensing structure (CE) with a 2-dimensional charge sensing layer to provide a gate capacitance (C_g) between the charge sensing structure (CE) and the gate electrode structure (G, BE) and a quantum capacitance (C_q) resulting in a total capacitance (C_{tot}); - a voltage detector to detect an output voltage (V_g) stored in the total capacitance (C_{tot}). The system further comprises means to apply a gate voltage (V_g) to the gate electrode structure (G, BE) selected to: - make the device operate around most sensitive point of fermi level of

DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

CHARGE SENSING DEVICE WITH GATE VOLTAGE SELECTED TO OPERATE AROUND THE CHARGE NEUTRALITY POINT AND TUNE THE QUANTUM CAPACITANCE

FIELD OF THE INVENTION

The present invention relates, in a first aspect, to a system comprising an electronic apparatus, comprising an electronic device constituting a capacitor that is used for charge sensing purposes and shows quantum capacitance tuneable by the system while operating the device around the most sensitive point of fermi level.

A second aspect of the present invention relates to an electronic apparatus like the one of the system of the first aspect of the invention, and adapted to allow the tuning of the quantum capacitance.

BACKGROUND OF THE INVENTION

Systems which comprise the features of the preamble clause of claim 1 of the present invention are known in the art, i.e. those which comprise an electronic apparatus comprising:

- an electronic device comprising:
 - a gate electrode structure;
 - a dielectric structure arranged over said gate electrode structure; and
 - a charge sensing structure comprising at least one 2-dimensional charge sensing layer configured to sense electrical charges and/or electrical charge density changes induced by an external physical quantity, and that is configured and arranged over said dielectric structure to provide a gate capacitance between the charge sensing structure and the gate electrode structure, wherein said charge sensing structure shows a quantum capacitance in series with said gate capacitance resulting in a total capacitance between the charge sensing structure and the gate electrode structure;
- a voltage detector electrically connected to the charge sensing structure or to the gate electrode structure, to detect an output voltage V_{out} that is representative of said sensed electrical charges Q_s stored on the capacitor C.

The output voltage is $V_{out}=Q_s/C$. To optimize the output voltage the capacitance needs to be minimized.

The classical capacitance of the gate capacitor C_g formed by the charge sensing structure and the gate electrode structure is given by the following formula:

$$C_g = \epsilon_r \epsilon_0 A / d$$

Where ϵ_r is the relative permittivity of the dielectric material, ϵ_0 is the vacuum permittivity, A the area of the capacitor and d the thickness of the dielectric material.

When a large sensitivity of the device is required the capacitance needs to be as small as possible and hence the thickness of the dielectric d needs to be as large as possible to maximize the output voltage for a given amount of charges Q_s . For those high sensitivity applications, the capacitances to the gate electrode structure and contacts and the parasitic capacitances of the voltage detector, and possible read-out circuitry, need to be minimized to be able to detect the output voltage or read an output signal associated thereto. One way to minimize parasitic capacitances to the read-out circuitry is to integrate the detectors in a silicon complementary metal oxide semiconductor (CMOS) circuit.

For 2-dimensional materials there is another capacitance that needs to be taken into account due to their finite density of states. This is the above mentioned quantum capacitance C_q . C_q is in series with the classical capacitance and thus reduces the total capacitance C_{tot} of the system ($1/C_{tot}=1/C_g+1/C_q$). Due to the quantum capacitance effect, the output voltage V_o can be enhanced for a certain charge Q_s that needs to be sensed.

For example, when the 2-dimensional material is graphene, the quantum capacitance per unit area C_q/A is described as follows:

$$C_Q = \frac{2e^2}{\hbar v_F \sqrt{\pi}} (|n_G| + |n^*|)^{1/2}$$

Where e is the electron charge, $\hbar$ the planck constant, v_F the Fermi velocity of graphene, n_G the induced carrier density in the graphene and n^* the residual impurity density.

C_g for a typical gate dielectric thickness of 10 nm made of Al_2O_3 is 0.0053 F/m². The minimum quantum capacitance of a capacitor with the same dielectric thickness for a high electronic quality graphene layer at room temperature ($n^*=7 \cdot 10^{10}$ cm⁻²) will be 0.0012 F/m². In this case the quantum capacitance will enhance the output voltage by a factor 5.

However, although those known apparatuses provide a high sensitivity, for many applications that sensitivity is not high enough or the dynamic range is not large enough.

Also, for that quantum capacitance have an effect on the total capacitance, the electronic device must operate around most sensitive point of fermi level of the charge sensing structure, i.e. around the charge neutrality point (cnp) when the 2-dimensional material is graphene, which does not occur by nature.

The following documents disclose different prior art electronic devices including a 2-dimensional charge sensing layer configured to sense electrical charges and/or electrical charge density changes induced by an external physical quantity:

-Konstantatos, G., Badioli, M., Gaudreau, L. et al. Hybrid graphene–quantum dot phototransistors with ultrahigh gain. *Nature Nanotech* 7, 363–368 (2012).

-Schedin, F., Geim, A., Morozov, S. et al. Detection of individual gas molecules adsorbed on graphene. *Nature Mater* 6, 652–655 (2007).

- 5 -Wangyang Fu, Lingyan Feng, Gregory Panaitov, et al., Biosensing near the neutrality point of graphene, *Science Advances* 3, e1701247, (2017).

It is, therefore, necessary to provide an alternative to the state of the art which covers the gaps found therein, by providing a system including the features described above, but which does not possess the above mentioned drawbacks, and is thus able
10 mainly to provide an active control between sensitivity level and dynamic range, so as to achieve the sensitivity level and dynamic range required, with the same system.

SUMMARY OF THE INVENTION

To that end, the present invention relates, in a first aspect, to a system comprising
15 an electronic apparatus, wherein the electronic apparatus comprises:

- an electronic device comprising:

- a gate electrode structure;

- a dielectric structure arranged over said gate electrode structure; and

20 - a charge sensing structure comprising at least one 2-dimensional charge sensing layer configured to sense electrical charges and/or electrical charge density changes induced by an external physical quantity (for example, as described in the above cited prior art references), and that is configured and arranged over said dielectric structure to provide a gate capacitance C_g between the charge sensing structure and the gate electrode structure; wherein said charge sensing structure (by having a
25 density of states low enough) shows a quantum capacitance C_q in series with the gate capacitance C_g resulting in a total capacitance C_{tot} between the charge sensing structure and the gate electrode structure;

30 - a voltage detector electrically connected to the charge sensing structure or the gate electrode structure, to detect an output voltage that is representative of the sensed electrical charges stored in the total capacitance C_{tot} .

In contrast to the systems of the state of the art, the one provided by the present invention further comprises means configured and arranged to apply a gate voltage to the gate electrode structure, wherein said gate voltage is selected to, both:

- make the electronic device operate around the most sensitive point of fermi level of the charge sensing structure, i.e. around the charge neutrality point (cnp) when the 2-dimensional material is graphene; and

5 - tune the quantum capacitance C_q to modify the sensitivity and dynamic range of the electronic device.

Therefore, the system of the first aspect of the present invention constitutes a hybrid system which can be actively controlled to operate as desired, for high sensitivity applications, and also for high dynamic range applications, depending on the gate voltage applied.

10 For an embodiment, said means comprise a voltage source that generates said gate voltage.

The terms "voltage source" must be interpreted in the present invention as any kind of real-world voltage source (i.e. with non-zero internal resistance and output impedance) known in the prior art, such as one comprising or formed by one or more
15 battery cells, by one or more voltage generators, etc., for providing one or any number of voltages.

For an implementation of said embodiment, the output of the voltage source is electrically connected to the gate electrode structure, whether directly or through a switch, to apply the gate voltage thereto.

20 For a preferred embodiment, the above mentioned means comprise a control unit configured and arranged to apply the gate voltage to the gate electrode structure, and to perform the above mentioned selection of the gate voltage.

The terms "select" and "selection", with respect to the gate voltage, means the action of carefully choosing the best or most suitable gate voltage value for achieving the
25 above stated goals, i.e.:

- make the electronic device operate around the most sensitive point of fermi level of the charge sensing structure, i.e. around the charge neutrality point (cnp) when the 2-dimensional material is graphene; and

30 - tune the quantum capacitance C_q to modify the sensitivity and dynamic range of the electronic device.

Any known selection process which the skilled person would consider as appropriate for the one of the present invention is embraced by the system of the present invention, including the selection of the gate voltage value directly from an available pool of gate voltage values, or indirectly by calculating the same from selected values of other
35 kind of electrical parameters (such as electric current values and/or electrical resistance values) out of a pool of available values for said other kind of electrical parameters.

Depending on the implementation of said embodiment, the control unit includes or has access to a voltage source configured to generate the gate voltage.

According to different embodiments, the gate voltage is a DC voltage, an AC voltage, or a combination of DC and AC voltages (such as an AC voltage superimposed on a DC offset, or any kind of frequency and/or temporal combination).

For an embodiment, the control unit is configured to select the properties of the gate voltage, at least regarding its magnitude, while for another embodiment for which the gate voltage includes an AC voltage, the control unit is configured to select the properties of the gate voltage also regarding its frequency and/or phase, and while for a further embodiment for which the control voltage includes an DC voltage, the control unit is configured to select the properties of the control voltage also regarding its polarity.

According to an embodiment, the control unit comprises a selection input to receive selection signals regarding operation modes, and the control unit is configured to select and apply the gate voltage to the gate electrode structure in response to a selection signal received through that selection input, to make the apparatus operate according to the selected operating mode.

Advantageously, the control unit is also configured not to apply the gate voltage to the gate electrode structure also in response to a selection signal received through the selection input, so that the control unit is suitable also to make the electronic device operate according to the conventional sensitive mode, for a certain charge that needs to be sensed, intrinsically provided by the electronic device.

For an embodiment, the operation modes include at least the following modes:

- a high sensitivity mode, in which the control unit does not apply said gate voltage to the gate electrode structure or selects and applies a gate voltage with an absolute magnitude below $(0.9 \cdot V_t - V_{cnp})$ volts, where $V_t = q_e \cdot n^* \cdot A / C_g$, where q_e is the electron charge, n^* the residual charge carrier density, A the area and C_g the capacitance of the gate and V_{cnp} the voltage at which C_q is lowest, to reduce, not to increase or increase just a percentage below 35% said quantum capacitance;

- a high dynamic range mode, in which the control unit selects and applies to the gate electrode structure a gate voltage with an absolute magnitude above $(1.1 \cdot V_t - V_{cnp})$ volts, to increase to a percentage above 45 % said quantum capacitance; and

- a trade-off mode, in which the control unit selects and applies to the gate electrode structure a gate voltage with an absolute magnitude between $(0.9 - 1.1 \cdot V_t - V_{cnp})$ volts range, to increase said quantum capacitance to a percentage between 35 and 45% range.

For an embodiment, the voltage detector includes a reset circuit to discharge the total capacitance C_{tot} under the control of the control unit, and the apparatus further comprises a read-out circuit operatively connected to the out of the voltage detector to provide a read-out signal based on the detected output voltage.

5 The gate electrode structure together with the dielectric and charge sensing structures arranged there over, is arranged, for an embodiment, on a substrate.

According to an embodiment of the system of the first aspect of the present invention, the control unit further comprises an adjustment input connected to an output of the voltage detector or of a read-out circuit operatively connected thereto, and is
10 configured to implement a closed-loop adjustment process to adjust the gate voltage based on a detected output voltage or read-out signal received through that adjustment input, and preferably also based on reference or set-point values with which the detected output voltage(s) or read-out signal(s) are compared, so that a desired sensitivity and/or dynamic range is achieved.

15 In other words, a close-loop arrangement is made, for that embodiment, electrically connecting said adjustment input of the control unit to an output of the voltage detector providing the detected output voltage or an output of a read-out circuit operatively connected to the out of the voltage detector to provide a read-out signal. Therefore, the control unit is configured to adjust the gate voltage as described in the above paragraph,
20 i.e. based at least on the signal received through that adjustment input.

For an implementation of said embodiment, the control unit is configured to implement the closed-loop adjustment process also based on the selected operation mode, so that the desired sensitivity and/or dynamic range to be achieved is established depending on the selected operation mode.

25 For that implementation, in addition to the signal received through the adjustment input the selected operation mode is taken into account in the selection process implemented by the control unit to select the appropriate gate voltage to make the device operate according to the selected mode, check, by the detected output voltage or read-out signal, that the device is really operating in the selected mode (which occurs when the
30 values of the output voltage or read-out signal are within an appropriate range for the selected operation mode) and adjust the gate voltage to assure that the device is maintained in the selected operation mode (i.e. with the values of the output voltage or read-out signal within the appropriate range for the selected operation mode).

According to some embodiments, the electronic device of the electronic apparatus
35 of the system of the first aspect of the present invention further comprises a sensitizing or functionalizing structure arranged over the charge sensing structure, wherein the

sensitizing or functionalizing structure is configured to induce the electrical charge carriers and/or modify the charge carrier density therein induced by said external physical quantity. Generally the sensitizing or functionalizing structure is only sensitive to said external physical quantity.

5 The term “functionalizing” means for the present invention, to add a species to the charge sensing structure that not only provides a sensitizing function, but also adds another functionality. For example, in the paper by Wangyang Fu (Wangyang Fu, Lingyan Feng, Gregory Panaitov, et al., Biosensing near the neutrality point of graphene, Science Advances 3, e1701247, (2017).) a pPNA linker molecule is added to the surface of the
10 graphene to allow ssDNA to link to the graphene and a Tween 20 molecule was added to the graphene surface to make the sensing of the ssDNA more specific by inhibiting attachment of other species to the surface to the graphene. Hence in this case the pPNA linker molecule functionalizes AND sensitizes the graphene.

 While the term “sensitizing” refers to any species that is added on top of the charge
15 sensing structure that sensitizes it to an external physical quantity or analyte.

 For an embodiment, said sensitizing or functionalizing structure is a photoactive structure configured and arranged to, upon illumination, generate electron-hole pairs which, due to a field created by either a Schottky junction between the charge sensing structure and the photoactive structure or a topgate electrode on top of the photoactive
20 structure or an interlayer between the charge sensing structure and the photoactive structure, are separated and either the electrons or holes gets transported, as said induced electrical charge carriers, to the charge sensing structure, so that the optoelectronic apparatus constitutes a photodetector or an image sensor.

 For an implementation of that embodiment, the system of the first aspect of the
25 present invention implements an image sensor comprising an array of pixels, wherein the electronic apparatus comprises a plurality of the above mentioned electronic devices each constituting one pixel of said array of pixels, implementing different alternative read-out schemes, for addressing and reading the pixels of the rows and columns of the array, including rolling and global shutter, etc. Different variants of that implementation are
30 covered by the present invention, for some of which a common gate voltage is applied simultaneously to the gate electrode structures of all or part of the electronic devices, while for other variants different gate voltages are applied individually to the gate electrode structures of all or part of the electronic devices.

 According to an alternative embodiment, the electronic device is absent of any
35 sensitizing or functionalizing structure arranged over the charge sensing structure, the charge sensing structure being configured to undergo a change in the electrical charge

carriers and/or modify the charge carrier density therein induced by the external physical quantity. Examples of these kind of electronic devices which do not need of the existence of any sensitizing or functionalizing structure are given in Schedin, F., Geim, A., Morozov, S. et al. Detection of individual gas molecules adsorbed on graphene. Nature Mater 6,
5 652–655 (2007).

Therefore, the present invention is generally applied to sensing devices that rely sensing a change in the electrical charge carriers and/or in the charge carrier density in the charge sensing structure induced by said external physical quantity, whether directly on an exposed charge sensing structure, through the intermediation of a sensitizing layer
10 (such as a photo-sensitizing layer, for example made up of PbS colloidal quantum dots, where light can induce the charge carriers in the charge sensing structure, or a linker biomolecule grafted on the charge sensing structure) or through the functionalization of the charge sensing structure (e.g. for biosensing).

The charge sensing structure of the electronic device of the electronic apparatus
15 of the system of the first aspect of present invention comprises one or more 2-dimensional charge sensing layers made of, for example, one or more of the following materials: graphene (pure graphene, modified graphene, or functionalized graphene), black phosphorus, MoS₂, WS₂, WSe₂, etc.

Different physical quantities or analytes can be sensed by the electronic apparatus
20 of the system of the first aspect of the invention, as long as they induce electrical charge carriers in the charge sensing structure and/or a change in the charge carrier density therein, such as light, gas molecules or sensing neuronal signals. The analyte of interest transfers charge to the charge sensing structure or induces an electric field that modifies the charge carrier density thereof.

Another application is for direct sensing of in vivo electrical signals, or for
25 implementing biosensors using chemically bonded linker molecules that enhance the selectivity for specific bio-molecules. When the molecule of interest binds to the linker, it transfer charge to the charge sensing structure or induces an electric field therein that modifies its charge carrier density.

30 A second aspect of the present invention relates to an electronic apparatus, comprising:

- an electronic device comprising:
 - a gate electrode structure;
 - a dielectric structure arranged over said gate electrode structure; and
 - 35 - a charge sensing structure comprising at least one 2-dimensional charge sensing layer configured to sense electrical charges and/or electrical

charge density changes induced by an external physical quantity, and that is configured and arranged over said dielectric structure to provide a gate capacitance between the charge sensing structure and the gate electrode structure, wherein the charge sensing structure shows a quantum capacitance in series with said gate capacitance resulting in a total capacitance between the charge sensing structure and the gate electrode structure;

- a voltage detector electrically connected to the charge sensing structure or the gate electrode structure, to detect an output voltage that is representative of said sensed electrical charges stored in said total capacitance.

In contrast to the electronic apparatuses known in the state of the art, the one of the second aspect of the present invention comprises at least an input terminal electrically connected to the gate electrode structure and that is accessible to apply thereto a gate voltage selected to, both:

- make the electronic device operate around most sensitive point of fermi level of the charge sensing structure, i.e. the charge neutrality point when the 2-dimensional material is graphene; and

- tune the quantum capacitance to modify the sensitivity and dynamic range of the electronic device.

The embodiments described in the present document regarding the electronic apparatus of the system of the first aspect of the present invention are valid for describing corresponding embodiments of the electronic apparatus of the second aspect of the present invention.

BRIEF DESCRIPTION OF THE FIGURES

In the following some preferred embodiments of the invention will be described with reference to the enclosed figures. They are provided only for illustration purposes without however limiting the scope of the invention.

Figure 1 schematically shows the system of the first aspect of the present invention, for an embodiment;

Figure 2 is a schematic side view of the structure of the electronic device of the electronic apparatus of the second aspect of the invention and of the electronic apparatus of the system of the first aspect, for an embodiment, with electrical connections indicated as round circles: CE = charge sensing layer electrode and BE = bottom electrode.

Figure 3 is a schematic side view of the of the electronic device of the electronic apparatus of the second aspect of the invention and of the electronic apparatus of the

system, for an embodiment for which the electronic device comprises a photoactive structure for, upon illumination, generate electron-hole pairs which are separated and one of them gets transported to the charge sensing structure (CE), as indicated by the charge flow illustrated.

5 Figure 4 is a plot of the capacitance for a conventional parallel plate capacitor with two metal plates (MIM: "Metal-Insulator-Metal") and the total capacitance (including quantum capacitance) for a parallel plate capacitor of which one plate is a layer of 2D material (MI2D: "Metal-Insulator-2D material").

10 Figure 5 is a plot of the capacitance of the electronic device of the electronic apparatus of the second aspect of the invention and of the electronic apparatus of the system of the first aspect of the present invention, as a function of the applied gate voltage V_g with respect to the charge neutrality point ($d=10$ nm, $\epsilon_r=6$, $n^*=7 \cdot 10^{10}$ cm⁻²).

DESCRIPTION OF THE PREFERRED EMBODIMENTS

15 Figure 1 shows an embodiment of the system of the first aspect of the present invention, for which the system comprises an electronic apparatus which comprises the components depicted within a dotted-line square, i.e. an electronic device comprising:

- a gate electrode structure G;
- a dielectric structure D arranged over the gate electrode structure G; and
- 20 - a charge sensing structure CE comprising a 2-dimensional charge sensing layer configured to sense electrical charges and/or electrical charge density changes induced by an external physical quantity, and that is configured and arranged over the dielectric structure D to provide a gate capacitance C_g between the charge sensing structure CE and the gate electrode structure G.

25 The charge sensing structure CE has a density of states low enough to provide a quantum capacitance C_q in series with the gate capacitance C_g resulting in a total capacitance C_{tot} in value between C_q and C_g ($C_{tot}=1/(1/C_q+1/C_g)$) when measured between the charge sensing structure CE and the gate electrode structure G.

30 As shown in Figure 1, also within the dotted-line square, the electronic apparatus further comprises a voltage detector, formed by an amplifier A which input is electrically connected to the charge sensing structure CE, to detect an output voltage V_o that is representative of the sensed electrical charges stored in the total capacitance C_{tot} .

35 The system of the first aspect of the present invention further comprises means which for the illustrated embodiment comprise a control unit CU configured and arranged

to apply a gate voltage V_g to the gate electrode structure G, wherein the gate voltage V_g is selected by the control unit CU to, both:

- make the electronic device operate around the most sensitive point of fermi level of the charge sensing structure CE, i.e. around the charge neutrality point when the 2-dimensional material is graphene; and
- tune the quantum capacitance C_q to modify the sensitivity and dynamic range of the electronic device.

As shown in Figure 1, the voltage detector includes a reset circuit, formed by a transistor F, to discharge the total capacitance C_{tot} under the control of the control unit CU (by closing the transistor F so as to connect C_{tot} to the gate electrode structure G), and the apparatus further comprises a read-out circuit R operatively connected to the out of the voltage detector to provide a read-out signal S_o based on the detected output voltage V_o .

For the illustrated embodiment, the voltage detector includes an amplifier A, which needs to have a low input capacitance and thus a very high input impedance, although other kind of known voltage detectors are also covered by the present invention.

The read sequence is as follows:

1. Close Reset transistor F
2. Apply V_g
3. Read S_o
4. Open reset transistor F to drain charges

Figure 1 also shows an embodiment of the electronic apparatus of the second aspect of the present invention which comprises the components depicted within or in contact with the contour of the dotted-line square, i.e. the components of the electronic apparatus of the system of the first aspect of the present invention and further an input terminal TV_g electrically connected to the gate electrode structure G and that is accessible to apply thereto a gate voltage V_g selected to, both:

- make the electronic device operate around the most sensitive point of fermi level of the charge sensing structure CE, i.e. around the charge neutrality point when the 2-dimensional material is graphene; and
- tune the quantum capacitance to modify the sensitivity and dynamic range of the electronic device.

For an implementation of that embodiment, the components of the electronic apparatus are embedded in an integrated circuit chip, which has an input pin for terminals TV_g , a further input pin to connect to the illustrated reset terminal T_{Reset} and also an output

pin connected to terminal TS_o , so that a control unit CE can be connected to those input pins to provide gate voltage V_g and Reset signal, while S_o goes out through output terminal TS_o .

In Figure 2, an embodiment of the system and electronic apparatus of the present invention is shown, for which the electronic device is a photodetector which comprises a substrate S, a bottom electrode structure BE (as the above mentioned gate structure), and a sensitizing or functionalizing structure PS constituted by a photoactive structure PS (formed by colloidal quantum dots, III-V semiconductor, perovskites, 2D material, etc.) arranged over the charge sensing structure CE (for example, formed by a single layer or few layer graphene, black phosphorus, MoS2, WS2, WSe2 etc.) configured and arranged to, upon illumination, generate electron-hole pairs which, due to a built-in field created by a Schottky junction between the charge sensing structure CE and the photoactive structure PS, are separated and either the electrons or holes (depending on the type of Schottky junction) gets transported to the charge sensing structure CE. A voltage now builds up on the gate capacitor C_g . In case of a photosensitive layer it is the total photogenerated charge: $Q_{ph} = EQE \cdot q_e \cdot \tau_{tr} A / E_p I$, (EQE is the external quantum efficiency, q_e the electron charge, τ_{tr} the trapping time of the photogenerated charges and I the irradiance, A the area of the device and E_p the photon energy). This process is illustrated in Figure 3.

Figure 4 plots the total capacitance of a conventional parallel plate capacitor with two metal plates (MIM) and the total capacitance (including quantum capacitance) for a parallel plate capacitor of which one plate is a layer of 2D material exhibiting quantum capacitance effects (MI2D). A typical gate dielectric thickness of 10 nm made of Al_2O_3 ($\epsilon_r=6$) and the minimum quantum capacitance for a high electronic quality graphene layer in a capacitor with the same dielectric at room temperature ($n^*=7 \cdot 10^{10} \text{ cm}^{-2}$): 0.0012 F/m² were taken. For a typical gate dielectric thickness of 10 nm made of Al_2O_3 the normal capacitance is 0.0053 F/m². In this case the signal will be enhanced by a factor 5.

For the present invention, particularly when a large detector sensitivity is not required, the electronic device can be tuned to the classical regime by applying a different V_g to allow for more photogenerated charges (or charges generated by other means, for those embodiments not including a photosensitizing structure) to be stored and thus enable a larger dynamic range. This effect is illustrated in Figure 5 with the results obtained from a simulation of the present invention for the arrangement of Figures 2 and 3. As shown in that Figure, applying a gate voltage of 3V with respect to the charge neutrality point gives a capacitance that is 3x enhanced.

A person skilled in the art could introduce changes and modifications in the embodiments described without departing from the scope of the invention as it is defined in the attached claims.

Claims

1.- A system comprising an electronic apparatus, wherein the electronic apparatus comprises:

- 5 - an electronic device comprising:
- a gate electrode structure (G, BE);
 - a dielectric structure (D) arranged over said gate electrode structure (G, BE); and
 - a charge sensing structure (CE) comprising at least one 2-dimensional charge sensing layer configured to sense electrical charges and/or electrical charge density changes induced by an external physical quantity, and that is configured and arranged over said dielectric structure (D) to provide a gate capacitance (C_g) between the charge sensing structure (CE) and the gate electrode structure (G, BE); wherein said charge sensing structure (CE) shows a quantum capacitance (C_q) in series with said gate capacitance (C_g) resulting in a total capacitance (C_{tot}) between the charge sensing structure (CE) and the gate electrode structure (G, BE);
 - a voltage detector electrically connected to the charge sensing structure (CE) or to the gate electrode structure (G, BE), to detect an output voltage (V_o) that is representative of said sensed electrical charges stored in said total capacitance (C_{tot});
- 10 **characterised in that** the system further comprises means configured and arranged to apply a gate voltage (V_g) to said gate electrode structure (G, BE), wherein said gate voltage (V_g) is selected to, both:
- make the electronic device operate around the most sensitive point of fermi level
 - 25 of the charge sensing structure (CE); and
 - tune the quantum capacitance (C_q) to modify the sensitivity and dynamic range of the electronic device.

2.- The system according to claim 1, wherein said means comprise a voltage source that generates said gate voltage (V_g).

30 3.- The system according to claim 1 or 2, wherein said means comprise a control unit (CU) configured and arranged to apply said gate voltage (V_g) to said gate electrode structure (G, BE), and to perform said selection of the gate voltage (V_g).

4.- The system according to claim 1, 2 or 3, wherein said gate voltage (V_g) is a DC voltage, an AC voltage, or a combination of DC and AC voltages, and wherein the control unit (CU) is configured to select the properties of said gate voltage (V_g), at least regarding its magnitude.

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5.- The system according to any of the previous claims, wherein the control unit (CU) comprises a selection input to receive selection signals regarding operation modes, and wherein the control unit (CU) is configured to select and apply said gate voltage (V_g) to said gate electrode structure (G, BE) in response to a selection signal received through said selection input, to make the apparatus operate according to the selected operating mode.

6.- The system according to claim 5, wherein the control unit (CU) is configured not to apply said gate voltage (V_g) to said gate electrode structure (G, BE) also in response to a selection signal received through said selection input.

7.- The system according to claim 5 or 6, wherein said operation modes include at least the following modes:

- a high sensitive mode, in which the control unit (CU) does not apply said gate voltage (V_g) to the gate electrode structure (G, BE) or selects and applies a gate voltage (V_g) with an absolute magnitude below $(0.9 \cdot V_t - V_{cnp})$ volts, where $V_t = q_e \cdot n^* \cdot A / C_g$, where q_e is the electron charge, n^* the residual charge carrier density, A the area and C_g the capacitance of the gate and V_{cnp} the voltage at which C_q is lowest, to reduce, not to increase or increase just a percentage below 35% said quantum capacitance (C_q);

- a high dynamic range mode, in which the control unit (CU) selects and applies to the gate electrode structure (G, BE) a gate voltage (V_g) with an absolute magnitude above $(1.1 \cdot V_t - V_{cnp})$ volts, to increase to a percentage above 45 % said quantum capacitance (C_q); and

- a trade-off mode, in which the control unit (CU) selects and applies to the gate electrode structure (G, BE) a gate voltage (V_g) with an absolute magnitude between $0.9 \cdot (1.1 \cdot V_t - V_{cnp})$ volts range, to increase said quantum capacitance (C_q) to a percentage ranging between 35 and 45%.

8.- The system according to any of the previous claims, wherein the control unit (CU) further comprises an adjustment input connected to an output of said voltage detector or of a read-out circuit (R) operatively connected thereto, and is configured to implement a closed-loop adjustment process to adjust the gate voltage (V_g) based on a detected output voltage (V_o) or read-out signal (S_o) received through said adjustment input.

9.- The system according to claim 8 when depending on claim 7, wherein the control unit (CU) is configured to implement said closed-loop adjustment process also based on the selected operation mode.

10.- The system according to any of the previous claims, wherein said voltage detector includes a reset circuit to discharge the total capacitance (C_{tot}) under the control

of the control unit (CU), and wherein the apparatus further comprises a read-out circuit (R) operatively connected to the out of the voltage detector to provide a read-out signal (S_o) based on the detected output voltage (V_o).

11.- The system according to any of the previous claims, wherein the electronic device further comprises a sensitizing or functionalizing structure (S) arranged over said charge sensing structure (CE), wherein said sensitizing or functionalizing structure (S) is configured to induce said electrical charge carriers and/or modify the charge carrier density therein induced by said external physical quantity, wherein the sensitizing or functionalizing structure (S) is only sensitive to said external physical quantity.

12.- The system according to claim 11, wherein said sensitizing or functionalizing structure (PS) is a photoactive structure configured and arranged to, upon illumination, generate electron-hole pairs which, due to a field created by either a Schottky junction between the charge sensing structure (CE) and the photoactive structure (PS) or a topgate electrode on top of the photoactive structure (PS) or an interlayer between the charge sensing structure (CE) and the photoactive structure (PS), are separated and either the electrons or holes gets transported, as said induced electrical charge carriers, to the charge sensing structure (CE).

13.- The system according to claim 12, implementing an image sensor comprising an array of pixels, wherein the electronic apparatus comprises a plurality of said electronic devices each constituting one pixel of said array of pixels.

14.- The system according to any of claims 1 to 10, wherein the electronic device is absent of any sensitizing or functionalizing structure (S) arranged over said charge sensing structure (CE), the charge sensing structure being configured to induce itself said electrical charge carriers and/or modify the charge carrier density therein induced by said external physical quantity.

15.- An electronic apparatus, comprising:

- an electronic device comprising:

- a gate electrode structure (G, BE);

- a dielectric structure (D) arranged over said gate electrode structure (G, BE); and

- a charge sensing structure (CE) comprising at least one 2-dimensional charge sensing layer configured to sense electrical charges and/or electrical charge density changes induced by an external physical quantity, and that is configured and arranged over said dielectric structure (D) to provide a gate capacitance (C_g) between the charge sensing structure (CE) and the gate electrode structure (G, BE), wherein said charge sensing

structure (CE) shows a quantum capacitance (C_q) in series with said gate capacitance (C_g) resulting in a total capacitance (C_{tot}) between the charge sensing structure (CE) and the gate electrode structure (G, BE);

- 5 - a voltage detector electrically connected to the charge sensing structure (CE) or the gate electrode structure (G, BE), to detect an output voltage (V_o) stored in said total capacitance (C_{tot}) and that is representative of said sensed electrical charges;

characterised in that the electronic apparatus further comprises at least an input terminal (TV_g) electrically connected to said gate electrode structure (G, BE) and that is accessible to apply thereto a gate voltage (V_g) selected to, both:

- 10 - make the electronic device operate around the most sensitive point of fermi level of the charge sensing structure (CE); and

 - tune the quantum capacitance (C_q) to modify the sensitivity and dynamic range of the electronic device.

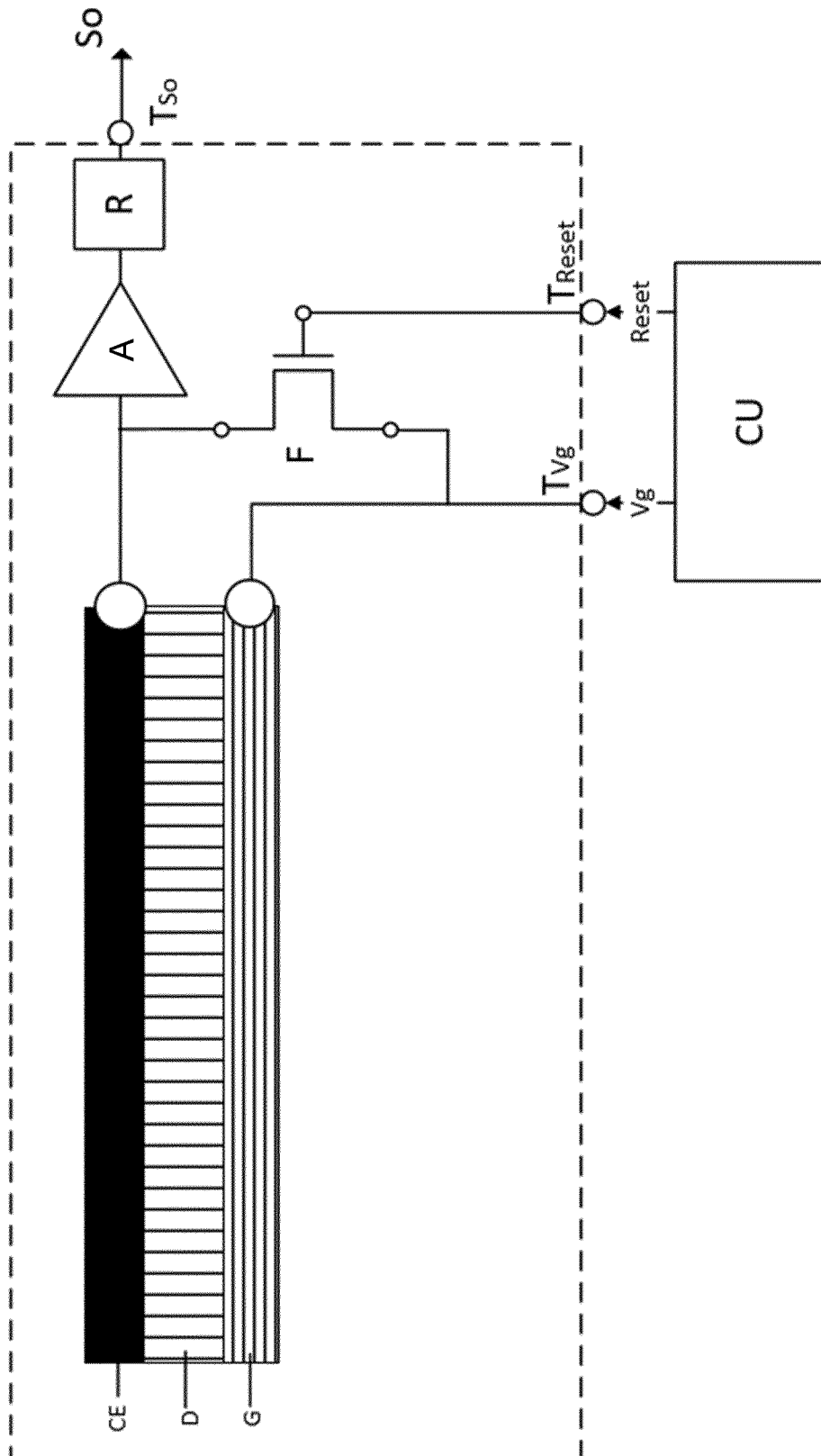


Fig. 1

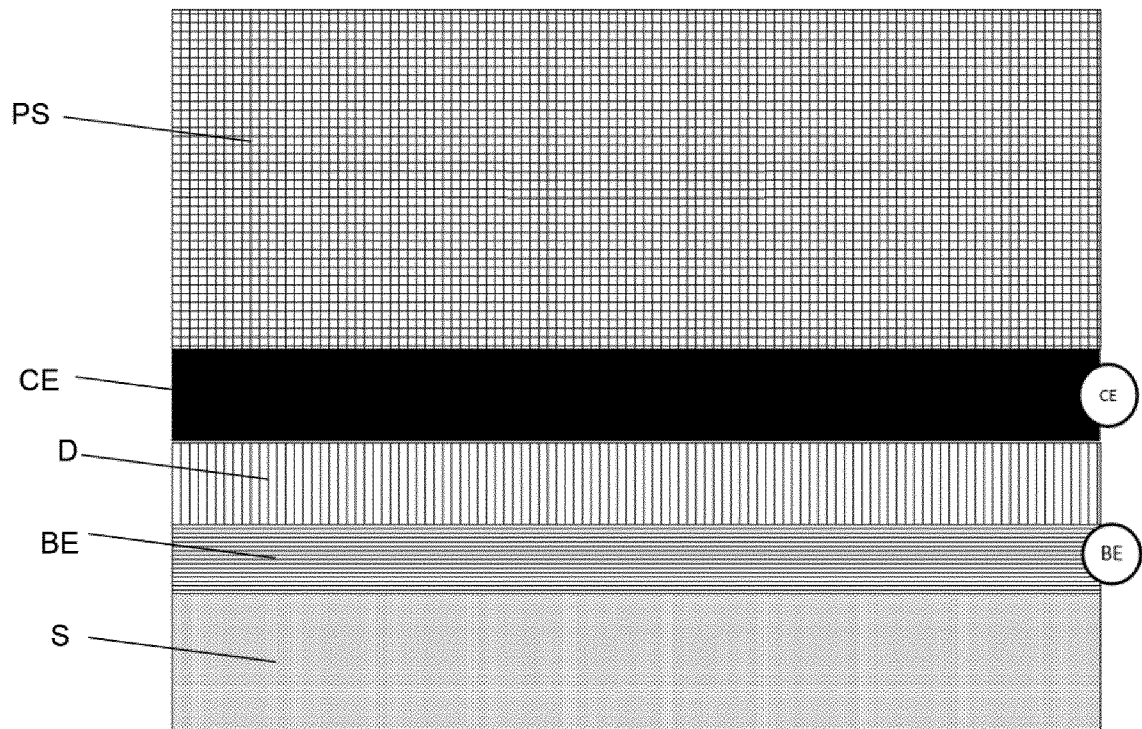


Fig. 2

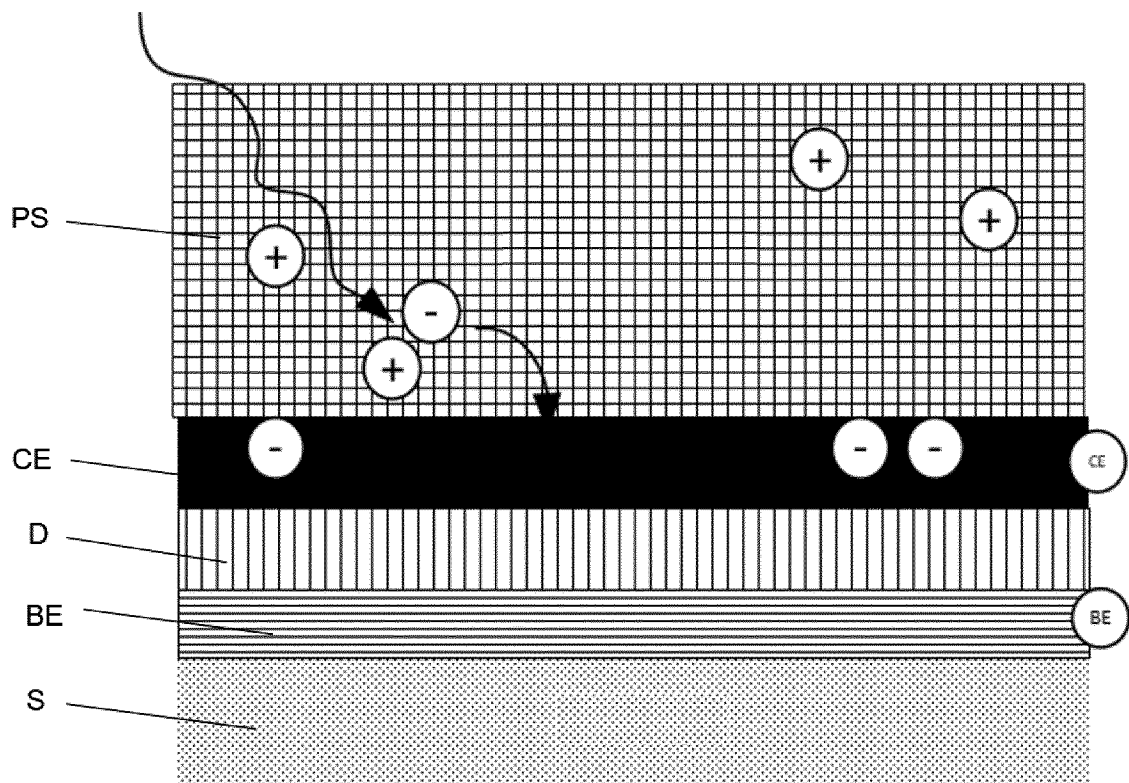
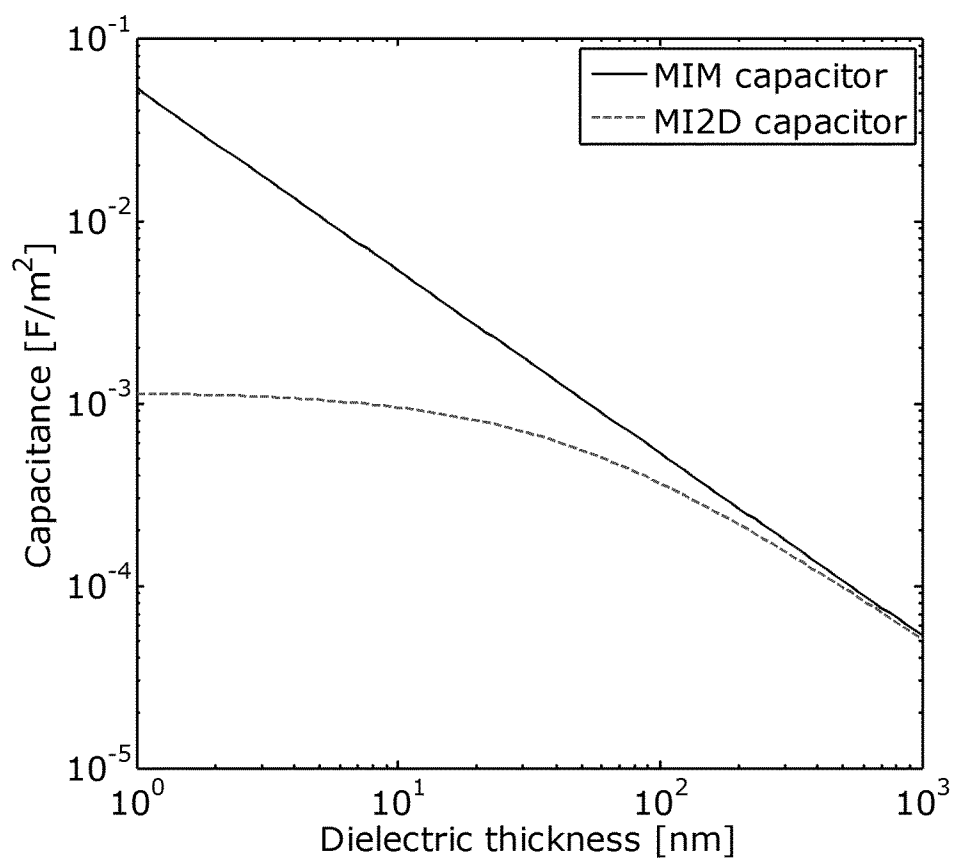
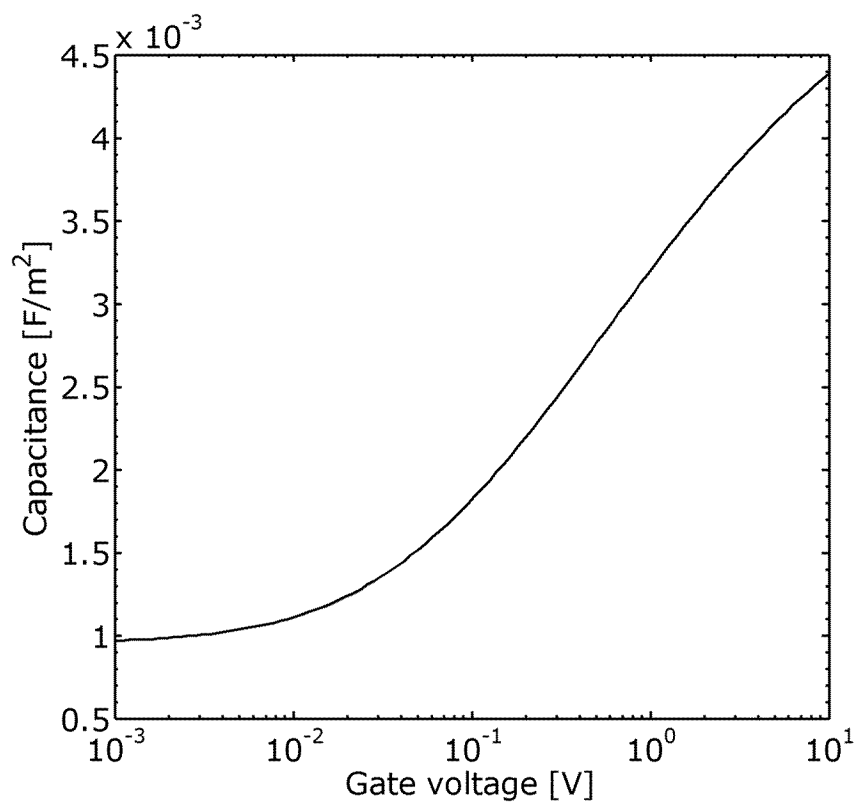


Fig. 3

**Fig. 4****Fig. 5**

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2020/052468

A. CLASSIFICATION OF SUBJECT MATTER

INV. H04N5/374 H01L29/786 H01L31/0264
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04N H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Further documents are listed in the continuation of Box C.



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Date of the actual completion of the international search

26 February 2020

Date of mailing of the international search report

04/03/2020

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Moorhouse, David

INTERNATIONAL SEARCH REPORT

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