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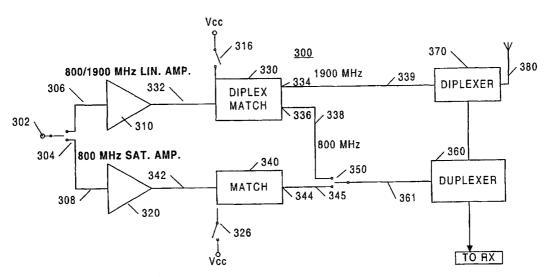
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(54) Title: A DUAL-BAND, DUAL-MODE POWER AMPLIFIER



(57) Abstract: A power amplifier circuit has a driver amplifier stage including a low band driver amplifier (412) and a high band driver amplifier (402). A final amplifier stage includes a linear mode amplifier (404) for amplifying digitally modulated signals and a saturated (nonlinear) mode amplifier (414) for amplifying frequency modulated (analog) signals. A switching network (418) interconnects the driver amplifier stage and the final amplifier stage. Depending on the desired mode of operation, an appropriate driver amplifier can be coupled to an appropriate final amplifier to most effectively and efficiently amplify analog or digital RF signals in either of a plurality of frequency bands. A diplex matching circuit (430) is coupled to the linear mode final amplifier (404) for impedance matching and for separating D-AMPS (800 MHz band) and PCS (1900 MHz band) digital signals. A power impedance matching circuit (440) is coupled to the output of the saturated mode final amplifier.



O 01/05028

A Dual-Band, Dual-Mode Power Amplifier

RELATED APPLICATIONS

This application is a continuation-in-part of copending

U.S. patent application serial no. 08/888,168 filed July 3,
1997 (Attorney Docket EUS00502) and U.S. patent application
serial no. 08/939,870 filed September 29, 1997 (Attorney
Docket EUS00806), each of which is assigned to the assignee of
the present application and each of which is hereby
incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of Invention

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The present invention relates generally to power amplifiers and in particular to a dual-band, dual-mode power amplifier.

2. Description of Related Art

In the United States, cellular operating licenses have been awarded by the Federal Communication Commission (FCC) pursuant to a licensing scheme which divides the country into geographic service markets. Cellular licenses were originally granted for radio frequency (RF) blocks in the 800 MHz range. Most 800 MHz cellular telephone systems in the United States utilize the Advanced Mobile Phone Service (AMPS) analog air interface standard. A later generation air interface standard for the 800 MHz band, known as D-AMPS, has subsequently been developed and implemented. The D-AMPS standard comprises both digital and analog cellular communication. Thus, there are presently both analog (AMPS) and digital (D-AMPS) cellular telephone networks in operation at 800 MHz in the United States.

In response to increased demand for cellular services, a number of digital air interface standards were developed for providing efficient digital communication of voice, data, fax

and text messages under the umbrella of "personal communications services" or PCS.

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Operational PCS systems, such as systems based on the GSM TDMA (Time Division Multiple Access) or IS-95 CDMA (Code Division Multiple Access) air interface standards, are being implemented in the United States in the 1900 MHz frequency range. Meanwhile, existing 800 MHz cellular systems are continuing to operate.

Thus, there are presently operating in the United States analog and digital cellular systems at 800 MHz and digital PCS systems at 1900 MHz. Mobile subscribers who desire to receive services from systems operating at 800 MHz and from systems operating at 1900 MHz must either use two different mobile transceivers capable of operating within the cellular or 800 MHz band and the PCS or 1900 MHz band, respectively, or, preferably, use a single "dual-band" mobile transceiver which can receive and transmit RF signals in both frequency bands. Moreover, mobile subscribers who wish to communicate using both analog and digital systems must again either use two different mobile transceivers or, preferably, use a single "dual-mode" transceiver. Ideally, a mobile transceiver is capable of both dual-mode and dual-band operation to provide the user with maximum flexibility and functionality.

A problem arises, however, in that the power amplifier used in a mobile transceiver is typically optimized for use in a particular band (i.e. PCS or AMPS) and in a particular mode (i.e. analog or digital). This problem is manifested in two ways: as an impedance matching problem and as an amplifier biasing problem.

For maximum efficiency, the impedance at the output of the amplifier must be matched to the impedance of a duplexer/diplexer prior to transmission. However, the impedance of the matching circuit is dependent on the frequency of operation. Thus, a conventional matching circuit

optimized for matching the impedance of an amplifier at 800 MHz will generally not optimally match the impedance of the same amplifier operating at 1900 MHz. Moreover, the impedance of the amplifier is dependent on the mode of operation. Thus, a conventional matching circuit optimized for matching the impedance of an amplifier operating at 800 MHz in the AMPS mode will not adequately match the impedance of the same amplifier operating at 800 MHz in the D-AMPS digital mode.

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The biasing problem arises due to the fact that the efficiency of an amplifier is dependent on the mode or class of operation of the amplifier which is determined by the modulation technique employed. Typically, analog communication systems employ well known frequency modulation (FM) techniques to modulate analog information onto a carrier signal, while digital communication systems employ digital modulation schemes, such as $\pi/4$ DQPSK (Differential Quadrature Phase Shift Keying) modulation. Signals transmitted using frequency modulation are most efficiently amplified by a power amplifier biased and operating in non-linear or saturated mode. Signals transmitted using $\pi/4$ DQPSK modulation, on the other hand, are most efficiently amplified by a power amplifier biased and operating in linear mode.

One possible solution to these problems is to provide a separate amplifier chain for both high-band (1900 MHz) and low-band (800 MHz) operation, as illustrated in **Figure 1**. However, this solution is expensive, redundant and wasteful. Moreover, the problem of biasing the low-band amplifier still exists, since the low-band amplifier must amplify both digital and analog signals.

In transceivers having a single amplifier chain, one possible solution to the impedance matching problem is to provide the amplifier with separate, switched high-pass and low-pass matching networks at its output. However, the switch must be capable of handling high power, which tends to require

a large, costly switch. Moreover, the match at 800 MHz will necessarily be a blended match, causing a loss of efficiency in the analog mode.

Another solution to the impedance matching problem is to provide a broadband power matching circuit covering both desired frequency bands and having peaks at the transmit bands. Such a configuration would tend to waste bandwidth, however, when the desired match frequencies differ by an octave or more and the desired bandwidth in each band is relatively narrow. Fano's Limit shows that there is a physical limitation on broadband matching when a reactive element (such as the drain-source capacitance of a transistor) is present.

In transceivers having a single amplifier chain, prior art solutions to the impedance matching problem address the biasing problem by providing separate bias levels, although the impedance match remains constant. If a single amplifier is used to amplify both analog and digital signals, the amplifier must be biased to barely meet linearity requirements while retaining as much analog efficiency as possible. Such an arrangement tends to be inefficient. As radiotelephones become smaller and power consumption requirements become stricter, such inefficient operation is highly undesirable.

Therefore, there is a need in the art for a power amplifier circuit capable of efficient operation in both 800 MHz and 1900 MHz systems and in both analog and digital systems. Such a dual-band, dual mode power amplifier preferably provides an integrated, efficient solution to the problems described above.

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SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a power amplifier circuit for a radio transceiver

capable of efficiently amplifying RF signals in a linear or saturated mode of operation.

It is a further object of the present invention to provide a power amplifier circuit for efficiently amplifying RF signals in a plurality of frequency bands or ranges.

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It is a further object of the present invention to provide a dual-band, dual-mode power amplifier circuit that may be selectably placed in a linear mode of operation for amplifying DQPSK modulated signals and a saturated mode of operation for amplifying frequency modulated signals.

The foregoing and other objects are accomplished in a power amplifier circuit having a driver amplifier stage including a low band driver amplifier and a high band driver amplifier. A final amplifier stage includes a linear mode amplifier for amplifying digitally modulated signals and a saturated (nonlinear) mode amplifier for amplifying frequency modulated (analog) signals. A switching network interconnects the driver amplifier stage and the final amplifier stage. Depending on the desired mode of operation, an appropriate driver amplifier can be coupled to an appropriate final amplifier to most effectively and efficiently amplify analog or digital RF signals in either of a plurality of frequency bands.

A diplex matching circuit is coupled to the linear mode final amplifier for impedance matching and for separating D-AMPS (800 MHz band) and PCS (1900 MHz band) digital signals. A power impedance matching circuit is coupled to the output of the saturated mode final amplifier.

The amplifier circuit includes means for selectably placing the amplifier circuit in a linear mode or a saturated mode, corresponding to digital and analog modes of operation of the radiotelephone, respectively. In the linear or digital mode, the linear final amplifier is biased in the on state and the saturated mode amplifier may be biased in the off state.

Similarly, in the saturated or analog mode of operation, the saturated mode final amplifier is biased in the on state and the linear amplifier may be biased in the off state.

The amplifier circuit may include means for selectably coupling either the first diplex matching circuit output or the low pass matching circuit output to an output line when the amplifier circuit is selectably placed in linear mode or saturated mode, respectively.

These and other objects of the invention, together with features and advantages thereof will become apparent from the following detailed specification when read with the accompanying drawings in which like reference numerals refer to like elements.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of a dual amplifier chain configuration known in the art.

Figure 2 is a schematic diagram of a single amplifier chain with diplex power matching circuit for dual band operation.

Figure 3 is a schematic diagram of a dual band, dual mode amplifier chain.

Figure 4 is a schematic diagram of another embodiment of a dual band, dual mode amplifier chain.

Figure 5 is a circuit diagram of a harmonic trap for use with the embodiment of Figure 4.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. However, this invention may be embodied in many different forms and should not be construed

as limited to the specific embodiments shown. Rather, the preferred embodiments are provided so that this disclosure is thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

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In this application, the terms "duplexer" and "diplexer both refer to a three port, frequency selective splitter. A duplexer is used to enable an RF transceiver to simultaneously transmit and receive on nearly adjacent frequencies using a common antenna, whereas a diplexer separates input signals into high band or low band signals.

Referring first to **Figure 2**, a dual-band power amplifier circuit is indicated generally by reference numeral **200**. Power amplifier circuit **200** has a diplex matching circuit **205** for matching the impedance of a multi-band power amplifier. Radio Frequency (RF) signals are input to a multi-band amplifier **220** at RF input port **210**. Amplifier **220** amplifies the RF signals and outputs the amplified RF signals to a diplex power matching circuit **205** at port **225**.

In the embodiment shown in **Fig. 2**, the amplified RF signals may fall into one of two frequency bands. However, it will be readily apparent to one skilled in the art that the present invention could modified for use in connection with a power amplifier capable of amplifying RF signals contained in more than two frequency bands.

RF signals falling in the first frequency band will be passed by filter/match circuit 230 to duplexer 235. Likewise, RF signals falling in the second frequency band will be passed by filter/match circuit 240 to duplexer 245.

Filter/match circuit 230 blocks RF signals in the second frequency band while providing a suitable impedance match for signals in the first frequency band. Likewise, filter/match circuit 240 blocks RF signals in the first frequency band while providing a suitable impedance match for signals in the second frequency band.

RF signals passed by filter/match circuit 230 are passed through duplexer 235 (if necessary) and into diplexer 260 for transmission using antenna 270. Depending on the communication system in which the amplifier 200 is being used and whether full duplex operation at 1900 MHz is required, duplexer 235 may or may not be necessary. RF signals passed by filter/match circuit 240 are passed through duplexer 245 and into diplexer 260 for transmission using antenna 270.

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The embodiment illustrated in **Figure 2** and implementations thereof are described in greater detail in copending U.S. patent application serial no. 08/888,168 (Attorney Docket EUS00502).

Referring now to Figure 3, a dual-mode, dual-band amplifier circuit is indicated generally by reference numeral 300. Amplifier circuit 300 is advantageously included in the transmitter or transceiver of a radiotelephone (not shown) for amplifying both analog and digital signals in two different frequency bands or ranges, thereby providing the radiotelephone with dual-band, dual-mode functionality. Amplifier circuit 300 includes an RF input port 302 which is coupled to a mode select switch 304. Depending on whether the radiotelephone is being operated in a digital or analog mode, the setting of mode select switch 304 will cause input RF signals to be transmitted down digital path 306 or analog path 308, respectively. The position of mode select switch 304 is controlled by a mode control signal from a microprocessor (not shown) within the radiotelephone. The control signal provided by the microprocessor is used to selectively place amplifier circuit 300 in a linear mode or a saturated (nonlinear) mode of operation.

Digital path 306 includes a linear amplifier 310, which efficiently amplifies signals which have been modulated using a linear modulation technique such as DQPSK modulation. The

output of linear amplifier 310 is coupled to a diplex matching circuit 330 which efficiently separates 1900 MHz signals from 800 MHz signals while providing an impedance match for linear amplifier 310 in both frequency ranges. The structure and function of diplex matching circuit 330 is described in greater detail below.

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Diplex matching circuit 330 has a 1900 MHz output 334 and an 800 MHz output 336. The 1900 MHz output is coupled via path 339 to a diplexer 370, which couples the 1900 MHz output signal to an antenna 380. Additionally, a duplexer may be provided between the 1900 MHz output 334 and diplexer 370 if full duplex operation is desired for 1900 MHz operation, for example in a CDMA or multirate TDMA system.

Analog path 308 includes a nonlinear amplifier 320 which efficiently amplifies frequency modulated signals. The output of nonlinear amplifier 320 is coupled to a matching circuit 340 which provides a 50-Ohm impedance match for nonlinear amplifier 320. Matching circuit 340 also helps suppress harmonic content that could feed back down the 1900 MHz path 339.

Since separate linear and nonlinear amplifiers 310, 320, respectively are provided, the nonlinear amplifier may be operated as a deeply saturated Class C amplifier or as a switched mode class E amplifier. Previous solutions in which a single amplifier was used for both linear and nonlinear amplification required that the amplifier be biased (in Class AB) to barely meet linearity requirements while retaining as much nonlinear efficiency as possible. The result was a blended match that was not optimal for either linear or nonlinear amplification. The present invention overcomes this limitation while providing an amplifier circuit that can effectively and efficiently amplify signals in different frequency bands.

The output of matching circuit 340 on line 345 and the 800 MHz output of diplex matching circuit 330 on line 338 are provided to a high power switch 350. High power switch 350 couples either the 800 MHz output of diplex match circuit 330 (corresponding to a digital 800 MHz signal) or the output of matching circuit 340 (corresponding to an analog 800 MHz signal) to duplexer 360 via output line 361, depending on whether the cellular telephone is being operated in a digital or analog mode, respectively. As with mode select switch 304, high power switch 350 is controlled by the mode control signal from the radiotelephone's microprocessor. Additionally, high power switch 350 provides isolation for linear amplifier 310, thus preventing linear amplifier 310 from being loaded by nonlinear amplifier 320 and matching circuit 340.

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DC biasing for linear amplifier 310 and nonlinear amplifier 320 is provided by switching Vcc inputs 316, 326 on or off depending on the desired mode of operation of the cellular telephone (i.e. digital or analog).

Duplexer 360 is a conventional duplexer designed to permit full duplex operation at 800 MHz. Duplexer 360 couples 800 MHz signals to diplexer 370, which in turn couples the signals to antenna 380 for transmission.

The embodiment illustrated in **Figure 3** is particularly suited for use in a TDMA transceiver, which operates at half duplex at 1900 MHz. However, as described above, the circuit can be easily adapted for use in a CDMA or multirate TDMA transceiver by providing an additional duplexer in path **339** to permit full duplex operation at 1900 MHz.

Diplex matching circuit 330, which is essentially the same circuit as diplex matching circuit 205 shown in Figure 2, is described in detail in copending U.S. application serial no. 08/888,168 (Attorney Docket EUS00502) and will not be discussed further. The embodiment illustrated in Figure 3 and

implementations thereof are described in greater detail in copending U.S. patent application serial no. 08/939,870 (Attorney Docket EUS00806).

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Referring now to Figure 4, a second dual-band dual-mode amplifier architecture is indicated generally as 400.

Amplifier 400 improves on the designs illustrated in Figures 2 and 3 by separating the amplifier into a driver stage and a final stage, and selectively coupling the appropriate driver and final stages depending on the desired mode of operation of the amplifier 400. Amplifier 400 includes a 1900 MHz driver amplifier 402 tuned and biased to efficiently amplify signals in the 1900 MHz frequency band and an 800 MHz driver amplifier 412 tuned and biased to efficiently amplify signals in the 800 MHz frequency band.

Amplifier 400 also includes a pair of final stage amplifiers 404 and 414. Final stage amplifier 404 is biased and tuned for linear operation as a class AB amplifier to efficiently amplify digitally modulated RF signals, while final stage amplifier 414 is biased and tuned for saturated operation in an efficient mode of operation, such as a deeply saturated class C amplifier or a switched mode class E amplifier or some other highly efficient mode of operation to efficiently amplify frequency modulated analog RF signals.

The driver stage amplifiers 402, 412 are connected to the final stage amplifiers 404, 414 by means of a switching network 418 which includes switches 422, 424 and 426. Each of switches 422, 424 and 426 may be a field-effect transistor (FET) switch whose design is well known to those skilled in the art. Other suitable types of switches may be substituted by those having skill in the art. The open/closed state of switches 422, 424 and 426 is controllable by means of control lines (not shown) from an associated microprocessor or other control logic (not shown).

Switch 422 couples the output of 1900 MHz driver amplifier 402 to the input of linear final amplifier 404. The output of 800 MHz driver amplifier 412 is coupled to node 428. Node 428 is in turn coupled to the input of linear final amplifier 404 via switch 424 and to the input of saturated final amplifier 414 via switch 426.

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The signal output by final amplifier 404 is passed through diplex matching circuit 430 which filters and passes the signal to duplexer 460 (if necessary) or duplexer 465 (via switch 445) depending on the frequency content of the signal.

In one embodiment, a first filter 410 is provided between the output of 1900 MHz driver amplifier 402 and switch 422, and a second filter 420 is provided between the output of 800 MHz driver amplifier 412 and node 428. These filters 410, 420 filter the input signals prior to the final gain stage thereby providing receive band noise rejection and reduction of the harmonic content of the signal. In one embodiment, Filters 410, 420 are surface acoustic wave (SAW) bandpass filters, the design of which is well known in the art.

By providing a filtered signal to the final amplifier stage, final amplification by the linear amplifier is more effective. Placing filters between the gain stages of the amplifier allows the duplexers 460, 465 to be implemented with one less pole, decreasing the insertion loss of the overall amplifier circuit 400 and resulting in lower dc current drain. Because of the lower insertion loss of amplifier 400, the final amplifier stage does not need to develop as much output RF power. This has a number of desirable consequences, including a smaller die size and lower dc current consumption.

In one embodiment, a harmonic trap 455 is coupled to the input of diplex matching circuit 430. The function of harmonic trap 455 is to reduce the harmonic content of signals output by diplex matching circuit 430 and to supply VDD to

final stage amplifier 404. An embodiment of harmonic trap 455 is shown in Figure 5. Figure 5 shows an embodiment of harmonic trap 455, which includes a high-power switch 510 coupled to a pair of parallel switchable inductors 520, 525.

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Inductors 520, 525 are in turn coupled to capacitor 530, which is coupled to the input of diplex matching circuit 430. Inductor 520 and capacitor 530 combine to form a parallel resonant circuit that is resonant at 800 MHz, while inductor 525 and capacitor combine to form a parallel resonant circuit that is resonant at 1900 MHz. Thus, depending on the state of switch 510 (which is set according to the operating state of amplifier 400), the harmonic trap 455 will operate to attenuate harmonic signals in the 800 MHz band or the 1900 MHz band. As with switches 422, 424 and 426, switch 510 is controllable by means of control lines (not shown) from an associated microprocessor or other control logic (not shown).

Since the linear final amplifier 404 is operated in a class AB mode, harmonic content of the output signal is higher than it would be using a class A amplifier. Providing a harmonic trap at the output of final amplifier 404 therefore increases the efficiency of final amplifier 404 by constraining the output energy to the desired frequencies.

Referring again to Figure 4, the amplifier may be operated in one of a number of selectable modes to amplify analog or digital signals in the 800 MHz frequency band or digital signals in the 1900 MHz frequency band. For the 1900 MHz mode of operation, switch 422 is closed, while switch 424 is open. Additionally, in the 1900 MHz mode of operation switch 426 may be open to provide additional isolation of the final stage amplifiers 404, 414. Digitally modulated input signals in the 1900 MHz frequency band are input to amplifier 400 via input terminal 405 and provided to 1900 MHz driver amplifier 402. The signal output by 1900 MHz driver amplifier 402 is coupled

to the input of final amplifier 404 which, as noted above, is biased for operation in linear mode. Amplifier 404 efficiently amplifies the digitally modulated signal and outputs the amplified signal to diplex matching circuit 430.

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To amplify analog RF signals in the 800 MHz band, (800 MHz analog mode) switches 422 and 424 are open, while switch 426 is closed. Frequency modulated (i.e. analog or FM) input signals in the 800 MHz frequency band are input to amplifier 400 via input terminal 415 and provided to 800 MHz driver amplifier 412. The signal output by 800 MHz driver amplifier 412 is coupled to the input of final amplifier 414 via closed switch 426. Final amplifier 414 is biased for operation in saturated mode, and therefore efficiently amplifies the FM signal and outputs the amplified signal to matching circuit 440.

To amplify digitally-modulated (e.g. •/4 DQPSK) RF signals in the 800 MHz band, (800 MHz digital mode) switches 422 and 426 are open, while switch 424 is closed. Digitally modulated input signals in the 800 MHz frequency band are input to amplifier 400 via input terminal 415 and provided to 800 MHz driver amplifier 412. The signal output by 800 MHz driver amplifier 412 is coupled to the input of final amplifier 404 via node 428 and switch 426. As noted above, final amplifier 404 is biased for operation in linear mode. Amplifier 404 efficiently amplifies the digitally modulated signal and outputs the amplified signal to diplex matching circuit 430. The operation of switch 445 is similar to that of switch 350 described in reference to Figure 3.

While the present invention has been described with respect to its preferred embodiment, those skilled in the art will recognize that the present invention is not limited to the specific embodiment described and illustrated herein. Different embodiments and adaptations besides those shown

herein and described as well as many variations, modifications and equivalent arrangements will now be apparent or will be reasonably suggested by the foregoing specification and drawings, without departing from the substance or scope of the invention. Accordingly, it is intended that the invention be limited only by the scope of the claims appended hereto.

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What is claimed is:

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1. A power amplifier circuit for amplifying RF signals, said power amplifier circuit selectively operable in a linear mode or a nonlinear mode and selectively operable to amplify RF signals in a first frequency band or a second frequency band, characterized by:

a first driver amplifier (402) for amplifying RF signals in a first frequency band;

first and second final amplifiers (404,414);

a diplex matching circuit (430) coupled to said first final amplifier (404); and

a switching network (418) for selectively coupling said first driver amplifier (402) to said first and second final amplifiers (404,414) in response to said amplifier circuit being placed in a linear or nonlinear mode of operation, respectively.

20 2. The power amplifier circuit as recited in claim 1, further characterized by:

a low pass matching circuit (440) coupled to an output of said second final amplifier; and

switching circuitry (445), coupled to a first output of said diplex matching circuit and an output of said low pass matching circuit (440), for selectively coupling said first diplex matching circuit output or said low pass matching circuit output to an output line when said amplifier circuit is selectively placed in linear mode or nonlinear mode,

30 respectively.

3. The power amplifier circuit as recited in claim 1, further characterized by:

a second driver amplifier (412) for amplifying RF signals in a second frequency band; and

wherein said switching network (418) includes a first switch (422) coupled between said first driver amplifier (402) and said first final amplifier (404).

- The power amplifier circuit as recited in claim 3, wherein said switching network (418) further includes a node (428) coupled to an output of said second driver amplifier
 (412), a second switch (424) coupled between said node (428) and an input of said first final amplifier (404) and a third switch (426) coupled between said node (428) and an input of said second final amplifier (414).
- 5. The power amplifier circuit as recited in claim 4, further characterized by a first filter (410) disposed between the output of said first driver amplifier (402) and said first switch (422), and a second filter (420) disposed between said second driver amplifier (412) and said node (428).

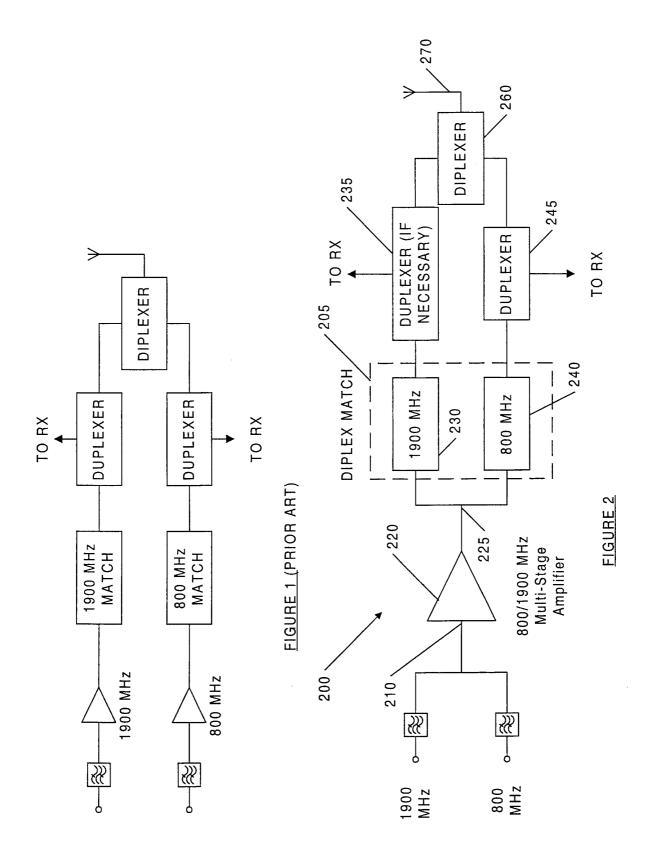
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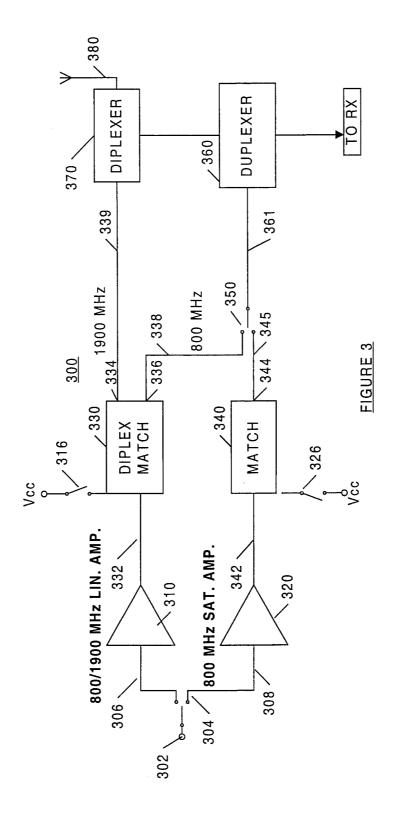
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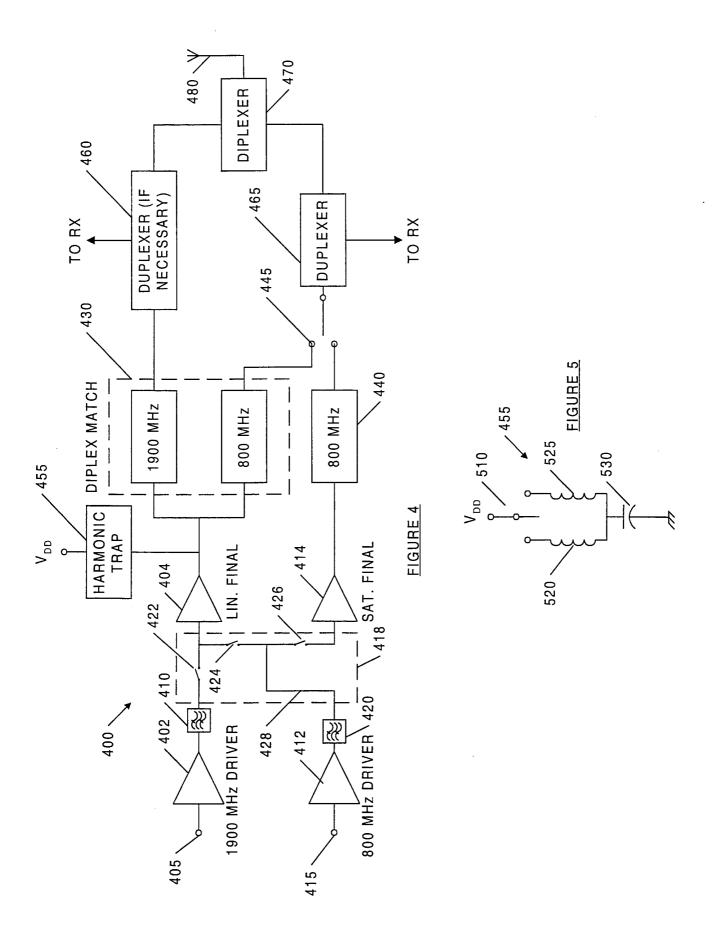
- 6. The power amplifier as recited in claim 3, further characterized by a harmonic trap (455) coupled to an output of said first final amplifier (404).
- 7. The power amplifier as recited in claim 5, wherein said first and second filters (410,420) are surface acoustic wave filters.
- 8. A power amplifier circuit for amplifying RF signals, said power amplifier circuit selectively operable in a linear mode or a nonlinear mode and selectively operable to amplify RF signals in a first frequency band or a second frequency band, characterized by:

a driver amplifier stage having a high band input (405) and a low band input (415);

- a final amplifier stage having a linear amplifier (404) and a nonlinear amplifier (414);
- a switching network (418) coupling said driver amplifier stage and said final amplifier stage responsive to a mode selection.
- 9. The power amplifier circuit as recited in claim 8,10 further characterized by:
 - a filter stage (410,420) interposed between said driver stage and said switching network.







INTERNATIONAL SEARCH REPORT

Im. .ational Application No PCT/IB 99/01255

A. CLASSIFICATION OF SUBJECT MATTER IPC 7 H03H7/38 H03I H03H7/46 H03F3/72 According to international Patent Classification (IPC) or to both national classification and IPC B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H03H H03F IPC 7 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practical, search terms used) C. DOCUMENTS CONSIDERED TO BE RELEVANT Category ° i Citation of document, with indication, where appropriate, of the relevant passages Relevant to dalm No. US 5 438 684 A (OSMANI RASHID M ET AL) X 8 1 August 1995 (1995-08-01) 1-7.9 abstract; figures 3,4,7 A WO 99 17445 A (ERICSSON GE MOBILE INC) 1-9 8 April 1999 (1999-04-08) the whole document EP 0 837 559 A (MATSUSHITA ELECTRIC IND CO 1-9 Α LTD) 22 April 1998 (1998-04-22) the whole document A US 5 774 017 A (ADAR AHARON) 30 June 1998 (1998-06-30) WO 98 47222 A (QUALCOMM INC) A 22 October 1998 (1998-10-22) -/--Further documents are listed in the continuation of box C. Patent family members are listed in annex. X X Special categories of cited documents: "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled "O" document referring to an oral disclosure, use, exhibition or "P" document published prior to the international filing date but later than the priority date claimed in the art. "&" document member of the same patent family Date of the actual completion of the international search Date of mailing of the international search report 13 March 2000 23/03/2000 Name and mailing address of the ISA **Authorized officer** European Patent Office, P.B. 5818 Patentiaan 2 NL – 2280 HV Rijewljk Tel. (+31-70) 340-2040, Tx. 31 651 epo ni, Segaert, P Fax: (+31-70) 340-3016

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Information on patent family members

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